CHAPTER 15

# Tester Interfacing—DIB Design

The device interface board (DIB) customizes the generic ATE to a specific device under test (DUT). With the wide variance of DUT, pure digital, pure analog, mixed signal up to high speed and RF devices, the DIB requirements lead to a high variance of design requirements. This chapter will give an overview on DIB design for a wide range of DUTs but discuss specific requirements for high-speed and high-frequency devices.

## 15.1 DIB BASICS

### 15.1.1 Purpose of a Device Interface Board

On any given day, a general-purpose ATE tester may be required to test a wide variety of device types. A mixed-signal tester may test video converters in the morning, modem chips in the afternoon, and standalone ADCs in the evening. Obviously, the electrical testing requirements of each type of device are unique to that device. Also, the mechanical requirements of each device are unique. The tester's various electrical resources must be connected to each of the DUT's pins, regardless of the mechanical configuration of the DUT package. For example, an 8-bit DAC might be available in several different packages such as the small outline IC (SOIC), quad flat pack (QFP), leadless chip carrier (LCC), and a chip scale package (CSP). Or this DAC can be part of a system on chip (SOC) in a ball grid array (BGA) of leadless quad flat pack (QFN). These package types are illustrated in Figure 15.1. Also, the tester needs to be connected to the bare die during wafer probing. Clearly, a general-purpose tester cannot be expected to provide all electrical resources and mechanical fixtures to test any arbitrary device type in any package.

The device interface board (DIB) provides a means of customizing the general-purpose tester to specific DUTs and families of DUTs. The DIB serves two main purposes. First, it gives the test engineer a place to mount DUT-specific circuitry that is not available in the ATE tester. This circuitry can be placed near the DUT to enhance electrical performance during critical tests. Second, the DIB provides a temporary electrical interface to each DUT during electrical performance testing. When testing packaged devices, the temporary connection is achieved using a hand-test

**Figure 15.1.** Common IC package types.

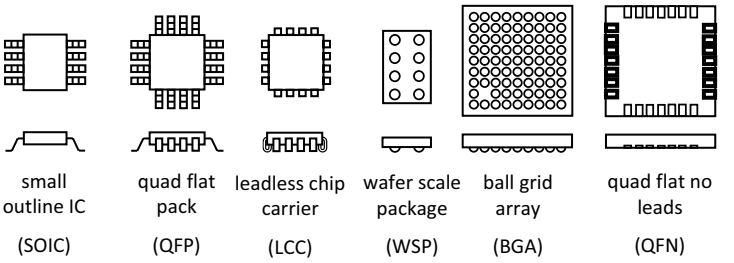
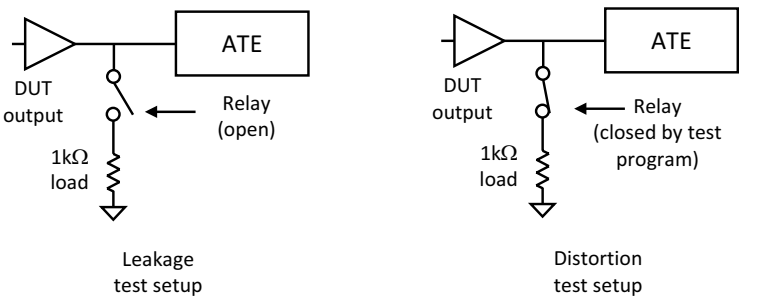



**Figure 15.2.** Electromechanical relays modify the DUT's electrical environment.




socket or a handler-specific mechanism called a *contactor assembly*. For this reason the DIB is called often also as HIB (handler interface board). Thus a DIB is often intended for use with only one type of DUT mounted in a particular mechanical package. When testing bare die on a wafer, the temporary DUT connection is made using the tiny probes of a probe card. A probe interface board (PIB) is usually required to interface the probe card to the tester's resources. Together, the PIB and probe card serve the same purpose as a DIB and contactor assembly. If the same device is offered in three different packages, then three different DIBs and a PIB may be required. Clearly, electromechanical hardware design represents a large portion of the test-engineering task.

DUTs that are purely digital in nature typically require a very simple DIB that simply provides point-to-point connectivity between the DUT pins and the tester's power supplies and digital pin card electronics. RF, analog and mixed-signal DUTs usually require much more elaborate DIBs. An RF DIB and PIB often require a matching circuit to adapt the tester impedance to the device impedance as well as decoupling circuits to provide a good device ground to accomplish the wave distribution of the stimulus and measure signals. A lower-frequency mixed-signal DIB often contains a variety of active and passive circuits that must be connected to or disconnected from various DUT pins as the test program progresses. For example, the harmonic distortion of an analog output may be specified with a 1-kΩ load connected between the analog output and ground. The same output may also have an off-state output leakage specification. The 1-kΩ load resistor must be disconnected during the leakage test to prevent current from leaking through the resistor to ground. Using electromechanical relays or solid state switches, the DIB can modify the DUTs electrical environment under test program control. The relays act as electrical switches that can be turned on and off by commands in the test program (Figure 15.2).

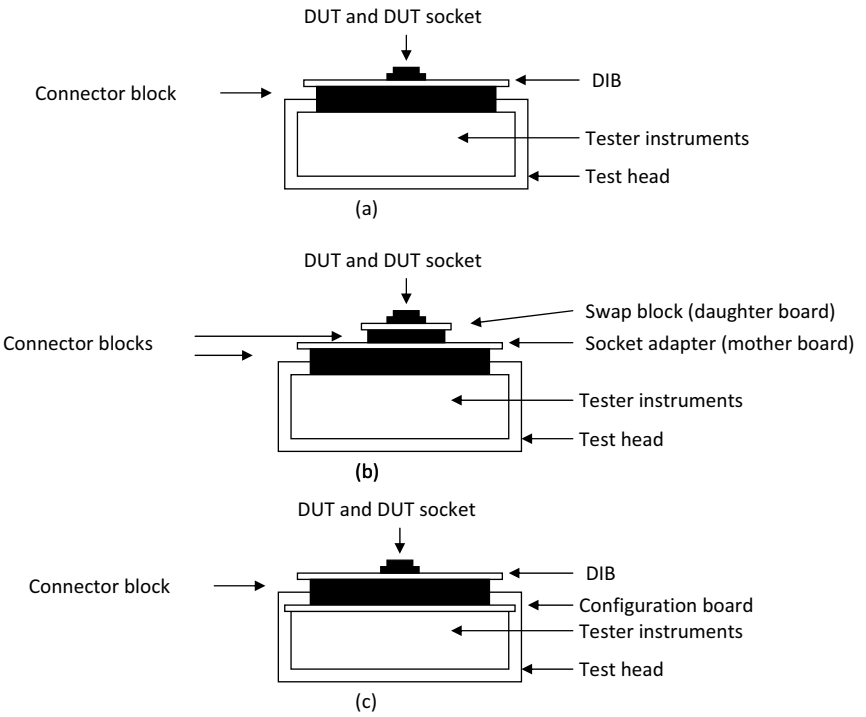
### 15.1.2 DIB Configurations

Thus far, we have talked about DIBs as if they are the same for each type of tester. In reality, the mechanical details of interface hardware vary widely from one tester type to another. Mechanical configurations may even vary within the same company, even when the various test development organizations all use the exact same tester. Figure 15.3 shows three possible interfacing schemes. The first is the simple DIB interfacing scheme. In this type of configuration, the DIB and contactor assembly form the entire interface between the tester and the DUT.

The second scheme shows a socket adapter/swap block stackup that is often used to test families of similar devices. In this configuration, the socket adapter (also called a *family board* or *mother board*) contains the support circuitry required to test a family of devices, such as video ADCs. The swap block (daughter board) provides the customization needed to test a particular video ADC in a particular type of package. For example, one swap block might be compatible with 64-pin LCCs while another is compatible with 64-pin QFPs. This scheme allows a relatively complex and expensive socket adapter to be reused for a family of similar DUTs. Of course, this scheme is not limited to only two layers of interfacing, but the attachment of a fully custom swap block to a semi-custom socket adapter is the most common multilayer configuration. The daughter board can be even mounted into a special machined mother board, so that the will become flat or as a stack-up as shown in Figure 15.3b.

A third possibility is the configuration board/DIB scheme. The configuration board is similar to the family board, except that it is located inside the test head. It is generally only intended to customize the tester for a particular organization's needs. Unlike the family board, which may

**Figure 15.3.** DIB interfacing schemes: (a) Simple DIB, (b) socket adapter/swap block, and (c) DIB and configuration board.



be changed daily, the configuration board is usually left in place for all device types. All DUT-specific circuitry is located on the DIB.

The terminology used to describe each layer of interface hardware varies widely from one ATE vendor to another. The terminology even varies from one vendor's tester to another. Throughout this book and for the remainder of this chapter, we will use the term DIB to refer to all the layers of custom and semi-custom interfacing hardware, including mother boards, daughter boards, swap blocks, and DIBs. In other words, we will treat the subject of DIB design as if all testers used the configuration illustrated in Figure 15.3.

### 15.1.3 Importance of Good DIB Design

One of the major causes of long test program development time is poor mixed-signal or RF DIB design and printed circuit board (PCB) layout. A DIB schematic shows only an idealized view of the DIB. Resistors are shown as ideal resistances, capacitors as ideal capacitances, and traces as perfect connections with no parasitic resistance, inductance, or capacitance. In reality, the exact mechanical layout of the components and traces on the DIB may make the difference between failing test results and passing results.

The performance of RF, analog, and mixed-signal devices is highly dependent on the quality of the surrounding circuit design. It is important to be able to distinguish between legitimate DUT failures and failures caused by poor design of the DIB. Consequently, a DIB should represent the best-case environment for the DUT, rather than a worst-case environment. With that said, the actual tests are more commonly designed to provide the worst-case conditions (e.g., supply voltage, input signal levels, input signal jitter, etc.) that the device is guaranteed to tolerate. Unfortunately, it is difficult to provide the DUT with a perfect environment using a general-purpose tester with bulky electromechanical interconnections. For example, the pins of the DUT socket will typically add more inductance and capacitance to the DUT's environment than the DUT will encounter when it is soldered directly onto a printed circuit board in the end application. Also the placement of the components close to the DUT is limited by the bulky socket causing a degradation of the performance. The RF lines on the test board will cause an impedance transformation when not matched to the DUT and ATE impedance. Nevertheless, the test engineer must try to design a DIB that does not present the DUT with unfair electrical handicaps.

There are so many performance considerations in mixed-signal and RF DIB design that many people consider it a mystical black art. Actually, DIB design is more of a "light gray" art, since many of the major considerations are fairly well understood. In this chapter, we will examine some of the main considerations in mixed-signal and RF DIB design such as transmission lines, matching circuits, power supply and grounding connections, shielding schemes, parasitic circuit elements, component selection, common DIB circuits, and common DIB mistakes.

First, let us look at one of the DIB's most important electrical components: the printed circuit board. Although the printed circuit board is often thought to be nothing more than a mechanical frame onto which the circuit components are fastened together, its physical construction is absolutely key to the performance of many mixed-signal DUTs.

## 15.2 PRINTED CIRCUIT BOARDS

### 15.2.1 Prototype DIBs Versus PCB DIBs

One of the common debates in test engineering is the choice between hand-wired prototype DIBs versus printed circuit board (PCB) DIBs when developing a DIB for lower-performing mixed-signal or digital devices. Hand-wired DIBs can be quickly constructed from prefabricated blank prototype boards. The alternate approach is to produce a production-worthy custom PCB version

of the DIB without first building a hand-wired prototype. Each approach has advantages and disadvantages.

The hand-wired approach results in rapid turn-around at relatively low production cost. However, the resulting board is typically not very production-worthy, since the loose wires are easily broken. Also, hand-wired DIBs may not give the same high-quality electrical performance that can be achieved using PCB-based DIBs. When multiple DIBs are required or when the customer or the performance of the DUT requires, the PCB approach is usually the superior solution. PCB DIBs are easily manufactured in quantity, they are mechanically robust during debug and production, they provide superior electrical performance, and they provide good consistency (i.e., correlation) from one board to another. Correlation between hand-wired DIBs can be very problematic, since each is electrically unique depending on the exact length and physical layout of the wires on each board. At higher frequencies, hand-wired boards are often useless, since they can produce incorrect readings due to their inferior electrical characteristics. PCBs also have the advantage that commercial tools can be used to check their functionality with flying probes when being mass-produced.

The downside to PCB-based DIBs is primarily longer cycle time and higher initial cost. It may take several weeks to get a PCB DIB designed, laid out, and fabricated. Also, PCB DIBs are more expensive than hand-wired DIBs, at least in small quantities. However, assuming that the test engineer is skilled enough to produce a usable PCB DIB design on the first pass, the PCB DIB is actually a less expensive approach. After all, a PCB DIB will eventually be required for a robust production solution anyway.

Rapid turnaround is a problem that can be solved by good methodology. PCB-based DIBs can be designed, laid out, and fabricated in a matter of a week or two if the test engineer is skilled in the proper use of computer-aided design (CAD) tools. To achieve a rapid turnaround with minimal errors, a CAD-based design, layout, and fabrication approach must be established between the test organization and the PCB layout organization (which may either be an external vendor or an internal support group).

### 15.2.2 PCB CAD Tools

A streamlined PCB design and layout process requires the use of netlist-based CAD tools. A netlist is a database describing each interconnection in the circuit. For example, one line of a typical netlist file might tell the PCB layout tool that, for example, circuit node 55 interconnects resistor R1 pin 1, inductor L1 interconnects pin 2, and amplifier U37 interconnects pin 15. In addition to the point-to-point interconnection information, the netlist also includes such information as the footprint, or shape, of each component in the circuit as well as keeps out areas required for handler and prober docking interface. A footprint represents the mechanical specification of the component's package. Information such as $(X,Y)$ pin locations, pad sizes, hole sizes, and package outline shapes to be printed on the finished PCB are included in the footprint description for each type of component.

Using a netlist-compatible schematic capture tool, the test engineer draws the circuit schematic on a computer workstation or PC. Then the schematic database (including the netlist) is transferred to the PCB designer for use in the DIB layout process. Once the netlist has been extracted from the database, the PCB designer begins laying out the DIB from a standard DIB template. The DIB template database represents a head start DIB design, which includes the shape of the DIB and its standard mechanical mounting holes as well as many preplaced standard components, such as tester connectors.

The netlist directs the PCB layout software to import all the required DIB components from a standard parts library. The PCB designer then places these components and connects them as shown in the schematic. The netlist prevents errors in point-to-point interconnections by refusing

to let the layout designer place traces where they do not belong. The netlist also guarantees that none of the desired connections are mistakenly omitted. Once the DIB layout is completed, each layer of the design is plotted onto transparent film for use in PCB fabrication. These plots are commonly known as *Gerber* or *Gerber plots*, named after the company that pioneered some of the early plotting equipment (Gerber Scientific). Figure 15.4 illustrates the CAD-based DIB design, layout, and fabrication process.

### 15.2.3 Multilayer PCBs

Low-cost PCBs can be designed and fabricated using one or two layers of copper trace, as shown in Figure 15.5. Traces on opposite sides of a double-layer PCB can be connected using a copper plated through-hole called a *via*. Double-layer PCB fabrication starts with a blank PCB consisting of a sheet of insulator (e.g., fiberglass) plated with a thin layer of copper on both sides. The component lead holes and vias are drilled first. Then the holes are plated with copper to form the layer-to-layer interconnects. Finally, the traces are printed and etched using a photolithographic process similar to that used in IC fabrication. The via can be filled in a final step to have a solid surface and to avoid any problems when soldering components on the via pad.

Multilayer PCBs having four or more layers can be formed by stacking multiple two-layer boards together, as shown in Figure 15.6. The internal, or buried, layers are first printed and

**Figure 15.4.** CAD-based DIB design and fabrication process.

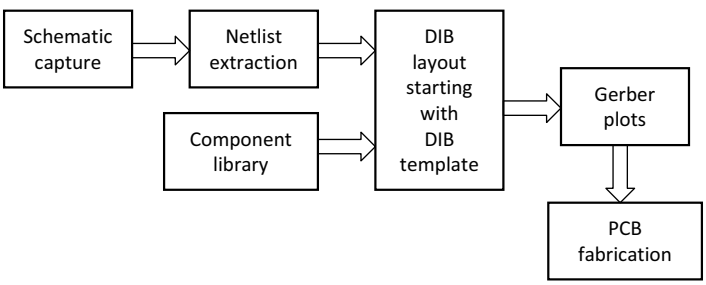



**Figure 15.5.** Single- and double-layer PCBs.

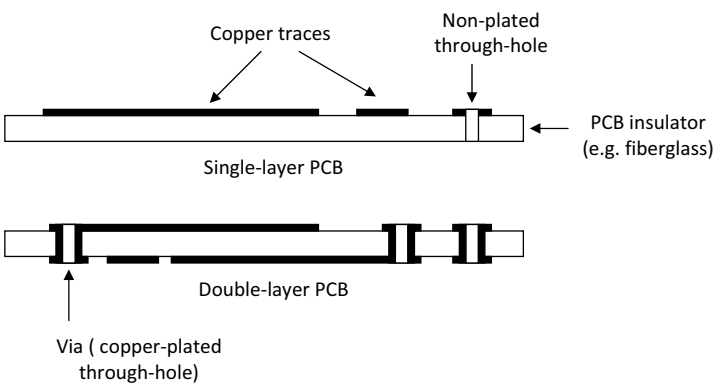
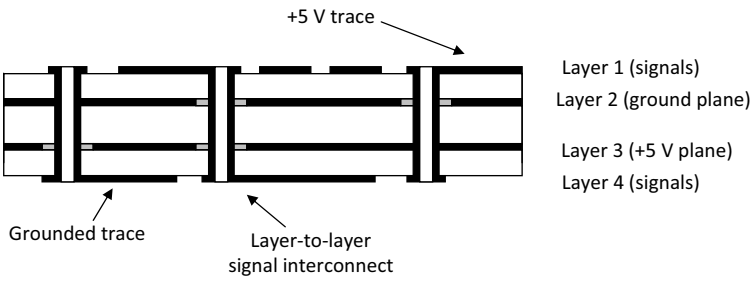


**Figure 15.6.** Multilayer PCBs.




etched. The layers are all stacked and pressed together under heat to form a single board. Finally, the vias are drilled and plated and the outer layers are etched to form the finished PCB. In some instances, buried vias are added. These are vias that do not extend completely between the top and bottom layers, but rather go between sublayers of the PCB. These are often used to keep trace lengths short but add significant cost to the DIB.

Most mixed-signal DIBs are formed using 6- to 25-layer PCBs. The arrangement of layers in a PCB is known as the *stackup*. The stackup of a DIB may vary from one type of DUT to another, but some general guidelines are commonly followed. The internal layers are typically used for ground and power distribution, as well as for various noncritical signal traces. The outer layers are usually reserved for critical signals or those signal traces that might need to be modified after the DIB has been fabricated. External traces are also easier to access for observation during the test program debug process. If desired, test point vias can be added to a DIB to access buried signals for debugging purposes.

In addition to the trace layers and insulator layers in a PCB, the outer layers are usually coated with a material called a *solder mask*. This thin, nonconductive layer keeps solder from flowing all over the traces when the DIB components are soldered onto the PCB. The solder mask helps to prevent unwanted solder shorts between adjacent traces. Some test socket vendor require to have the solder mask excluded in the area the test socket is mounted onto the PCB.

A silkscreen pattern may also be printed on the outer layers of the PCB. The silkscreen patterns show the outline and reference numbers for all the DIB components, such as resistors, capacitors, relays, and connectors. The silkscreen patterns are quite useful during the DIB component assembly process, and they are equally useful during the test program debugging process.

## 15.2.4 PCB Materials

Printed circuit boards can be constructed using a variety of materials. The most common trace material is copper, due to its excellent electrical conductivity. The most common insulator material is FR4 (fire retardant, type 4) fiberglass. Fiberglass is an inexpensive material that exhibits good electrical properties up to several hundred megahertz. As frequencies approach 1 GHz, more exotic materials such as Teflon®* or cyanate ester may be the better choice.

Teflon® exhibits excellent RF characteristics, including low signal loss and an equally distributed dielectric constant. However, it suffers from poor mechanical stiffness. A DIB made exclusively of Teflon® insulator would be too weak to stand up to the force of DUT insertions by a handler. Cyanate ester is a material with reasonably good RF properties and yet it is stiff enough to withstand the mechanical stress of production testing. A hybrid stackup consisting of sandwiched

*Teflon® is a registered trademark of DuPont.

layers of Teflon® and cyanate ester provides a compromise between the good electrical properties of Teflon® and the good mechanical properties of cyanate ester.

## 15.3 DIB TRACES, SHIELDS, AND GUARDS

A trace on a PCB is the connection of two components. Other than in the schematics, however, this trace is not only a connection of two or more components, but rather needs to be treated as a component with parasitics itself, where the parasitics becomes more critical with higher frequencies. In the following section we discuss the basic parasitics like trace resistance, inductance, and capacitance; in a separate section we will discuss the trace as an RF component and its potential impact on the performance.

### 15.3.1 Trace Parasitics

One of the most important DIB components is the printed circuit board trace. It is easy to think that wires and traces are not components at all, but are instead represented by the connecting lines that appear in a schematic. However, PCB traces (and wires in general) are resistive, slightly inductive, and slightly capacitive in nature and have impedance, which can be calculated or simulated based on their geometry, proximity to another line, board thickness, and material constants. For RF boards these board traces become a component, which can even be used to match the DUT to the tester instruments.

The nonideal circuit characteristics are known as *parasitic elements*, though they are often simply referred to as *parasitics*. Often, trace parasitics can be ignored, especially when working with low frequencies and low to moderate current levels. Other times, the parasitics will have a significant effect on a circuit's behavior. The test engineer should always be aware of the potential problems that trace parasitics might pose.

Trace resistance on DIBs seldom exceeds a few ohms. Inductance can be anywhere from one or two nanohenries* (nH) to several microhenries (μH). Capacitance can range from one or two picofarads,† (pF) to tens of pF. Although these values are very approximate, they can be used as a thumbnail estimate to determine whether the parasitic elements might be large enough to affect the DUT's performance. To estimate trace parasitics with a little more accuracy, we need to review the equations for trace resistance, inductance, and capacitance.

### 15.3.2 Trace Resistance

The parasitic resistance of a PCB trace is directly proportional to the length of the trace, and inversely proportional to the height and width of the trace. The equation for resistance in a uniform conductive material with a rectangular cross section is

$$R = \frac{L_{Trace}}{\sigma WT} \tag{15.1}$$

where $R$ is trace resistance, $L_{TRACE}$ is trace length, $W$ is trace width, $T$ is trace thickness, and $\sigma$ is the conductivity of the trace material. This resistance R is the DC resistance and not the same than the line impedance $Z$ and is not considering the skin effect, which will have an effect at higher frequencies.

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*Named in honor of the American scientist Joseph Henry (1797–1878), who discovered the electromagnetic phenomenon of self-inductance.

†Named in honor of the English chemist and physicist Michael Faraday (1791–1867), who contributed to the fields of electromagnetism and electrochemistry.

Most PCB traces are constructed using copper, which has a conductivity of about $5.7 \times 10^7$ $(\Omega\ \text{m})^{-1}$. The trace thickness is usually about 1 mil, although PCBs can be fabricated with a copper sheet thickness of 3 mils or more if desired. When working with equations such as Eq. (15.1), we will consistently convert all units of length to meters, since electrical units such as resistance, current, and voltage are metric units. Since the mil is an English unit (1 mil = 1/1000 in.), we will convert it to meters before using any of our electrical equations. The conversion factor is

$$1\ \text{mil} = 25.4\ \mu\text{m} \tag{15.2}$$

Often Eq. (15.2) is approximated by 1 mil = 1/39,000 meter.

## EXAMPLE 15.1

Calculate the parasitic resistance of a PCB trace that is 15 in. long, 1 mil thick, and 20 mils wide.

**Solution:**

First we convert all units of length into meters

$$L_{TRACE} = 15\ \text{in.} \times (1\ \text{m} / 39\ \text{in.}) = 0.385\ \text{m}$$

$$T = 1\ \text{mil} \times (1\ \text{m} / 39{,}000\ \text{mils}) = 2.56 \times 10^{-5}\ \text{m}$$

$$W = 20\ \text{mil} \times (1\ \text{m} / 39{,}000\ \text{mils}) = 5.12 \times 10^{-4}\ \text{m}$$

Applying Eq. (15.1) to a copper trace with $\sigma = 5.7 \times 10^7\ (\Omega\ \text{m})^{-1}$, we get a total parasitic trace resistance of

$$R = \frac{0.385}{5.7 \times 10^7 \times 5.12 \times 10^{-4} \times 2.56 \times 10^{-5}} = 515\ \text{m}\Omega$$

### 15.3.3 Trace Inductance

The inductance of a DIB trace depends on the shape and size of the trace, as well as the geometry of the signal path through which the currents flow to and from the load impedance. Figure 15.7 shows a signal source feeding a load impedance through a pair of signal lines. In this example, the current is forced to return to the source through a dedicated current return line. The signal line and the current return line form a loop through which the load current flows. The larger the area of this loop, the higher the inductance of the signal path. This inductance can be modeled as a single inductor in series with the signal source, as shown in Figure 15.8.

A parasitic inductance such as the one in Figure 15.8 is generally an undesirable circuit component. We wish to minimize the effects of parasitic trace inductance on the DUT and DIB circuits. There are a number of ways to reduce this inductance. The first way is to minimize the area enclosed by the load current path. One easy way to do this is to lay a dedicated current return trace beside each signal trace. Of course, if we did this with every signal, we would have a very cluttered PCB layout. An easier way to obtain low inductance is to use one or more solid ground planes as current return paths.

By routing each signal trace over a solid ground plane, the load current can return underneath the trace along a path with very low cross-sectional area. The cross-sectional area can be minimized by placing the trace and ground plane very close together in the PCB layer stackup. Another way to reduce inductance is to make the trace as wide as is practical, since a wide trace over a

**Figure 15.7.** Signal source, load impedance, and current path.

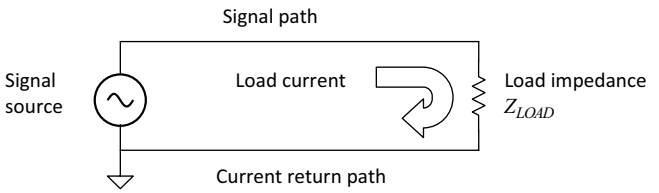



**Figure 15.8.** Schematic representation of signal path inductance.

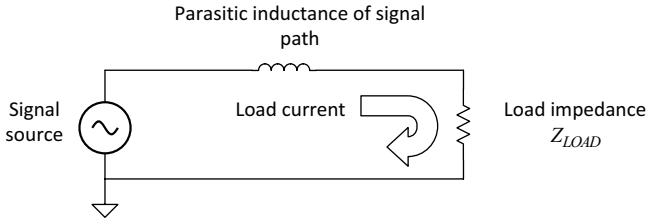
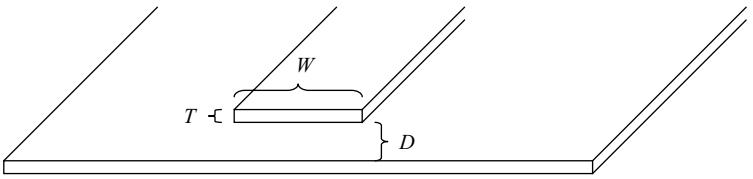



**Figure 15.9.** Cross section of a long trace over a ground plane (stripline).



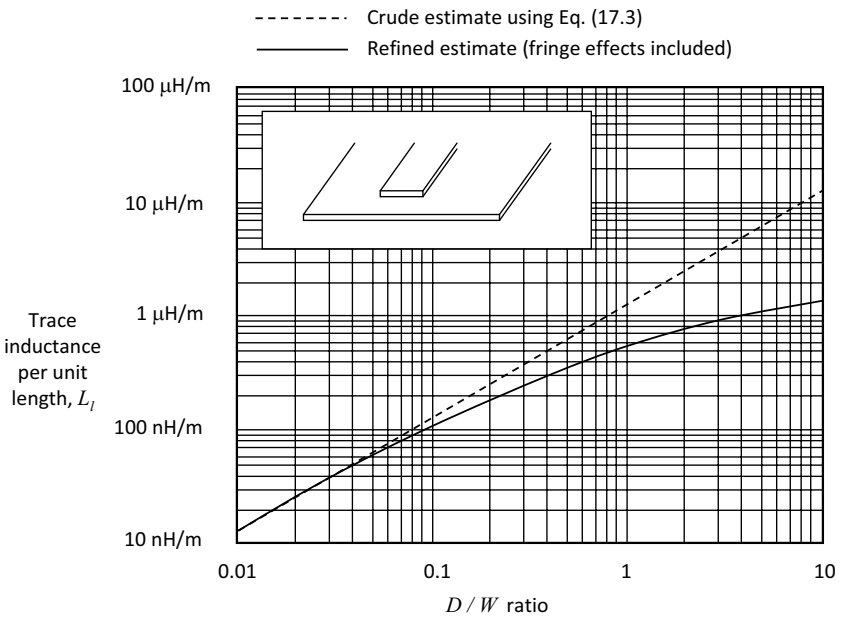

ground plane has minimal inductance. A thicker trace will also have somewhat less inductance, though PCBs are normally fabricated with trace thicknesses of 1 to 3 mils. We have less control over trace thickness than we have over trace width and layer spacing.

The inductance of a trace over a ground plane (examples are *microstrip* or *stripline* configurations) is dominated by the ratio of the trace-to-ground spacing, $D$, divided by the trace width, $W$ (Figure 15.9). The parasitic inductance of a wide trace routed over a ground or power plane can be estimated using the equation

$$L_l = \mu_0 \mu_r \frac{D}{W} \tag{15.3}$$

where $L_l$ is Inductance per unit length (H/m), $\mu_0$ is magnetic permeability of free space (400π nH per meter), $\mu_r$ is magnetic permeability of the PCB material divided by $\mu_0$, $W$ is trace width, and $D$ is separation between trace and ground plane.

**Figure 15.10.** Stripline trace inductance per meter versus *D/W* ratio ($\mu_r = 1$).




The value of $\mu_r$ is very nearly equal to 1.0 in all common PCB materials, so we can drop it from our calculations. The total inductance of the trace is directly proportional to the length of the trace

$$L = L_{TRACE} L_l \tag{15.4}$$

where $L$ is total inductance and $L_{TRACE}$ is trace length (meters).

Thus trace inductance increases as trace length increases and also increases as trace width decreases. Therefore, if we want to minimize parasitic inductance in PCB traces, we should make them as wide as possible, as short as possible, and as close to the ground or power plane as possible.

Unfortunately, Eq. (15.3) is only valid for traces in which $W >> D$. In most PCB designs, the width of the trace is not much larger than the trace-to-ground spacing. In these cases, the magnetic fields between the trace and ground plane are not uniform, making Eq. (15.3) invalid. Figure 15.10 shows a more accurate relationship between the space-to-width ratio and the inductance per meter of a trace over a ground plane.* The dashed line represents the inductance per meter as estimated using Eq. (15.3). As we can see, the more accurate estimation converges with the estimations using Eq. (15.3) as the value of $W$ becomes much larger than $D$.

It should be noted that the inductance of a stripline is approximately the same as the inductance of a trace over a second trace of equal size and shape. This is because most of the higher-frequency current returning through a stripline's ground plane returns directly underneath the stripline trace (i.e., the path of least inductance). However, the two-conductor configuration in

*The graph in Figure 15.10 was derived using a mathematical approximation, so its values should not be taken as absolutely accurate. However, the approximations are adequate for estimating the effects of parasitic elements on DIB circuits. The derivation of this graph and others in this chapter are based on electromagnetic field theory, a subject that is beyond the scope of this book.

**Figure 15.11.** Parallel traces on adjacent PCB layers.

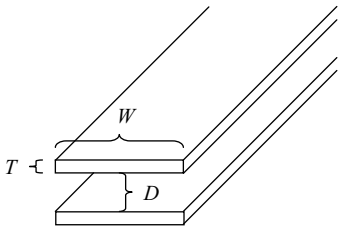
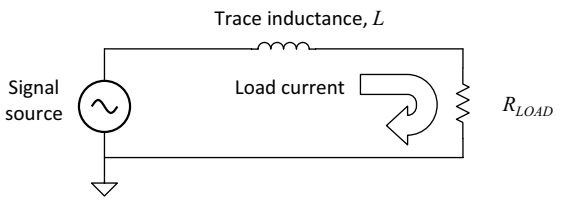



Figure 15.11 is seldom used in DIB design, since a ground plane permits a much easier means of achieving the same low inductance.

## EXAMPLE 15.2

Calculate the parasitic inductance of a trace having a 16-mil width, running over a ground plane for 6 in. The spacing between the trace and the plane is 8 mils. If this trace is connected in series with a 50-Ω resistor to ground (as in Figure 15.12), what is the 3-dB bandwidth of the low-pass filter formed by the trace inductance and the 50-Ω resistance? Can a 50-MHz sine wave be passed through the trace to the resistor without significant loss of amplitude? What is the phase shift caused by the inductance at 50 MHz?

**Figure 15.12.** Low-pass filter formed by trace inductance and load resistance.




**Solution:**
Combining Eqs. (15.3) and (15.4), we write

$$L = 6 \text{ in.} \times \frac{1 \text{ m}}{39 \text{ in.}} \times \pi \times 400 \frac{\text{nH}}{\text{m}} \times 1.0 \times \frac{8 \text{ mils}}{16 \text{ mils}} = 97 \text{ nH}$$

However, we can see from the graph in Figure 15.11 that the actual inductance per meter at a *D*/*W* ratio of 0.5 is lower than that predicted from Eq. (15.3). If we use the more accurate value of inductance per meter from this graph (about 350 nH per meter), then we get a more accurate prediction of the trace inductance. The refined estimation of inductance is

$$L = 6 \text{ in.} \times \frac{1 \text{ m}}{39 \text{ in.}} \times 350 \frac{\text{nH}}{\text{m}} = 54 \text{ nH}$$

The trace inductance and load resistance form an *RL* low-pass filter, as shown in Figure 15.12. The 3-dB cutoff frequency, $F_c$, of this *RL* low-pass filter is given by

$$F_C = \frac{R_{LOAD}}{2\pi L} \tag{15.5}$$

Thus the 3-dB bandwidth of the low-pass filter formed by the trace inductance and load resistor is equal to

$$F_C = \frac{50}{2\pi \cdot 54 \cdot 10^{-9}} = 147 \text{ MHz}$$

At a frequency *f*, the trace inductance and load resistance form a voltage divider having a transfer function equal to

$$H(f) = \frac{R_{LOAD}}{R_{LOAD} + Z_L(f)} \tag{15.6}$$

where $Z_L$ is the complex impedance of the trace inductance. Substituting $Z_L(f) = j2\pi fL$, calculating the magnitude of $H(f)$, and combining the result with Eq. (15.5) gives us the gain of the *RL* low-pass filter at any frequency *f*

$$\text{gain}(f) = |H(f)| = \left[ \frac{1}{\sqrt{1 + \left( \frac{f}{F_C} \right)^2}} \right] \text{ V/V} \tag{15.7}$$

At 50 MHz, the gain calculated using Eq. (15.7) is equal to = 0.947 V/V. Therefore, we get an attenuation due to the low-pass nature of the *RL* circuit that attenuates the 50-MHz sine wave by a factor of 0.947 V/V. This attenuation is probably unacceptable, unless we do not mind a 5% error in the amplitude of the signal at the load resistor.

The phase shift of the *RL* low-pass filter is given by

$$\Phi(f) = \angle H(f) = -\frac{180}{\pi} \tan^{-1}\left( \frac{f}{F_C} \right) \text{ degrees} \tag{15.8}$$

Thus, at 50 MHz, the phase shift produced by the trace inductance and resistance is equal to –18.7 degrees. This is a fairly serious phase error. If we wanted to measure phase mismatch or group delay at a frequency near 50 MHz, the parasitic inductance of this example would be completely unacceptable.

If we want to achieve less attenuation and phase shift due to the trace inductance in Example 15.2, we must either shorten the trace, widen the trace, or reduce the spacing between the trace and ground. The spacing between the trace and ground in this example is 8 mils, which is about as thin as we can reliably fabricate a PCB. Rather than trying to fabricate a board with even thinner layer spacing, it is much easier to simply widen the trace.

As we will see in the following sections, widening the trace or reducing the trace-to-ground spacing has the unfortunate side effect of increasing the parasitic capacitance of the trace to ground. The extra capacitance may be just as undesirable as having too much inductance. Therefore, the

**Exercises**

| | | |
|---|---|---|
| **15.1.** | Calculate the parasitic resistance of a 5.7-in. PCB trace having a width of 2.5 mm and a thickness of 2 mils. If this trace feeds a 2.5-V DC signal to a 1-Ω load resistance, what will be the error of the voltage at the load as a percentage of the source voltage? (Assume a zero-resistance current return path.) How much power is dissipated by the trace? | ANS. $R = 18$ mΩ; $V_{ERR} = -44$ mV = –1.77%; power = 109 mW. |
| **15.2.** | Using Eq. (15.3), calculate the parasitic inductance of a 23 cm PCB trace having a width of 12 mils, and a spacing of 15 mils to the current-return ground plane. If this trace feeds a 125 kHz, 1.25-V RMS sinusoidal signal to a 10-Ω load resistance, what will be the error of the RMS voltage at the load as a percentage of the source voltage? (Assume zero trace resistance). Compare your answers with those obtained using the refined inductance estimate of Figure 15.10. | ANS. Using Eq. (15.3), L = 361.3 nH and $V_{ERR} = -503$ μV = –0.04%. Using Figure 15.10, $L = 115$ nH and $V_{ERR} = -50.9$ μV = –0.004%. Eq. (15.3) yields significant error. |

best solution is to keep traces as short as possible, since this reduces both the trace inductance and trace capacitance to ground.

## 15.3.4 Trace Capacitance

The capacitance between two parallel traces such as those in Figure 15.11 can be estimated using the standard parallel plate capacitance equation. The parasitic capacitance between two metal plates of area $A$ is given by the equation

$$C = \varepsilon_r \varepsilon_0 \frac{A}{D} \tag{15.9}$$

where $A$ is area of either plate ($L_{\text{TRACE}} \times W$ for rectangular traces), $D$ is distance between the plates, $\varepsilon_0$ is electric constant* of free space ($8.8542 \times 10^{-12}$ F/m), and $\varepsilon_r$ is relative dielectric constant† of the dielectric material between the plates.

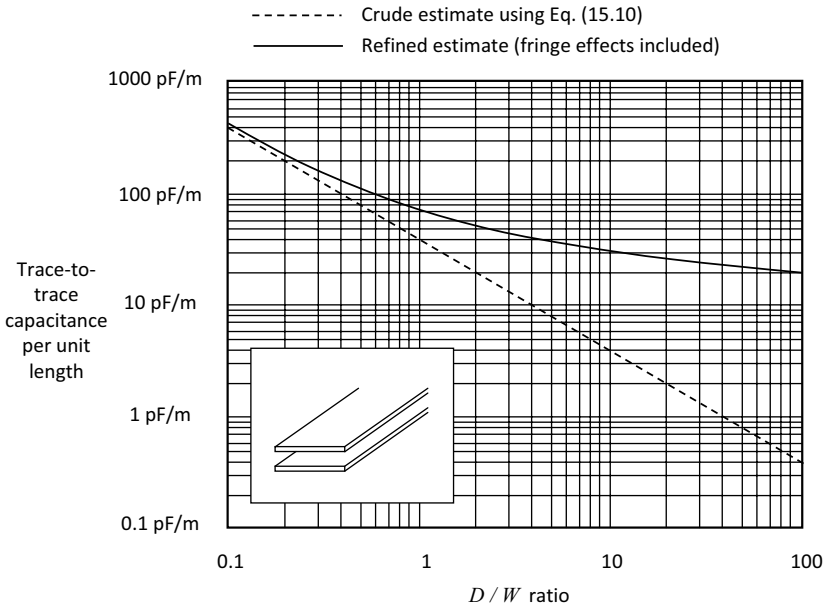
The value of $\varepsilon_r$ depends on the PCB insulator material. Air, for example, has a relative dielectric constant very near 1.0, while FR4 fiberglass has a relative dielectric constant of about $\varepsilon_r = 4.5$. Teflon®, by contrast, has a relative dielectric constant of about $\varepsilon_r = 2.7$. Therefore, Teflon® PCBs exhibit less capacitance per unit area than FR4 PCBs.

Equation (15.9) is only accurate for capacitor plates in which the length and width of the plates is much larger than the dielectric thickness, $D$. If $W$ is about 10 times larger than $D$, then we can use Eq. (15.9) to estimate the capacitance per unit length of the trace

$$C_l = \frac{C}{L_{TRACE}} = \varepsilon_r \varepsilon_0 \frac{A/L_{TRACE}}{D} = \varepsilon_r \varepsilon_0 \frac{W}{D} \tag{15.10}$$

*The electric constant $\varepsilon_0$ is also known as vacuum permittivity or permittivity in free space.
†The (relative) dielectric constant $\varepsilon_r$ is also known as relative permittivity.

**Figure 15.13.** Trace capacitance per meter versus $D/W$ ratio ($\varepsilon_r = 4.5$).




To calculate the total capacitance between two traces, we multiply the capacitance per unit length by the trace length. This is true for the configuration in Figure 15.11 as well as for any other configuration illustrated in this chapter.

$$C = L_{TRACE} \cdot C_l \tag{15.11}$$

When either the length or width is less than about 10 times the dielectric thickness, the so-called *fringe effects* in the electric field between the plates cause Eq. (15.10) to become inaccurate. Unfortunately, trace capacitance can seldom be accurately calculated using Eq. (15.10) since the width of the trace is often less than 10 times the trace to trace spacing. The graph in Figure 15.13 shows a more accurate estimation of the capacitance per meter between two parallel traces. The dashed line shows the capacitance per unit length as calculated by Eq. (15.10). Note that as the value of $W$ becomes much larger than $D$, the refined estimation converges with the estimation from Eq. (15.10).

The chart in Figure 15.13 assumes a relative dielectric constant, $\varepsilon_r$, of $\varepsilon_r = 45$. If our PCB material has a different relative dielectric constant, $\varepsilon'$, then we simply multiply the capacitance per unit length obtained from Figure 15.13 by the ratio of $\varepsilon'/4.5$ to calculate the correct capacitance per unit length. Equivalently, we can multiply the total capacitance (calculated using Eq. (15.11)) by $\varepsilon'/4.5$ to achieve the same result.

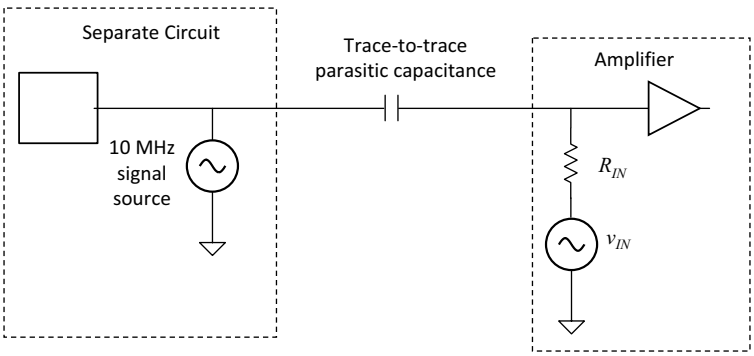
Example 15.3 shows how important it is to keep high-impedance nodes protected from potential sources of crosstalk. The best form of crosstalk prevention is to simply keep the sensitive trace as short as possible. Another method for reducing crosstalk is to place a ground plane underneath the critical signal traces, thus preventing layer-to-layer crosstalk such as that in Example 15.3. Each of the traces would then see a parasitic capacitance to ground, but the ground plane would block the trace-to-trace capacitance altogether. The effect of a ground plane on trace-to-trace capacitance is illustrated in Figure 15.15. The trace-to-trace capacitance is replaced by two parasitic capacitances to ground. This effectively shunts the offending source to ground so that it cannot inject its signal into the sensitive node.

## EXAMPLE 15.3

An insulator thickness of 10 mils separates a pair of 12-mil-wide traces on adjacent layers in a multilayer FR4 DIB. One trace is 7 in. long, while the other is 5 in. long. The traces run directly over one another for a distance of 3 in., as shown in Figure 15.13, but do not cross each other at any other point. The upper trace carries a 10-MHz sine wave at 1.0 V RMS, while the lower trace is connected to an amplifier with an input impedance of 100 kΩ. What is the signal level of the crosstalk coupling from the 10-MHz signal into the input of the amplifier? Would a Teflon® PCB reducethe capacitance enough to give significantly better performance?

**Solution:**
First, we draw a model of the signal source and amplifier stage, including the parasitic trace-to-trace capacitance (Figure 15.14). The parasitic capacitance between the two traces will interact with the 100-kΩ input impedance of the amplifier to form a first-order high-pass filter.

**Figure 15.14.** Parasitic capacitance between a signal source and a high-impedance amplifier input.




To estimate the value of the capacitance between the two traces, we first need to calculate the *D*/*W* ratio of this parasitic capacitor. The value of *D* is 10 mils, while the value of *W* is 12 mils. Thus the *D*/*W* ratio is equal to 0.833. From the graph in Figure 15.13 we can estimate a trace-to-trace capacitance of about 85 pF per meter. Applying Eq. (15.11), we calculate the total capacitance:

$$C = 3\,\text{in.} \cdot \frac{1\text{m}}{39\,\text{in.}} \cdot 85\text{pF/m} = 6.5\ \text{pF}$$

The 3-dB cutoff frequency of an *RC* high-pass filter is given by

$$F_C = \frac{1}{2\pi RC} \qquad \textbf{(15.12)}$$

Using Eq. (15.12), we calculate the cutoff frequency

$$F_C = \frac{1}{2\pi \cdot 100 \times 10^3 \cdot 6.5 \times 10^{-12}} = 245 \text{ kHz}$$

Because the 10-MHz signal is well beyond the cutoff frequency, this would be a very bad DIB design.Using a Teflon® PCB rather than an FR4 fiberglass PCB, we would multiply the 6.5 pF capacitance by a factor of 2.7/4.5 (2.7 = relative permittivity of Teflon®, 4.5 = relative permittivity of FR4 fiberglass). This would result in a capacitance of 3.9 pF. The value of $F_c$ would change to 408 kHz, which would not significantly reduce the crosstalk. To solve the crosstalk problem in this example, the traces must be moved farther away from one another. Also, the sensitive 100-kΩ line should be shortened to a fraction of an inch to minimize capacitive coupling from the 10-MHz signal source as well as any other potential sources of crosstalk.

The amount of capacitance between a trace and a ground plane (see Figure 15.9) is tricky to calculate. If the length and width of the trace are much larger than the trace-to-ground separation, then we can simply use Eq. (15.10) to calculate the capacitance per unit length. For most practical situations, though, the width of the trace is not much larger than the trace-to-ground separation. We again have to resort to a more accurate estimation, as shown in Figure 15.16. The dotted line shows the capacitance per unit length as calculated using Eq. (15.10). The solid line represents a more accurate calculation that takes the fringing effects of the electric fields into account. As expected, the two lines converge as $W$ becomes much larger than $D$.

Next we consider the capacitance between two parallel traces on the same PCB layer (Figure 15.17). This configuration occurs very frequently in PCB designs, since many traces run parallel to each other for several inches on a typical DIB.

If the trace-to-trace spacing, $S$, is equal to or larger than the trace width, $W$, we can approximate this configuration as two circular wires having the same cross-sectional area as the traces and

**Figure 15.15.** Ground planes prevent layer-to-layer crosstalk.

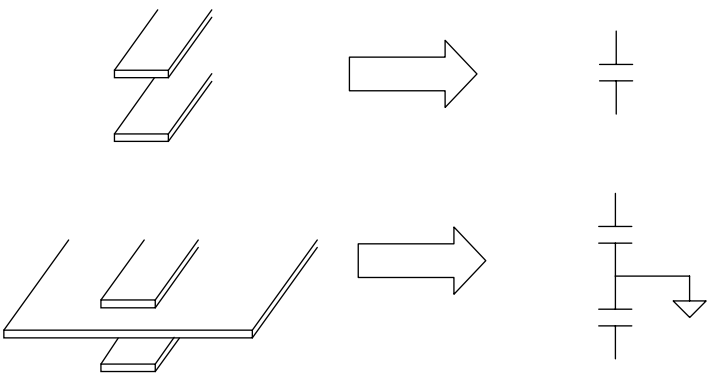


**Figure 15.16.** Trace capacitance per meter versus $D/W$ ratio ($\varepsilon_r = 4.5$).

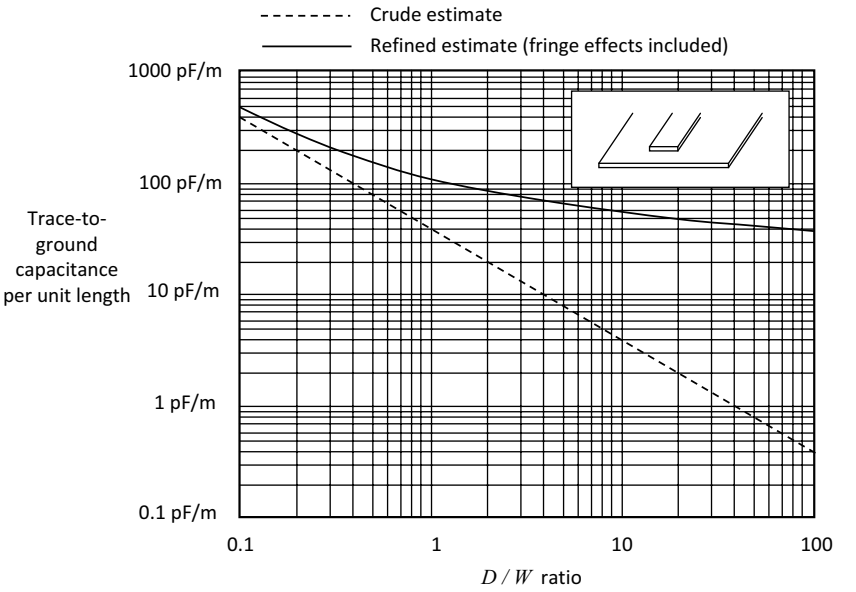
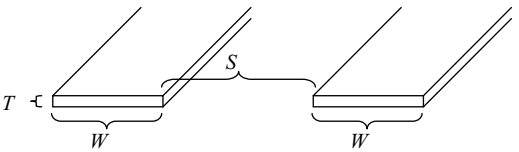



**Figure 15.17.** Coplanar PCB traces.




having a center-to-center spacing of $S+W$. The equation for the capacitance per unit length of two circular conductors having this geometry is given by[1]

$$C_l = \left[ \frac{12.1 \times 10^{-12} \cdot \varepsilon_r}{\log_{10}\left[ \frac{\left(\frac{S+W}{2}\right)}{\sqrt{\frac{T \cdot W}{\pi}}} + \sqrt{\frac{\left(\frac{S+W}{2}\right)^2}{\frac{T \cdot W}{\pi}} - 1} \right]} \right] \tag{15.13}$$

where $C_l$ is capacitance per unit length (F/m), $\varepsilon_0$ is electrical constant, $\varepsilon_r$ is relative dielectric constantof the PCB material, $W$ is width of the rectangular trace, and $T$ is thickness of the rectangular trace.

Comparing this crude circular conductor approximation to a more accurate estimation based on flattened rectangular traces, we can see how closely the two approximations agree with one

**Figure 15.18.** Capacitance between two coplanar traces of equal width ($\varepsilon_r = 4.5$).

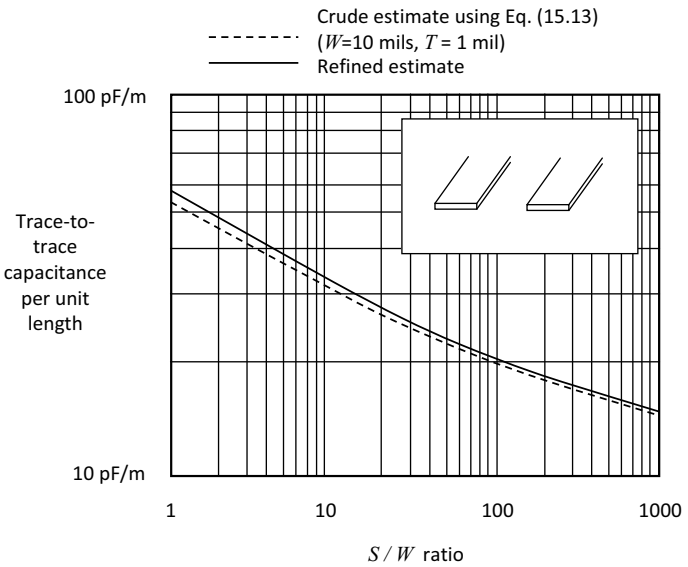
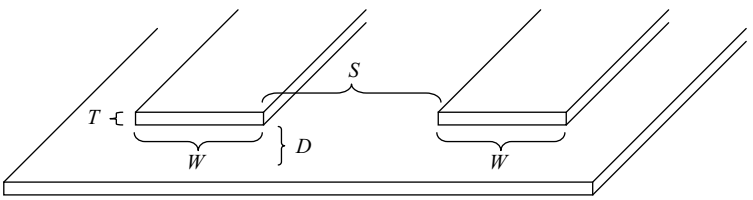



**Figure 15.19.** Coplanar traces over a ground plane.




another (Figure 15.18). The dashed line shows the trace-to-trace capacitance per unit length using Eq. (15.13) while the solid line shows a more accurate calculation based on a flat trace geometry. These estimates are close enough to each other that Eq. (15.13) can probably be used in many cases as a reasonably good approximation.

We can reduce the effects of trace-to-trace crosstalk between coplanar traces using a ground plane. Figure 15.19 shows a pair of coplanar traces with a width of $W$ separated from one another by a distance $S$ and spaced a distance $D$ over a ground plane.

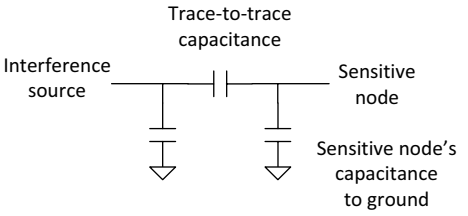
The ground plane forms two parasitic capacitances to ground that serve to shunt the interference signal to ground (Figure 15.20). While this may not eliminate the crosstalk, it reduces it by a significant amount. From Figure 15.16 and Figure 15.18, we can see that the trace-to-ground capacitance will be several times larger than the trace-to-trace capacitance for values of $S > D$. Thus, if we lay out our traces so that the trace-to-trace spacing, $S$, is larger than our trace-to-ground spacing, $D$, we can make the shunt capacitance larger than the trace-to-trace coupling capacitor. This forms a capacitive voltage divider with good interference rejection.

When working with RF frequencies, a more prudent approach to quantifying the parasitics present with each interconnection is to simulate the structure using a CAD tool. This will not only

**Exercises**

| | |
|---|---|
| **15.3.** Using Eq. (15.10), calculate the parasitic capacitance of a 14-cm-long, 25-mil-wide stripline trace with a spacing of 8 mils to the ground plane, fabricated on an FR4 PCB. Compare your answer with that obtained using the refined capacitance estimate of Figure 15.16. | ANS. Using Eq. (15.10), $C = 17.4$ pF; using Figure 15.16, $C = 28$ pF; Eq. (15.10) yields significant error. |
| **15.4.** Using Eq. (15.13), calculate the parasitic capacitance between two 4-cm-long, 16-mil-wide coplanar traces separated by a spacing of 30 mils, fabricated on an FR4 PCB. Compare your answer with that obtained using the refined capacitance estimate of Figure 15.18. | ANS. Using Eq. (15.13), $C = 1.61$ pF; using Figure 15.18, $C = 1.6$ pF; Eq. (15.13) agrees very well. |
| **15.5.** Using Eq. (15.10), calculate the parasitic capacitance of a 7.3-inch-long, 25-mil-wide stripline trace with a spacing of 10 mils to the ground plane, fabricated on a Teflon® PCB. This trace feeds a 50-kHz, 1.25-V RMS sinusoidal signal from a DUT output having a 100-kΩ output resistance to a buffer amplifier having an input capacitance of 2 pF. How much will the combined capacitance of the trace and buffer amplifier input capacitance attenuate the DUT signal? (Express your answer as a voltage gain in decibels.) Would this be an acceptable attenuation if the signal were the output of a gain test having ±0.8-dB limits? Compare your answer with that obtained using the refined capacitance estimate of Figure 15.16. | ANS. Using Eq. (15.10), $C = 11$ pF + 2 pF, $G$ (50 kHz) = -0.69 dB, acceptable; using Figure 15.16, $C$=20 pF + 2 pF, $G$(50 kHz) = –1.72 dB, not acceptable. |

**Figure 15.20.** Equivalent circuit for coplanar traces over a ground plane.




give better accuracy, but will also include effects caused by, for example, adjacent lines causing mutual inductance. We will have more to say about these CAD tools in a moment.

## 15.3.5 Shielding

Electrostatic shields can also be used to reduce coplanar trace-to-trace crosstalk. A shield is any conductor that shunts electric fields to ground (or a similar low-impedance node) so that the fields do not couple into a sensitive trace, causing crosstalk.[4] The electric fields can originate from external noise sources such as radio waves or 60-Hz power line radiation, or they can originate

**Figure 15.21.** Electrostatic shielding reduces trace-to-trace crosstalk.

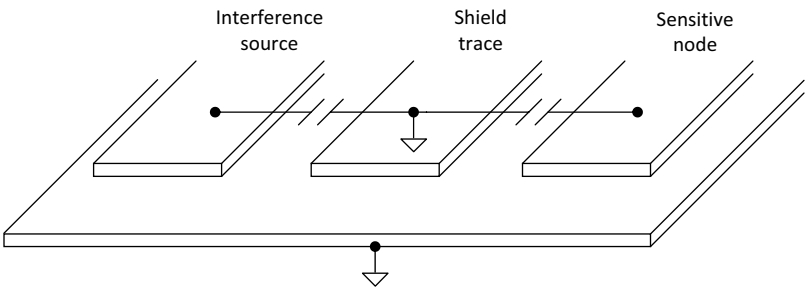
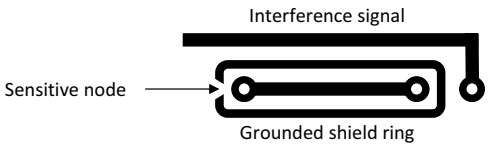



**Figure 15.22.** Shield trace routed around a sensitive node.




from other signals on the DIB. The ground plane in Figure 15.15 is one type of electrostatic shield. Ideally, a shield should completely enclose the sensitive node. A coaxial cable is one example of a fully shielded signal path. In most cases, it is impractical to completely shield every signal on a DIB using coaxial cables. However, we can achieve a close approximation of a fully shielded signal path by placing shield traces around sensitive signal traces. This configuration is called *coplanar shielding*.

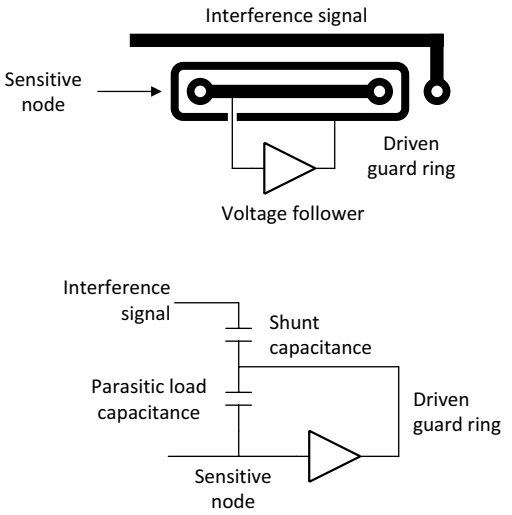
Figure 15.21 illustrates how coplanar shielding can reduce crosstalk between a interference source and a sensitive DIB signal. The shield trace is connected to the ground plane to provide an extra level of protection for the sensitive node. Sometimes, a shield trace is routed all the way around a sensitive node, as illustrated in Figure 15.22. This type of shielding helps to reduce the coupling of electromagnetic interference from all directions.

### 15.3.6 Driven Guards

Electrostatic shields suffer from one small drawback. The shield forms a parasitic load capacitance between the sensitive signal and ground. The parasitic capacitance is both a blessing and a curse. It is a blessing because it shunts interference signals to ground, but a curse because it loads the sensitive node with undesirable capacitance. The capacitive loading problem can be largely eliminated using a driven guard instead of a shield. A driven guard is a shield that is driven to the same voltage as the sensitive signal. The guard is driven by a voltage follower connected to the sensitive node (Figure 15.23). The interference signal is shunted to the low-impedance output of the voltage follower, reducing its ability to couple into the sensitive signal node. A common mistake made by novice test engineers is to connect the tester's driven guards to analog ground. As seen in Figure 15.23, this is obviously a mistake.

The voltage follower drives the guard side of the parasitic load capacitance to the same voltage as the sensitive signal line. Since the parasitic load capacitance always sees a potential difference of 0 V, it never charges or discharges. Thus, the loading effects of the parasitic capacitance on the signal trace are eliminated by the voltage follower.

**Figure 15.23.** Driven guard—PCB layout and equivalent circuit.




Of course, all voltage followers exhibit a finite bandwidth. Therefore, the parasitic capacitance can only be eliminated at frequencies within the voltage follower's bandwidth. For this reason, driven guards are typically used on relatively low frequency applications that cannot tolerate any crosstalk (e.g., high-performance audio circuits).

## 15.4 TRANSMISSION LINES

The previous section outlined the critical parameters of transmission lines for analog and mixed signal applications. This section will discuss the applications of transmission lines for RF circuits and device interface boards.

### 15.4.1 Various TEM Transmission Line Configurations

Here we will provide a brief summary of the most commonly used transmission line types for an RF DIB. This includes a coaxial line, a stripline, a microstrip line, a coplanar waveguide, and a coupled transmission line. The geometry of each line will offer its own advantages and disadvantages. A detail theoretical description is given in reference 5.

#### *Coaxial Line*

The coaxial line shown in Figure 15.24 provides perfect shielding, and its propagating energy does not radiate. This type of line is most commonly used to interface the ATE test head to the DIB. It generally consists of an SMA or SMP connector-type flexible cable assembly, which allows for flexible routing and easy access for debugging of RF circuits. The impedance of a coaxial line can be approximated by

$$Z = \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}}\ln\left(\frac{D}{d}\right) \approx \frac{138\ \Omega}{\sqrt{\varepsilon_r}}\log\left(\frac{D}{d}\right) \tag{15.14}$$

**Figure 15.24.** Coaxial RF transmission line.

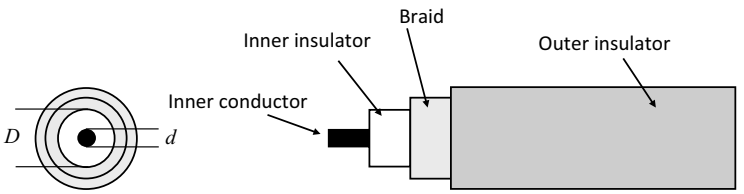
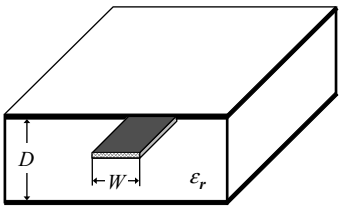



**Figure 15.25.** RF stripline with line width *W*, board thickness *D* and board dielectric constant $\varepsilon_r$.




where *D* is the diameter of the braided conductor and *d* is the diameter of the inner conductor as shown in Figure 15.24.

### *Stripline*

The stripline shown in Figure 15.25 is realized in printed circuit boards by placing the RF line symmetrically in between two parallel ground planes. These ground planes shield the RF lines when they are both connected through several vias. The stripline allows for low-cost integrated passive load board elements, like directional couplers and filters. The stripline configuration is most commonly used when high signal integrity is required and a well controlled via process is available to route the RF signal between the different board layers. A minor disadvantage is that striplines are not accessible for debugging and matching, and any access to this line will be made with a via, which is a discontinuity in itself.

### *Microstrip Line*

Another variation of a stripline is as an open center conductor trace on the top layer of the PCB just above a ground plane. This is called a microstrip transmission line, and it is the most commonly used transmission line geometry for RF circuits (Figure 15.26). This configuration allows easy access for debugging purposes, and it allows for the addition of components to tune the RF performance when necessary if a GND plane is placed just below it.

One significant difference between the microstrip line and the stripline, and coaxial line configuration is that the dielectric medium through which the electromagnetic wave is traveling is not homogeneous, since parts of the EM wave will be in the PCB board with dielectric constant $\varepsilon_r$ and the other part will be in the free air space above the line, which causes different phase velocities and wavelengths (see also Section 12.2.1). This effect is called dispersion. Since the EM wave propagates in two different dielectric media, it is necessary to calculate the effective dielectric constant $\varepsilon_{r,\,eff}$ ,which lies somewhere between the values of the relative dielectric constant of the PC board, and substrate and air. The effective dielectric constant is also dependent on the line

**Figure 15.26.** RF microstrip line with line width *W*, board thickness *D*, and board dielectric constant $\varepsilon_r$.

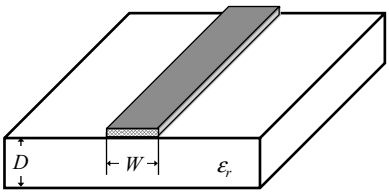
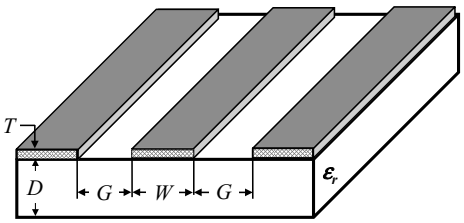



**Figure 15.27.** Coplanar waveguide with adjacent GND planes.




width *W* and the thickness of the dielectric material *D*. For higher frequencies, even the line thickness and surface roughness has an impact on the propagating parameter. There are multiple programs on the market for calculating or analyzing line parameters. Some of the most commonly used ones are LINECALC of the Agilent EESOF package, AWR's TXLINE, or Ansoft's TRL.

### *Coplanar Waveguide*

Coplanar waveguide (CPW) was invented in 1969 by Cheng P. Wen, who worked for RCA Laboratories. CPW is formed from a conductor separated from a pair of adjacent ground planes as shown in Figure 15.27. For the ideal case, the thickness of the dielectric *D* is infinite, while in practice it needs to be thick enough so that the entire EM field will fit within the substrate. A variance of the CPW is a grounded coplanar waveguide (GCPW), where a ground plane is positioned on the opposite site of the substrate. The main advantage of CPW is that it provides an extremely high frequency response, because it uses no vias in the ground path. This is quite unlike that which occurs with striplines or microstrip lines where the presence of vias introduce parasitic discontinuities. A disadvantage of the CPW approach is that it requires substrate space, as the ground plane is placed on the component side of the board. The line impedance depends on the ratio of the strip width *W* to the ground plane spacing *G*, which allows for a given board thickness to control a wide variance of line impedances. Another advantage of CPW is that it offers a good transition to the coaxial board connector.

### *Coupled Transmission Lines*

Coupled transmission lines are built by placing two uniform transmission lines close enough to each other so that their EM fields interact as shown in Figure 15.28. The interaction between each EM field is usually controlled by the separation distance *S* between each line. Typical applications for coupled transmission lines are directional couplers, or the lines connecting balanced

**Figure 15.28.** Coupled microstrip lines.

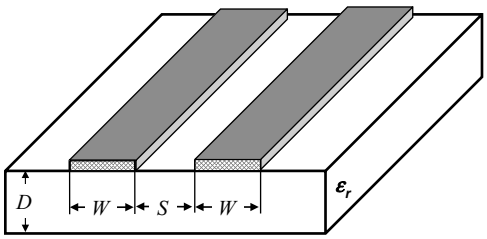
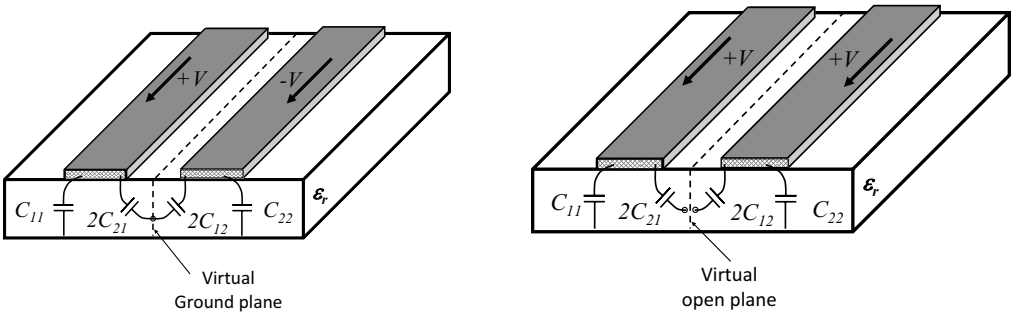



**Figure 15.29.** Coupled transmission line with (a) even mode configuration and (b) odd mode.




(differential) device ports. The line impedance is a function of the line width *W* and the board thickness *D*, as well as the separation distance between the two lines *S*.

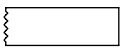
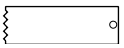
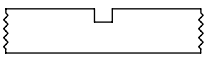
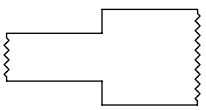
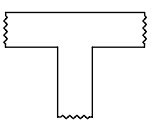
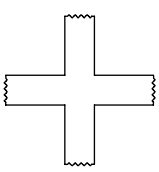
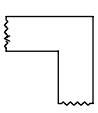
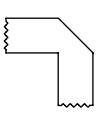
The EM field of a coupled transmission line is somewhat more complex than the EM field of a single line, because the combined fields will have two different configurations. When the two lines are driven with the same in-phase signal as shown in Figure 15.29a, we refer to it as the even mode response. When both signals are out of phase as shown in Figure 15.29b, we refer to it as the odd mode response. Therefore, a coupled line has two sets of parameters, even and odd mode impedances, even and odd mode losses, and so forth. Only the electrical length will be the same, since it does not depend on the phase of the wave.

## 15.4.2 Transmission Line Discontinuities

Most RF DIBs will not use transmission line discontinuities as part of its design—for example, for a filter. It is important to understand the fundamental impact of line elements. Every time an EM wave hits a discontinuity in a transmission line, the RF current will crowd, which will behave like an inductor, or the electrical field will fringe, which makes it have a capacitance effect.

The most common discontinuities in transmission lines are shown below in Table 15.1. For the best and simplest design of an RF DIB, it is recommended to avoid any line discontinuities. As shown in Table 15.1, it should be obvious that RF lines cannot be connected in a tee or cross configuration without creating a new RF element. When designing the landing pattern for an RF-socket, it is recommended to avoid any open line stubs by following the recommendation provided by the specific socket vendor. Steps can be avoided by tapering the end, thereby making the transition of the line width smooth.

**Table 15.1.** Typical Discontinuities in Transmission Lines and Their Impact to the Wave Propagation

| | | |
|---|---|---|
| Open line stub |  | An open line stub or unterminated transmission line will cause a stray capacitance at the open end, as long the electrical length is less than 90°. |
| Shorted line stub |  | A shorted line stub behaves as an inductance, as long the electrical length is less than 90°. |
| Notch |  | A notch is built by a cut into the transmission line and can be represented by a series inductor. |
| Step |  | Two transmission lines with different line widths are connected to build a step. The current crowding takes place on both sides of the junction, and causes a stray capacitance on the wider line open edge. |
| Tee |  | Two lines are connected at a junction with a tee. The tee causes an excess capacitance to ground. |
| Cross |  | Two lines are crossing results in a complex discontinuity, which needs to be simulated with an EM simulation tool. |
| Bend |  | A line turning with a high angle leads to a significant discontinuity. The bend can be formed in a radius of at least three times the line width or by a mitered bend to avoid this. |
| Mitered bend |  | A mitered bend reduces the area of metallization of a bend, which leads to a reduction of excess capacitance. The mitered bend consumes less area of the DIB with similar RF performance, compared to a curved path. |

## 15.4.3 Lumped- and Distributed-Element Models

In Example 15.2, we treated the PCB trace feeding the 50-Ω load resistor as if it had no capacitance to ground. In reality, the *RL* low-pass filter formed by the trace inductance and load resistance also includes a parasitic capacitance to ground, as shown in Figure 15.30. This simplistic model of a transmission line is known as a *lumped-element* model. The series inductance per unit length of the 6-in. trace in Example 15.2 was found to be 350 nH per meter. From the graph in Figure 15.30, we can determine that the capacitance per unit length of this trace is about 160 pF per meter, assuming FR4 PCB material. Therefore, the capacitance in Figure 15.30 is

**Figure 15.30.** Parasitic trace inductance and capacitance (lumped-element model).

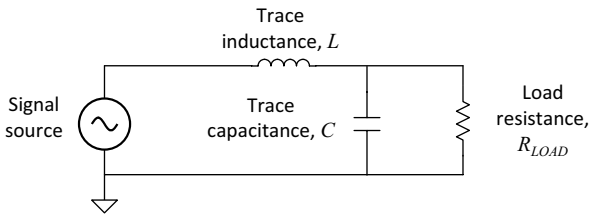
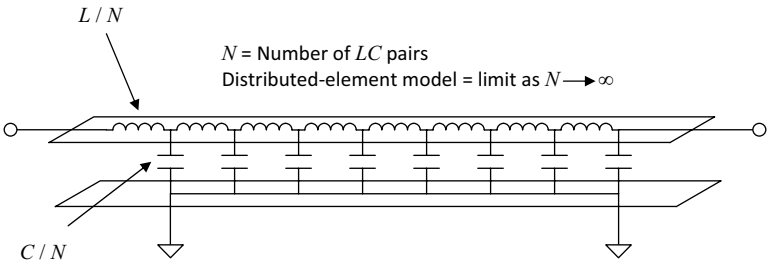



**Figure 15.31.** Distributed-element model of a transmission line.




about 160 pF/m × [6 in.×(1 m/39 in.)] = 24.6 pF. At 50 MHz, this capacitance has an impedance of 130 Ω, which is not insignificant when placed in parallel with the 50-Ω load resistance. Therefore`, we should consider the trace inductance as well as the capacitance when evaluating the effects of trace parasitics on circuit performance.

Unfortunately, even the refined lumped-element model of Figure 15.30 becomes deficient at higher frequencies. In reality, the parasitic trace inductance and capacitance can only be modeled as a lumped inductance and capacitance at relatively low frequencies. At higher frequencies, we have to realize that the inductance and capacitance are distributed along the length of the trace. The effect of this distributed inductance and capacitance causes the true model of the trace to look more like an infinite series of infinitesimally small inductors and capacitors, as shown in Figure 15.31. This model is known as a *distributed-element* model. If we let the number of inductors and capacitors approach infinity as their values approach zero, the PCB trace becomes a circuit element known as a *transmission line*. The transmission line exhibits unique electrical properties, which the test engineer needs to understand.

As the voltage at the input to a transmission line changes, it forces current through the first inductor into the first capacitor. In turn, the rising voltage on the first capacitor forces current through the second inductor, into the second capacitor, and so on. The signal thus propagates from one *LC* pair to the next as a continuous flow of inductive currents and capacitive voltages. Notice that the transmission line is symmetrical in nature, meaning that signals can propagate in either direction through this same inductive/capacitive process.

Parallel trace pairs can form a transmission line as shown in Figure 15.31. These two traces can represent a stripline, a microstrip line, or a coaxial line. For the most part, these transmission

lines are governed by the exact same equations. For example, one of the key parameters of a transmission line is its *characteristic impedance*, defined as

$$Z_0 = \sqrt{\frac{L_l}{C_l}} \tag{15.15}$$

where $Z_0$ is characteristic impedance of the transmission line, $L_l$ is trace inductance per unit length, and $C_l$ is trace capacitance per unit length.

Notice that the characteristic impedance of a trace or cable is not dependent on its length. It is dependent only on the inductance per unit length and on the capacitance per unit length. Therefore, a 6-in. trace of a particular width and spacing to ground has the same characteristic impedance as one that is 10 ft long.

Signals injected into a transmission line travel down the line at a speed determined by the inductance and capacitance per unit length. The equation for the signal velocity $v_{signal}$ is

$$v_{signal} = \sqrt{\frac{1}{L_l \cdot C_l}} \quad \text{m/s} \tag{15.16}$$

The total time it takes a signal to travel down a transmission line is therefore equal to the length of the line divided by the signal velocity. This time is commonly called the transmission line's *propagation delay* $T_d$,

$$T_d = \frac{l_{line}}{v_{signal}} = l_{line}\sqrt{L_l \cdot C_l} \quad \text{s} \tag{15.17}$$

Combining Eqs. (15.11), (15.15), and (15.17), we can find the total distributed capacitance of a transmission line as a function of its propagation delay and characteristic impedance:

$$C = \frac{T_d}{Z_0} \text{ F} \tag{15.18}$$

The wavelength of a sine wave travelling along a transmission line is given by

$$\lambda_{signal} = \frac{v_{signal}}{f_{signal}} \quad \text{m/cycle} \tag{15.19}$$

If the wavelength of a signal's *highest-frequency component of interest* is significantly larger than the length of the transmission line, we can use a lumped-element model, such as the one in Figure 15.30. Note that the highest-frequency component of a digital signal such as a square wave is determined by its rise and fall time, not by its period. A common rule of thumb for a digital signal is that the wavelength of the highest-frequency component must be 10 to 20 times the transmission line length before we can treat the line as a lumped-element model. Otherwise, we must treat the signal path as a transmission line with distributed rather than lumped parasitic elements. Another way to state this is that the period of the signal should be at least 10 times larger than the transmission line's propagation delay before we can treat the parasitic elements as lumped, rather than distributed. Another practical rule of thumb is that the highest-frequency component of interest in a digital signal is roughly equal to 1/3 the inverse of its rise or fall time.

In the case of RF devices transmitting analog information, most of the time we can assume sinusoidal signals with a single given frequency $f_{signal}$. For this case the wavelength can be calculated using Eq. (15.19). For RF systems and devices with multiple RF signals, the wavelength

of the highest frequency needs to be considered when designing the PCB board as mentioned in Chapter 12, Section 2.1.

## EXAMPLE 15.4

Determine the characteristic impedance of the PCB trace in Example 15.2 made from FR4 material. What is the velocity of a signal traveling along this transmission line? At what fraction of the speed of light does it travel? What is the propagation delay of this line? If we wish to transmit a 50-MHz sine wave along this trace, should we treat the parasitic capacitance and inductance as lumped elements, or should we treat the trace as a transmission line?

**Solution:**
Because the *D*/*W* ratio of this trace is 0.5, using Figure 15.10 we find that the inductance per unit length is 350 nH per meter. Similarly, using Figure 15.16, we find the capacitance per unit length to be 160 pF per meter. Using Eq. (15.15), the characteristic impedance of the trace is then found to be

$$Z_0 = \sqrt{\frac{350\frac{\text{nH}}{\text{m}}}{160\frac{\text{pF}}{\text{m}}}} = 46.77\ \Omega$$

The velocity of a signal traveling along this line is given by Eq. (15.16) as

$$v_{signal} = \sqrt{\frac{1}{350\frac{\text{nH}}{\text{m}} \times 160\frac{\text{pF}}{\text{m}}}} = 133.63 \times 10^6\ \text{m/s}$$

The speed of light, $c_0$, is $300 \times 10^6$ m/s. Therefore, signals travel down this transmission line at a speed of 133.63/300 times the speed of light, or 0.445*c*.

The propagation delay can be calculated using either of two methods. First we can divide the length of the transmission line by the signal velocity:

$$T_d = \frac{l_{line}}{v_{signal}} = \frac{6\ \text{in.} \times \frac{1\ \text{m}}{39\ \text{in.}}}{133.63 \times 10^6\ \text{m/s}} = 1.15\ \text{ns}$$

An alternative calculation uses Eq. (15.18) to find

$$T_d = C \cdot Z_0 = 24.6\ \text{pF} \times 46.77\ \Omega = 1.15\ \text{ns}$$

The wavelength of a 50-MHz signal, as calculated using Eq. (15.19), is

$$\lambda_{signal} = \frac{133.63 \times 10^6\ \text{m/s}}{50\ \text{MHz}} = 2.67\ \text{m}$$

Since the length of the trace is only 6 in. and the wavelength of the 50-MHz signal is much larger (2.67 m × 39 in./m = 104 in.), we can safely treat this line as a lumped-element model.

### 15.4.4 Transmission Line Termination

Transmission lines can behave in a fairly complicated manner. We have discussed some of this behavior in Chapter 12 when defining the reflection coefficient for RF lines. Although their behavior is well-defined, a full study of transmission line theory is beyond the scope of this book, however, the theory required to design a good DIB will be explained in this subsection.

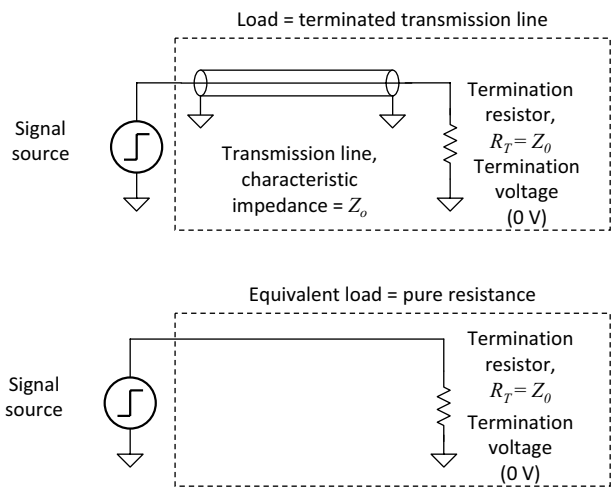
Fortunately, we can easily predict the basic behavior of a transmission line as long as we provide proper termination at one or both of its ends, as we have already seen in Chapter 12. Here we will apply a simple model sufficient for all mixed signal DIB designs.

To understand the purpose of transmission line termination, let us first examine the behavior of an unterminated line. An unterminated transmission line behaves as a sort of electronic echo chamber. If we transmit a stepped voltage down an unterminated transmission line, it will bounce back and forth between the ends of the line until its energy is dissipated and the echoes die out. The energy can be dissipated as electromagnetic radiation, as well as heat in the source resistance and parasitic resistance in the line. The resulting reflections appear as undesirable ringing on the stepped signal. Properly chosen termination resistors placed at either the source side or the load side of a transmission line cause it to behave in a much simpler manner than it would behave without termination. The purpose of termination resistors is to dissipate the energy in the transmitted signal so that reflections do not occur.

The simplest termination scheme to understand is the far-end termination scheme shown in Figure 15.32. As shown in this diagram, transmission lines are commonly drawn in circuit schematics as if they were coaxial cables, even if they are constructed using a PCB trace. This is because the basic behavior of a transmission line is dependent only on its characteristic impedance and propagation delay, rather than its physical construction.

If the termination resistor $R_T$ is equal to the characteristic impedance of the transmission line, the transmitted signal will not reflect at all. The energy associated with the currents and voltages propagating along the transmission line is completely dissipated by the termination resistor. As far as the signal source is concerned, *a terminated transmission line looks just like a resistor whose value is equal to* $Z_0$. The distributed inductance and capacitance of the transmission line *completely disappear as far as the source is concerned*. The only difference between a purely resistive load and a terminated transmission line is that the signal reaching the termination resistor is

**Figure 15.32.** Terminated transmission line and resistive equivalent.

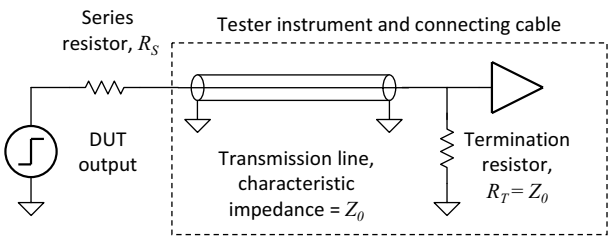


delayed by the propagation delay of the transmission line. It is also important to note that while the termination resistor is usually connected to ground (0 V), it can be set to any DC voltage, and the transmission line will still be properly terminated. The terminated line then appears to the source as a pure resistance connected to the DC termination voltage.

The ability to treat a terminated transmission line as a purely resistive element is very useful. Many tester instruments are connected to the DUT through a 50-Ω transmission line, which is terminated with a 50-Ω resistor at the instrument's input (see Figure 15.33). As far as the DUT is concerned, this instrument appears as a 50-Ω resistor attached between its output and ground. If the DUT output is unable to drive such a low impedance, we can add a resistor, $R_S$, between the DUT output and the terminated transmission line. The DUT output then sees a purely resistive load equal to $R_S + Z_0$. Although the signal amplitude is reduced by a factor of $Z_0/(Z_0 + R_S)$, we can compensate for this gain error using focused calibration (see Chapter 5).

If we observe the signals at the DUT output, the input to the transmission line, and the input to the tester instrument, we can see the effects of the resistive divider and the propagation delay of the transmission line as depicted in Figure 15.34. The signal is attenuated by the series resistor and termination resistor and is also delayed by a time equal to $T_d$.

**Figure 15.33.** Tester instrument with terminated transmission line.



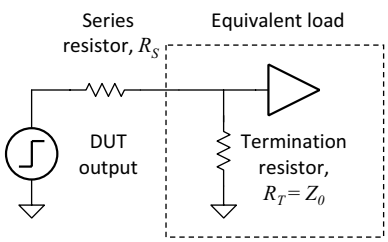




**Figure 15.34.** DUT output, transmission line input, and instrument input.

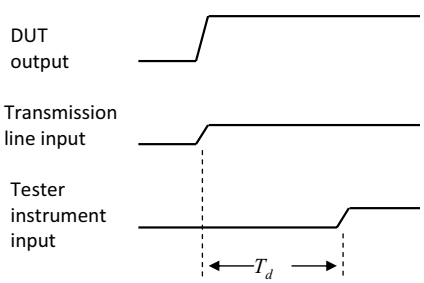
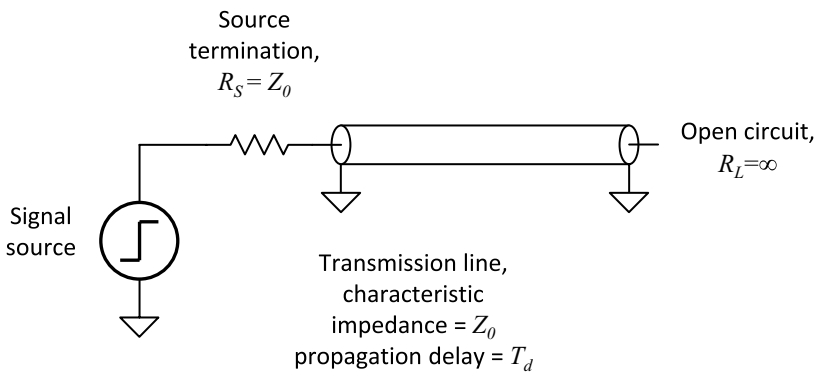


**Figure 15.35.** Transmission line with source termination.




If we observe the voltage at a particular point along the transmission line, we will see a delayed version of the signal at the DUT output. For example, if we look at a point halfway down the transmission line, we will see a signal that has a rising transition that occurs halfway between the rising edge at the transmission line input and the rising edge of the transition at its output. Of course, if the signal had a falling edge instead of a rising edge, this same delay would occur. In fact *any* signal that is transmitted down the transmission line, whether it is a voltage step, sine wave, or complex signal, will exhibit the same attenuation and time delay described previously.

The next common method of transmission line termination is the source termination scheme shown in Figure 15.35. In this scheme, the transmitted signal is allowed to reflect off the unterminated far end of the transmission line. As the signal returns to the source end of the transmission line, the source resistance $R_S = Z_0$ absorbs all the energy in the currents and voltages of the transmitted signal. No further reflections occur. Source termination is used in the digital pin card driver electronics of most ATE testers to prevent ringing in the high-speed digital signals generated by the tester's digital subsystem.

While the signal propagates down the transmission line and back, the source cannot tell whether the far end is terminated or unterminated. *For a short period of time, the transmission line appears to the source as if it were a pure resistance of* $Z_0$. Therefore, during the period of time that the signal travels down the transmission line and back, the voltage at the transmission line input will be ½ that at the source output (since $R_S = Z_0$). Once the reflected signal returns to the source, the source resistor absorbs all the reflected energy and the voltage at the transmission line input becomes equal to the voltage at the output of the source. Therefore, the source only sees a load of $2 \times Z_0$ for a period of $2 \times T_d$. Afterwards, the source sees an open circuit.

At the far end of the transmission line, the voltage remains at the termination voltage until the incident signal arrives. The incident signal arrives at ½ the amplitude of the source signal, but it immediately adds to the reflected signal whose amplitude is also ½ the amplitude of the source signal. Therefore, the far end sees the unattenuated source signal with a delay of $T_d$. Figure 15.36 shows a stepped voltage as it appears at the source output, transmission line input, and transmission line output.

If we observe the voltage at a particular point along the source terminated transmission line, we will see a signal that is similar in shape to the signal at the transmission line input. However, the spacing between the first edge and the second edge will be closer together. At a point halfway

down the transmission line, for instance, the edges will be spaced by a time equal to $T_d$, as illustrated in Figure 15.36. As shown, the edges observed at an intermediate point on the transmission line are always centered around the time the incident signal reflects off the unterminated transmission line output. Transmission lines can consist of multiple controlled-impedance segments, each having the same characteristic impedance. For example, the digital channel drivers from a tester are routed to the DIB through a series of cascaded coaxial cables and controlled impedance PCB traces (Figure 15.37). To create a cascaded controlled impedance transmission line, the DIB's traces must also exhibit the same characteristic impedance as the tester's transmission lines. If any of the impedances of the transmission line segments are not matched, then the point where they connect will generate signal reflections. Therefore, we have to make sure we lay out our DIB

**Figure 15.36.** Source output, transmission line input, and transmission line output.

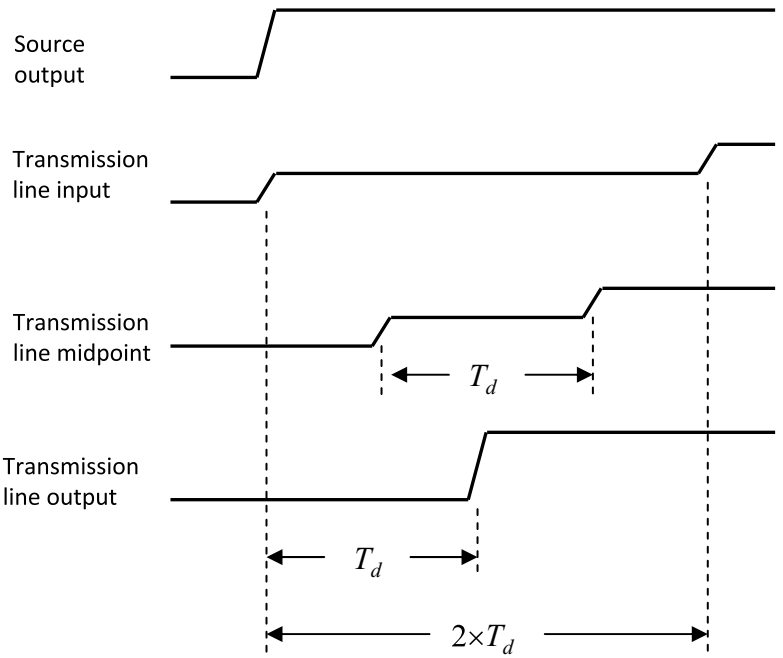
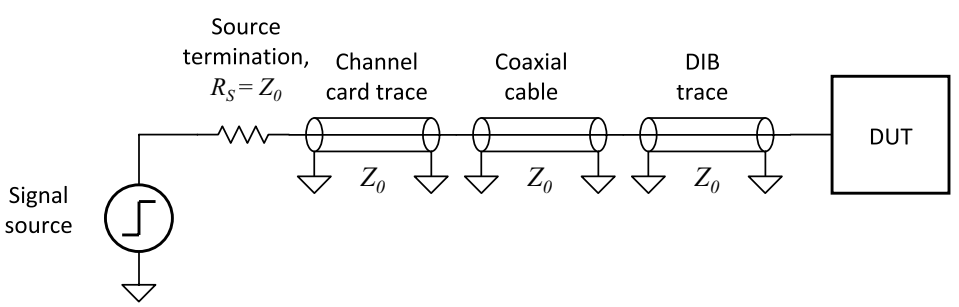



**Figure 15.37.** Cascaded transmission lines.



with a characteristic impedance equal to the tester instrument's characteristic impedance to avoid unwanted signal reflections.

One of the common mistakes made by novice test engineers is to observe the output of a digital channel at the point where the DIB connects to the test head. Such an observation point represents an intermediate point along the cascaded transmission line. As a result, a rising edge will appear as a pair of transitions such as those shown in Figure 15.36 rather than a single transition. The novice test engineer often thinks the tester driver is defective, when in fact it is working perfectly well in accordance with the laws of physics. The only way to see the expected DUT signal is to observe it at the DUT's input.

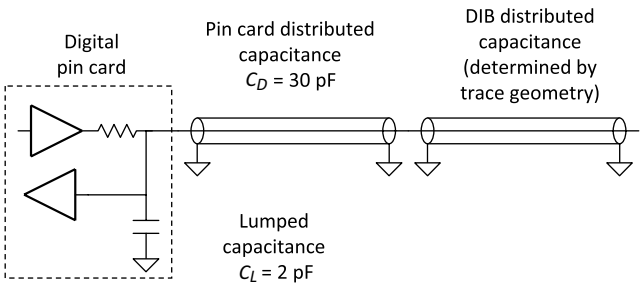
Notice that we can measure the propagation delay of a transmission line by measuring the time between the first and second step transitions at the source end of a source-terminated transmission line. This time is equal to $2 \times T_d$. We can divide the measured time by two to calculate the transmission line's propagation delay. This is how modern testers measure the propagation delays from the digital channel card drivers to the DUT's digital inputs. The tester can automatically compensate for the electrical delay in each transmission line, thereby removing timing skew from the digital signals. This measurement process is known as *time-domain reflectometry*, or TDR. On older testers, TDR deskew calibrations were not used. The timing edges of the digital channels were deskewed at a point inside the test head, and any delays caused by the various transmission lines were not taken into account. The test engineer had to lay out DIB traces that were equal in length to avoid channel-to-channel skew. This is the reason that DIBs are often round rather than square. The round board allows a radial layout, like spokes on a bicycle wheel. The spokes can be laid out with equal lengths, leading to matched delay times.

### 15.4.5 Parasitic Lumped Elements

So far we have only considered transmission lines that have been terminated with a pure resistance. Unfortunately, there are usually a few picofarads of parasitic capacitance, or a few nanohenries of parasitic inductance located at various points along a transmission line. These parasitic reactances arise from interconnections from one cascaded transmission line segment to another and from electromechanical relays located inside the tester instrument. There are also small amounts of inductance and capacitance at the ends of the transmission line. These are caused by the DUT's input or output parasitics, the DUT socket parasitics, or the pin card input and output parasitics. These parasitic elements are known as *lumped elements*, to distinguish them from the distributed inductance and capacitance of the transmission line itself. Lumped reactances can cause undesirable ringing, overshoot, and/or undershoot in our signals. Unfortunately, often there is not much we can do about the problem, other than to be aware of its existence.

Tester instruments are often specified using both lumped and distributed transmission line parameters. For example, a digital channel card is typically specified with a distributed capacitance and a lumped capacitance. The lumped capacitance is usually only a few picofarads, while the distributed capacitance (as defined by Eq. (15.18)) may be 30 pF or more. To accurately model the tester's load on a DUT output, we should use a model that includes both the transmission line and the lumped elements. We can use this type of model for simulations using software tools such as SPICE. Figure 15.38 shows a typical model for a tester's digital pin card electronics. The distributed capacitance listed in a tester's specifications may or may not include that associated with the DIB trace; thus the test engineer should read the channel card specifications carefully. A number of good books have been written on the subject of transmission lines and high-speed digital design. The reader is encouraged to refer to Johnson and Martin[2] and Wadell.[3]

**Figure 15.38.** Typical digital channel card model.




## 15.5 IMPEDANCE MATCHING TECHNIQUES FOR RF DIB

In many cases, the input and output impedance of RF DUT differsfrom that associated with the characteristic impedance of the ATE measurement path (normally 50 Ω). In these cases, the device will need to be matched by an impedance transformation in order to be able to measure the specified performance. In Chapter 12, we discussed the impact of mismatch resulting in a reflection coefficient other than zero, which also causes a mismatch loss and uncertainty. To be able to measure the true device performance accurately, it will be necessary to find the required matching circuit and implement it on the DIB.

The term *matching* implies performing an impedance transformation on some termination impedance. In the case of RF test, it usually refers to the transformation of the input impedance of a DUT to the port impedance of the ATE, which, in most cases, is 50 Ω. In principle there are three different kinds of matching:

1. Conjugate matches transform the load impedance $Z_L$ to the conjugate match of the source impedance $Z_S$ with $Z_S = Z_L^*$. This type of matching will maximize the power delivery to the load, but will not minimize the reflections, unless $Z_S$ is real.
2. Load matching matches the load impedance $Z_L$ to the line impedance $Z_0$. This matching minimizes the reflections, but does not maximize the delivered power, unless $Z_0$ is real. Load matching is best used at the ends of a transmission line.
3. Functional matching which will load the device with an impedance level that optimizesits system performance. This match is done, for example, when optimizing the noise figure of an LNA, since the best noise performance does not necessarily require the same load impedance as the best gain or power performance.

In the following, we will introduce the Smith Chart, an easy-to-use graphical tool to calculate matching components and topologies, which is well established and available as a paper chart, or as software tool from a number of vendors.

### 15.5.1 Introduction to the Smith Chart

In the previous section, we have seen that not only discrete RF components, like inductors and capacitors, need to be treated as RF circuits, but also RF lines connecting two points on a circuit board. In Table 15.1 we have seen that line elements, like stub lines, can even be used as matching components. Here we will describe the basics of a tool called the Smith Chart, which is used extensively by RF engineers. This tool is named after its inventor, Philip H. Smith (1905–1987), an engineer at the time with AT&T.

**Exercises**

**15.6.** A 12-in. stripline trace is fabricated on an FR4 PCB with a width of 15 mils. It is separated from its ground plane by a spacing of 12 mils. Using the refined estimates of Figures 15.10 and 15.16, calculate the stripline's parasitic capacitance per meter and inductance per meter. What is the stripline's characteristic impedance? Repeat the exercise for the same stripline fabricated using a Teflon® PCB.

ANS. FR4: $C_l$ = 110 pF/m, $L_l$ = 500 nH /m, $Z_0$ = 67.4 Ω; Teflon®; $C_l$ = 66 pF/m, $L_l$ = 500 nH /m, $Z_0$ = 87.0 Ω.

**15.7.** What is the velocity of a signal propagating along the stripline of Exercise 15.6? Express your answer in m/s and in a percentage of the speed of light. What is the stripline's propagation delay? Is the delay for the Teflon® PCB longer or shorter than the FR4 PCB?

ANS. FR4: $v_{signal} = 1.35 \times 10^8$ m/s, 0.45 $c$, $T_d$ = 2.28 ns; Teflon®; $v_{signal} = 1.74 \times 10^8$ m/s, 0.58 $c$, $T_d$ = 1.77 ns; Teflon® PCB propagation delay is shorter (signal velocity is higher) than FR4.

**15.8.** What is the wavelength, in inches, of a 500-MHz sine wave traveling along the FR4 stripline in Exercise 15.6? Can we treat the parasitic reactance of the stripline as lumped elements or do we have to treat the stripline as a transmission line at this frequency? Could we approximate the stripline using a lumped-element model if we used Teflon® instead?

ANS. FR4: λ = 10.5 in.—transmission line. Teflon®: λ = 13.6 in.—transmission line.

**15.9.** A 900-MHz sinusoidal signal is transmitted from a DUT output to tester digitizer along a 1.5-foot terminated 50-Ω coaxial cable having a signal velocity of $0.65 \cdot c_0$. What load resistance is presented to the DUT during the time the signal propagates? What resistance is presented to the DUT after the signal has settled? What is the distributed capacitance of this coaxial cable? What is the phase shift, in degrees, between the DUT output and the digitizer input? (The phase shift is equivalent to the propagation delay expressed in degrees, that is, $\phi = 360 \times f \times T_d$).

ANS. $R_{LOAD}$ = 50 Ω, again $R_{LOAD}$ = 50 Ω, $C$ = 47.3 pF, phase shift = 766.9 degrees.

The Smith Chart is based on the principle of conformal transformation (mapping) associated with complex number theory. This theory says that any complex function, say the complex function $Z = x + jy$ in the $x,y$-plane, can be mapped into another function in another plane, say the $u$–$v$-plane, such that its angles are preserved. For example, the rectangle shown in the $x$–$y$ plane on the left-hand side of Figure 15.39, when transformed to the $u$–$v$-plane using the appropriate conformal map, creates another rectangle rotated by about 45 degrees and doubled in size. The angles made between the various contours remain orthogonal to one another. This kind of mathematical transformation is used to map the complex right half of the impedance plane $z = r + jx$ into the complex plane of the reflection coefficient $\Gamma = \Gamma_r + \Gamma_i$ to generate what is referred to as the Smith Chart. This transformation is illustrated in Figure 15.40, where the entire right half pane of the impedance plane $z$ is mapped inside the unit circle of the Γ-plane.

**Figure 15.39.** Mathematical transformation.

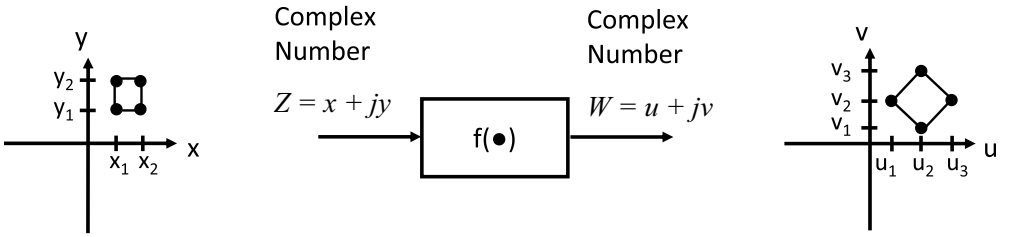
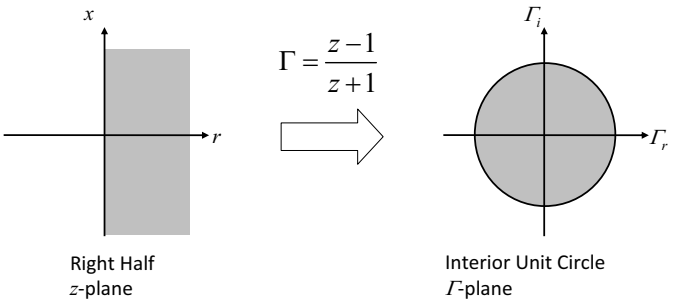



**Figure 15.40.** Bilinear conformal transformation of the right half of the complex impedance plane into the interior unit circle of the complex reflection coefficient Γ-plane.




## 15.5.2 Impedance Smith Chart

The Smith Chart is a polar plot of the reflection coefficient overlaid with an impedance or admittance grid. The rectangular coordinates of the impedance can be mapped with a mathematical bilinear conformal complex transformation given by

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} = \frac{\frac{Z}{Z_0} - \frac{Z_0}{Z_0}}{\frac{Z}{Z_0} + \frac{Z_0}{Z_0}} = \frac{z-1}{z+1} \tag{15.20}$$

where $z \triangleq Z / Z_0$ is referred to as the normalized complex impedance. This impedance is typically expressed in terms of a real resistance component, $r$, and an imaginary reactance $x$ whereby $z = r + jx$. Mathematically, this transformation expresses the following:

1. Every single point in the $z$-plane is mapped to a single point in the Γ-plane.
2. Circles in the $z$-plane map into circles in the Γ-plane, and vice versa. Radius and center point will be transformed. Straight lines can be seen as circles with an infinite radius. In the Γ-plane, constant-resistance circles (constant resistance with varying amount of reactance) have their center along the horizontal axis and are collinear, but not concentric. All circles have one common point at $z = \infty$ as shown in Figure 15.41.
3. The entire real positive half-plane is mapped inside of the circle of the Γ-plane. Since for all passive circuits $\mathrm{Re}\{Z\} \geq 0$, we can use the Smith Chart for all passive circuits without any limitations. For most active circuits, $\mathrm{Re}\{Z\} \geq 0$ is also valid, which underlines the power und usefulness of this tool.

4. This mapping is analytic. Therefore continuous contours in the $z$-plane are mapped into continuous contours in the Γ-plane.
5. The mapping is conformal. Contours in the $z$-plane that are orthogonal to each other will map into contours in the Γ-plane that are likewise orthogonal to each other.

The magnitude of the complex reflection coefficient seen at any point along a lossless transmission line of length $l$ at a distance $d$ from the load termination can be described in terms of the complex load reflection coefficient $\Gamma_L$ as

$$\Gamma(d) = \frac{\text{reflected wave @ } d}{\text{incident wave @ } d} = \Gamma_L e^{-j4\pi d/\lambda_{eff}} \tag{15.21}$$

where $\lambda_{eff}$ is the effective wavelength of the signal. Substituting $\Theta = 2\pi l/\lambda_{eff}$, the so-called electrical length parameter expressed in radians, we write

$$\Gamma(d) = \Gamma_L e^{-j2\Theta d/l} \tag{15.22}$$

It interesting to note that for an arbitrary load reflection coefficient described as $\Gamma_L = \rho e^{j\phi}$, the reflection coefficient at any point on the line can be expressed as

$$\Gamma(d) = \rho e^{j(\phi - 2\Theta d/l)} \tag{15.23}$$

As is clearly evident from Eq. (15.23) the magnitude of the reflection coefficient is constant along the transmission line, regardless where we are along the line, and equal to the magnitude of the load reflection coefficient. Therefore, on the complex Γ-plane of the Smith Chart, reflection coefficients are represented by constant circles (Figure 15.42).

For the full length of the line (i.e., $d=l$), the phase angle of the reflection coefficient seen at the input side of the line is rotated clockwise from $\phi$ by twice the electrical length of the line, $2\Theta$, that is,

$$\Gamma_{IN} = \Gamma_L e^{-j2\Theta} = \rho_L \angle(\phi - 2\Theta) \tag{15.24}$$

**Figure 15.41.** The Impedance Smith Chart as a bilinear transformation of the infinite right (positive) half of the $z$-plane to the inside of the circular Γ-plane. (a) Constant resistance vertical lines are mapped to constant resistance circles. (b) Constant reactance horizontal lines are mapped to constant reactance arcs.

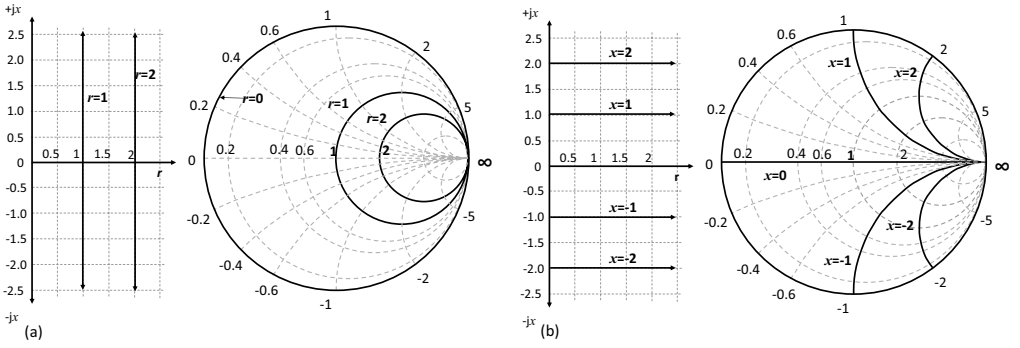
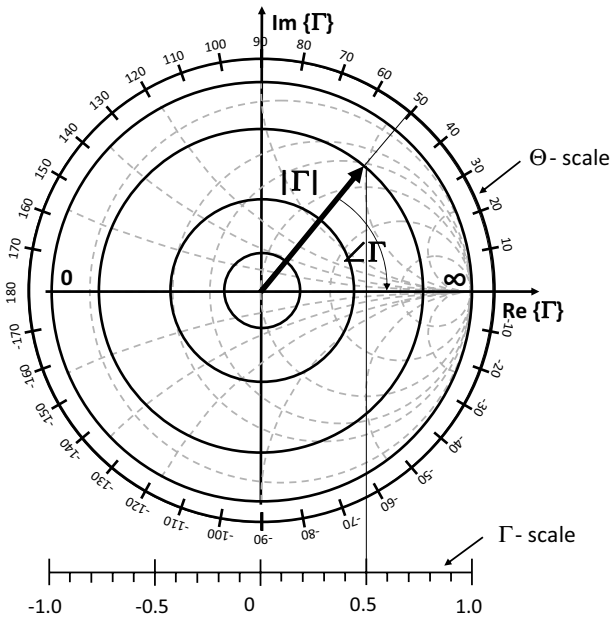


**Figure 15.42.** Smith Chart with constant reflection coefficient Γ circles. The shown reflection coefficient is Γ= 0.5∠50°. The phase Θ can be read on the circular Θ-scale, the magnitude of the reflection coefficient Γ on the Γ-scale below the Smith Chart.




Because the phase angle is derived from the Smith Chart in degrees, the actual length of the line $l$ is computed according to

$$l = \frac{\Theta\big|_{\text{deg}}}{360} \times \lambda_{eff} \tag{15.25}$$

where Θ is expressed in degrees.

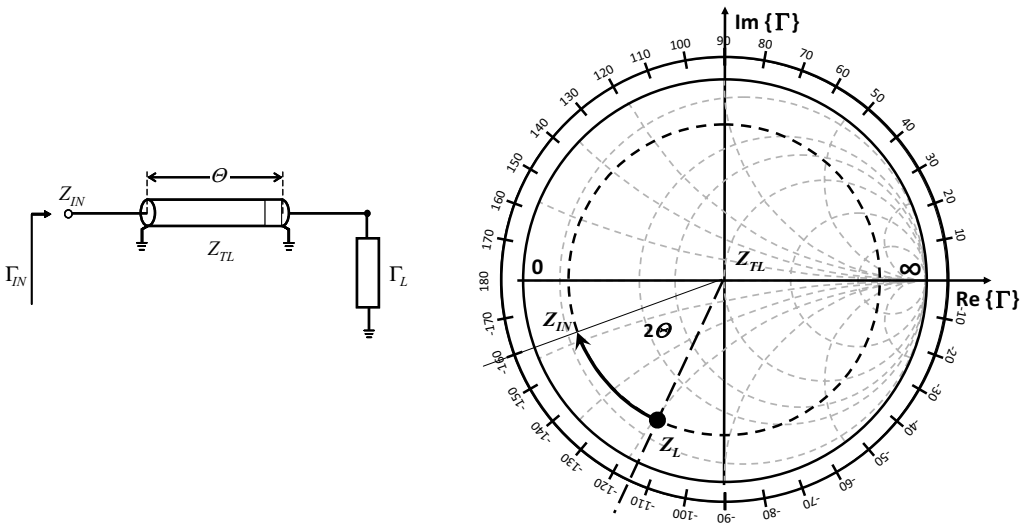
With the reflection coefficient known at any point on the lossless line, the value of the complex impedance seen looking into the line toward the load can be determined directly from the Smith Chart. Consider that the input impedance $Z_{IN}$ of a lossless line with characteristic impedance $Z_{TL}$ connecting a complex load impedance $Z_L$ (Figure 15.43) is given by

$$Z_{IN} = Z_{TL}\left[\frac{Z_L + jZ_{TL}\tan\Theta}{Z_{TL} + jZ_L\tan\Theta}\right] \tag{15.26}$$

Equation (15.26) defines the input impedance $Z_{IN}$ as a function of the transmission line parameters including their electrical length Θ. This equation can be simplified by setting the source impedance equal to $Z_{TL}$ and normalizing the circuit with respect to this quantity, thus obtaining $z_L = Z_L/Z_{TL}$ and $z_{TL} = Z_{TL}/Z_{TL} = 1$. If the transmission line is lossless, the magnitude of the amount of reflected power is constant throughout the entire length of the transmission line and only the phase of the reflected wave will change. The normalized form of Eq. (15.26) can then be written as

$$z_{IN} = \frac{z_L + j\tan\Theta}{1 + jz_L\tan\Theta} \tag{15.27}$$

**Figure 15.43.** The Γ-plane representation of the load impedance $Z_{TL}$ connected with a transmission line with the impedance $Z_{TL}$ and the electrical length Θ.




In a later subsection we will explain how this impedance transformation with transmission lines can be used to match a load to a given source impedance.

## 15.5.3 Admittance Smith Chart

When working with circuits that are parallel, it is often easier to use admittance instead of impedance. As such, we can rewrite the conformal transformation first seen in Eq. (15.20) from an admittance perspective as follows:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} = \frac{\frac{1}{Y} - \frac{1}{Y_0}}{\frac{1}{Y} + \frac{1}{Y_0}} = \frac{Y_0 - Y}{Y_0 + Y} = \frac{\frac{Y_0}{Y_0} - \frac{Y}{Y_0}}{\frac{Y_0}{Y_0} + \frac{Y}{Y_0}} = \frac{1 - y}{1 + y} \tag{15.28}$$

Here we make use of the normalized admittance, $y \triangleq Y/Y_0$. This admittance is normally expressed as $y = g + jb$, where the real part of $y$is the conductance $g$ and the imaginary part is the susceptance, $b$. The denormalized admittance $Y = yY_0 = G + jB$ is measured in siemens.

Comparing Eq. (15.28) with Eq. (15.20), we see that that the general form differs by a negative sign. This implies that the admittance Smith Chart is rotated by 180 degrees with respect to its impedance form. In rectangular admittance coordinates, the vertical lines represent constant conductance, while the constant conductance in the Γ-plane is represented by collinear circles as illustrated in Figure 15.44a. Constant susceptance becomes constant semicircles or arcs as shown in Figure 15.44b. The open circuit point ($g = 0$) is as shown on the right side of the admittance chart, and the short circuit ($g = \infty$) is represented on the left side of the horizontal axis.

**Figure 15.44.** Admittance Smith Chart as bilinear transformation of the infinite right (positive) half y-plane to the inside of the circular Γ-plane: (a) Constant conductance vertical lines are mapped to constant conductance circles, and (b) constant susceptance horizontal lines are mapped to constant susceptance arcs.

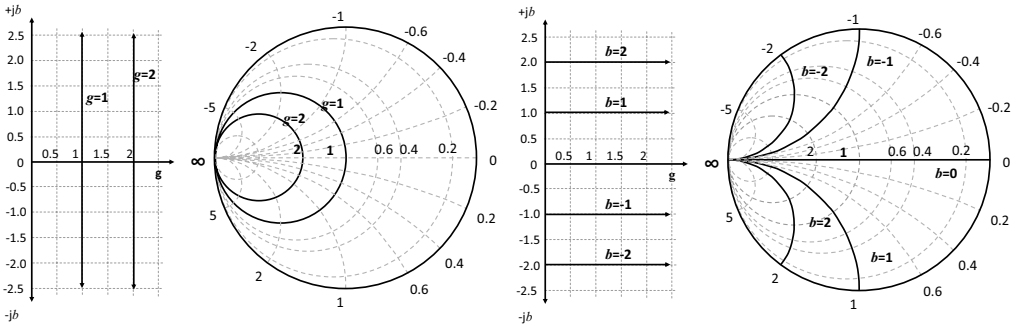
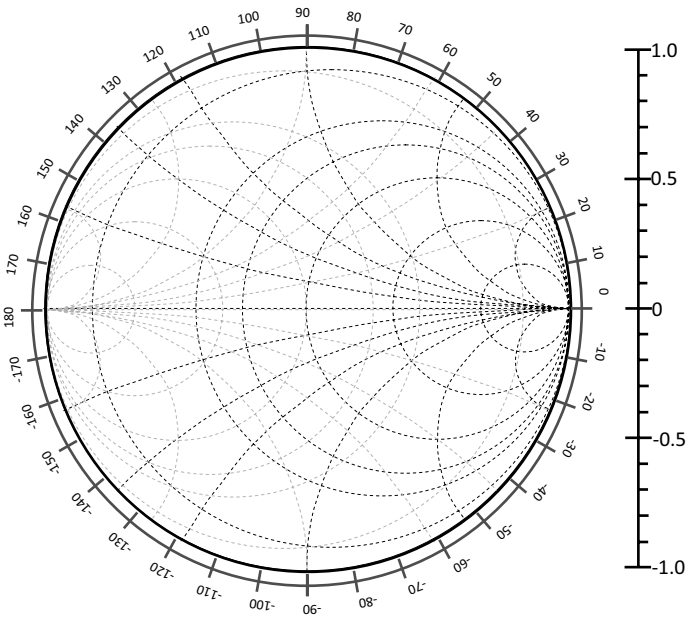



**Figure 15.45.** Immitance Smith Chart. The impedance grid is shown in black, and the admittance grid is shown in gray. Commercially available charts use two colors for easier usage.




## 15.5.4 Immitance Smith Chart

To have a tool for developing a complex impedance transformation with parallel and serial components, both the impedance and the admittance Smith Charts are overlaid in one so-called immitance Smith Chart. The impedance and admittance parameters can be displayed simultaneously as shown in Figure 15.45. The immitance Smith Chart is typically colored, with the admittance part in another color. Here we use a black and gray scale to distinguish between impedance and

admittance. In the next subsection, we will discuss how to use the Smith Chart for impedance transformations that match any impedance to a specified value.

### 15.5.5 Impedance Transformation with Discrete Components on Smith Chart

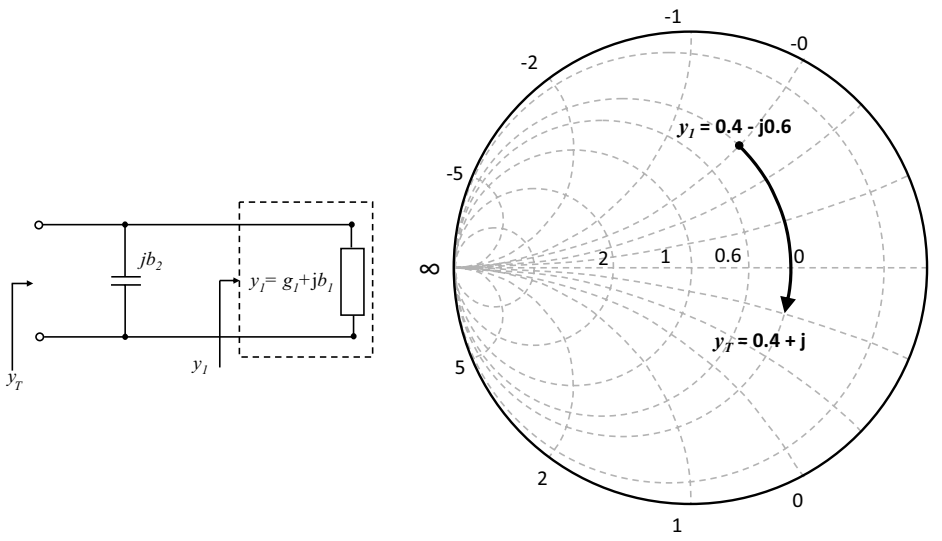
A common problem in the development of a test board, like a DIB, is to "match" the DUT to the test environment. The RF engineer understands the term "match" to be the impedance transformation of the input or output impedance of the DUT to the impedance of the ATE, or components on the test board, like a SAW filter. In this subsection we will demonstrate how to match a specific input or load condition using a circuit combination of two discrete components. We will show the use of the Smith Chart in a practical example, but we will also see the power of this tool and also some its limitations.

To aid the test engineer, Table 15.2 provides a brief overview of the most important formulas used for calculating reactance, susceptance, inductance and capacitance. These formulas come in handy when solving for a matching network. As a reminder, in general, impedance $Z(j\omega)$ is a complex function of frequency, consisting of real and imaginary parts. The real part of impedance is defined as the resistance $R = \mathrm{Re}\{Z(j\omega)\}$ and the imaginary part is known as the reactance $X = \mathrm{Im}\{Z(j\omega)\}$. Conversely, we can also speak in terms of admittance, defined as the inverse of the impedance, that is, $Y(j\omega) = \dfrac{1}{Z(j\omega)}$. Because admittance is also a complex function of frequency, the real part is referred to as the conductance, $G = \mathrm{Re}\{Y(j\omega)\}$, and the imaginary part is called the susceptance, $B = \mathrm{Im}\{Y(j\omega)\}$. Uppercase symbols represent denormalized values, and lowercase symbols represent normalized values, that is, $x = X/Z_0$ and $b = B/Y_0$, depending on the nature of the parameter.

**Table 15.2.** Summary of Basic Formulas to Calculate Lumped Components Reactance, Susceptance, Inductance and Capacitance

| **Denormalized Form** | **Normalized Form Using $Z_0 = 50\ \Omega$ and $Y_0 = 0.02$ S** |
|---|---|
| **Ideal Lumped Component Reactance and Susceptance** | |
| $X_L = 6.283 \cdot f[\mathrm{GHz}] \cdot L[\mathrm{nH}]$ | $x_L = 0.1257 \cdot f[\mathrm{GHz}] \cdot L[\mathrm{nH}]$ |
| $B_L = -\dfrac{0.159}{f[\mathrm{GHz}] \cdot L[\mathrm{nH}]}$ | $b_L = -\dfrac{7.96}{f[\mathrm{GHz}] \cdot L[\mathrm{nH}]}$ |
| $X_C = -\dfrac{159}{f[\mathrm{GHz}] \cdot C[\mathrm{pF}]}$ | $x_C = -\dfrac{3.183}{f[\mathrm{GHz}] \cdot C[\mathrm{pF}]}$ |
| $B_C = 0.006283 \cdot f[\mathrm{GHz}] \cdot C[\mathrm{pF}]$ | $b_C = 0.314 \cdot f[\mathrm{GHz}] \cdot C[\mathrm{pF}]$ |
| **Ideal Lumped Inductance and Capacitance in nH and pF** | |
| $L[\mathrm{nH}] = \dfrac{0.159 X_L}{f[\mathrm{GHz}]} = \dfrac{0.159}{f[\mathrm{GHz}] \cdot (-B_L)}$ | $L[\mathrm{nH}] = \dfrac{7.96 \cdot x_L}{f[\mathrm{GHz}]} = \dfrac{7.96}{f[\mathrm{GHz}] \cdot (-b_L)}$ |
| $C[\mathrm{pF}] = \dfrac{159}{f[\mathrm{GHz}] \cdot (-X_C)} = \dfrac{159 B_C}{f[\mathrm{GHz}]}$ | $C[\mathrm{pF}] = \dfrac{3.183}{f[\mathrm{GHz}] \cdot (-x_C)} = \dfrac{3.183\ b_C}{f[\mathrm{GHz}]}$ |

**Figure 15.46.** Adding a parallel (shunt) capacitor with admittance $jb_2$ to a one-port circuit with input admittance $y_1$.




Parallel additions of components are most conveniently handled with the admittance Smith Chart, whereas series addition of components is most conveniently and efficiently handled using the impedance Smith Chart. Consider the parallel combination of an arbitrary admittance $y_1 = g_1 + jb_1$ and a lossless capacitor with admittance $y_2 = jb_2$ as illustrated in Figure 15.46. Beginning with a point in the admittance Smith Chart corresponding to $y_1$, the addition of the parallel capacitor shifts the admittance level along a clockwise path of constant conductance such that the total admittance point in the Smith Chart is equal to

$$y_T = y_1 + jb_2 = (g_1 + jb_1) + jb_2 = g_1 + j(b_1 + b_2) \tag{15.29}$$

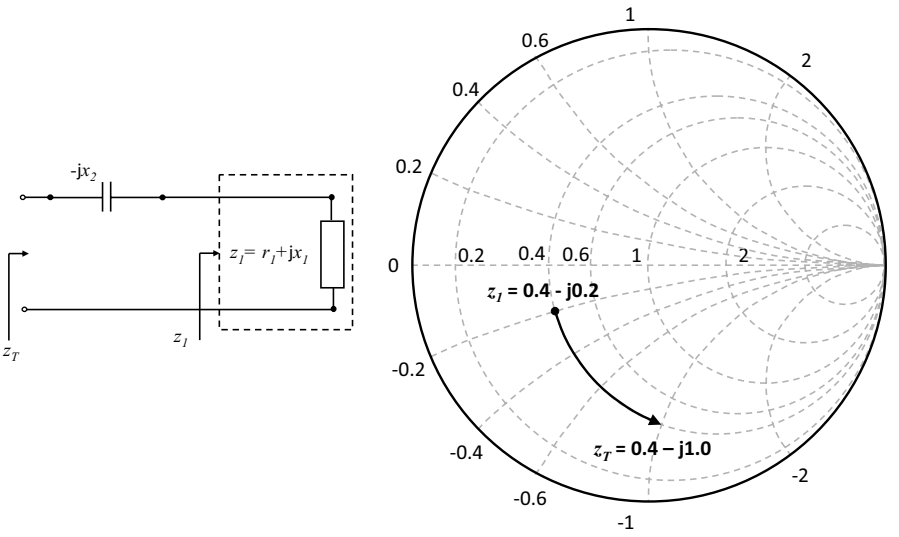
The specific value of parallel capacitance $C_p$ placed in parallel to the admittance $y_1$ that gives rise to the susceptance of $b_2$ is simply found by rearranging the expression listed in Table 15.2 for a normalized impedance level of 50 Ω, that is,

$$C_p\,[\text{pF}] = \frac{b_2}{0.314 f\,[\text{GHz}]} \tag{15.30}$$

Next, consider the series combination of arbitrary impedance $z_1 = r_1 + jx_1$ and a loss-less capacitor with impedance $z_2 = -jx_2$ as illustrated in Figure 15.47. Beginning with a point in the impedance Smith Chart corresponding to $z_1$, the addition of the series capacitor shifts the impedance level in a counterclockwise direction (more negative reactance) along a path of constant resistance such that the total impedance point in the Smith Chart is equal to

$$z_T = z_1 + z_2 = z_1 - jx_2 = r_1 + j(x_1 - x_2) \tag{15.31}$$

**Figure 15.47.** Adding a series capacitor with impedance $-jx_2$ to a one-port circuit with input impedance $z_1$.




The series capacitance $C_S$ can be calculated (as listed in Table 15.2) with negative reactance $-x_2$ at a normalized impedance level of 50 Ω corresponding to the following

$$C_s\,[\text{pF}] = \frac{3.183}{f\,[\text{GHz}]\cdot x_2} \tag{15.32}$$

This same approach can easily be extended to the parallel or series addition of an inductor or resistor. The details are left for the reader to verify.

## EXAMPLE 15.5

Assume that a capacitor with the susceptibility $b_2$ is connected in parallel to an admittance of $y_1 = 0.4 - j0.6$. The admittance of this parallel circuit can be read from the Smith Chart to be $y_T = 0.4 - j0.2$. What is the value of the capacitance placed in parallel with this admittance if the frequency is 2.0 GHz and the reference impedance level is 50 Ω?

**Solution:**
From Eq. (15.29), we write

$$y_T = y_1 - jb_2$$

allowing us to solve for $b_2$ according to

$$jb_2 = y_T - y_1 = (0.4 + j0.2) - (0.4 - j0.6) = j0.8$$

resulting in

$$b_2 = 0.8 \text{ units}$$

The actual capacitance that gives rise to this (normalized) susceptance is derived from Eq. (15.30) to be

$$C_p = \frac{b_2}{0.314 \cdot f} = \frac{0.8}{0.314 \cdot 2} = 1.274 \text{ pF}$$

The admittance for the one-port with and without the parallel capacitance included is highlighted in the Smith Chart shown on the right-hand side of Figure 15.46. Here it is shown how the initial one-port admittance of $y_1 = 0.4 - j0.6$ is transformed to a new admittance level of $y_T = 0.4 - j0.2$ along a path of constant conduction through the addition of a parallel capacitor with a normalized susceptance of 0.8 units.

### 15.5.6 Impedance Matching with a Series and Shunt Component Using the Immitance Smith Chart

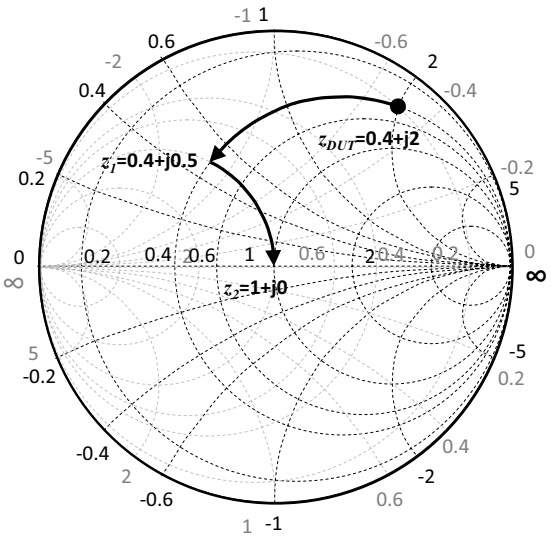
In the previous subsection, we have seen how the Smith Chart was used to transform the impedance or admittance of a one-port circuit through the addition of a single passive element (i.e., resistor, capacitor, or inductor). In this subsection, we shall extend this approach to multiple additional passive elements so that a greater range of impedance or admittance transformation can be achieved. Throughout this subsection we will assume that the signal wavelength is long compared to the physical dimension of the components and RF lines. This enables one to neglect the propagation behavior of the connecting lines.

Since most matching networks require series and shunt elements, we shall make use of the immitance Smith Chart, because it combines both the impedance and admittance grids on the same graph. As before, all inductors and capacitors will be treated as reactance or susceptance and will thus follow the constant resistance or conductance circles of the Smith Chart. For serial components, we will use the impedance portion of the Immitance Smith Chart, as well as the admittance grid for parallel or shunt components. The goal will be to transform the impedance to be reflection-free, or moving the input impedance into the center point at $z = 1$, which is equivalent to a denormalized impedance level of $Z = 50 + j0\ \Omega$.

In order to illustrate the matching technique using the Smith Chart, let us assume that a DUT has an output impedance of, say $Z_{DUT} = 20 + j100\ \Omega$ at an operating frequency of 2 GHz. It is fair to assume that the test equipment has been designed with a nominal input impedance of $Z = 50\ \Omega$. It is our objective here to construct a matching network that connects between the DUT output and the test equipment input, such that the test equipment sees a matched condition, that is, an impedance level equal to 50 Ω at 2-GHz operation. This point is located at the center of the Smith Chart at $z_T = 1 + j0\ \Omega$.

We begin by first normalizing the DUT output impedance by 50 Ω, resulting in an initial normalized impedance level of $z_{DUT} = \dfrac{20 + j100}{50} = 0.4 + j2$ units. This point is then marked on the impedance Smith Chart, along with the desired impedance level, $z_T = 1 + j0$. Because $z_{DUT}$ has a positive imaginary part (positive susceptance) corresponding to some inductive behavior, we will consider adding a series capacitor because it has a negative susceptance and will cause the impedance level to move toward zero. We also recognize that a series capacitor will cause the impedance level to move along the circle of constant resistance in a counterclockwise manner having a normalized level of 0.4 units. Recognizing that the final impedance point of $1 + j0$ lies

**Figure 15.48.** Immitance Smith Chart as tool to calculate the matching circuit for an impedance transformation involving multiple passive components.




on a circle of constant admittance on the admittance Smith Chart of 0.5 units, we shall add a series capacitor $C_s$ having an impedance of $-j1.5$ units, or equivalently, a capacitance value of

$$C_s = \frac{3.183}{f\,[\text{GHz}]\cdot x_{C_s}} = \frac{3.183}{2\times 1.5} = 1.061\,\text{pF}$$

The DUT impedance seen after the series capacitor is simply the sum of the initial DUT impedance and the impedance of the series capacitor, that is,

$$z_{T1} = z_{DUT} + z_{C_s} = 0.4 + j2 - j1.5 = 0.4 + j0.5 \text{ units}$$

It is at this point that we convert the present impedance $z_{T1}$ to an admittance, $y_{T1}$, so that we can make use of the admittance Smith Chart (gray scale in Figure 15.48), that is,

$$y_{T1} = \frac{1}{z_{T1}} = \frac{1}{0.4 + j0.5} = 0.976 - j1.22 \text{ units}$$

Here we see that the admittance seen looking into the DUT-series-capacitor combination consists of a conductance very close to unity (error is due to limited accuracy of the Smith Chart) and a susceptance of –1.22 units (recall that a negative susceptance is caused by a shunting inductor). By shunting a capacitance with a susceptance of 1.22 units across the present network terminals, the imaginary component of the admittance can be eliminated, resulting in the desired admittance of

$$y_T = y_{T1} - y_{C_p} = (0.976 - j1.22) + j1.22 = 0.976 \cong 1 \text{ units}$$

The value of the parallel capacitor $C_p$ at 2 GHz having an admittance of $j1.22$ is then found from Eq. (15.30) to be

$$C_p = \frac{1.22}{0.314\times 2} = 1.94\ \text{pF}$$

## Exercises

**15.10.** A DUT with a normalized output impedance $z_{DUT} = 0.4 + j2\ \Omega$ is to be matched with an LC network to 50 Ω at 2 GHz, where the matching network needs to be design in such a way that the device output will not be shorted to GND (inductors typically have a very low DC resistance).

ANS.

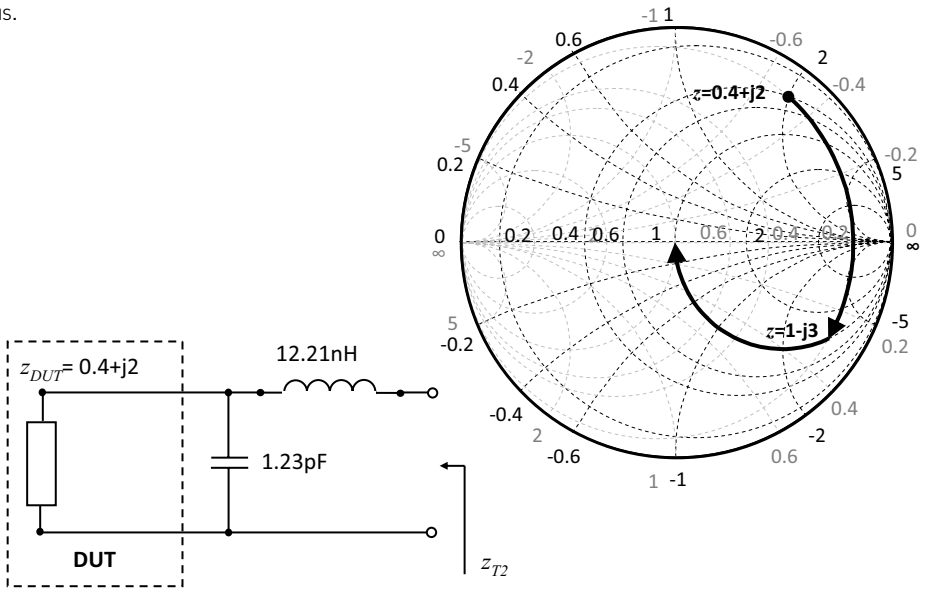
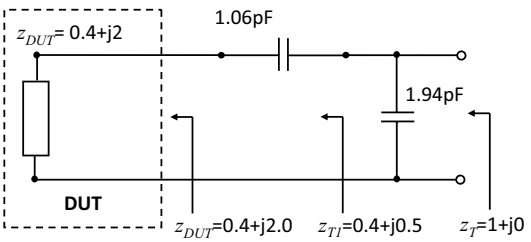



**Figure 15.49.** Matching network transforming the DUT impedance $z_{DUT}$ to the test equipment impedance level.



The final matching circuit is shown in Figure 15.49, together with the impedance levels at each node in the circuit.

## 15.6 GROUNDING AND POWER DISTRIBUTION

### 15.6.1 Grounding

The term "grounding" refers to the electrical interconnection and physical layout of the various ground nodes in an electronic system such as an ATE tester and DIB. In a circuit schematic, grounds are treated as perfect zero volt reference points exhibiting zero impedance. In a real system, there can only be one point that is defined as true ground. All other ground nodes are connected to true ground through resistive and inductive traces, wires, or ground planes. These parasitic resistors and inductors often play a significant role in the performance of the DUT and the ATE tester instruments.

Grounding is one of the more difficult DIB design subjects to master. Proper grounding is essential to a DUT's electrical performance. Poor grounding can lead to resistive voltage drops, inductive transients, capacitive crosstalk, interference, and a host of other electrical ailments that result in poor measurement accuracy, or noisy DUT performance. Grounding is not a subject taught in most college curricula. Instead, it is often learned through experience (i.e., bad experience!). Fortunately, a few books have been written on the subject of grounding and other related topics. Henry Ott's book,[4] *Noise Reduction Techniques in Electronic Systems*, provides an excellent introduction to the subjects of grounding, shielding, electromagnetic interference (EMI), and electromagnetic compatibility (EMC).

One way to achieve proper grounding is to pay close attention to the flow of currents through the traces, wires, and planes in the DIB and tester. The first thing we have to consider is DC measurement errors caused by resistive drops in ground connections. Figure 15.50 shows a simple test setup including a DC current source, a DC voltmeter, and a DUT (a simple load resistor in this case). We wish to measure the value of the resistor by forcing a current, $I_{TEST}$, and measuring the voltage drop across the resistor, $V_{TEST}$. The resistor's value is calculated by dividing $V_{TEST}$ by $I_{TEST}$.

As we have seen in previous sections, the ground path from the DUT to the DC source will not be a 0-Ω path. If the ground path is several feet long, it may exhibit several ohms of series resistance, $R_G$. Therefore, the parasitic model illustrated in Figure 15.51 should be used to predict the measurement results obtained using the grounding scheme of Figure 15.50. Since the DC meter in this example is connected to the tester's internal ground, it measures the voltage across the series combination of the DUT resistance $R_L$ and the ground interconnection resistance, $R_G$. Therefore, the measured resistance is equal to $R_L + R_G$, resulting in an error of several ohms. Notice that the value of $R_S$ is unimportant, since the current source will force $I_{TEST}$ through the DUT load resistance regardless of the value of $R_S$. Also, notice that the value of $R_M$ is unimportant, since it carries little or no current (assuming the DC voltmeter's input impedance is sufficiently high).

Obviously, accurate mixed-signal testers cannot be constructed using such a simple grounding scheme. Instead, they use a signal, which we will call *device ground sense*, or DGS, to carry

**Figure 15.50.** Resistor measurement test setup: idealized model.

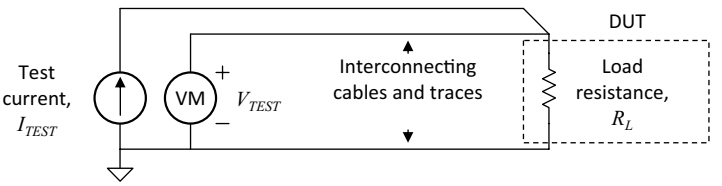


**Figure 15.51.** Resistor measurement test setup: parasitic model.

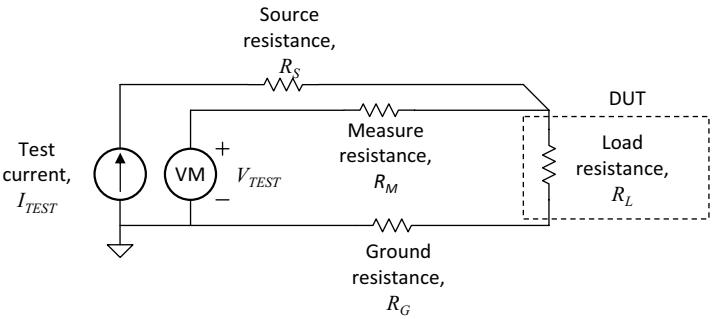
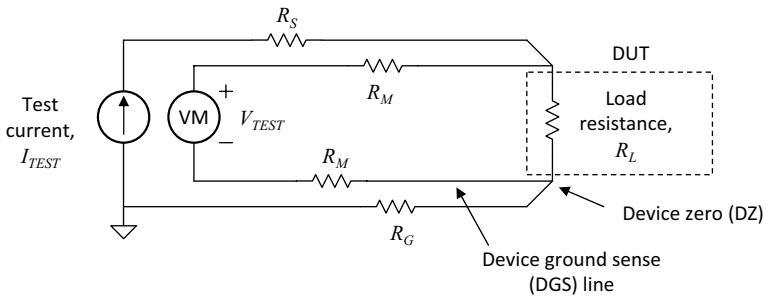



**Figure 15.52.** Resistor measurement test setup using device ground sense (DGS) line.




the DUT's 0-V reference back to each tester instrument. Since the DGS signal is carried on a network of zero-current wires, the series resistances of these wires do not result in voltage measurement errors. Figure 15.52 shows a resistor measurement test setup using the DGS reference signal. Note that any number of tester instruments can use DGS as a zero-volt reference, provided that they do not pull current through the DGS line. Consequently, each tester instrument typically contains a high input impedance voltage follower to buffer the voltage on DGS.

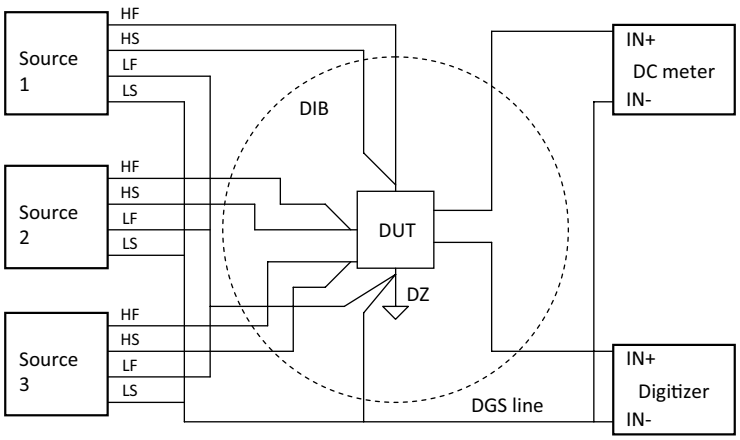
The DGS line is often routed all the way to a point near the DUT, which serves as the true 0-V reference point of the entire test system. This single point is known by several names, including *star ground* and *device zero*. We will use the term "device zero," or DZ, to refer to this point in the circuit. All measurement instruments should be referenced to the DIB's DZ voltage.

## 15.6.2 Power Distribution

As shown in Figure 15.53, the power supplies and sources in a mixed-signal tester are typically connected using a four-wire Kelvin connection (see Section 2.2.2). Each Kelvin connection includes a separate wire for high-force (HF), low-force or ground current return (LF), high-sense (HS), and low-sense (LS). The low-sense line is equivalent to DGS. Therefore all supplies may use a single DGS line as their low-sense reference, resulting in only three DIB connections per source.

All currents from a power supply must return through its low-force line, in accordance with Kirchhoff's current law. Therefore, we can control the path of DUT power supply currents by forcing them through separate DIB traces back to the low-force line of the supply. Separate return

**Figure 15.53.** Power and ground distribution in a mixed-signal ATE tester.




of each supply's current prevents unexpected voltage drops across the various current paths in the ground network. Some testers do not provide separate ground return lines for each supply. In these testers, it is impossible to isolate the currents from each power supply and DC source. Instead, the return currents are lumped together and returned to the tester through a common current return path, as shown in Figure 15.53.

The PCB traces in a DZ grounded DIB should be laid out as shown in Figure 15.54a. If the DGS line or the force and sense lines of a power supply are not connected properly, the full effectiveness of the zero-volt sense lines will not be realized.

In some situations, the DZ is placed on chip by routing ground force and sense traces through separate I/O pins of the IC to a common pad on the die. Power pins can also be connected to force and sense lines connected on chip in a similar fashion. In addition to improving the accuracy of DZ, this technique will cause a part to fail if either of the two wire bonds are left disconnected during assembly. The cost of joining power or ground Kelvin connections on the chip is extra package pins. In some cases this is not feasible, in others it is well worth the cost.

### 15.6.3 Power and Ground Planes

At this point in the chapter, the reader should be catching on that ground planes are a good idea for many reasons. The ground plane provides a low inductance connection between all the grounds on a DIB. Similarly, power supplies can be routed using power planes to reduce the series inductance between all power supply nodes. Power and ground planes can be divided into sections, forming what are known as *split planes*. Each section of a split plane can carry a different signal, such as +12 V, +5 V, and –5 V. This provides the electrical superiority of copper planes without requiring a separate PCB layer for each supply. Typically, power is applied through split planes while grounds are connected to solid (nonsplit) planes, but even the ground planes can be split if desired.

There are usually at least two separate ground planes in a mixed-signal DIB. One plane forms the ground for the transmission line traces carrying digital signals. This plane is subject to rapidly changing current flows from the digital signals, and therefore exhibits fairly large voltage spikes caused by the interactions of the currents with its own inductance. This ground plane is often called DGND (digital ground) in the DIB schematics. The second plane, AGND (analog ground), is for use by analog circuits. Ideally, this plane should carry only low-frequency, low-current signals that will not give rise to voltage spikes.

**Figure 15.54.** Physical layout of Kelvin connections and DZ grounding system: (a) Proper connections. (b) Improper connections.

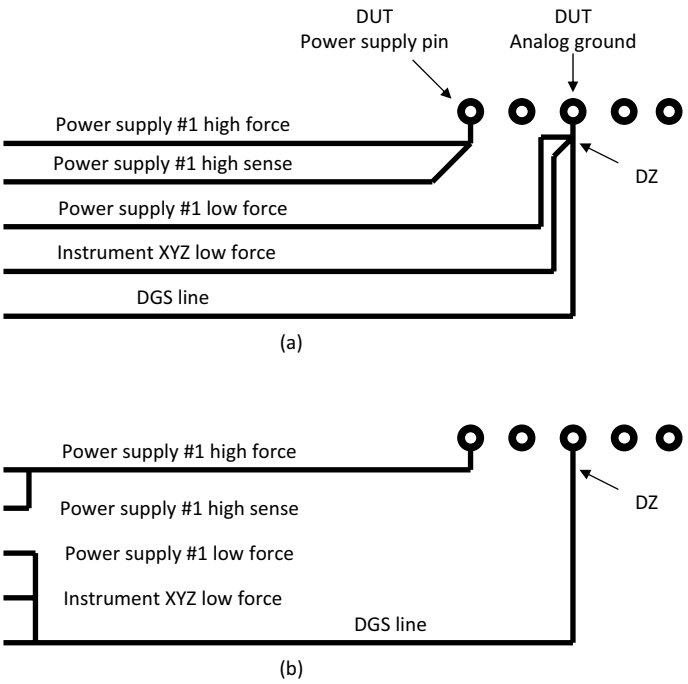
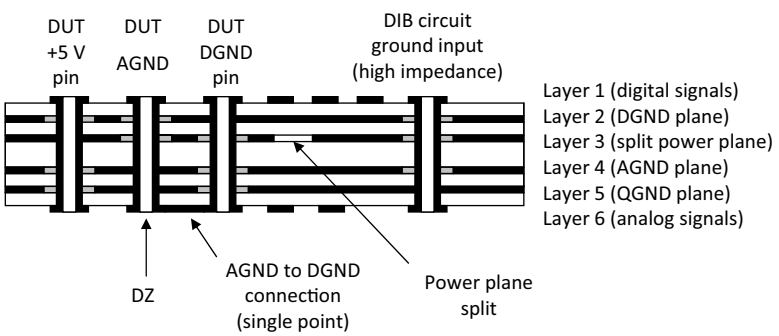
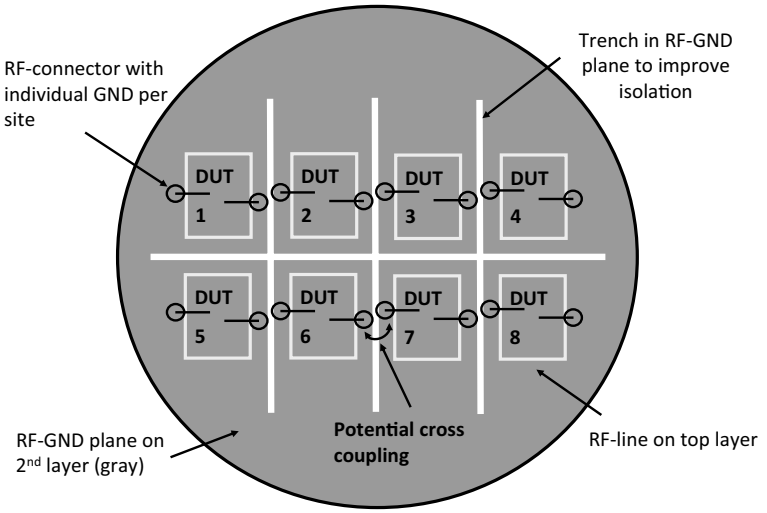



**Figure 15.55.** Three-plane grounding scheme.




A third plane is occasionally used as a DIB-wide zero volt reference. This "quiet ground" plane (QGND) can be used by any analog circuits on the DIB that need a low noise ground reference. The QGND plane must be connected in such a way that it does not carry any currents exceeding a few milliamps. To guarantee this, the QGND plane should be tied only to the DZ node at a single point and to relatively high-impedance DUT pins and DIB circuit nodes. Often, the analog ground plane and the quiet ground plane are combined into a single plane, resulting in a DIB with only two ground planes (analog and digital). Figure 15.55 shows a cross section of a DIB with a three-plane grounding scheme.

**Figure 15.56.** DIB with RF-GND plane with trenches to improve site-to-site isolation.



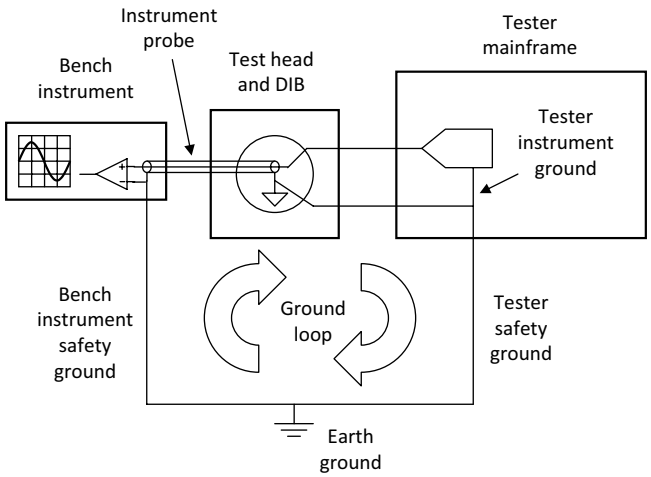

RF ground planes are placed typically on the second layer of the DIB to build microstrip lines with a defined characteristic impedance. This RF-GND plane is connected with the RF launcher and the DUT GND as solid as possible. To reduce cross coupling between test sites in a multisite test configuration, trenches in the GND plane can be build in between the test sites as shown in Figure 15.56.

### 15.6.4 Ground Loops

A star-grounding scheme is formed by connecting the grounds of multiple circuits to a single ground point, rather than connecting them in a daisy chain. Star grounds prevent a common grounding error known as a *ground loop*. A ground loop is formed whenever the metallic traces and wires in a ground network are connected so that a loop is formed (Figure 15.57). In a world without magnetic fields, ground loops would not be problematic. Unfortunately, fluctuating magnetic fields surround us in the form of 60-Hz power fields and various electromagnetic radio signals, such as those produced by cell phone and wireless networks. A fluctuating magnetic field passing through a loop of wire gives rise to a fluctuating electric current in the wire. The fluctuating current, in turn, gives rise to a fluctuating voltage in the wire due to the wire's parasitic resistance and inductance. Thus AC voltages can be induced into ground wires if we carelessly connect them in a loop. Ground loops are most commonly formed when we connect instruments such as oscilloscopes and spectrum analyzers to our DIB. The tester housing and its electrical ground must be connected to earth ground for safety reasons to prevent electrical shock. Likewise, an oscilloscope's housing and electronics must be connected to earth ground. When we connect a bench instrument's ground clip to the DIB ground, we form a large ground loop, as shown in Figure 15.57. Ground loops can also be formed when we attach test equipment to other external equipment such as handlers and probers.

Any fluctuating magnetic fields that intersect the area of the ground loop cause currents to flow around the loop. The parasitic resistance of the wires and cables in the loop cause voltage drops, which in turn cause unwanted noise in our grounding system, corrupting whatever

**Figure 15.57.** Bench instrumentation ground loop.




measurement we are trying to make. A ground loop often causes the tester's signals to appear terribly corrupted with 60-Hz power hum and other noise components. The test engineer has to realize that these signals are not present in the tester itself. They disappear as soon as we disconnect the bench instrument. Unfortunately, the instrumentation ground loop problem cannot be easily solved without violating company safety rules (e.g., by disconnecting the third prong of the oscilloscope's power cord from earth ground using a "cheater plug"). Ground loops caused by handlers and probers can sometimes be resolved by breaking unnecessary ground connections between the handler or prober and the test head.

## 15.7 DIB COMPONENTS

### 15.7.1 DUT Sockets and Contactor Assemblies

The DUT pins and the circuit traces on a DIB must be connected temporarily during test program execution. A hand-test socket or a handler contactor assembly makes the temporary connection. There are many different socket and contactor schemes, so we will not try to discuss them in any detail. The most important thing to note is that the metallic contacts of the socket or contactor assembly represent an extra resistance, inductance, and capacitance to ground that will not exist when the DUT is soldered directly to the PCB in the customer's system-level application. Sometimes the parasitic elements are unimportant to a device's operation, but other times, particularly at high frequencies, they can be extremely critical. When designing a DIB for an RF DUT it is important to compare the parasitics of the test socket especially the pin and GND inductance and compare with the device requirements. Often a good compromise needs to be found between the electrical, mechanical robustness and thermal performance. Often socket vendors provide the expected 1-dB or 3-dB bandwidth performance of their socket. This number is a first indicator of its high-frequency operation taken within a 50-Ω environment. It is a good practice to compare the parasitics and align them with the DUT requirement. Occasionally, the test engineer will find that socket or contactor pins are the cause of correlation errors between measurements made on the customer's application and measurements made on the tester.

### 15.7.2 Contact Pads, Pogo Pins, and Socket Pins

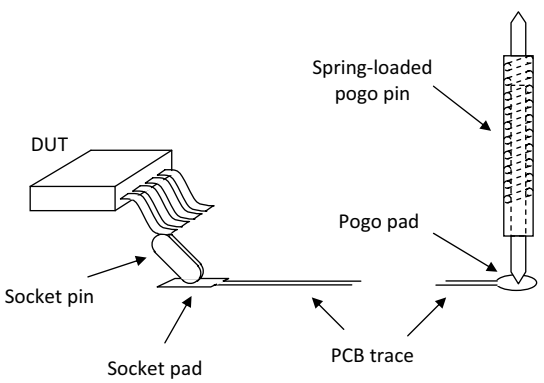
Contact pads are metal pads formed on the outer trace layers of a DIB PCB. They appear on DIB schematics as circles, black dots, or connector bars. These pads allow a relatively reliable, nonabrasive connection between one layer of interface hardware and the next. Two common uses for connector pads are pogo pin connections and DUT socket pin or contactor pin connections (Figure 15.58). A pogo pin is a spring-loaded gold-plated rod that provides a connection between two connector pads. Pogo pins may have blunted ends, pointed ends, or crown-shaped ends, depending on the connection requirements. Pointed or crown-shaped ends tend to dig into the pad surface, providing a reliable, low-resistance connection to the pad. However, the digging action may eventually destroy the pad. Blunted pogo pins are less abrasive to the pads, but are slightly less reliable since they do not dig into the pad surface. Contact pads can also be used to form a connection to DUT socket pins, such as illustrated in Figure 15.58.

Contact pads are usually plated with gold to prevent corrosion and to lower the contact resistance between the pad and the gold-plated pogo pin or socket pin. Without the gold plating, corrosion would lead to higher contact resistance, or even worse, it might result in a complete open circuit even when the pogo pin and pad are in physical contact. Since gold and copper are both soft metals, gold-on-copper contact pads can be damaged by repeated connect/disconnect cycles. To increase their hardness, the copper pads are often coated with a nickel alloy before the gold plating is applied.

A connection formed with a contact pad can be treated as an ideal zero-resistance connection in most cases. The connection adds a small amount of resistance, usually on the order of a few tens of milliohms. However, the resistance may change by 50% or more as the pad is connected and reconnected to the pogo pin or socket pin.

Pogo pins and socket pins also add inductance to the signal path. The inductance may be as little as a quarter of a nanohenry or as large as a few tens of nanohenries. Socket pins and pogo pins may also introduce pin-to-pin or pin-to-ground parasitic capacitance on the order of a few picofarads. In general, long thin pins add more inductance than short fat ones. One way to reduce the effects of pogo or socket pin inductance is to return all high-frequency currents through an adjacent pin. This minimizes the area of the loop through which the current must flow, reducing the inductance of the loop. Unfortunately, the shape and size of the current loops are often determined by the pinout of the device; thus the test engineer can do little to lower the inductance caused by socket pins. Of course, the best way to minimize parasitic socket pin inductance and

**Figure 15.58.** Contact pads, pogo pins, and DUT socket pins.



capacitance is to choose a socket with very short pins. Pogo pins can be also build with a defined impedance mainly 50 Ω, which allows us to minimize the reflection losses for devices with an equal input impedance.

In addition to the electrical performance, often the thermal performance is of interest. Most devices for the automotive applications will need to be tested at a specified elevated temperature, or power devices need to be cooled down to a specified ambient temperature. This will require a defined airflow during test as well as a thermal conductance bridging the thermal path from the device to the DIB. Socket vendors developed different approaches to this requirement: Some are building into their test socket a high number of pogo pins embedded in a solid socket housing, while others optimize the thermal performance with a solid metal (copper) insert bridging the thermal flow from the device to the test board.

Table 15.3 lists the specification of a RF socket and the impact that each parameter has on its operation. The parasitics of the test socket is a major concern during the selection of the socket, and its impact on the DUT performance needs to be considered carefully.

**Table 15.3.** Specification of a High-Performance RF Socket and Selection Criteria

| **Electrical Specification** | | **Typical Value**[a] | **Measure or Indicator for** |
|---|---|---|---|
| Electrical length (compressed height) | | 1.10 mm | potential if socket can be treated as lumped element and potential rotation of the reflection coefficient when not matched to $Z_{IN}$ |
| Inductance | Self | 0.23 nH | the impact to the device performance |
| | Mutual | 0.14 nH | the efficiency to reduce inductance by placing multiple contact pins in parallel |
| Capacitance | Ground | 0.16 pF | the impact to the device performance |
| | Mutual | 0.05 pF | the efficiency to reduce inductance by placing multiple contact pins in parallel |
| S21 Insertion loss/bandwidth (ground–signal–ground) | | –1 dB @ >40 GHz | the maximum frequency the socket can be used |
| S11 Return loss/bandwidth (ground–signal–ground) | | –20 dB @ 14.5 GHz | potential reflections causing mismatch uncertainty |
| S41 Crosstalk/bandwidth (ground–signal–signal–ground) | | –20 dB @ 32 GHz | cross coupling between two pins |
| Average contact dc resistance | | 50 mΩ | IR drop |
| Current carrying capability | | 3 A | current limit |
| Current leakage | | <1 pA @ 10 v | leakage current measurement capability |
| Nearest decoupling area | | 1.25 mm | together with electrical length set the RF performance impact of the test socket |
| **Mechanical Specifications** | | **Typical Value**[a] | **Measure or Indicator for** |
| Contact Compliance | | 0.175–0.200 mm | together with contact compliance a measure for acceptable mechanical tolerances |
| Contact wipe on pad | | 0.12 mm | cleaning effect |
| Contact force (per contact) | | 60 g | important by high pin count DUT |
| Contact tip coplanarity | | 0.05 mm | together with contact compliance a measure for allowable mechanical tolerances |
| Environmental | | –40°C to 155°C | DUT test temperature range |
| Contact material | | BeCuNiAu | together with roughness the capability to test specific lead materials |

[a]Johnstech International, Product specification of ROL100 high-performance test socket.

### 15.7.3 Electromechanical Relays

One of the more common DIB components used in mixed-signal testing is the electromechanical relay. The relay is an electromagnetically controlled mechanical switch. Relays allow the DIB circuits to be appropriately reconfigured for each measurement in the test program. As one of the few moving parts on a DIB, relays represent a potential reliability problem in production. Very high-reliability relays must be chosen so that the DIB can operate through hundreds of millions of open/close cycles without failure.

The metal contacts in a relay are pulled open or closed using an electromagnetic field generated by a DC current passing through a coil of wire (Figure 15.59). The current is switched on and off under test program control as the test code is executed. As mentioned in Chapter 2, "Tester Hardware," flyback diodes are sometimes added to the DIB in parallel with each relay coil to prevent the coil's inductive kickback voltage from damaging the current-driving electronics located inside the tester.

In conventional relays such as the one in Figure 15.59, the moving armature is called the *wiper*. Since it pivots on its pole, it may eventually wear out and get stuck. A more reliable relay is the reed relay, which uses two springy metal reeds that become magnetized by the coil's electromagnetic field. They are attracted to each other by the induced magnetism. Since the reeds do not swing on any pivot, there are no parts to wear out other than the point of contact between the two reeds. Reed relays are often used on DIBs because of their superior reliability.

Occasionally, a resistive buildup can occur between the contacts of a relay, causing an open circuit. Relay damage can also result from poor DIB design. Care should be taken to avoid passing currents through a relay that exceed its rated current specifications. Damage can also be caused to the wiper and contacts by abrupt changes in the current passing through the contacts as they open and close. The high $\partial i/\partial t$ current changes can induce large inductive voltage spikes, leading to a spark that welds the contacts together. Care should be taken to avoid discharging capacitors directly through relays without a series resistance to limit the discharge current. Otherwise, the sudden surge in current from the capacitor may weld the relay contacts together.

Relays, like manually activated switches, are available in a variety of configurations. The most common versions are single-pole/single-throw (SPST), single-pole/double-throw (SPDT), double-pole/single-throw (DPST), and double-pole/double-throw (DPDT). The schematic representation of each of these configurations is shown in Figure 15.60.

The parasitic behavior of relays is fairly complicated. They may exhibit a number of possible nonideal characteristics, including series resistance through the wiper and posts ($R_{WP}$), series inductance through the wiper and contacts ($L_W$), capacitive coupling between the contacts and

**Figure 15.59.** Electromechanical relay (single-pole, double-throw).

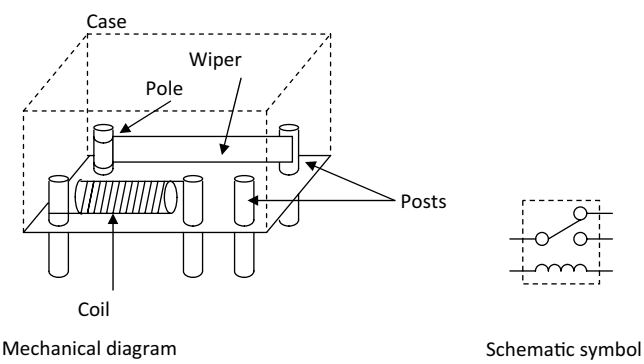


**Figure 15.60.** Electromechanical relay schematic representations.

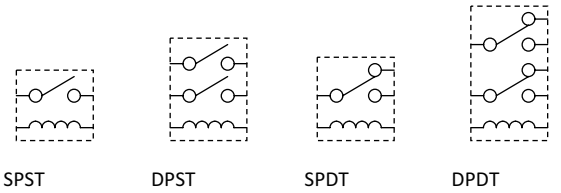
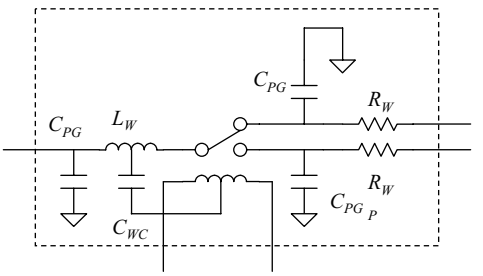



**Figure 15.61.** Parasitic model of SPDT relay.




ground ($C_{PG}$), capacitive coupling between the wiper and the coil ($C_{WC}$), capacitive coupling from contact to contact, and mutual inductance between the coil and the wiper. A simplified model of a SPDT relay is shown in Figure 15.61. Series resistance is typically only a few hundred microhm, although the exact value changes from one closure to the next. Series inductance is often fairly high and may exceed 10 mH. Capacitance values are usually around 1 to 5 pF.

Some relays contain a built-in electrostatic shield that can be grounded to prevent capacitive coupling from external signals to the wiper. The shield helps to prevent electromagnetic interference from corrupting the signal passing through the relay. Similarly, controlled-impedance relays contain a shield conductor that can be grounded to form a continuation of a transmission line. This allows high-frequency signals to propagate smoothly through the relay without generating signal reflections. (Cascaded transmission lines were discussed in Section 15.4.4).

It is good design practice to connect relays so that they are in the most commonly desired position when they are not activated (i.e., when there is no current passing through the coil). For example, if a 1-kΩ resistor is to be connected from a DUT pin to ground during only one test, then it makes sense to connect the relay in the normally open configuration as shown in Figure 15.62a. Configuring the relay in this manner, the resistor is only connected when the test code sets the relay driver into the non-default state. This is a minor point, but it tends to save debug time since the test engineer does not have to explicitly add or remove the resistor during each of the remaining tests. Conversely, if the resistor is desired in all but one test, the relay should be connected in the normally closed configuration Figure 15.62b.

Good alternative solutions for mechanical relays are solid-state FET switches, or for very-high-frequency applications, MEMS switches. Solid-state FET switches are LED-driven MOS FET drivers that have an on-resistance as low as 1 Ω and an output capacitance of 1 pF or less. Since the solid-state FET switch has no mechanical parts, it can be constructed extremely small and can achieve hundreds of millions switching cycles. The principle structure is shown in Figure 15.63.

**Figure 15.62.** Relay default configurations: (a) Normally open. (b) Normally closed.

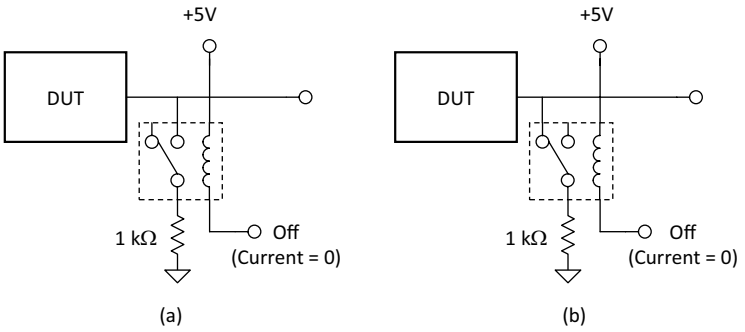
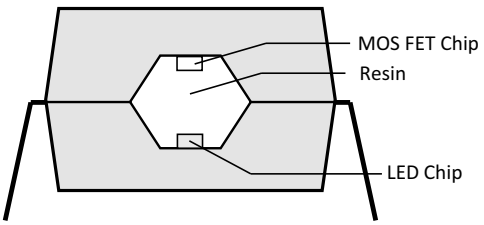



**Figure 15.63.** Solid-state FET switch.




MEMS (micro-electro-mechanical systems) switches are typically used in RF DIB designs to utilize the low insertion loss over a wide frequency range. MEMS switches are built typically using a wafer process. Two electrodes within a DC electrostatic field actuate a thin membrane acting as the switch wiper. The insertion loss can be as low as 1dB or less, while the frequency characteristic have been reported as high as 40 GHz. A disadvantage of most MEMS switches is that they required high actuation voltage; also, they require a DC path through the switching electrodes.

## 15.7.4 Socket Pins

Since relays and active circuits such as op amps are subject to electrical or mechanical failures, they must be replaced from time to time. Although op amps and relays can be soldered directly onto the DIB PCB, replacement is far easier to perform if the relays are mounted in socket pins (Figure 15.64). Socket pins should ideally be used for any component having more than two or three leads.

Surface-mounted components with more than two pins are more difficult to unsolder without damaging the board. Unfortunately, the reduced pin inductance of surface-mount components is sometimes required for very-high-frequency testing. Also, the extra capacitance and inductance of socket pins may make a socket connection inferior at high frequencies. In such cases, surface-mounted relays, op amps, and other active devices may be the only viable alternative, even though they make the DIB more difficult to repair. Surface-mounted relays and active components should be used when needed for electrical performance.

**Figure 15.64.** Socket pins allow easy repair and maintenance of DIBs.

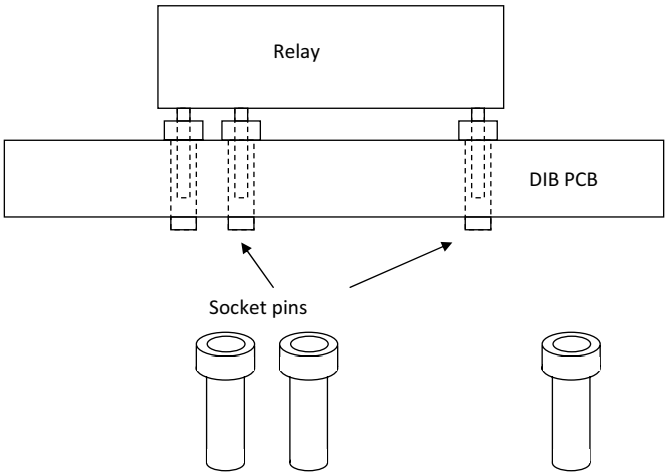
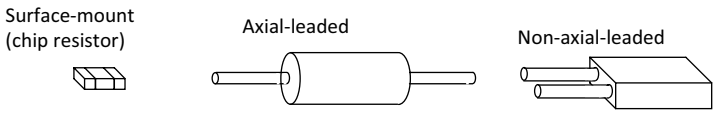



**Figure 15.65.** Common resistor packages.




## 15.7.5 Resistors

Resistors are available in a variety of package types, including surface-mount, axial-leaded, and non-axial-leaded varieties (Figure 15.65). They can be constructed using a wide variety of resistive materials, most commonly carbon or metal (e.g., aluminum). Resistors can be constructed as either a solid core of resistive material, a coil of resistive wire, or a thin film of resistive carbon or metal. Carbon film and metal film resistors are constructed by depositing a thin film of the resistive material onto an insulator such as ceramic. The thin film gives a higher resistance than a solid core of the same material.

The choice of material and package type determines the power dissipation capabilities of the resistor, its accuracy, its stability over time and temperature, and its cost. Power dissipation is basically a function of the resistor's size. Larger resistors can typically dissipate more heat than small resistors. The test engineer should determine the maximum power that must be dissipated by each resistor on a DIB using the equation

$$\text{power} = \frac{V^2}{R} \text{ watt} \tag{15.33}$$

where $V$ is the maximum RMS voltage dropped across the resistor at any point in the test program. The RMS voltage should include both DC and AC components.

The test engineer should also consider the accuracy requirements of each resistor. In general, metal film and wire-wound resistors are more accurate than carbon resistors. For tolerances of 5%

to 20%, solid carbon or carbon film resistors are typically acceptable. Tolerances of 1% generally require metal film resistors. Tolerances below 1% can be attained using a trimmed metal film resistor. Some component vendors are able to provide resistor tolerances of 0.01% or better using a trimmed metal film process. These resistors are not only highly accurate, but are also very stable over time and temperature. Extremely high accuracy can also be achieved using a wire-wound resistor constructed from a coil of wire.

In general, the cost of a resistor is inversely proportional to its accuracy. A 20% carbon resistor is far less expensive than a custom-trimmed 0.001% metal film resistor. However, DIBs are usually constructed for maximum accuracy and reliability. Therefore, the cost of components is a secondary issue in DIB design. It is far more important to get a high-test yield than to save a few dollars on DIBs. For this reason, resistors (and most other DIB components for that matter) are chosen based on their performance rather than their cost.

Performance is not only determined by a resistor's accuracy and power-handling capabilities, but is also determined by how closely the resistor can be modeled as a pure resistance. A resistor's material, shape, and size affect its nonideal performance characteristics. Resistors can be modeled to a first approximation as a resistance in series with an inductance and a parallel capacitor as shown in Figure 15.66a. In many cases a parallel equivalent circuit is easier to use; this parallel RLC model is shown in Figure 15.66b, where $L$ is the lead inductance and $C$ is the combination of parasitic capacitance which depends strongly on the resistor structure and build. At low frequencies, the inductance and capacitance may not be important, and the resistor can be modeled as a pure resistance. At higher frequencies, the series inductance and parallel capacitance may become a significant reactive element that affects circuit performance.

The most highly inductive resistors are wire-wound varieties, since they are constructed from a long, highly inductive coil of wire. These resistors are therefore used mainly in low-frequency applications requiring high-power dissipation and high accuracy. Leaded resistors suffer from a small amount of inductance caused by their wire leads, typically on the order of 1 to 10 nH. However, this inductance is often quite tolerable up to several tens of megahertz.

At higher frequencies, the smaller surface-mount packages typically provide the least series inductance. This is partly due to their lack of wire leads and partly due to the fact that they can be soldered directly onto the DIB without the use of a through-hole or via. Through-holes and vias add a small amount of series inductance as well as a few picofarads of parasitic capacitance to ground. Beyond the range of a few megahertz, the series inductance of vias, PCB traces, IC bond wires, and socket pins may become more of an issue than the inductance of the resistor itself.

For very-high frequency applications, resistors are normally selected based on maintaining their ratio of impedance-magnitude-to-resistance ($|Z|/R$) over a range of frequencies to be less than 1.2. A typical plot of this metric is shown in Figure 15.67 for several commercially available 50-Ω termination resistors. Another critical parameter of a resistor when used in high-frequency

**Figure 15.66.** Circuit model of a practical resistor: (a) Parallel-series RLC combination. (b) Equivalent parallel RLC circuit model representation.

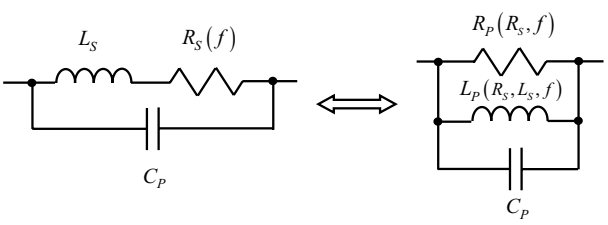
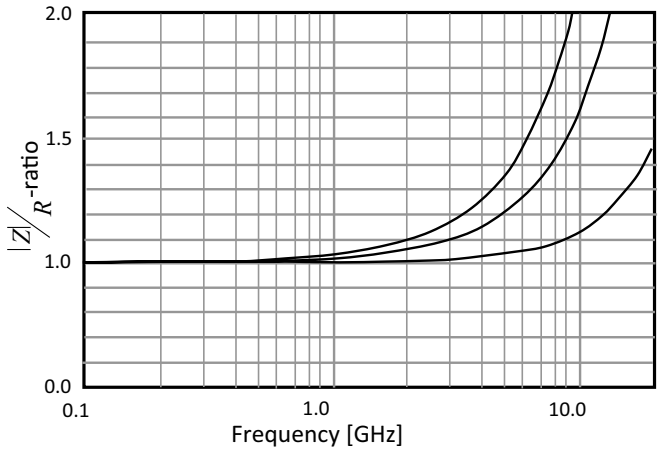


**Figure 15.67.** Typical |Z|/R-ratio for 50-Ω resistors.




applications is its resonance frequency. Near the resonance frequency, minor changes in working frequency will cause major changes in impedance. We'll have more to say about this effect in a moment.

## 15.7.6 Capacitors

Like resistors, capacitors are also available in axial-leaded, non-axial-leaded, and surface-mount varieties. They can be constructed using a simple configuration of two parallel plates (called *electrodes*) separated by a nonconductive dielectric material, a sandwich of plates, or a pair of rolled foil plates. Capacitor performance is largely dependent on the shape and size of the capacitor as well as the type of dielectric material.

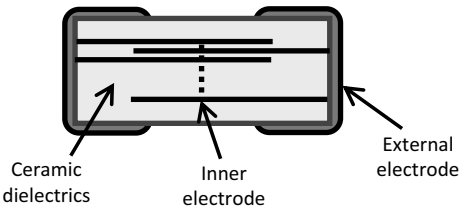
Small values of capacitance can be achieved using the simple two-plate arrangement in which capacitance is given by Eq. (15.9). The value $A$ is the area of one of the plates, $D$ is the distance separating the plates, and $\varepsilon = \varepsilon_r \varepsilon_0$ is the electrical permittivity of the dielectric material separating the plates. Small-value two-plate capacitors are often separated by a thin dielectric film of ceramic, mica, NPO, or even air. These capacitors are limited by physical constraints to a few hundred picofarads.

A larger value of capacitance requires either a larger area $A$, a smaller distance $D$, or a larger permittivity $\varepsilon$. Larger area can be achieved by stacking multiple layers of dielectric materials between parallel plates as illustrated in Figure 15.68. In effect, this forms a group of parallel capacitors in a small space, leading to a relatively large capacitor value in a compact package. High-value surface-mount capacitors up to 1 μF or more can be fabricated using this type of stacked configuration.

Various types of foil capacitors can be constructed using a pair of long metal foil strips separated by a dielectric film such as Mylar, polystyrene, or polypropylene. The long foil strips provide a large area $A$, but the strips and dielectric film must be rolled up and encapsulated in a tubular package to reduce the physical size of the capacitor.

To achieve dramatically larger values of capacitance, the dielectric film can be replaced by a permeable material such as paper soaked in an electrolytic liquid such as ammonia. The foil/liquid roll is sealed in an airtight package to prevent the liquid from evaporating. Then a small current is passed from one foil plate to the other through the electrolytic liquid. This process deposits an

**Figure 15.68.** Cross section of a multilayer chip capacitor.




extremely thin layer of insulating material on one foil plate, while the other plate remains in contact with the conducting liquid.

In effect, the liquid becomes one plate, while the extremely thin insulating deposit forms the dielectric. This produces a very small value of $D$ and allows very high values of capacitance in a small package. Such a capacitor is known as an *electrolytic capacitor*. Aluminum electrolytic and tantalum electrolytic capacitors are constructed using foils of aluminum and tantalum, respectively.

Unfortunately, the deposition of the insulting layer in electrolytic capacitors is a reversible process. DC current passing through the capacitor in the wrong direction can lead to destruction of the insulating dielectric film, and the two plates of the capacitor can come into direct electrical contact through the electrolytic liquid. The large short circuit that results can lead to a rather destructive explosion. Therefore, electrolytic capacitors are marked with a polarity marker, typically a plus or minus sign or a black band representing a minus sign.

Electrolytic capacitors must never be reverse biased, although two of them can sometimes be connected in a back-to-back series connection to form a nonpolarized electrolytic capacitor. In this configuration, DC current is always blocked in one direction by the insulating film of one of the capacitors, regardless of the polarity of the applied voltage. Thus, neither capacitor's insulating layer can be damaged by a reversed DC current.

Ideally, a capacitor should lose no energy; however, an actual capacitor dissipates energy due to internal losses. These losses can be attributed to the series resistance of the internal and external electrodes and current leakage through the dielectric material. A model of a discrete capacitor is shown in Figure 15.69a, where $R_e$ represents the resistance of the external electrode, $R_d$ represents the effective energy loss associated with the polarization of the dielectric material, and $R_{LEAK}$ represents the leakage resistance of dielectric material. $R_{LEAK}$ is usually quite large, exceeding tens of mega-ohms in many cases. The highest leakage occurs in electrolytic capacitors, while the lowest leakage typically occurs in polystyrene or polypropylene capacitors. Smaller values of capacitance generally exhibit lower leakage currents than large ones simply because they generally have less plate and dielectric area. Also included in this model is the inductance $L_s$ associated with magnetic flux self-coupling in the signal path through the capacitor. Because the makeup of each capacitor type is different, it is customary to approximate the high-frequency behavior of a capacitor with the series equivalent model shown in Figure 15.69b. This model includes an equivalent series resistance ESR, an equivalent series inductor ESL, and the nominal effective capacitance, $C_{eff}$. It is these three components that are specified in any technical literature made available from the component supplier.

The series inductance of a capacitor can vary widely from a fraction of one nanohenry to hundreds of nanohenries, depending on the shape and size of the capacitor. Typical values are given in Tables 15.4 and 15.5 for a select group of commercially available capacitors. In general, electrolytic capacitors exhibit very high series inductance, while surface-mounted chip capacitors

**Figure 15.69.** Parasitic model of a practical capacitor: (a) Individual parasitic components for each element of the capacitor. (b) Equivalent RLC series model.

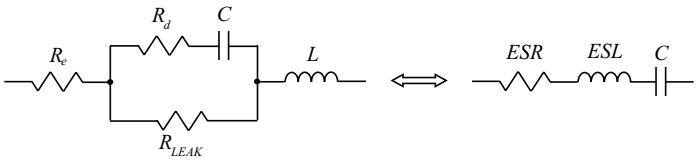



**Table 15.4.** Typical ESL Values for Common SMD Capacitor Sizes

| Package | Size [mm] | ESL [pH] |
|---|---|---|
| 0201 | 0.6 x 0.3 | 400 |
| 0402 | 1 x 0.5 | 550 |
| 0603 | 1.6 x 0.8 | 700 |
| 0805 | 2.0 x 1.25 | 800 |
| 1206 | 3.2 x 1.6 | 1250 |
| 0612 | 1.6 x 3.2 | 60 |

**Table 15.5.** Typical ESL Values for Leaded and Electrolytic Capacitors

| Capacitor Type | Value | ESL (pH) |
|---|---|---|
| Leaded disc ceramic | 0.01 mF | 3000 |
| Leaded monolithic ceramic | 0.01 mF | 1600 |
| Leaded monolithic ceramic | 0.1 µF | 1900 |
| SMD aluminum electrolytic | 47 µF | 6800 |
| SMD tantalum electrolytic | 47 µF | 3400 |

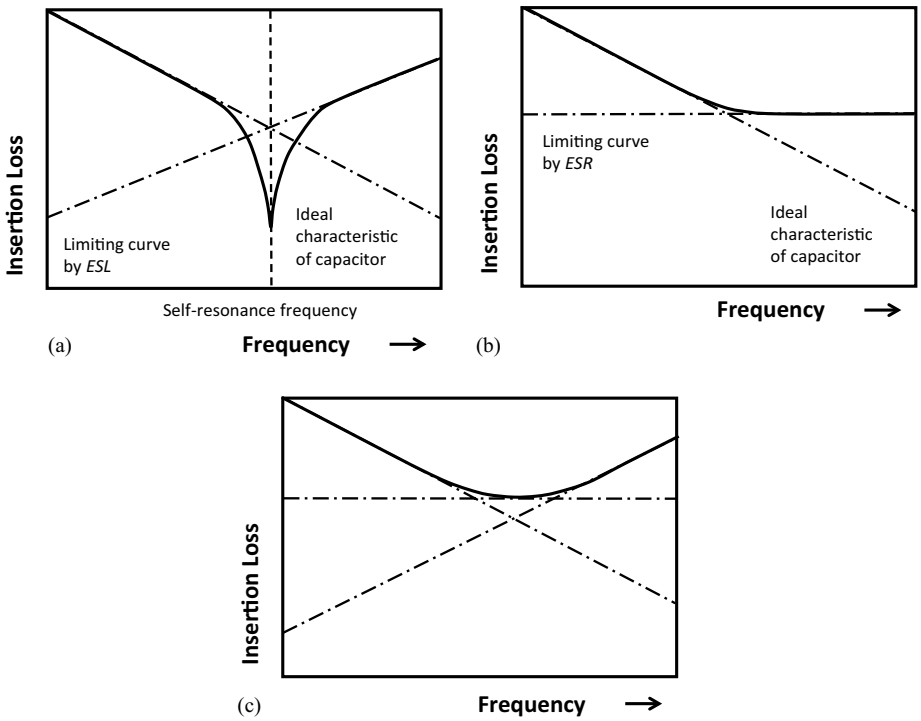
exhibit very low series inductance. A typical self-resonance frequency of a leaded capacitor is in the range of 20 MHz, while for an SMD 1206 type capacitor it can be as low as 50 MHz. The exact value will be given in the data sheet of the individual capacitor series.

One important measure of a capacitor is the *quality factor Q*, where $Q$ is defined as the ratio of the expected reactance of the capacitor (i.e., $|X_C| = 1/2\pi f C_{eff}$) to the equivalent series resistance ESR, given by

$$Q = \frac{|X_C|}{\text{ESR}} \tag{15.34}$$

An ideal capacitor has an ESR of 0, which leads to an infinite quality factor. Capacitors with very good $Q$ factors are required in very-high-frequency applications such as microwave and RF systems. Surface-mounted NPO chip capacitors exhibit very low dielectric losses and series resistance, making them ideal for high-frequency applications. Also, surface-mounted ceramic capacitors are fairly well suited to high-frequency applications.

**Figure15.70.** Insertion loss frequency characteristic of an actual capacitor affected by (a) ESL, (b) ESR, and (c) ESL and ESR.




Another important metric of a capacitor is the *self-resonance frequency* SRF expressed in Hertz. It is defined in terms of the reactive components of the capacitor as follows:

$$\mathrm{SRF} = \frac{1}{2\pi\sqrt{\mathrm{ESL}\cdot C_{eff}}} \tag{15.35}$$

The smaller the values of ESL, the larger SRF becomes; therefore, a small capacitor can be used to provide capacitive impedance for a higher frequency range. Figure 15.70 illustrates the impact of various parasitic components of the capacitor on its insertion loss (or equally impedance) as a function of frequency. Figure 15.70a illustrates the effect that ESL has on the insertion loss of an ideal capacitor. Instead of a decreasing value with frequency for all frequencies, at frequencies around the SRF, the insertion loss is dominated by the behavior of the parasitic inductor (ESL). In Figure 15.70b, we see the effect of the parasitic resistor (ESR) on the insertion loss. While effect of the ESR on insertion loss is the same across all frequencies, its effect on the capacitor is to limit its insertion loss to some minimum value. With both effects combined, we see from Figure 15.70c that the capacitor behaves as a capacitor only for frequencies below the SRF. By selecting the appropriate type of capacitor, this effect can be adjusted so that the required capacitance is realized over the appropriate frequencies. Table 15.6 lists the typical ESR values for a variety of capacitor types.

**Table 15.6.** Common Capacitor Parameter and Tradeoffs

| Type | Picture | Capacitance Range | ESR | Leakage | Voltage Rating | Temperature Range | General Notes |
|---|---|---|---|---|---|---|---|
| Ceramic |  | pF to µF | Low | Medium | High | -55°C to +125°C | Multipurpose, inexpensive |
| MICA |  | pF to nF | Low 0.01Ω to 0.1Ω | Low | High | -55°C to +125°C | For RF filters,expensive, very stable |
| Plastic Film |  | few µF | Medium | Medium | High | varies | For low frequency, inexpensive |
| Tantalum |  | µF | High 0.5Ω to 5.0Ω | Low | Lowest | -55°C to +125°C | Expensive, nonlinear (limited for audio) |
| OSCON |  | µF | Low 0.01Ω to 0.5Ω | Low | Low | -55°C to +105°C | Best quality, highest price |
| Aluminum electrolytic |  | High µF | High 0.05Ω to 2.0Ω | Medium | Low | varies | For low to med frequencies, inexpensive, hold charge for long time, not for production test |

## 15.7.7 Inductors and Ferrite Beads

Inductors are usually built using a length of wire, often looped into a coil to increase the magnetic coupling and, in turn, its inductance. Larger values of inductance can be achieved by wrapping the wire coil around a magnetic core, such as iron or a ceramic material with magnetic properties. Inductors are available in both surface-mount packages and leaded packages. However, the surface-mounted packages are typically limited to smaller values of inductance.

Inductors are occasionally required as part of a DUT circuit such as a voltage doubler. They may also be used as part of a passive load circuit that must be connected to a DUT output to simulate a speaker coil or similar system-level component. Inductors can also be used in conjunction with capacitors to simulate long transmission lines by building an *LC* network like the one in Figure 15.31. For RF DIB applications, inductors are frequently used as part of a matching circuit or as a choke to bias a DUT via an RF line. In matching circuits, the value of the inductor is of primary interest, however, for choke circuits, the self-resonant frequency is the key parameter of interest.

**Figure 15.71.** Parasitic model of a practical inductor: (a) Individual parasitic components for each element of the inductor. (b) Equivalent parallel RLC model.

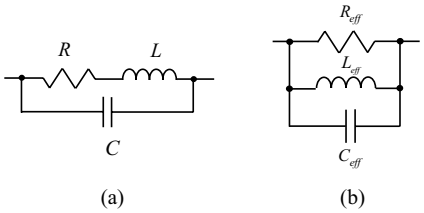
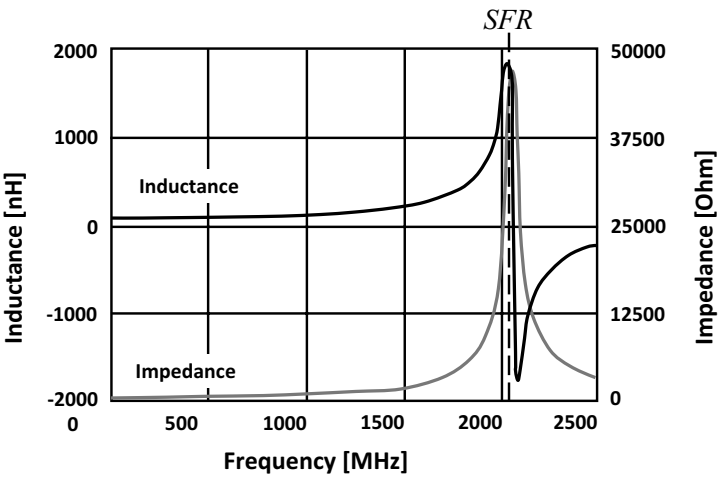



**Figure 15.72.** Typical inductance and impedance for a 100-nH wire wound inductor.




A practical inductor can be modeled by the combinational RLC circuit shown in Figure 15.71a. Here the inductor consists of an ideal inductor of value $L$, two parasitic elements, a series resistor $R$, and a shunting capacitor $C$. Because the specific circuit model varies with the device type, it is customary to model the inductor as an equivalent parallel RLC circuit shown in Figure 15.71b. In general, the series resistance $R_{eff}$ of an inductor is quite low and often neglected. At low frequencies, the capacitor $C_{eff}$ acts as an open circuit and the terminal behavior of the inductor is dominated by the behavior of inductor $L_{eff}$, that is, impedance increases linearly with frequency. At very high frequencies, the impedance of $C_{eff}$ drops to very low levels, thereby shorting out the influence of the inductor. It is fair to say at very high frequencies the real inductor behaves like a capacitor. Somewhere in between these two extremes, both elements are contributing to the terminal behavior. An important frequency point within this range is the self-resonance frequency SRF expressed in Hertz, described by

$$\text{SRF} = \frac{1}{2\pi\sqrt{L_{eff} \cdot C_{eff}}} \tag{15.36}$$

A plot of the terminal impedance as a function of frequency is shown in Figure 15.72. Also superimposed on this plot is the effective inductance between the device terminals. As is evident from

this plot, the impedance peaks around the SRF, as well, the effective inductance changes quickly from a positive to negative quantity (signifying capacitive behavior).

For impedance matching applications it is important to have constant inductance versus. frequency near the operating frequency. This requires selecting an inductor with an SRF well above the designated frequency of operation. A rule of thumb is to select an inductor with an SRF that is a decade higher than the operating frequency. Typically, the SRF is higher for lower inductance values. Also, tight inductance tolerance is desired. Wire-wound inductors typically achieve tighter tolerances than multilayer or thick film-type inductors.

If the inductor is to be used as a single-element high-frequency choke to supply a DC level via a RF terminal to the DUT, the inductor selection will be based on the highest reject frequency required. At the self-resonant frequency of an inductor, the series impedance is at its maximum. So, for a simple RF choke, the inductor selection will be based on finding an inductor whose SRF is very near the frequency where the choking is required. For a wider frequency range, a choke network with multiple inductors in series can be designed.

A high quality factor $Q$ results in a narrow bandwidth, which is important if the inductor is to be used as part of a $LC$ tank circuit of a VCO or a narrow band filter application. High $Q$ also leads to a low insertion loss minimizing power consumption. The $Q$ factor of an inductor is defined as

$$Q = \frac{\Im m\{Z\}}{\Re e\{Z\}} \tag{15.37}$$

where $Z$ represents the impedance seen between the two terminals of the device. Typically, wire wound inductors have a much higher $Q$ value than a multilayer inductor of the same size and value.

Other important parameters associated with an inductor are its current rating, DC resistance and temperature rating. While a small size is typically desired to keep the board space small and the operating frequency high, the laws of physics limit how small an inductor can be made for a given application.

Applications that require large current levels requires larger wire or more strands of the same wire size to keep losses and temperature rise to a minimum. Larger wires reduce the DC resistance and increase the $Q$ factor, but will also increase the size and, in turn, reduce the self-resonance frequency. The current ratings for wire-wound inductors are typically better than the current rating for multilayer inductors of the same inductance value and size. The current capacity and lower DC resistance can be achieved by using a ferrite core inductor with a lower turns count. Ferrite, however, may introduce other limitations such as larger variations in the inductance value with temperature, looser tolerances, and a lower $Q$ factor.

Inductor are often constructed with a magnetic core to increase its inductance. Depending on the magnetic core material used, the inductor may also exhibit lossy behavior at high frequencies, resulting in an apparent increase in the series resistance of the inductor. In fact, a class of inductors called *ferrite beads* is intentionally designed with very lossy core materials to achieve a component with near-zero resistance at low frequencies and higher resistance at higher frequencies. A typical ferrite bead impedance chart is shown in Figure 15.73. As shown, both the inductance $Z_L(f)$ and the series resistance $R(f)$ of the ferrite bead are functions of frequency.

Ferrite beads are useful for blocking high-frequency interference signals. They can reduce AC crosstalk from one circuit to another while allowing DC current to flow freely. For example, a ferrite bead can be placed in series with a power supply to prevent supply current spikes drawn by one circuit block from disturbing another circuit block, as shown in Figure 15.74. Both the inductance and resistance of the bead are near zero at DC; thus power supply current can flow freely

**Figure 15.73.** Typical ferrite bead impedance chart.

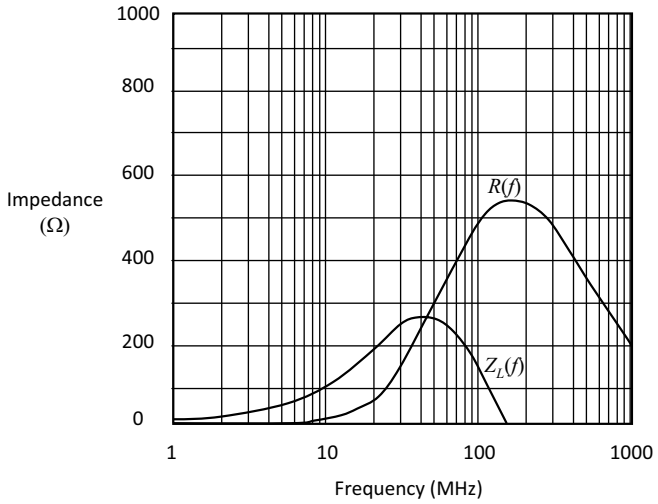
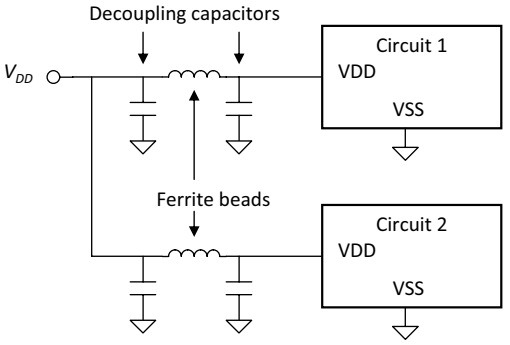



**Figure 15.74.** Ferrite beads in power supply connections.




through the ferrite beads. Note that the schematic symbol for a ferrite bead is the same as that for an inductor. This is because a ferrite bead is an inductor with a lossy core.

## 15.7.8 Transformers and Power Splitters

Transformers are sometimes used on DIBs to translate a high-frequency single-ended signal into a differential signal or vice versa. Unfortunately, the transformer's frequency response is highly dependent on the output impedance of the transmitting circuit as well as on the input impedance of the receiving circuit. Consequently, the frequency response of the transformer is difficult to accurately calibrate, since it may change from one DUT to the next.

**Exercises**

| | | |
|---|---|---|
| **15.11.** | What is the self-resonance frequency of a 1-nF capacitor with a package size of 0402? Use the ESL data of Table 15.4. | ANS. 214.6 MHz. |
| **15.12.** | A Vcc line of a 5.5-GHz circuit needs to be decoupled with a capacitor. A 0201-sized capacitor can be used. What maximum capacitor value can be selected, when the SRF should be 30% above the blocked frequency? | ANS. $C$ = 1.239 pF. |
| **15.13.** | What is the $Q$ value of a 1-nF capacitor of the size 0402 if the ESR is per data sheet 0.1 Ω at 1 MHz? | ANS. 1592. |

Power splitters are typically used in RF and microwave systems, but occasionally find use on mixed-signal DIBs. Their useful operation can be limited to a small range of frequencies, whereas resistive power splitters are generally able to handle a fairly wide range of frequencies.

Active circuits such as instrumentation amplifiers and other op-amp circuits are often superior to transformer circuits, since they can be accurately calibrated. Also, they present a consistent, high-impedance load to the DUT. Transformers and power splitters, by contrast, present a low-impedance inductive or resistive load to the DUT. Since many DUTs cannot drive low impedances, transformers and power splitters are often unusable. However, because they can pass frequencies well above those passed by active op-amp circuits, they are sometimes the only viable choice. Also, when attached to differential DUT inputs, transformers allow the DUT to set its own common-mode voltage at the differential input. By contrast, the active differential outputs of an op-amp single-ended to a differential converter forces the common-mode input voltage to a predetermined voltage, which may or may not be acceptable for a particular DUT input.

## 15.8 COMMON DIB CIRCUITS

### 15.8.1 Analog Buffers (Voltage Followers)

Sometimes a device output is incapable of driving the parasitic capacitance presented by the traces, cables, and relays leading to a tester instrument. An analog voltage follower with higher capacitive drive capability can be used to buffer the output signal before it is passed to the tester. The primary concerns with analog buffers are offset, signal bandwidth, and added noise from the amplifier. Generally, higher-bandwidth amplifiers generate more noise while low-noise amplifiers have a limited bandwidth. Offset and gain errors can be removed through a focused calibration process (see Chapter 5). However, noise generated from the buffer may or may not be removable through a calibration process. Figure 15.75 shows a simple op-amp buffer circuit including a relay for calibration and functional checking of the buffer.

Sometimes, an oscillating DUT amplifier can be stabilized using a small series resistor between the amplifier output and the tester. The resistor restores phase margin to the amplifier, eliminating the need for a buffer amplifier. This saves considerable complexity on the DIB.

### 15.8.2 Instrumentation Amplifiers

Another type of commonly used op-amp circuit is the differential to single-ended converter, also known as the *instrumentation amplifier*. Figure 15.76 shows an instrumentation amplifier

**Figure 15.75.** Buffer amplifier with calibration relay.

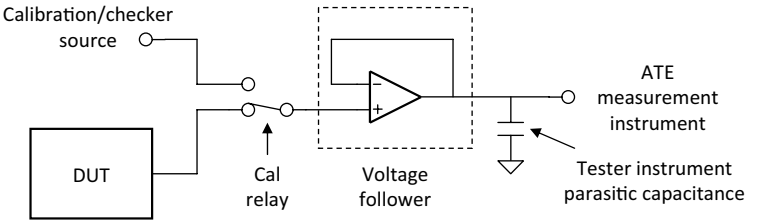
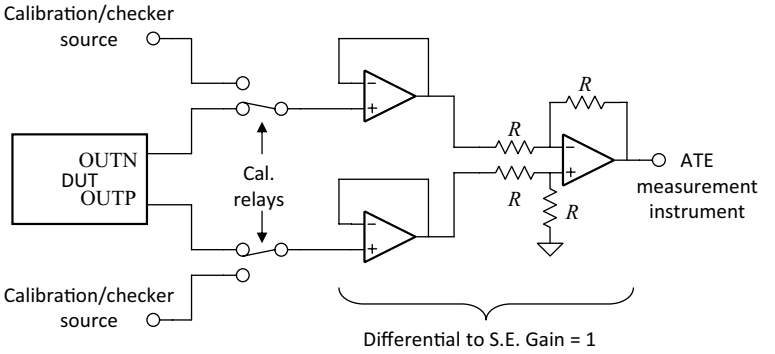



**Figure 15.76.** Op-amp differential to single-ended converter with calibration relays.




constructed using three op amps and four matched resistors. Today, such an arrangement can be found in a single IC with excellent performance specifications The two voltage followers at its input give the instrumentation amplifier a very high input impedance. Without these voltage followers, the resistors surrounding the third amplifier would present a load impedance of $2R$ to one of the DUT outputs and $R$ to the other output. Of course, if the DUT outputs can drive these resistors without a problem, then the voltage followers are unnecessary. Like the previous analog buffer circuit, this circuit needs calibration relays to allow focused calibrations and checkers using a differential calibration/checker source.

The reason this type of circuit is sometimes needed on a DIB is that certain tester instruments are not capable of receiving a differential signal. In such instances, the differential DUT output must be converted to a single-ended signal before the tester can measure it.

A related problem arises with differential inputs that must be driven from an instrument having only a single-ended output. The simple single-ended to differential converter in Figure 15.77 uses an inverter to generate an inverted image of a single-ended input. The differential signal is centered around a common mode voltage, $V_{CM}$, which is set to the desired voltage level by a tester instrument or by a DUT $V_{MID}$ output. Notice that this single-ended to differential converter has a gain of 2 V/V. Therefore, the signal level of the single-ended source must be attenuated to one-half of the desired differential signal level.

Since the inverter in Figure 15.77 may introduce a significant phase shift at higher frequencies, this circuit is not ideal for high-frequency differential circuits. A somewhat better circuit can

**Figure 15.77.** Single-ended to differential converter.

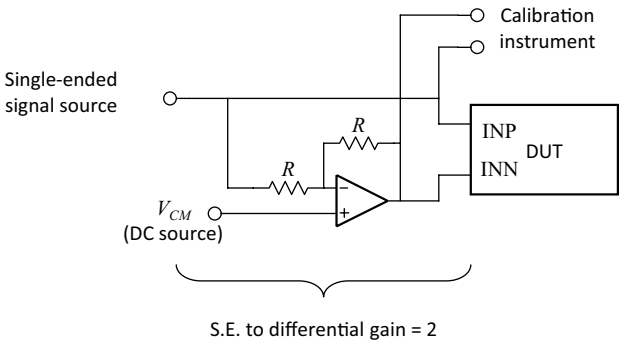
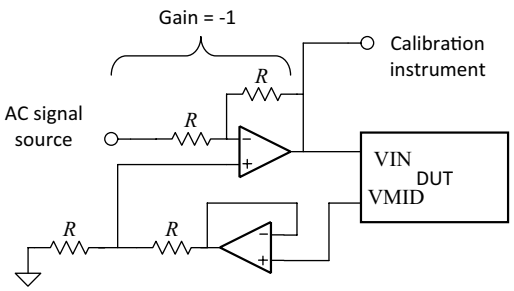



**Figure 15.78.** $V_{MID}$ reference adder.




be built using a voltage follower in series with the noninverted signal to balance out the phase shift somewhat. Since the amplifiers are not in the same configuration, even the enhanced circuit produces some phase mismatch at very high frequencies. Fortunately, the circuit in Figure 15.77 is good enough for many DUTs having differential inputs.

## 15.8.3 $V_{MID}$ Reference Adder

Sometimes, a DUT produces a $V_{MID}$ voltage to which all input signals must be referenced. This type of input is commonly used in microphone inputs. Since microphones are basically differential signal generators, any noise or ripple present on the $V_{MID}$ output gets canceled by the differential input circuits of the DUT. Therefore, an input signal generated by the tester has to fluctuate with any noise and ripple on the $V_{MID}$ signal to simulate the differential nature of a microphone. A $V_{MID}$ adder can be built using the simple op-amp circuit in Figure 15.78. The $V_{MID}$ signal is added to the input signal from the tester, simulating the differential nature of a microphone. Since many DUTs are designed with a very weak $V_{MID}$ output driver, a voltage follower is used to buffer the $V_{MID}$ output before it is passed to the op-amp adder. Obviously, if the DUT's $V_{MID}$ driver is strong enough to drive a load of $2R$, then this extra buffer is unnecessary.

The limitations of this circuit are its bandwidth and the small amount of noise generated by the op amps. The gain and offset of this circuit must be calibrated for maximum accuracy. A transformer might be used instead of the active op-amp circuit to work around noise and bandwidth limitations, but the transformer's frequency response would have to be carefully calibrated.

### 15.8.4 Current-to-Voltage and Voltage-to-Current Conversions

Tester instruments do not generally provide a means to directly measure AC currents. We can measure an AC current by dropping it across a resistor, but the parasitic capacitance of the tester instruments sometimes makes this an unacceptable solution. A low-impedance voltage output is a preferable signal for measurement. The circuit in Figure 15.79 can be used to convert current outputs to voltage outputs. The current-to-voltage translation is defined by Ohm's law ($V = I\,R$), although the op amp injects a factor of –1 into the equation ($V_{out}/I_{in} = -R$). The DUT sees a virtual ground at its output due to the feedback loop of the op amp. If the DUT is designed to drive its current into a different termination voltage (such as $V_{MID}$), then the noninverting input of the op amp can be connected to the desired termination voltage instead of ground. The simple $I$-to-$V$ amplifier in Figure 15.79 is limited by the bandwidth, gain, and offset of the op amp. Its exact offset and voltage-over-current "gain" versus frequency must be calibrated using a focused calibration process.

Tester instruments also do not generally provide a means to force AC currents into the DUT. A transconductance amplifier circuit (Figure 15.80) can be used to make this conversion. In this circuit, the instrumentation amplifier senses the voltage drop across the source resistor, $R_S$, and feeds that voltage back to the inverting input of an op amp. The op amp adjusts its output voltage until the current forced across $R_S$ generates a voltage drop equal to $V_{in}$. Of course, this transconductance amp must be calibrated at all frequencies of interest if maximum accuracy is to be achieved.

**Figure 15.79.** Current to voltage converter.

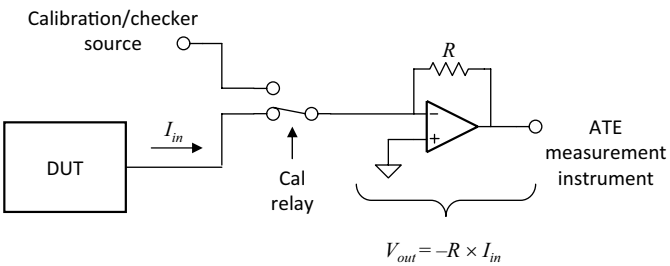
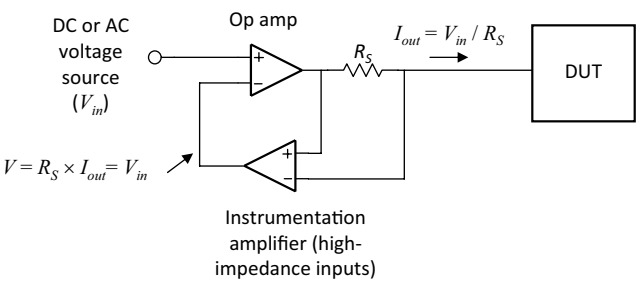



**Figure 15.80.** Voltage-to-current converter (transconductance amplifier).



## 15.8.5 Power Supply Ripple Circuits

For some reason, mixed-signal testers have never included easily programmed ripple sources compatible with PSRR tests. PSRR tests require that we add a sinusoidal or multitone signal to one or more of the DUT's power supply voltages. This is not as easy as it might seem, since the output of power supplies include large bypass capacitors specifically designed to dampen ripple on the supply voltage. If the desired ripple cannot be provided by the tester itself, the test engineer can utilize any of a number of DIB circuits.

The simplest ripple injection approach takes advantage of the programmable DUT power supply's Kelvin sense line to force it to ripple its output. This ripple scheme is illustrated in Figure 15.81. The ripple source (a sine wave generator or arbitrary waveform generator) applies an AC signal to the sense line of the Kelvin connection through a resistor.

The power supply is forced to adjust its output to maintain a fixed voltage at its sense line. The power supply thus behaves as an op amp, with the sense line acting as a high-impedance inverting input and the programmed voltage level acting as a DC source at the op amp's noninverting input. The addition of the two resistors in the sense path forms an inverting gain stage, as shown in Figure 15.82. Once the Kelvin-connected DUT source is redrawn in this manner, it is easy to see how an AC signal can be injected into the power supply's output voltage. The output signal is given by

$$v_S = -\frac{R_2}{R_1}(v_R - V_P) \tag{15.38}$$

where $v_S$ is the DUT power supply voltage (including its normal DC value and the injected AC ripple), $v_R$ is the signal from the ripple source, and $V_P$ is the programmed DC voltage level set by the test program.

**Figure 15.81.** Kelvin sense ripple injection circuit.

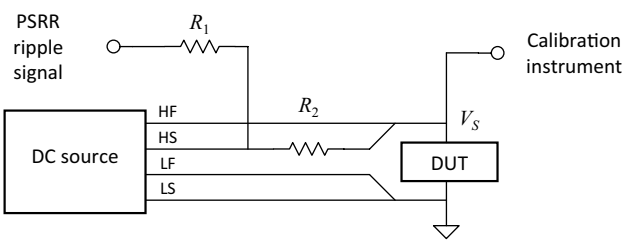



**Figure 15.82.** Equivalent op-amp inverting gain stage.

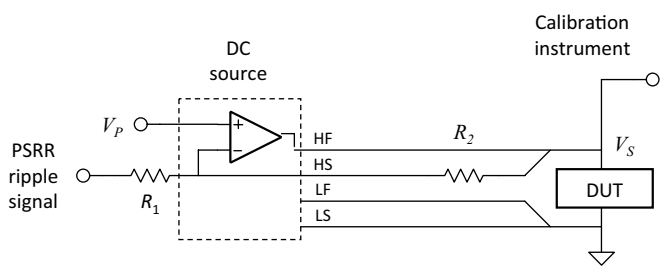
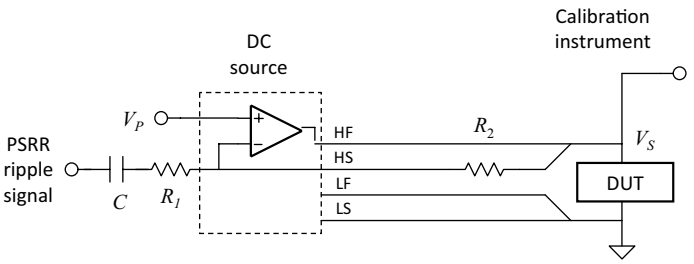


**Figure 15.83.** Equivalent ripple circuit with DC blocking capacitor.




The values of $R_2$ and $R_1$ are chosen to give an attenuation, rather than a gain. This allows very small ripple voltages to be applied to the power supply using a fairly large ripple source amplitude. (Remember from Chapter 5 that large tester signal amplitudes are desirable because they are less susceptible to noise.) Values of $R_1 = 10$ kΩ and $R_2 = 1$ kΩ are commonly used, giving the ripple circuit a gain of 1/10.

If the circuit in Figure 15.82 is used, the ripple signal must include a DC offset equal to $V_P$. Otherwise, the ripple signal will introduce a DC offset into the power supply voltage. To use a ripple signal with no DC offset, a DC blocking capacitor can be added in series with the ripple source. Of course, this turns the ripple circuit into a first order high pass filter, as shown in Figure 15.83.

The cutoff frequency $F_c$ of this filter is given by

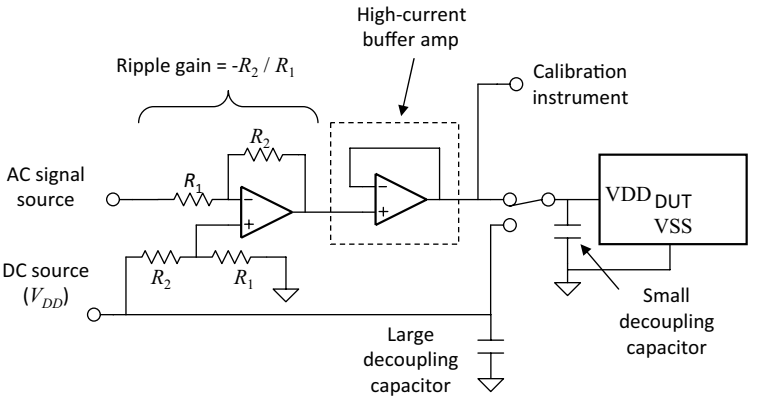
$$F_C = \frac{1}{2\pi R_1 C} \quad \text{Hz} \tag{15.39}$$

Note that the circuit in Figure 15.83 includes a calibration path. This connection is absolutely necessary, since the frequency response of the Kelvin ripple circuit is not known. Each frequency in the injected signal must be calibrated during a focused calibration process to achieve acceptable accuracy in the injected power supply ripple signal. If the DUT needs a large DIB decoupling capacitor on the rippled power, the capacitor must be removed from the circuit temporarily (with a relay) to prevent it from damping the ripple signal. The Kelvin ripple circuit has one major drawback. It is impossible to ripple most power supplies at a frequency higher than a few kilohertz. At higher frequencies, a different approach must be taken.

One possibility is to use a DIB ripple buffer, which can provide the DC plus AC signals needed to drive the DUT during the supply ripple tests. This circuit is simply an op-amp adder circuit with a high-current buffer amplifier connected to its output (Figure 15.84). Again, a calibration path is added to improve the circuit's accuracy. This supply ripple circuit can be inserted into the power supply line using a SPDT relay, as shown.

Note that the large decoupling capacitor is automatically removed when the relay is thrown to the ripple circuit output. The large decoupling capacitor, typically a 10-μF electrolytic variety, provides relatively low-frequency currents to the DUT. Its own series inductance is many times that of the relay; thus we can safely connect and disconnect it using the relay. A smaller decoupling capacitor is often needed to provide higher-frequency currents to the DUT. It must be located very close to the DUT to minimize series inductance between the capacitor and the DUT power pin. Since the ripple circuit relay would provide too much series inductance, the small capacitor must be located next to the DUT. Therefore, the small high-frequency capacitor cannot be removed by the relay during the power supply ripple tests.

**Figure 15.84.** Buffer amp ripple injection circuit.




## 15.9 COMMON DIB MISTAKES

### 15.9.1 Poor Power Supply and Ground Layout

One of the most common sources of noise injection in mixed-signal DIBs is poor power and ground layout. The best way to avoid problems with power distribution and grounding is to use as many planes as needed, without regard to DIB cost. Although each layer in a multilayer DIB adds fabrication cost, the expense is fairly negligible compared to the production yield loss due to poor DIB performance. Therefore, a good DIB might include one or two layers dedicated to digital transmission line ground and noisy current returns, one layer dedicated to analog current returns, one layer dedicated to low-current analog ground (quiet ground serving the purpose of a zero-volt reference layer), and at least one layer dedicated to split power planes. Thus a 10-layer DIB may contain five or six layers dedicated to power and ground distribution.

### 15.9.2 Crosstalk

Another common problem on mixed-signal DIBs is crosstalk, especially between digital and analog signal lines. The digital-to-analog crosstalk problem can be dramatically reduced by placing analog signals on a separate PCB layer from digital signals, with an analog ground plane between the two signal layers. Analog-to-analog crosstalk can be minimized by simply realizing which signals are most susceptible (i.e., which signals have the highest impedance) and preventing high-frequency, high-amplitude signals from passing nearby. Also, the sensitive high-impedance nodes should be as short as possible to avoid crosstalk and coupling of external noise sources such as radio waves.

One of the most common sensitive nodes on a mixed-signal DUT is its current reference input. This input is typically tied to $V_{DD}$ or ground through a very high-impedance bias resistor. The node between the bias resistor and the DUT is an extremely sensitive one. Noise injected into this node will translate directly into noise throughout the DUT. Therefore, current bias nodes should always be kept extremely short, preferably surrounded by a shield ring.

Another type of sensitive node is the DUT reference voltage. Reference voltages are typically driven by a low-impedance tester source and are therefore less susceptible to crosstalk than high-impedance bias nodes. However, any noise injected into the reference voltage will translate

**Exercises**

**15.14** When placed in a particular test mode, a DUT routes a weak internal circuit node to an analog test pin for measurement. The signal at the test node contains frequencies from DC to 100 kHz. Its output impedance is 10 kΩ (purely resistive). We wish to measure the signal using a digitizer having a distributed cable capacitance of 350 pF plus a lumped input capacitance of 50 pF. Can this signal node be measured directly, or will a buffer amplifier be needed on the DIB?

ANS. At relatively low frequencies, the DUT output impedance forms a low-pass filter with the digitizer input capacitance.
The 3-dB cutoff frequency of the filter is 3.98 kHz, preventing accurate measurement at 100 kHz. A local buffer amplifier, such as the one in Figure 15.75, will be needed on the DIB.

**15.15** The Kelvin PSRR ripple circuit illustrated in is constructed using the values $R_2 = 1\ \text{k}\Omega$ and $R_1 = 10\ \text{k}\Omega$. The power supply is programmed to 3.3 V DC. Describe a signal, $v(t)$, at the input to $R_1$ that would produce a DUT power supply ripple of 75 mV RMS at 1 kHz. (Assume no errors due to circuit bandwidth, component mismatch, etc.)

ANS. $$v(t) = 3.3\ \text{V} - \sqrt{2} \times 75\ \text{mV} \times \frac{10\ \text{k}\Omega}{1\ \text{k}\Omega} \sin(2\pi f \cdot t)$$
$$= 3.3\ \text{V} - 1.06\ \text{V} \times \sin(2\pi \times 1000t)$$

**15.16** Repeat exercise 15.16 using the PSRR buffer circuit illustrated in Figure 15.84. (Assume $V_{DD}$ is set to 3.3 V DC.)

ANS. $v(t) = -1.06\ \text{V} \times \sin(2\pi \times 1000t)$

directly into noise in the DUT circuits. Therefore, reference voltage nodes should also be laid out as if they were extremely vulnerable to crosstalk.

### 15.9.3 Transmission Line Discontinuities

Small discontinuities in transmission lines can lead to glitches on the rising and falling edges of very fast digital signals. Such glitches can sometimes lead to timing errors or double-clocked logic in the DUT. The discontinuities are caused by lumped capacitance or inductance at transition points along the transmission line. For example, a lumped capacitance and/or inductance exists whenever a digital signal trace is routed between layers through a via or other through hole. It is best to avoid routing digital signals from one layer to another, unless absolutely necessary.

### 15.9.4 Resistive Drops in Circuit Traces

As we saw in Example 15.1, even relatively short traces may have a series resistance of several hundred millohms. If we try to force current through such a trace, we will get a voltage drop due to the parasitic resistance of the trace (this effect is also referred as IR drop). Sometimes these voltage drops are unimportant, but other times they can lead to errors nearly as large as the parameter we are trying to measure. The test engineer should always consider the effects of series resistance on each trace on the DIB. If the series resistance is serious enough to cause a problem, the trace

can either be made wider, or a sensing circuit such as a Kelvin connection can be used to compensate for the resistive drops in the PCB trace.

### 15.9.5 Tester Instrument Parasitics

The various cables and wires that connect a DUT to a tester's instruments can present a significant capacitive load to the DUT's pins. Often, the loading is high enough to cause gain errors, phase shifts, or even DUT circuit oscillations. It is very important for a test engineer to ask the design engineer responsible for each DUT circuit what its capacitive drive capabilities will be.

If the output impedance of the DUT is incompatible with the tester's load capacitance, then a voltage follower will probably be needed on the DIB buffer the DUT's output. Even if the DUT is designed with a low output impedance, the load capacitance of some tester instruments may cause it to break into oscillations. The test engineer and design engineer should determine whether the unbuffered tester inputs might cause any DUT oscillations. If so, analog buffers must be added to the DIB design.

### 15.9.6 Oscillations in Active Circuits

Operational amplifiers used in buffer amplifiers or other DIB circuits may break into oscillations if they are not laid out properly. For example, the inverting and noninverting inputs to an op amp are extremely sensitive to parasitic capacitance. If these PCB traces are laid out so that they are more than a few tenths of an inch long, the amplifier will often break into oscillations. This problem is commonly seen in the nulling amplifier circuits described in Chapter 3, "DC and Parametric Measurements."

Another source of oscillations is poor power supply and decoupling capacitor layout. If the decoupling capacitors attached to an amplifier's power supplies are not positioned very close to the amplifier's power pins and ground plane, then the amplifier may break into oscillations. The oscillations are due to the extra parasitic inductance of the connecting PCB traces. This is especially true of high-bandwidth operational amplifiers. Decoupling capacitors in general should always be placed very close to their supply pin.

Oscillating amplifiers pose a particularly tricky problem. When measuring a DC offset using an oscillating buffer amplifier, the tester's DC voltmeter ignores the oscillation. Instead, it measures the average voltage level at the oscillating amplifier's output, which may or may not have any relation to the DUT signal to be buffered. Thus significant DC errors can be introduced by the oscillating amplifier.

### 15.9.7 Poor DIB Component Placement and PCB Layout

If the test engineer gets nothing else out of this chapter, at least one fact should come across loud and clear. The physical layout of the DIB is extremely critical to mixed-signal DUT performance. We have seen many cases throughout this chapter in which a short PCB trace is the ideal interconnection. Short traces have less parasitic resistance, inductance, and capacitance than long traces. The best way to achieve short PCB traces is to arrange the DIB components in a way that allows short traces, especially in critical nodes.

Component placement, power and ground schemes, trace layout, and other physical decisions must be made with knowledge of the DUT and DIB circuits and their required performance. This fact makes it very difficult for automatic routing software to lay out mixed-signal DIBs. In fact, it is very difficult to get a good DIB layout from a manual process, unless the test engineer sits with the PCB designer as the critical components and traces are placed on the DIB. This fact escapes many novice test engineers, who literally throw the DIB schematic into the PCB designer's lap and walk away, assuming all will turn out well.

## 15.10 SUMMARY

A good DIB is one of the most critical elements in a successful mixed-signal test solution. Without good DIB performance, the DUT may be unable to meet its specifications, regardless of the quality of the test code. Many things lead to good mixed-signal DIB design, including proper component selection and placement, proper power and ground layout, proper PCB stackup, and proper attention to parasitic components related to PCB traces and DIB components.

A good schematic design is essential as well as a good DIB layout. If the test engineer forgets to provide for an important connection between the tester and the DUT, then all the clever software routines in the world will not make the DIB usable. Also, if the test engineer does not provide for all the necessary hardware hooks to calibrate the DIB circuits, then it will be equally useless because it will not provide the necessary accuracy.

Often, the only way to produce a good DIB schematic is to have a complete test plan and data sheet to begin with. If the design specifications, DUT pinout, and test list are constantly changing, then it will be impossible to design a good DIB. Also, if the test engineer and design engineers do not work together closely, the DIB and DUT will often be incompatible with one another. It is critical for the test engineer to review his test plan and DIB design with the design engineers before the DIB is laid out and fabricated. Otherwise, the DIB may turn out to be an expensive but useless piece of test hardware, proving once again that concurrent engineering is critical to mixed-signal product development.

## PROBLEMS

**15.1.** Calculate the parasitic resistance of a 13-in. PCB trace having a width of 20 mils and a thickness of 1 mil. A pair of these traces are used as the high-force and low-force lines of a Kelvin-connected voltage regulator located on the DIB. The regulator feeds a 3.3-V DC signal to a 5-Ω load resistance. How much current will flow through the four Kelvin lines? What will be the differential voltage between the high-force and low-force output of the voltage regulator, measured at the regulator side of the PCB traces?

**15.2.** Using Eq. (15.3), calculate the parasitic inductance per unit length and total inductance of a 3-in. stripline trace having a width of 50 mils and a spacing of 8 mils to the current-return ground plane. If this trace feeds a 5-MHz, 625-mV RMS sinusoidal signal to a 100-Ω load resistance, what will be the error of the RMS voltage at the load as a percentage of the source voltage? (Assume zero trace resistance and zero signal source impedance.) Compare your answers with those obtained using the refined inductance estimate of Figure 15.10.

**15.3.** Using Eq. (15.10), calculate the parasitic capacitance per unit length and total capacitance of a 3-cm-long, 35-mil-wide stripline trace with a spacing of 10 mils to the ground plane, fabricated on a Teflon® PCB. Compare your answer with that obtained using the refined capacitance estimate of Figure 15.16.

**15.4.** The stripline trace in Problem 15.3 is connected to the 50-kΩ source impedance of a DUT output. What are the gain and phase shift of the DUT output signal as a function of frequency, compared to its unloaded output (i.e., if it were not connected to the trace)? (Use the estimate of capacitance from Figure 15.16.)

**15.5.** Using Eq. (15.13), calculate the parasitic capacitance per unit length and total capacitance between two 8-in.-long, 10-mil-wide coplanar traces separated by a spacing of 20 mils with a thickness of 1 mil, fabricated on an FR4 PCB. Compare your answer with that obtained using the refined capacitance estimate of Figure 15.18.

**15.6.** Using Eq. (15.10), calculate the parasitic capacitance of an 11.5-in.-long, 15-mil-wide stripline trace with a spacing of 12 mils to the ground plane, fabricated on an FR4 PCB.

This trace feeds a 300-kHz, 1-V RMS sinusoidal signal from a DUT output having a 75-kΩ output resistance to an unterminated coaxial cable (tester instrument input) having a distributed capacitance of 35 pF. How much will the distributed capacitance of the trace and coaxial cable capacitance attenuate the DUT signal? (Express your answer as a voltage gain in decibels.) Would a DIB buffer amplifier be required for this output? Compare your answer with that obtained using the refined capacitance estimate of Figure 15.16.

**15.7.** An 8-in. stripline trace is fabricated on an FR4 PCB with a width of 24 mils. It is separated from its ground plane by a spacing of 16 mils. Using the refined estimates of Figure 15.10 and Figure 15.16, calculate the stripline's parasitic capacitance per meter and inductance per meter. What is the stripline's characteristic impedance? If we want to lower the characteristic impedance, would we make the layer spacing from trace to ground larger or smaller? If we were constrained to a layer spacing of 16 mils, would we make the trace wider or smaller? If we increased the length of the trace to 16 in., what would happen to the characteristic impedance?

**15.8.** What is the velocity of a signal propagating along the stipline of Problem 15.7? Express your answer in meters per second and in a percentage of the speed of light. What is the stipline's propagation delay? What is its distributed capacitance?

**15.9.** What is the wavelength, in meters, of a 20-MHz sine wave traveling along the FR4 stripline in Problem 15.7? Can we treat the parasitic reactances of the stripline as lumped elements, or do we have to treat the stripline as a transmission line at this frequency?

**15.10.** A 1.200-GHz sinusoidal signal is transmitted from a DUT output to tester digitizer along a 20-cm 50-Ω terminated coaxial cable having a signal velocity of $0.8c$. What is the wavelength of the transmitted signal as a percentage of the cable length? What is the distributed capacitance of this coaxial cable? What is the phase shift, in degrees, between the DUT output and the digitizer input? (Your answer may exceed 360 degrees.)

**15.11.** A DUT output signal under test contains frequencies from DC to 44 kHz. The DUT output impedance is guaranteed to fall between 50 and 100 Ω (purely resistive). We wish to measure the signal using a digitizer having a distributed cable capacitance of 120 pF plus a lumped input capacitance of 5 pF. Can this signal node be measured directly, or will a buffer amplifier be needed on the DIB?

**15.12.** A DUT with a normalized output impedance $z_{DUT} = 0.2 + j3.2\ \Omega$ is to be matched with an LC network to 50 Ω at 1 GHz, where the matching network needs to be design in such a way that the device output will not be shorted to GND.

**15.13.** A DUT with a normalized output impedance $z_{DUT} = 0.7 + j3.2\ \Omega$ is to be matched with an series-C shunt-C network to 50 Ω at 3 GHz. What are the values of these two capacitors?

**15.14.** Calculate the length and position for the open stub line matching of 50Ω with a load of $45 + j75$ . What is the denomralized input admittance of the open-circuit stub line?

**15.15.** Calculate the length and position for the short-circuit stub line matching of 50Ω with a load of $65 + j150\ \Omega$. What is the normalized input admittance of the short-circuit stub line?

**15.16.** What is the self-resonance frequency of a 10-nF capacitor with a package size of 0603. Use the ESL data of Table 15.4.

**15.17.** What is the Q value of a 10-nF capacitor of the size 0603 if the ESR is per data sheet 0.15 Ω at 1 MHz?

**15.18.** The in-phase and quadrature outputs (IOUT and QOUT) of a cellular telephone DUT are produced by two supposedly identical amplifier circuits. According the the data sheet, the resistive output impedance of each amplifier circuit is specified at 75 Ω (min) to 125 Ω (max). We wish to measure the phase mismatch between these two outputs when a 70-kHz sine wave is driven from each output. Assuming a perfectly matched capacitive

load of 300 pF from each of two digitizers, what is the worst-case phase mismatch caused by the tester loading? How could we eliminate the tester-induced phase error problem?

**15.19.** The Kelvin PSRR ripple circuit illustrated in Figure 15.81 is constructed using the values $R_2 = 1$ kΩ and $R_1 = 4.7$ kΩ. The power supply is programmed to 5.0 V DC. Describe a signal, $v(t)$, at the input to $R_1$ that would produce a DUT power supply ripple of 100 mV peak-to-peak at 2.4 kHz. (Assume no errors due to circuit bandwidth, component mismatch, etc.)

**15.20.** Repeat Problem 15.13 using the PSRR buffer circuit illustrated in Figure 15.84. (Assume $V_{DD}$ is set to 5.0 V DC.)

**15.21.** Explain the dissipasion of a RF line and which lines are showing no dissipation.

## REFERENCES


**1.** J. D. Kraus and K. R. Carver, *Electromagnetics*, 2nd edition, McGraw-Hill, New York, 1973, ISBN 0070353964, p. 85.

**2.** H. W. Johnson and G. Martin, *High Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, Englewood Cliffs, NJ, April 1993, ISBN 0133957241.

**3.** B. Wadell, *Transmission Line Modelling Handbook (Artech House Microwave Library)*, Artech House, Boston, June 1991, ISBN 0890064369.

**4.** H. W. Ott, *Noise Reduction Techniques in Electronic Systems*, 2nd edition, John Wiley & Sons, New York, March 1998, ISBN 0471850683.

**5.** Y. Konishi, *Microwave Electronic Circuit Technology*, Marcel Dekker, New York, 1998.