CHAPTER 2

Tester Hardware

This chapter explores the architecture of a mixed-signal ATE tester. While we do not focus on any particular ATE from any specific vendor, our intent here is to give a general overview of the common instruments found in such testers. This will include a discussion on DC sources and meters, waveform digitizers, arbitrary waveform generators, an RF measurement subsystem, and digital pattern generators with sources and capture functionality. We shall encounter these instruments again from time to time throughout the remainder of this textbook.

2.1 MIXED-SIGNAL TESTER OVERVIEW

2.1.1 General-Purpose Testers Versus Focused Bench Equipment

General-purpose mixed-signal testers must be capable of testing a variety of dissimilar devices. On any given day, the same mixed-signal tester may be expected to test video palettes, cellular telephone devices, data transceivers, and general-purpose ADCs and DACs. The test requirements for these various devices are very different from one another. For example, the cellular telephone base-band interface shown in Figure 1.2 may require a phase trajectory error test or an error vector magnitude test. Dedicated bench instruments can be purchased that are specifically designed to measure these application-specific parameters. It would be possible to install one of these stand-alone boxes into the tester and communicate with it through an IEEE-488 GPIB bus. However, if every type of DUT required two or three specialized pieces of bolt-on hardware, the tester would soon resemble Frankenstein's monster and would be prohibitively expensive.

The mixed-signal production tester cannot be focused toward a specific type of device if it is to handle a variety of DUTs. Instead of implementing tests like phase trajectory error and error vector magnitude using a dedicated bench instrument, the tester must emulate this type of equipment using a few general-purpose instruments. The instruments are combined with software routines to simulate the operation of the dedicated bench instruments.

2.1.2 Generic Tester Architecture

Mixed-signal testers come in a variety of "flavors" from a variety of vendors. Unlike the ubiquitous PC, testers are not at all standardized in architecture. Each ATE vendor adds special features that they feel will give them a competitive advantage in the marketplace. Consequently, mixed-signal testers from different vendors do not use a common software platform. Furthermore, a test routine implemented on one type of tester is often difficult to translate to another tester type because of subtle differences in the hardware tradeoffs designed into each tester. Nevertheless, most mixed-signal testers share many common features. In this chapter, we will examine these common features without delving too deeply into specific details for any particular brand of tester.

2.2 DC RESOURCES

2.2.1 General-Purpose Multimeters

Most testers incorporate a high-accuracy multimeter that is capable of making fast DC measurements. A tester may also provide a slower, very high-accuracy voltmeter for more demanding measurements such as those needed in focused calibrations. However, this slower instrument may not be usable for production tests because of the longer measurement time. The fast, general-purpose multimeter is used for most of the production tests requiring a nominal level of accuracy.

Figure 2.1. Generic mixed-signal tester architecture.

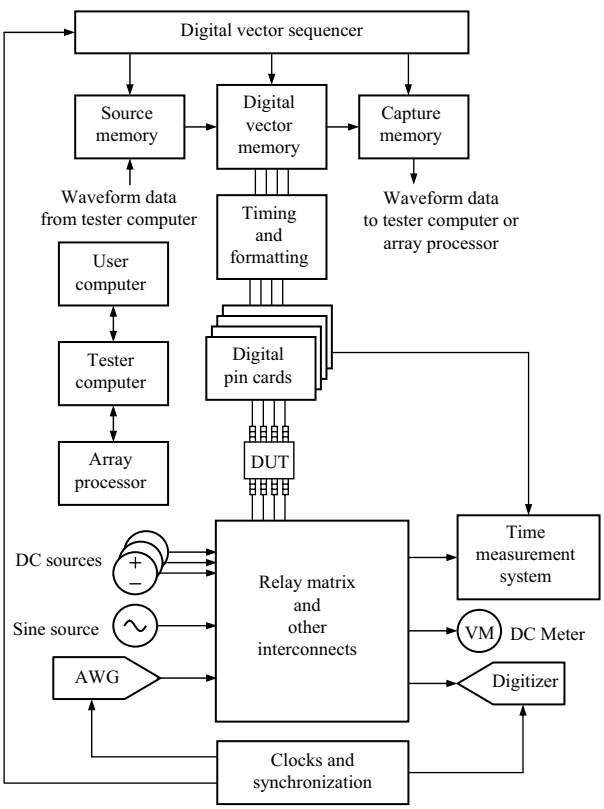


Figure 2.1 shows a generic mixed-signal tester architecture. It includes system computers, DC sources, DC meters, relay control lines, relay matrix lines, time measurement hardware, arbitrary waveform generators, waveform digitizers, clocking and synchronization sources, and a digital subsystem for generating and evaluating digital patterns and signals. This chapter will briefly examine the operation of each of these tester subsystems.

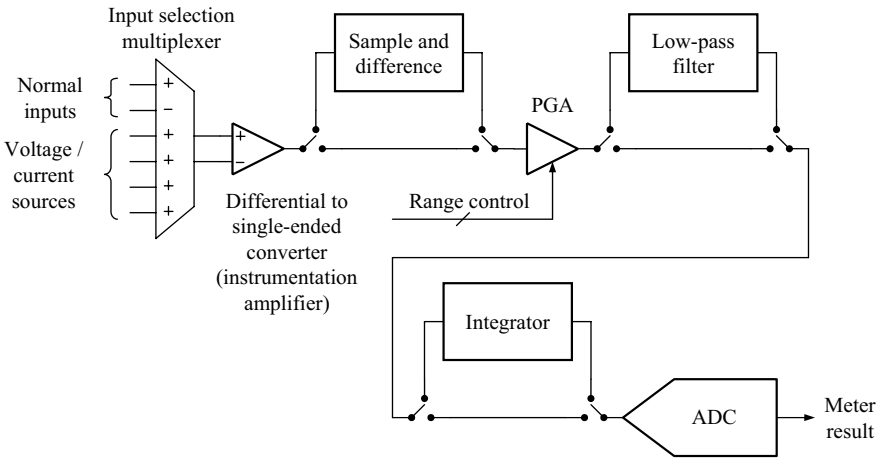
A detailed DC multimeter structure is shown in Figure 2.2. This meter can handle either single-ended or differential inputs. Its architecture includes a high-impedance differential to single-ended converter (instrumentation amplifier), a low-pass filter, a programmable gain amplifier (PGA) for input ranging, a high-linearity ADC, integration hardware, and a sample-and-difference stage. It also includes an input multiplexer stage to select one of several input signals for measurement.

The instrumentation amplifier provides a high-impedance differential input. The high impedance avoids potential DC offset errors caused by bias current leaking into the meter. For single-ended measurements, the low end of the meter may be connected to ground through relays in the input selection multiplexer. The multimeter can also be connected to any of the tester's general-purpose DC voltage sources to measure their output voltage. The meter can also measure current flowing from any of the DC sources. This capability is very useful for measuring power supply currents, impedances, leakage currents, and other common DC parametric values. A PGA placed before the meter's ADC allows proper ranging of the instrument to minimize the effects of the ADC's quantization error (see Section 5.2.4 and Section 5.5).

The meter may also include a low-pass filter in its input path. The low-pass filter removes high-frequency noise from the signal under test, improving the repeatability of DC measurements. This filter can be enabled or bypassed using software commands. It may also have a programmable cutoff frequency so that the test engineer can make tradeoffs between measurement repeatability and test time (see Section 5.6). In addition, some meters may include an integration stage, which acts as a form of hardware averaging circuit to improve measurement repeatability.

Finally, a sample-and-difference stage is included in the front end of many ATE multimeters. The sample-and-difference stage allows highly accurate measurements of small differences between two large DC voltages. During the first phase of the measurement, a hardware sample-and-hold circuit samples a voltage. This first reference voltage is then subtracted from a second voltage (near the first voltage) using an amplifier-based subtractor. The difference between the

Figure 2.2. General-purpose DC multimeter.



EXAMPLE 2.1

A single-ended DC voltmeter has a resolution of 12 bits. It also features a sample-and-difference front-end circuit. We wish to use this meter to measure the differential offset voltage of a DUT's output buffer. Each of the two outputs is specified to be within a range of 1.35 V ± 10 mV, and the differential offset is specified to be ±5 mV. The meter input can be set to any of the following ranges: ±10 V, ±1 V, ±100 mV, ±10 mV, and ±1 mV. Assuming that all components in the meter are perfectly linear (with the exception of the meter's quantization error), compare the accuracy achieved using two simple DC measurements with the accuracy achieved using the sample-and-difference circuit.

Solution:

The simplest way to measure offset using a single-ended DC voltmeter is to connect the meter to the OUTP output, measure its voltage, connect the meter to the OUTN output, measure its voltage, and subtract the second voltage from the first. Using this approach, we have to set the meter's input range to ±10 V to accommodate the 1.35 V DUT output signals. Thus each measurement may have a quantization error of as much as ± ½ (20 V/2^{12}–1) = ± 2.44 mV. Therefore the total error might be as high as ±4.88 mV, assuming that the quantization error from the first measurement is positive, while the quantization error from the second measurement is negative. Since the specification limit is ±5 mV, this will be an unacceptable test method.

Using the sample-and-difference circuitry, we could range the meter input to the worst-case difference between the two outputs, which is 5 mV, assuming a good device. The lowest meter range that will accommodate a 5-mV signal is ±10 mV. However, we also need to be able to collect readings from bad devices for purposes of characterization. Therefore, we will choose a range of ±100 mV, giving us a compromise between accuracy and characterization flexibility.

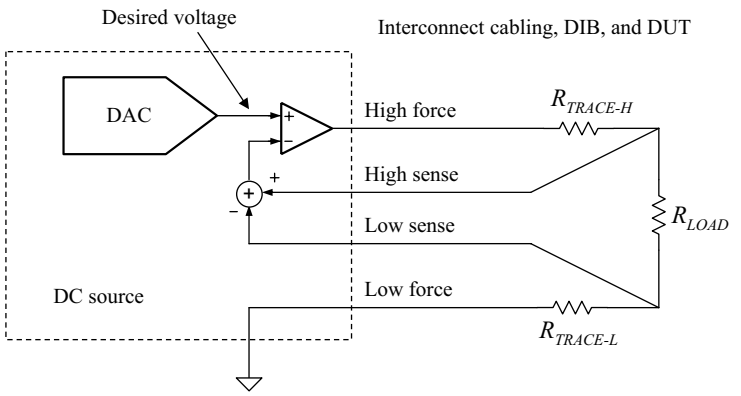
During the first phase of the sample-and-difference measurement, the voltage at the OUTN pin is sampled onto a holding capacitor internal to the meter. Then the meter is connected to the OUTP pin and the second phase of the measurement amplifies the difference between the OUTP voltage and the sampled OUTN voltage. Since the meter is set to a range of ±100 mV, a 100-mV difference between OUTP and OUTN will produce a full-scale 10-V input to the meter's ADC. This serves to reduce the effects of the meter's quantization error. The maximum error is given by ± ½ (100 mV/2^{12}–1) = ± 12.2 µV. Again, the worst-case error is twice this amount, or ±24.4 µV, which is well within the requirements of our measurement.

two voltages is then amplified and measured by the meter's ADC, resulting in a high-resolution measurement of the difference voltage. This process reduces the quantization error that would otherwise result from a direct measurement of the large voltages using the meter's higher voltage ranges.

2.2.2 General-Purpose Voltage/Current Sources

Most testers include general-purpose DC voltage/current sources, commonly referred to as *V/I sources* or *DC sources*. These programmable power supplies are used to provide the DC voltages and currents necessary to power up the DUT and stimulate its DC inputs. Many general-purpose

Figure 2.3. General-purpose DC source with Kelvin connections (conceptual diagram).



supplies can force either voltage or current, depending on the testing requirements. On most testers, these supplies can be switched to multiple points on the DIB board using the tester's DC matrix (see Subsection 2.2.5). As mentioned in the previous section, the system's general-purpose meter can be connected to any DC source to measure its output voltage or its output current.

Figure 2.3 shows a conceptual block diagram of a DC source having a differential Kelvin connection. A differential Kelvin connection consists of four lines (high force, low force, high sense, and low sense) for forcing highly accurate DC voltages. The Kelvin connection forms a feedback loop that allows the DC source to force an accurate differential voltage through the resistive wires between the source and DUT. Without the Kelvin connection, the small resistance in the force line interconnections ($R_{TRACE-H}$ and $R_{TRACE-L}$) would cause a small *IR* voltage drop. The voltage drop would be proportional to the current through the DUT load (R_{LOAD}). The small *IR* voltage drop would result in errors in the voltage across the DUT load. The sense lines of a Kelvin connection carry no current. Therefore, they are immune to errors caused by *IR* voltage drops.

A sense line is provided on the high side of the DC source and also on the low side of the source. The low-side sense line counteracts the parasitic resistance in the current return path. Since most instruments are referenced to ground, the low sense lines for all the DC instruments in a tester are often lumped into a single ground sense signal called DZ (device zero), DGS (device ground sense), or some other vendor-specific nomenclature. This is one of the most important signals in a mixed-signal tester, since it connects the DUT's ground voltage back to the tester's instruments for use as the entire test system's 0-V "golden zero reference." If any voltage errors are introduced into this ground reference signal relative to the DUT's ground, all the instruments will produce DC voltage offsets.

2.2.3 Precision Voltage References and User Supplies

Mixed-signal testers sometimes include high-accuracy, low-noise voltage references. These voltage sources can be used in place of the general-purpose DC sources when the noise and accuracy characteristics of the standard DC source are inadequate. One common example of a precision voltage reference application is the voltage reference for a high-resolution ADC or DAC. Any noise and DC error on the DC reference of an ADC or DAC translates directly into gain error and increased noise, respectively, in the output of the converter. A precision voltage reference is sometimes used to solve this problem.

Testers may also include nonprogrammable user power supplies with high output current capability. These fixed supplies provide common power supply voltages (±5 V, ±15 V, etc.) for

DIB circuits such as op amps and relay coils. This allows DIB circuits to operate from inexpensive fixed power supplies having high current capability instead of tying up the tester's more expensive programmable DC sources.

2.2.4 Calibration Source

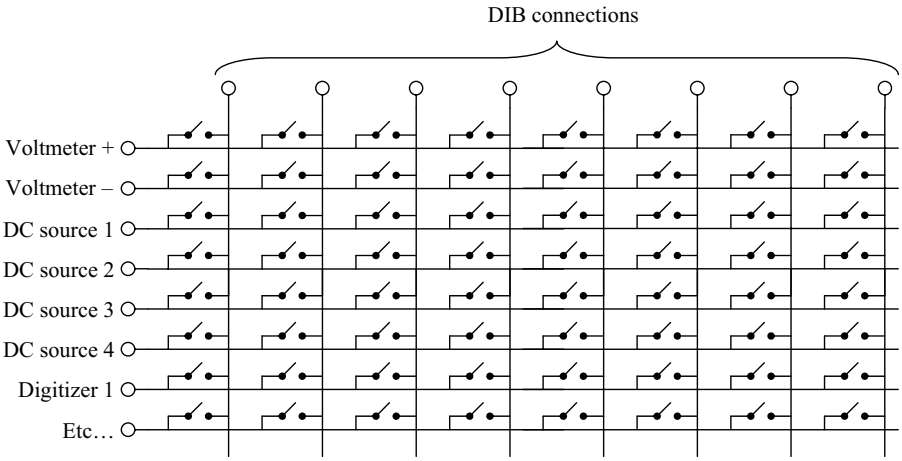
The mixed-signal tester's calibration source is discussed in detail in Section 5.4. The purpose of a calibration source is to provide traceability of standards back to a central agency such as the National Institute of Standards and Technology (NIST). The calibration source must be recalibrated on a periodic basis (six months is a common period). Often, the source is removed from the tester and sent to a certified standards lab for recalibration. The old calibration source is replaced by a freshly calibrated one so that the tester can continue to be used in production. On some testers, the high-accuracy multimeter serves as the calibration source. Also, some testers may have multiple instruments that serve as the calibration sources for various parameters such as voltage or frequency. Clearly, this is a highly tester-specific topic. Calibration and standards traceability is discussed in more detail in Chapter 5, "Yield, Measurement Accuracy, and Test Time."

2.2.5 Relay Matrices

A relay matrix is a bank of electromechanical relays that provides flexible interconnections between many different tester instruments and the DUT. There may be several types of relay matrix in a tester, but they all perform a similar task. At different points in a test program, a particular DUT input may require a DC voltage, an AC waveform, or a connection to a voltmeter. A relay matrix allows each instrument to be connected to a DUT pin at the appropriate time as illustrated in Figure 2.4. General-purpose relay matrices, on the other hand, are used to connect and disconnect various circuit nodes on the DIB board. They have no hardwired connections to tester instruments. Therefore, the purpose and functionality of a general-purpose relay matrix depends on the test engineer's DIB design. It allows flexible interconnections between specific tester instruments and pins of the DUT through connections on the DIB board.

In addition to relay matrices, many other relays and signal paths are distributed throughout a mixed-signal tester to allow flexibility in interconnections without adding unnecessary relays to

Figure 2.4. Instrument relay matrix.



the DIB board. The exact architecture of relays, matrices, and signal paths varies widely from one ATE vendor's tester to the next.

2.2.6 Relay Control Lines

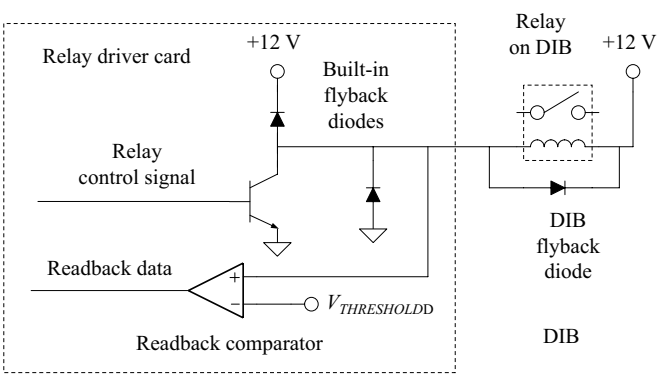
Despite the high degree of interconnection flexibility provided by the general-purpose relay matrix and other instrument interconnect hardware, there are always cases where a local DIB relay (placed near the DUT) is imperative. Usually the need for a local DIB relay is driven by performance of the DUT. For example, there is no better way to get a low-noise ground signal to the input of a DUT than to provide a local relay placed on the DIB directly between the DUT input and the DUT's local ground plane.

Certainly it is possible to feed the local ground through a DIB trace, through a remote relay matrix, and back through another DIB trace, but this connection scheme invariably leads to poor analog performance. The DIB traces are, after all, radio antennae. Many noise problems can be traced to poor layout of ground connections between the DUT and its ground plane. Local DIB relays minimize the radio antenna effect. Local DIB relays are also used to connect device outputs to various passive loads and other DIB circuits.

The test program controls the local DIB relays, opening and closing them at the appropriate time during each test. The relay coils are driven by the tester's relay control lines. A relay control line driver is shown in Figure 2.5. On some testers, the control line is capable of reading back the state of the voltage on the control line through a readback comparator. The readback comparator allows a low-cost method for determining the state of a digital signal.

Relay coils produce an inductive kickback when the current is suddenly changed between the on and off states. The inductive kickback, or flyback as it is known, is induced according to the inductance formula $v(t) = L\ di/dt$. Since high kickback voltages could potentially damage the output circuits of the relay driver, its output circuits contain flyback protection diodes to shunt the excess voltage to a DC source or to ground. Many test engineers also add flyback diodes across the coils of the relay, as shown in Figure 2.5. The extra diode is probably redundant. However, many engineers consider it good practice to add extra flyback diodes even though they ate up quite a bit of DIB board space. To eliminate the board space issue, the test engineer can choose slightly more expensive relays with built-in flyback diodes.

Figure 2.5. Relay coil driver with flyback protection diodes.



2.3 DIGITAL SUBSYSTEM

2.3.1 Digital Vectors

A mixed-signal tester must test digital circuits as well as mixed-signal and analog circuits. The mixed-signal and digital-only sections of the DUT are exercised using the tester's digital subsystem. The digital subsystem can present high, low, and high-impedance (HIZ) logic levels to the DUT. It can also compare the outputs from the DUT against expected responses to determine whether the digital logic of the DUT has been manufactured without defects. The tester applies a sequence of drive data to the device and simultaneously compares outputs against expected results. Each drive/compare cycle is called a *digital vector*. A series of digital vectors is called a *digital pattern*. Vectors of a digital pattern are usually sourced at a constant frequency, although some testers allow the period of each vector to be set independently. The ability to change digital timing on a vector-by-vector basis is commonly called *timing on the fly*.

2.3.2 Digital Signals

In addition to the simple pass/fail digital pattern tests, the tester must also be capable of sourcing and capturing digital signals. Digital signals are digitized representations of continuous waveforms such as sine waves and multitones. Digital signals are distinct from digital vectors in that they typically carry analog signal information rather than purely digital information. Usually, the samples of a digital signal must be applied to a DUT along with a repetitive digital pattern that keeps the device active and initiates DAC and/or ADC conversions. Each cycle of the repeating digital pattern is called a *frame*.

During a mixed-signal test, the repeating frame vectors must be combined with the nonrepeating digital signal sample information to form a repetitive sampling loop. Combining the digital frame vectors with digital signal data, a long sequence of waveform samples can be sent to or captured from the DUT with a very short digital frame pattern. In effect, the sampling frame results in a type of data compression that minimizes the amount of vector memory needed for the tester's digital subsystem.

Looping frames are commonly used when testing DACs and ADCs. A sequence of samples must be loaded into a DAC to produce a continuous sequence of voltages at the DAC's output. In the case of ADC testing, digital signals must be captured and stored into a bank of memory as the looping frame initiates each ADC conversion.

2.3.3 Source Memory

When testing DACs, the digital signal samples representing the desired DAC analog waveform are typically computed in the tester's main test program code. The digital signal samples are stored into a digital subsystem memory block called *source memory* (or *send memory* in some testers). The digital frame data, on the other hand, are stored in vector memory. To generate a repeating frame with a new sample for each loop, the contents of the vector memory and source memory are spliced together in real time as the digital pattern is executed.

A digital signal can be modified quickly without changing the frame loop pattern because its data are generated algorithmically by the main test program. The ability to quickly modify the digital signal data is especially useful during the DUT debug and characterization phase. For example, a DAC may normally be tested using a 1-kHz sine wave digital signal. During the DAC characterization phase, however, the frequency might be swept from 100 Hz to 10 kHz to look for problem areas in the DAC's design. This would be impossibly cumbersome if the digital pattern had to be generated using an expanded, nonlooping sequence of ones and zeros. In fact, some tester architectures attempt to substitute deep, nonlooping vector memory in place of source memory.

This may reduce the cost of tester hardware, but it invariably results in frustrated users. One of the main differences between a mixed-signal tester and a digital tester with bolt-on analog instruments is the presence of source and capture memories in the digital subsystem. Other differences will be pointed out throughout this chapter.

2.3.4 Capture Memory

Devices such as ADCs produce a series of digitized waveform samples that must be captured and stored into a bank of memory called *capture memory* (or *receive memory*). Capture memory serves the opposite function of source memory. Each time the sampling frame is repeated, the digital output from the device is stored into the capture memory. The capture memory address pointer is incremented each time a digital sample is captured. Once a complete set of samples have been collected, they are transferred to an array processor or to the tester computer for analysis.

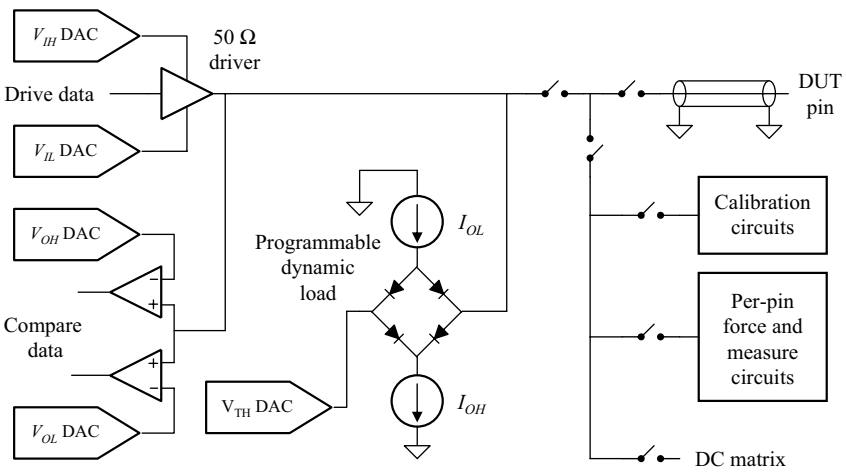
2.3.5 Pin Card Electronics

The pin card electronics for each digital channel are located inside the test head on most mixed-signal testers. A pin card electronics board may actually contain multiple channels of identical circuitry. Each channel's circuits consist of a programmable driver, a programmable comparator, various relays, dynamic current load circuits, and other circuits necessary to drive and receive signals to and from the DUT. A generic digital pin card is shown in Figure 2.6.

The driver circuitry consists of a fixed impedance driver (typically 50 Ω) with two programmable logic levels, V_{IH} and V_{IL}. These levels are controlled by a pair of driver-level DACs whose voltages are controlled by the test program. The driver can also switch into a high-impedance state (HIZ) at any point in the digital pattern to allow data to come from the DUT into the pin card's comparator. The driver circuits may also include programmable rise and fall times, though fixed rise and fall times are more common. Normally the fixed rise and fall times are designed to be as fast as the ATE vendor can make them. Rise and fall times between 1 ns and 3 ns are typical in today's testers.

The comparator also has two programmable logic levels, V_{OH} and V_{OL}. These are also controlled by another pair of DACs whose voltages are controlled by the test program. The pin card

Figure 2.6. Digital pin card circuits.



comparator is actually a pair of comparators, one for the V_{OH} level and one for V_{OL}. If the DUT signal is below V_{OL}, then the signal is considered a logic low. If the DUT is above V_{OH}, then it is considered a logic high. If the DUT output is between these thresholds, then the output state is considered a midpoint voltage. If it is outside these thresholds, then it is considered a valid logic level. Comparator results can also be ignored using a mask. Thus there are typically three drive states (HI, LO, and HIZ) and five compare states (HI, LO, and MID, VALID, and MASK).

The usefulness of the valid comparison is not immediately obvious. If we want to test for valid V_{OH} and V_{OL} voltages from the output of a nondeterministic circuit such as an ADC, we cannot set the tester to expect HI or LO. This is because electrical noise in the ADC and tester will produce somewhat unpredictable results at the ADC output. However, we can set the tester to expect valid logic levels during the appropriate digital vectors without specifying whether the ADC should produce a HI or a LO. While the pin card tests for valid logic levels, the samples from the ADC are collected into the digital capture memory for later analysis.

In addition to the drive and compare circuits, digital pin cards may also include dynamic load circuits. A dynamic load is a pair of current sources connected to the DUT output with a diode bridge circuit as shown in Figure 2.6. The diode bridge forces a programmable current into the DUT output whenever its voltage is below a programmable threshold voltage, V_{TH}. It forces current out of the DUT output whenever its voltage is above V_{TH}. The sink and source current settings correspond to the DUT's I_{OH} and I_{OL} specifications (see Section 3.12.4).

Another extremely important function that a digital pin card provides is its per-pin measurement capability. The per-pin measurement circuits of a pin card form a low-resolution, low-current DC voltage/current source for each digital pin. The per-pin circuits also include a relatively low-resolution voltage/current meter. The low-resolution and low-current capabilities are usually adequate for performing certain DC tests like continuity and leakage testing. These DC source and measure circuits can also be used for other types of simple DC tasks like input or output impedance testing.

Some testers may also include overshoot suppression circuits that serve to dampen the overshoot and undershoot characteristics in rapidly rising or falling digital signals. The overshoot and undershoot characteristics are the result of a low-impedance DUT output driving into the DIB traces and coaxial cables leading to the digital pin card electronics. The ringing is minimized as the signal overshoot is shunted to a DC level through a diode.

Digital pin cards also include relays connected to other tester resources such as calibration standards and system DC meters and sources. These connections can be used for a variety of purposes, including calibration of the pin card electronics during the tester's system calibration process. The exact details of these connections vary widely from one tester type to another.

2.3.6 Timing and Formatting Electronics

When looking at a digital pattern for the first time, it is easy to interpret the ones and zeros very literally, as if they represent all the information needed to create the digital waveforms. However, most ATE testers apply timing and formatting to the ones and zeros to create more complicated digital waveforms while minimizing the number of ones and zeros that must be stored in pattern memory.

Timing and formatting is a type of data compression and decompression. The pattern data are formatted using the ATE tester's formatter hardware, which is typically located inside the tester mainframe or on the pin card electronics in the test head. Figure 2.7 shows how the pattern data are combined with timing and formatting information to create more complex waveforms. Notice that the unformatted data in Figure 2.7 require four times as much 1/0 information and four times the bit cell frequency to achieve the same digital waveform as the formatted data. Another key advantage to formatted waveforms is that the formatting hardware in a high-end mixed-signal tester is

Figure 2.7. Drive data compression using formats and timing.

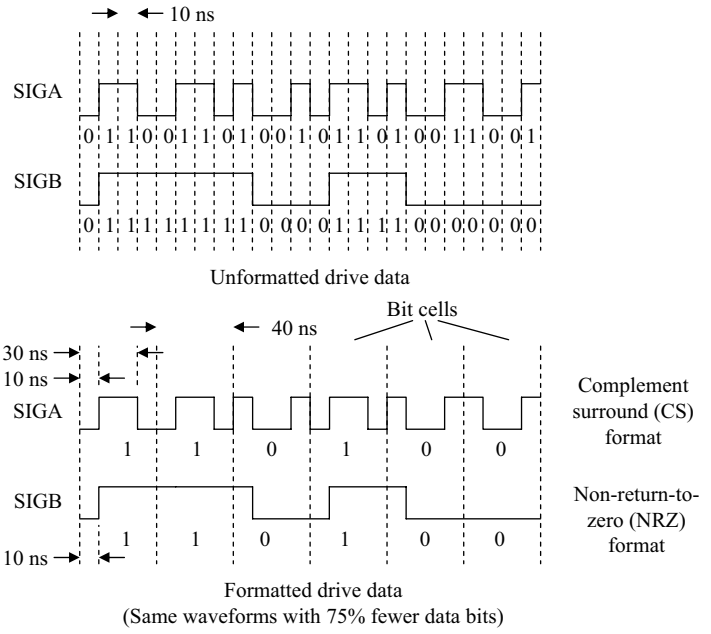
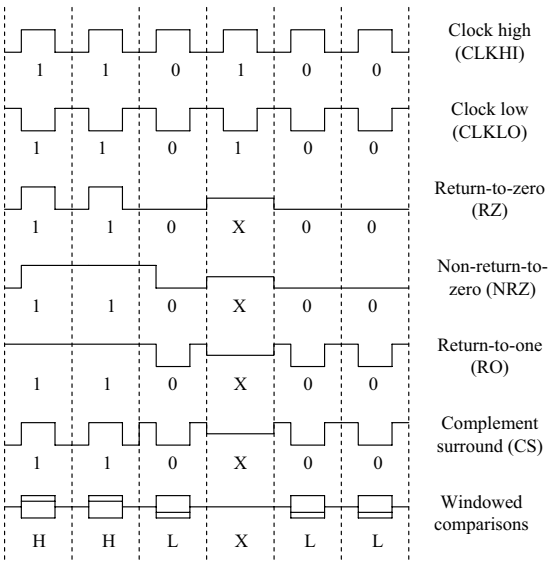


Figure 2.8. Some common digital formats.



capable of placing the rising and falling edges with an accuracy of a few tens of picoseconds. This gives us better control of edge timing than we could expect to achieve using subgigahertz clocked digital logic.

The programmable drive start and stop times illustrated in Figure 2.7 are generated using digital delay circuitry inside the formatter circuits of the tester. Drive and compare timing is

refined during a calibration process called *deskewing*. This allows subnanosecond accuracy in the placement of driven edges and in the placement of compare times (called *strobes* and *windows*). Strobe comparisons are performed at a particular point in time, while window comparisons are performed throughout a period of time. Window timing is typically used when comparing DUT outputs against expected patterns, while strobe timing is typically used when collecting data into capture memory. Again, this depends on the specific tester.

Figure 2.8 shows examples of several different formatting and timing combinations that create many different waveforms from the same digital data stream. In each case, the drive data sequence is 110X00. The compare data sequence is HHLXLL. Notice that certain formats such as Clock High and Clock Low ignore the pattern data altogether. Since digital pin cards can both drive and expect data, a distinction is made between a driven signal (1 or 0) and an expected signal (H or L). This notation is used for clarity in this book, though it is not universally used in the test industry. In fact, some digital pattern standards define H/L as driven data and 1/0 as expected data.

EXAMPLE 2.2

Two digital signals, SIGA and SIGB, are generated by an ATE tester's pattern generator. The pattern generator's vector rate (i.e., its bit cell rate) is set to 4 MHz. SIGA is programmed to RO format, while SIGB is programmed to NRZ format. The start time for SIGA is programmed to 50 ns and the stop time is programmed to 125 ns. Its initial state is programmed to logic high. The start time for SIGB is programmed to 25 ns and the stop time is programmed to 175 ns. Its initial state is programmed to logic low.

The following digital pattern is executed:

SIGA	SIGB
0	1
0	0
1	1
0	1
1	0
1	1

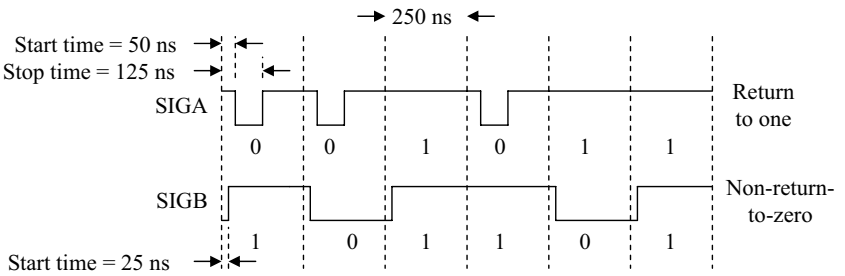
Draw a timing diagram for the two signals SIGA and SIGB produced by this pattern. Show the bit cells in the timing diagram and calculate their period. Assume that we want to produce this same pair of signals using a bank of static random access memory (SRAM) whose address is incremented at a fixed rate (i.e., nonformatted ones and zeros). What SRAM depth would be required to produce this same pair of signals?

Solution:

Figure 2.9 shows the digital waveforms resulting from the specified pattern and timing set. The vector rate is specified to be 4 MHz, so the bit cell period is 250 ns. Also notice that the NRZ format does not have a stop time, so the 175-ns stop time setting is irrelevant. In this example, all

timing edges fall on 25-ns boundaries. If we wanted to generate this same pattern using nonformatted data from a bank of SRAM clocked at a fixed frequency, we would have to source a sequence of 6 × (250 ns / 25 ns) = 60 bits from SRAM memory at a digital vector rate of 1/(25 ns) = 40 MHz.

Figure 2.9. Formatted data using return-to-one and non-return-to-zero formats.



2.4 AC SOURCE AND MEASUREMENT

2.4.1 AC Continuous-Wave Source and AC Meter

The simplest way to apply and measure single-tone AC waveforms is to use a continuous-wave source (CWS) and an RMS voltmeter. The CWS is simply set to the desired frequency and voltage amplitude to stimulate the DUT. The RMS voltmeter is equally simple to use. It is connected to the DUT output, and the RMS output is measured with a single test program command.

But the CWS and RMS voltmeter suffer from a few problems. First, they are only able to measure a single frequency during each measurement. This would be acceptable for bench characterization, but in production testing it would lead to unacceptably long test times. As we will see in Chapters 8 through 11, DSP-based multitone testing is a far more efficient way to test AC performance because multiple frequencies can be tested simultaneously.

Another problem that the RMS voltmeter introduces is that it cannot distinguish the DUT's signal from distortion and noise. Using DSP-based testing, these various signal components can easily be separated from one another. This ability makes DSP-based testing more accurate and reliable than simple RMS-based testing. DSP-based testing is made possible with a more advanced stimulus/measurement pair, the arbitrary waveform generator and the waveform digitizer.

2.4.2 Arbitrary Waveform Generators

An arbitrary waveform generator (AWG) consists of a bank of waveform memory, a DAC that converts the waveform data into stepped analog voltages, and a programmable low-pass filter section, which smoothes the stepped signal into a continuous waveform. An AWG usually includes an output scaling circuit (PGA) to adjust the signal level. It may also include differential outputs and DC offset circuits. Figure 2.10 shows a typical AWG and waveforms that might be seen at each stage in its signal path. (Mathematical signal samples are represented as dots to distinguish them from reconstructed voltages.)

An AWG is capable of creating signals with frequency components below the low-pass filter's cutoff frequency. The frequency components must also be less than one-half the AWG's sampling rate. This so-called Nyquist criterion will be explained in Chapter 8, "Sampling Theory."

Figure 2.10. Arbitrary waveform generator.

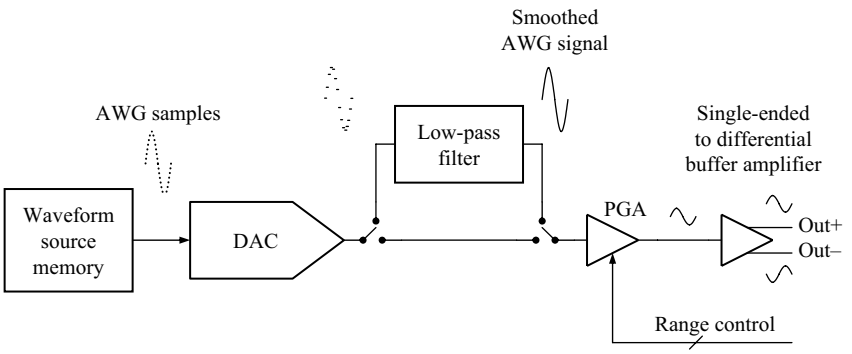
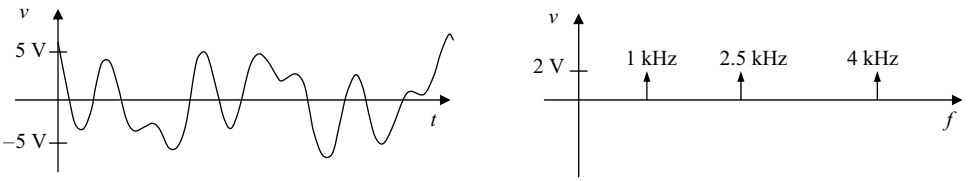


Figure 2.11. Time-domain and frequency-domain views of a three-tone multitone.



An AWG might create the three-tone multitone illustrated in Figure 2.11. It might also be used to source a sine wave for distortion testing or a triangle wave (up ramp/down ramp) for ADC linearity testing (see Chapter 7, "ADC Testing"). Flexibility in signal creation is the main advantage of AWGs compared to simple sine wave or function generators.

2.4.3 Waveform Digitizers

An AWG converts digital samples from a waveform memory into continuous-time waveforms. A digitizer performs the opposite operation, converting continuous-time analog waveforms into digitized representations. The digitized samples of the continuous waveform are collected into a waveform capture memory. The structure of a typical digitizer is shown in Figure 2.12. A digitizer usually includes a programmable low-pass filter to limit the bandwidth of the incoming signal. The purpose of the bandwidth limitation is to reduce noise and prevent signal aliasing, which we will discuss in Chapter 8, "Sampling Theory."

Like the DC meter, the digitizer has a programmable gain stage at its input to adjust the signal level entering the digitizer's ADC stage. This minimizes the noise effects of quantization error from the digitizer's ADC. Waveform digitizers may also include a differential to single-ended conversion stage for measuring differential outputs from the DUT. Digitizers may also include a sample-and-hold circuit at the front end of the ADC to allow undersampled measurements of very high-frequency signals. Undersampling is explained in more detail in Chapter 11, "Sampled Channel Testing."

2.4.4 Clocking and Synchronization

Many of the subsections and instruments in a mixed-signal tester derive their timing from a central frequency reference. This frequency determines the repetition rate of the sample loop and

Figure 2.12. Waveform digitizer.

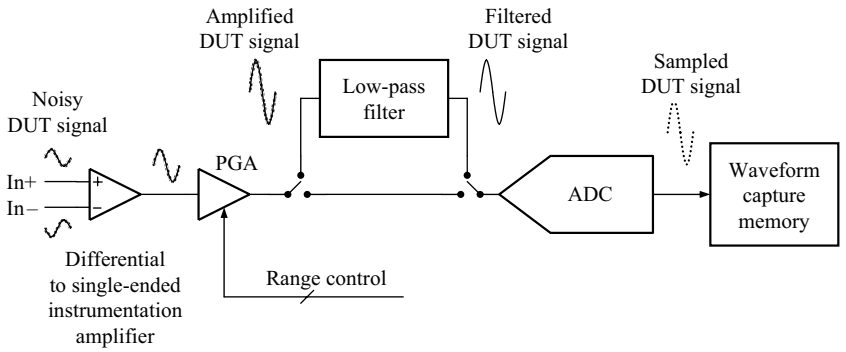
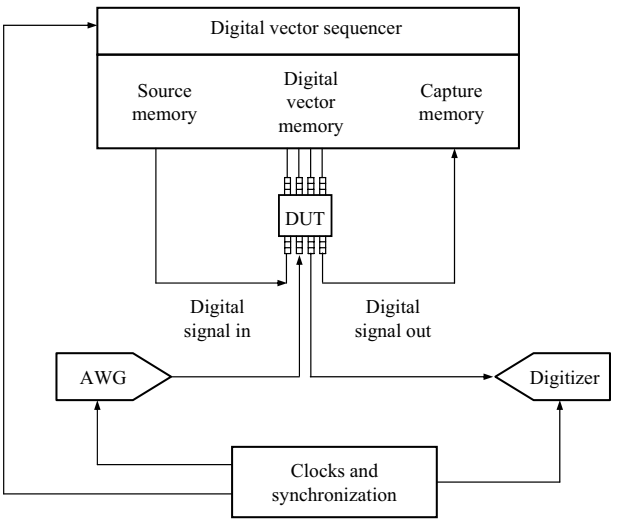


Figure 2.13. Synchronization in a mixed-signal tester.



therefore sets the frequency of the DAC or ADC sampling rates. The AWG and digitizer also operate from clock sources that must be synchronized to each other and to the digital pattern's frame loop repetition rate.

Figure 2.13 shows a clock distribution scheme that allows synchronized sampling rates between all the DSP-based measurement instruments. Since the clocking frequency for each instrument is derived from a common source, frequency synchronization is possible. Without precise sampling rate synchronization, the accuracy and repeatability of all the DSP-based measurements in a mixed-signal test program would be degraded.

The reason these clocks must all be synchronized will become more apparent in Chapter 8, "Sampling Theory," and Chapter 9, "DSP-Based Testing." Proper synchronization of sample rates between the various AWGs, digitizers, and digital pattern generators is another of the key distinguishing features of a mixed-signal tester. A digital tester with bolt-on analog instruments often lacks a good clocking and synchronization architecture.

2.5 TIME MEASUREMENT SYSTEM

2.5.1 Time Measurements

Digital and mixed-signal devices often require a variety of time measurements, such as frequency, period, duty cycle, rise and fall times, jitter, skew, and propagation delay. These parameters can be measured using the ATE tester's time measurement system (TMS). Most TMS instruments are capable of measuring these parameters within an accuracy of a few nanoseconds. Some of the more advanced TMS instruments can measure parameters such as jitter to a resolution of less than 1 ps.

Timing parameters that do not change from cycle to cycle (i.e., rise time, fall time, etc.) can sometimes be measured using a very high-bandwidth undersampling waveform digitizer. An undersampling digitizer is similar in nature to the averaging mode of a digitizing oscilloscope. Like digitizing oscilloscopes, undersampling digitizers require a stable, repeating waveform. Thus nonperiodic features such as jitter and random glitches cannot be measured using an undersampling approach. Unfortunately, undersampling digitizers are often considerably slower than dedicated time measurement instruments.

2.5.2 Time Measurement Interconnects

One of the most important questions to consider about a TMS instrument is how its input and interconnection paths affect the shape of the waveform to be measured. It does little good to measure a rise time of 1 ns if the shape of the signal's rising edge has been distorted by a 50-Ω coaxial connection. It is equally futile to try to measure a 100-ps rising edge if the bandwidth of the TMS input is only 300 MHz. Accurate timing measurements require a high-quality signal path between the DUT output and the TMS time measurement circuits.

2.6 RF SUBSYSTEM

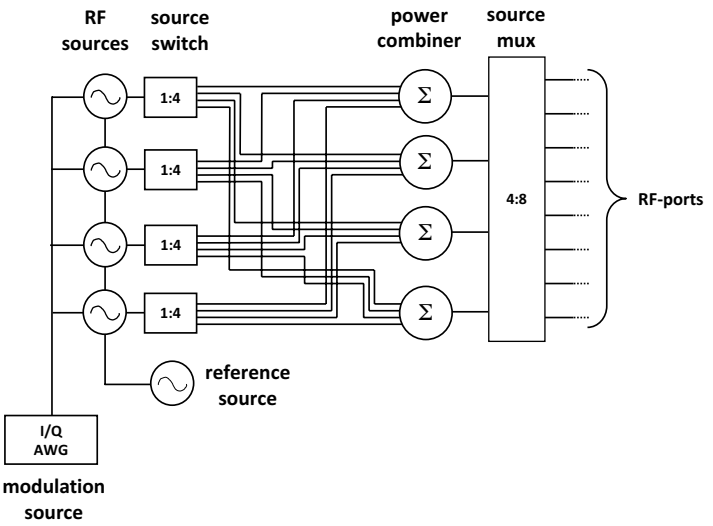
Testing RF parameters in production requires an ATE equipped with an RF subsystem. The architecture of the RF subsystem will not only have an impact on the measurements of performance and capabilities, but also has a significant impact on the test cost. A poor implementation might limit the test execution to a single site, whereas a more advanced one will enable octal site testing without necessarily increasing the ATE cost. For an easier understanding, we describe the source and measurement path of a typical RF subsystem below. The interface to the source and measurement path is connected with an RF switch to special RF ports on the test head.

2.6.1 Source Path

Figure 2.14 shows an implementation of the source path of a typical RF subsystem. In this implementation, four RF sources can be switched by a source switch matrix to power a combiner. This is followed by a source multiplexer connecting the RF ports on the test head. This system will be able to combine signals from four separate sources and present it to a single RF port to supply a device with a four-tone signal or supply a single-tone RF signal to four RF ports. The disadvantage of this architecture is that a number of expensive RF sources are required; in addition, the given architecture is limited to testing four devices at a time.

It is essential for all tests that the RF sources are synchronized in frequency. This is typically achieved by using a single source in the ATE as a reference as shown in Figure 2.14. This reference is used for all sources rather than operate from separate independent build-in reference oscillators.

Figure 2.14. Source path of an RF subsystem.



An important option is to have a modulation capability associated with the RF sources. This can be achieved as shown in Figure 2.14 with an AWG, or by a build-in AWG associated with the RF sources. Often the AWG of the mixed signal instrumentation can be routed to the modulation inputs of the RF sources.

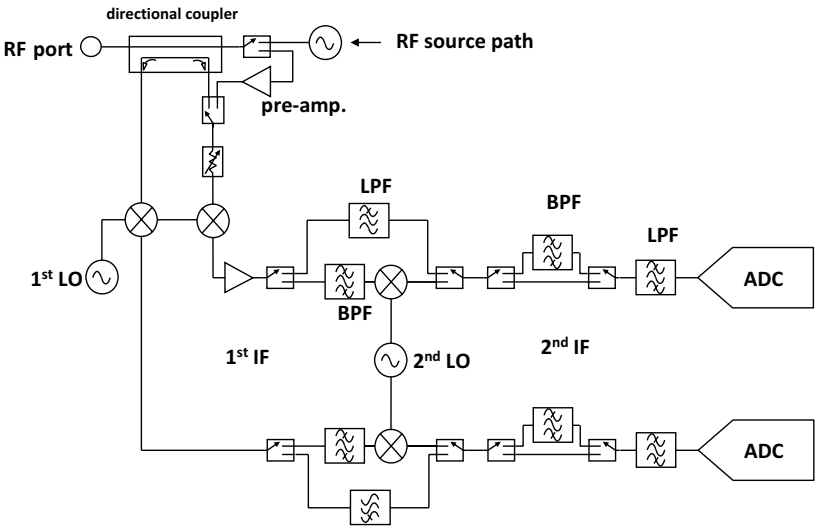
RF ATE vendors reduce the cost of their systems by replacing multiple RF sources as shown in Figure 2.14 by a single source, or two sources when a two-tone capability is required. The power level of each RF port can be controlled individually through a gain stage in series with each RF port. For this architecture, the frequency on all RF ports will be the same, which in most cases is not a significant disadvantage. The main advantage of this architecture is that additional RF ports can be realized with only minor additional cost associated with each gain stage. Octal site RF ATE systems can be easily built without adding the high cost of additional RF sources.

2.6.2 Measurement Path

The measurement path of an RF subsystem can be built as simple as a zero-IF system (ZIF) with a mixer mixing the RF DUT signal to a base-band frequency. The mixed signal digitizer of the ATE can then capture this base-band frequency signal. A more advanced architecture is shown in Figure 2.15. The RF signal of the RF port is directed to a directional coupler. This directional coupler enables the measurement of the *S*-parameter of the DUT. In the architecture shown in Figure 2.15, two ADCs are connected to each port of the directional coupler so that all the *S*-parameters of a DUT can be obtained during a single measurement. The two IF stages, including the low-pass/bandpass filter cascades, maintains the signal integrity of the signal captured by the ADC by limiting the measuring bandwidth. As well, this architecture enables the signal level to be adjusted through the enabling of either a gain or attenuator stage so that the measured signal exercises the full dynamic range of the ADC.

The measuring bandwidth of the fixed-frequency second IF section can be further reduced. This significantly improves the sensitivity of the system and is especially important when making noise figure measurements. When wide-band signals are measured, the bandpass filter can be bypassed. The pre-amp in the through-pass of the directional coupler is one of the most critical components of the measurement path. To enable the measurement of test signals with large

Figure 2.15. Measurement path with S-parameter measurement capability of an RF subsystem.



dynamic range, the pre-amp needs to have a low noise figure but at the same time must have a high compression point. This is critical when testing phase noise (see Chapter 13) with a strong carrier and a low phase noise.

2.7 COMPUTING HARDWARE

2.7.1 User Computer

Mixed-signal testers typically contain several computers and signal processors. The test engineer is most familiar with the user computer, since this is the one that is attached to the keyboard. The user computer is responsible for all the editing and compiling processes necessary to debug a test program. It is also responsible for keeping track of the datalogs and other data collection information. On low-cost testers, the user computer may also drive the measurement electronics as well. On more advanced mainframe testers, the execution of the test program, including I/O functions to the tester's measurement electronics, may be delegated to one or more tester computers located inside the tester's mainframe.

2.7.2 Tester Computer

The tester computer executes the compiled test program and interfaces to all the tester's instruments through a high-speed data backplane. By concentrating most of its processing power on the test program itself, the tester computer can execute a test program more efficiently than the user computer. The tester computer also performs all the mathematical operations on the data collected during each test. In some cases, the more advanced digital signal processing (DSP) operations may be handled by a dedicated array processor to further reduce test time. However, computer workstations have become fast enough in recent years that the DSP operations are often handled by the tester computer itself rather than by a dedicated array processor.

2.7.3 Array Processors and Distributed Digital Signal Processors

Many mixed-signal testers include one or more dedicated array processors for performing DSP operations quickly. This is another difference between a mixed-signal tester and a bolted-together digital/analog tester. Some mixed-signal instruments may even include local DSP processors for computing test results before they are transferred to the tester computer. This type of tester architecture and test methodology is called *distributed processing*. Distributed processing can reduce test time by splitting the DSP computation task among several processors throughout the tester. Test time is further reduced by eliminated much of the raw data transfer that would otherwise occur between digitizer instruments and a centralized tester computer or array processor. Unfortunately, distributed processing may have the disadvantage that the resulting test code may be harder to understand and debug.

2.7.4 Network Connectivity

The user computer and/or tester computer are typically connected into a network using Ethernet or similar networking hardware. This allows data and programs to be quickly transferred to the test engineer's desk for offline debugging and data analysis. It also allows for large amounts of production data to be stored and analyzed for characterization purposes.

2.8 SUMMARY

In this chapter we have examined many of the common building blocks of a generic mixed-signal tester. Of course, there are many differences between any two ATE vendors' preferred tester architectures. For example, ATE Vendor A may use a sigma-delta-based digitizer and AWG, while ATE Vendor B may choose to use a more conventional successive approximation architecture for its AWG and digitizer. Each architecture has advantages and disadvantages, which the test engineer must deal with. The test engineer's approach to measuring a given parameter will often be driven by the vendor's architectural choices. In the end, though, each tester has to test the same variety of mixed-signal parameters regardless of its architectural peculiarities. A test engineer's job often involves testing parameters the tester was simply not designed to measure. This can be one of the more challenging and interesting parts of a test engineer's task.

In later chapters we will see how digitizers, AWGs, and digital pattern generators, combined with digital signal processing, can provide greater speed and accuracy than conventional measurement techniques. We will also explain why it is so critical to mixed-signal testing that we achieve precise synchronization of sampling frequencies between all the tester's instruments. Most mixed-signal testing involves DSP-based measurements of one type or another; thus the student will need to devote special attention to these chapters.

PROBLEMS

2.1. Name at least six types of subsystems found in a typical mixed-signal tester.

2.2. What is the purpose of the low-pass filter in a DC multimeter's front end?

2.3. What is the purpose of the PGA in a DC multimeter's front end?

2.4. A single-ended DC voltmeter features a sample-and-difference front-end circuit. We wish to use this meter to measure the differential offset voltage of a DUT's output buffer. Each of the two outputs is specified to be within a range of 3.5 V ± 25 mV, and the differential offset is specified in the device data sheet to be ±15 mV. The meter input can be set to any of the following ranges: ±10 V, ±5 V, ±2 V, and ±1 V. The meter has a maximum error of 0.1% of its programmed range. The error includes all sources of inaccuracy (quantization

error, linearity error, gain error, etc.). Compare the accuracy achieved using two simple DC measurements with the accuracy achieved using the sample-and-difference circuit. Assume no errors due to nonrepeatability.

2.5. Why are Kelvin connections used to connect high-current DC power supplies to the DUT?

2.6. Name an instance where a local DIB relay might prove to be a better choice for interconnecting signals than a general-purpose relay matrix.

2.7. What is the purpose of the diodes in the output stage of the relay driver in Figure 2.5?

2.8. What is the difference between a digital pattern and a digital signal?

2.9. What is the purpose of source memory?

2.10. What is the purpose of capture memory?

2.11. Why is formatting and timing information combined with one/zero information to produce digital waveforms?

2.12. A series of digital bits are driven from a digital pin card at a rate of 1 MHz (1-μs period). The series of bits are 10110X1. The format for this pin is set to return-to-zero (RZ) format. Its initial state is set to logic low. The start time for the drive data is set to 500 ns, and the stop time is set to 900 ns. Draw this waveform using the notation in Figure 2.8. Draw the waveform timing approximately to scale. Next, draw the waveform that would result if we set the format to non-return-to-zero (NRZ). To produce these waveforms using clocked digital logic without timing and formatting circuits, what clock rate would be required? If we wanted to be able to set the start and stop times to 500 ns and 901 ns, respectively, at what rate would we have to operate the clocked digital logic?

2.13. Name two reasons that AWGs and digitizers are used in mixed signal testing rather than CW sources and RMS voltmeters.

2.14. What is the purpose of the low-pass filter in the AWG illustrated in Figure 2.10?

2.15. Why is a programmable gain amplifier needed in the front end of the waveform digitizer illustrated in Figure 2.12?

2.16. What is the purpose of distributed digital signal processing hardware?