CHAPTER 3

DC and Parametric Measurements

This chapter introduces the reader to basic DC measurement definitions, including continuity, leakage, impedance, offset, gain, and DC power supply rejection ratio tests. In addition, search techniques used to establish specific DC test conditions are described. The chapter concludes with a brief discussion about the DC tests performed on digital circuits.

3.1 CONTINUITY

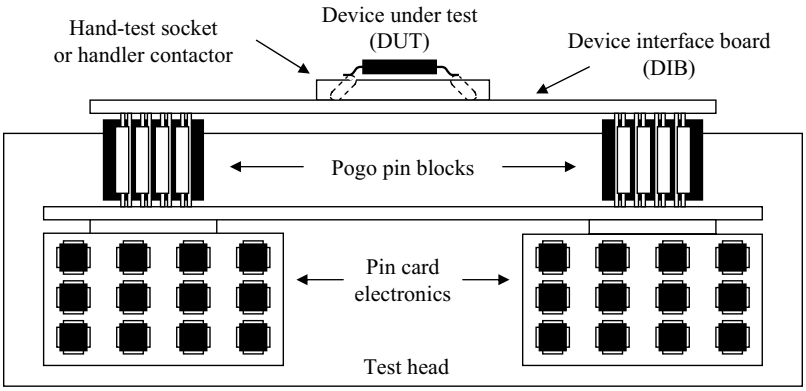
3.1.1 Purpose of Continuity Testing

Before a test program can evaluate the quality of a device under test (DUT), the DUT must be connected to the ATE tester using a test fixture such as a device interface board (DIB). A typical interconnection scheme is shown in Figure 3.1. When packaged devices are tested, a socket or handler contactor assembly provides the contact between the DUT and the DIB. When testing a bare die on a wafer, the contact is made through the probe needles of a probe card. The tester's instruments are connected to the DIB through one or more layers of connectors such as spring-loaded pogo pins or edge connectors. The exact connection scheme varies from tester to tester, depending on the mechanical/electrical performance tradeoffs made by the ATE vendor.

In addition to pogo pins and other connectors, electromechanical relays are often used to route signals from the tester electronics to the DUT. A relay is an electrical switch whose position is controlled by an electromagnetic field. The field is created by a current forced through a coil of wire inside the relay. Relays are used extensively in mixed-signal testing to modify the electrical connections to and from the DUT as the test program progresses from test to test.

Any of the electrical connections between a DUT and the tester can be defective, resulting in open circuits or shorts between electrical signals. For example, the wiper of a relay can become stuck in either the open or closed position after millions of open/close cycles. While interconnect problems may not pose a serious problem in a lab environment, defective connections can be a major source of tester down time on the production floor. Continuity tests (also known as *contact tests*) are performed on a device to verify that all the electrical connections are sound. If continuity

Figure 3.1. ATE test head to DUT interconnections.



testing is not performed, then the production floor personnel cannot distinguish between bad lots of silicon and defective test hardware connections. Without continuity testing, thousands of good devices could be rejected simply because a pogo pin was bent or because a relay was defective.

3.1.2 Continuity Test Technique

Continuity testing is usually performed by detecting the presence of on-chip protection circuits. These circuits protect each input and output of the device from electrostatic discharge (ESD) and other excessive voltage conditions. The ESD protection circuits prevent the input and output pins from exceeding a small voltage above or below the power supply voltage or ground. Diodes and silicon-controlled rectifiers (SCRs) can be used to short the excess currents from the protected pin to ground or to a power terminal.

An ESD protection diode conducts the excess ESD current to ground or power any time the pin's voltage exceeds one diode drop above (or below) the power or ground voltage. SCRs are similar to ESD protection diodes, but they are triggered by a separate detection circuit. Any of a variety of detection circuits can be used to trigger the SCR when the protected pin's voltage exceeds a safe voltage range. Once triggered, an SCR behaves like a forward-biased diode from the protected pin to power or ground (Figure 3.2). The SCR remains in its triggered state until the excessive voltage is removed. Since an SCR behaves much like a diode when triggered, the term "protection diode" is used to describe ESD protection circuits whether they employ a simple diode or a more elaborate SCR structure. We will use the term "protection diode" throughout the remainder of this book with the understanding that a more complex circuit may actually be employed.

DUT pins may be configured with either one or two protection diodes, connected as shown in Figure 3.3. Notice that the diodes are reverse-biased when the device is powered up, assuming normal input and output voltage levels. This effectively makes them "invisible" to the DUT circuits during normal operation.

To verify that each pin can be connected to the tester without electrical shorts or open circuits, the ATE tester forces a small current across each protection diode in the forward-biased direction. The DUT's power supply pins are set to zero volts to disable all on-chip circuits and to connect the far end of each diode to ground. ESD protection diodes connected to the positive supply are tested by forcing a current I_{CONT} into the pin as shown in Figure 3.4 and measuring the voltage, V_{CONT}, that appears at the pin with respect to ground. If the tester does not see the expected diode drops on each pin, then the continuity test fails and the device is not tested further. Protection

Figure 3.2. SCR-based ESD protection circuit.

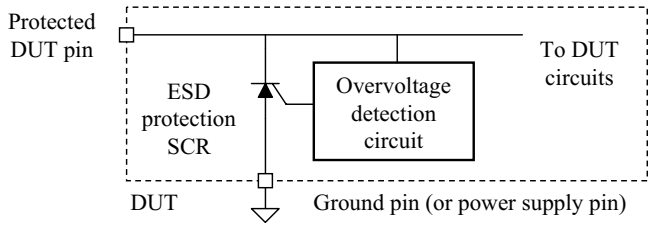
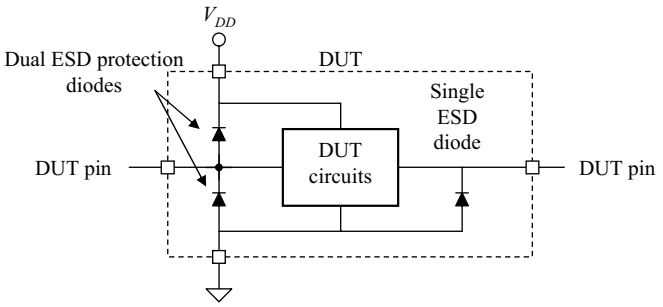


Figure 3.3. Dual and single protection diodes.



diodes connected to the negative supply or ground are tested by reversing the direction of the forced current.

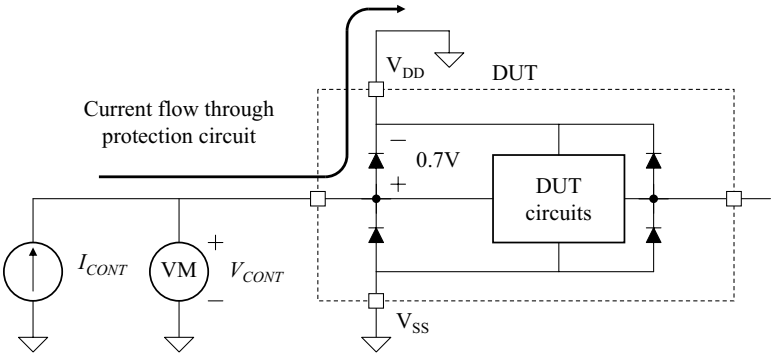
In the case of an SCR-based protection circuit, the current source initially sees an open circuit. Because the current source output tries to force current into an open circuit, its output voltage rises rapidly. The rising voltage soon triggers the SCR's detection circuit. Once triggered, the SCR accepts current from the current source and the voltage returns to one diode drop above ground. Thus the difference between a diode-based ESD protection circuit and an SCR-based circuit is hardly noticeable during a continuity test.

The amount of current chosen is typically between 100 μA and 1 mA, but the ideal value depends on the characteristics of the protection diodes. Too much current may damage the diodes, while too little current may not fully bias them. The voltage drop across a good protection diode usually measures between 550 and 750 mV. For the purpose of illustration, we shall assume that a conducting diode has voltage drop of 0.7 V. A dead short to ground will result in a reading of 0 V, while an open circuit will cause the tester's current source to reach a programmed clamp voltage.

Many mixed-signal devices have multiple power supply and ground pins. Continuity to these power and ground connections may or may not be testable. If all supply pins or all ground pins are not properly connected to ground, then continuity to some or all of the nonsupply pins will fail. However, if only some of the supply or ground pins are not grounded, the others will provide a continuity path to zero volts. Therefore, the unconnected power supply or ground pins may not be detected. One way to test the power and ground pins individually is to connect them to ground one at a time, using relays to break the connections to the other power and ground pins. Continuity to the power or ground pin can then be verified by looking for the protection diode between it and another DUT pin.

Occasionally, a device pin may not include any protection diodes at all. Continuity to these unprotected pins must be verified by an alternative method, perhaps by detecting a small amount

Figure 3.4. Checking the continuity of the diode connected to the positive supply. The other diode is tested by reversing the direction of the forced current.



of current leaking into the pin or by detecting the presence of an on-chip component such as a capacitor or resistor. Since unprotected pins are highly vulnerable to ESD damage, they are used only in special cases.

One such example is a high-frequency input requiring very low parasitic capacitance. The space-charge layer in a reverse-biased protection diode might add several picofarads of parasitic capacitance to a device pin. Since even a small amount of stray capacitance presents a low impedance to very high-frequency signals, the protection diode must sometimes be omitted to enhance electrical performance of the DUT.

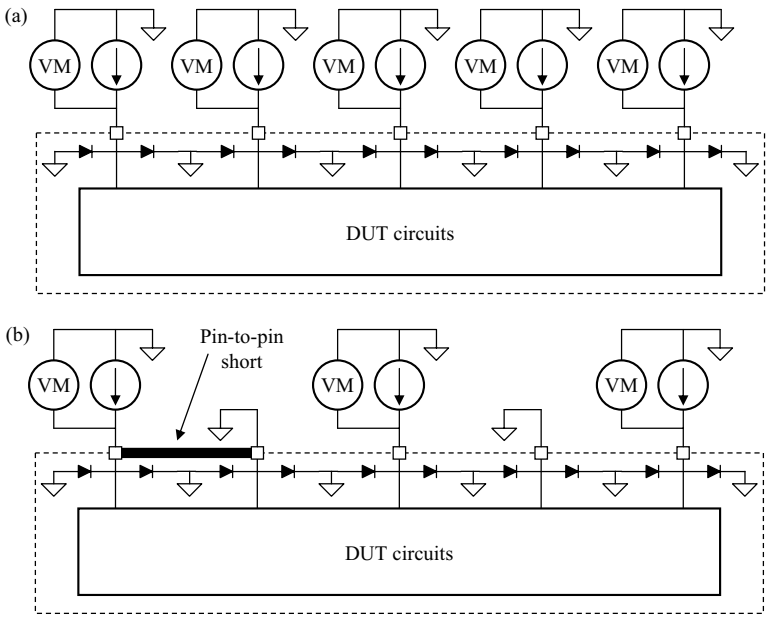
3.1.3 Serial Versus Parallel Continuity Testing

Continuity can be tested one pin at a time, an approach known as *serial continuity testing*. Unfortunately, serial testing is a time-consuming and costly approach. Modern ATE testers are capable of measuring continuity on all or most pins in parallel rather than measuring the protection diode drops one at a time. These testers accomplish parallel testing using so-called *per-pin measurement instruments* as shown in Figure 3.5a.

Clearly it is more economical to test all pins at once using many current sources and voltage meters. Unfortunately, there are a few potential problems to consider. First, a fully parallel test of pins may not detect pin-to-pin shorts. If two device pins are shorted together for some reason, the net current through each diode does not change. Twice as much current is forced through the parallel combination of two diodes. The shorted circuit configuration will therefore result in the expected voltage drop across each diode, resulting in both pins passing the continuity test. Obviously, the problem can be solved by performing a continuity test on each pin in a serial manner at the cost of extra test time. However, a more economical approach is to test every other pin for continuity on one test pass while grounding the remaining pins. Then the remaining pins can be tested during a second pass while the previously tested pins are grounded. Shorts between adjacent pins would be detected using this dual-pass approach, as illustrated in Figure 3.5b.

A second, subtler problem with parallel continuity testing is related to analog measurement performance. Both analog pins and digital pins must be tested for continuity. On some testers the per-pin continuity test circuitry is limited to digital pins only. The analog pins of the tester may not include per-pin continuity measurement capability. On these testers, continuity testing on analog pins can be performed one pin at a time using a single current source and voltmeter. These two instruments can be connected to each device pin one at a time to measure protection diode drops. Of course, this is a very time-consuming serial test method, which should be avoided if possible.

Figure 3.5. Parallel continuity testing: (a) Full parallel testing with possible adjacent fault masking; (b) Minimizing potential adjacent fault masking by exciting every second pin.



Alternatively, the analog pins can be connected to the per-pin measurement electronics of digital pins. This allows completely parallel testing of continuity. Unfortunately, the digital per-pin electronics may inject noise into sensitive analog signals. Also, the signal trace connecting the DUT to the per-pin continuity electronics adds a complex capacitive and inductive load to the analog pin, which may be unacceptable. The signal trace can also behave as a parasitic radio antenna into which unwanted signals can couple into analog inputs. Clearly, full parallel testing of analog pins should be treated with care. One solution to the noise and parasitic loading problems is to isolate each analog pin from its per-pin continuity circuit using a relay. This complicates the DIB design but gives high performance with minimal test time. Of course, a tester having per-pin continuity measurement circuits on both analog and digital pins represents a superior solution.

3.2 LEAKAGE CURRENTS

3.2.1 Purpose of Leakage Testing

Each input pin and output pin of a DUT exhibits a phenomenon called *leakage*. When a voltage is applied to a high-impedance analog or digital input pin, a small amount of current will typically leak into or out of the pin. This current is called *leakage current*, or simply *leakage*. Leakage can also be measured on output pins that are placed into a nondriving high-impedance mode. A good design and manufacturing process should result in very low leakage currents. Typically the leakage is less than 1 μA, although this can vary from one device design to the next.

One of the main reasons to measure leakage is to detect improperly processed integrated circuits. Leakage can be caused by many physical defects such as metal filaments and particulate matter that forms shorts and leakage paths between layers in the IC. Another reason to measure leakage is that excessive leakage currents can cause improper operation of the customer's end

application. Leakage currents can cause DC offsets and other parametric shifts. A third reason to test leakage is that excessive leakage currents can indicate a poorly processed device that initially appears to be functional but which eventually fails after a few days or weeks in the customer's product.[1] This type of early failure is known as *infant mortality*.

3.2.2 Leakage Test Technique

Leakage is measured by simply forcing a DC voltage on the input or output pin of the device under test and measuring the small current flowing into or out of the pin. Unless otherwise specified in the data sheet, leakage is typically measured twice. It is measured once with an input voltage near the positive power supply voltage and again with the input near ground (or negative supply). These two currents are referred to as I_{IH} (input current, logic high) and I_{IL} (input current, logic low), respectively.

Digital inputs are typically tested at the valid input threshold voltages, V_{IH} and V_{IL}. Analog input leakage is typically tested at specific voltage levels listed in the data sheet. If no particular input voltage is specified, then the leakage specification applies to the entire allowable input voltage range. Since leakage is usually highest at one or both input voltage extremes, it is often measured at the maximum and minimum allowable input voltages. Output leakage (I_{OZ}) is measured in a manner similar to input leakage, although the output pin must be placed into a high-impedance (HIZ) state using a test mode or other control mechanism.

3.2.3 Serial Versus Parallel Leakage Testing

Leakage, like continuity, can be tested one pin at a time (serial testing) or all pins at once (parallel testing). Since leakage currents can flow from one pin to another, serial testing is superior to parallel testing from a defect detection perspective. However, from a test time perspective, parallel testing is desired. As in continuity testing, a compromise can be achieved by testing every other pin in a dual-pass approach.

Continuity tests are usually implemented by forcing DC current and measuring voltage. By contrast, leakage tests are implemented by forcing DC voltage and measuring current. Since the tests are similar in nature, tester vendors generally design both capabilities into the per-pin measurement circuits of the ATE tester's pin cards. Analog leakage, like analog continuity, is often measured using the per-pin resources of digital pin cards. Again, a tester with per-pin continuity measurement circuits on both analog and digital pins represents a superior solution, assuming that the extra per-pin circuits are not prohibitively expensive.

3.3 POWER SUPPLY CURRENTS

3.3.1 Importance of Supply Current Tests

One of the fastest ways to detect a device with catastrophic defects is to measure the amount of current it draws from each of its power supplies. Many gross defects such as those illustrated in Figures 1.4–1.7 result in a low-impedance path from one of the power supplies to ground. Supply currents are often tested near the beginning of a test program to screen out completely defective devices quickly and cost effectively.

Of course, the main reason to measure power supply current is to guarantee limited power consumption in the customer's end application. Supply current is an important electrical parameter for the customer who needs to design a system that consumes as little power as possible. Low power consumption is especially important to manufacturers of battery operated equipment like cellular telephones. Even devices that draw large amounts of current by design should draw only

as much power as necessary. Therefore, power supply current tests are performed on most if not all devices.

3.3.2 Test Techniques

Most ATE testers are able to measure the current flowing from each voltage source connected to the DUT. Supply currents are therefore very easy to measure in most cases. The power supply is simply set to the desired voltage and the current from its output is measured using one of the tester's ammeters.

When measuring supply currents, the only difficulties arise out of ambiguities in the data sheet. For example, are the analog outputs loaded or unloaded during the supply current test? Is digital block XYZ operating in mode A, mode B, or idle mode? In general, it is safe to assume that the supply currents are to be tested under worst-case conditions.

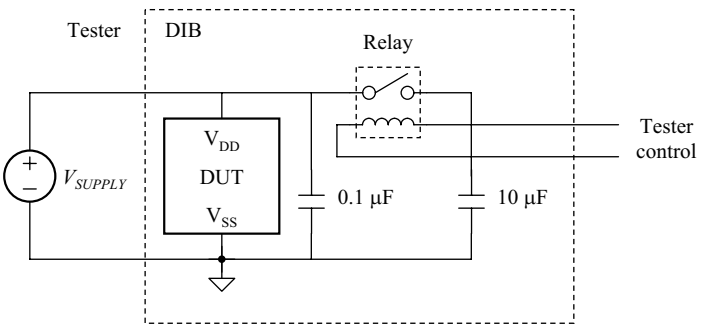
The test engineer should work with the design engineers to attempt to specify the test conditions that are likely to result in worst-case test conditions. These test conditions should be spelled out clearly in the test plan so that everyone understands the exact conditions used during production testing. Often the actual worst-case conditions are not known until the device has been thoroughly characterized. In these cases, the test program and test plan have to be updated to reflect the characterized worst-case conditions.

Supply currents are often specified under several test conditions, such as power-down mode, standby mode, and normal operational mode. In addition, the digital supply currents are specified separately from the analog supply currents. I_{DD} (CMOS) and I_{CC} (bipolar) are commonly used designations for supply current. I_{DDA}, I_{DDD}, I_{CCA}, and I_{CCD} are the terms used when analog and digital supplies are measured separately.

Many devices have multiple power supply pins that are connected to a common power supply in normal operation. Design engineers often need to know how much current is flowing into each individual power supply pin. Sometimes the test engineer can accommodate this requirement by connecting each power supply pin to its own supply. Other times there are too many DUT supply pins to provide each with its own separate power supply. In these cases, relays can be used to temporarily connect a dedicated power supply to the pin under test.

Another problem that can plague power supply current tests is settling time. The supply current flowing into a DUT must settle to a stable value before it can be measured. The tester and DIB circuits must also settle to a stable value. This normally takes 5–10 ms in normal modes of DUT operation. However, in power-down modes the specified supply current is often less than 100 μA.

Figure 3.6. Arranging different-sized bypass capacitors to minimize power supply current settling behavior.



Since the DIB usually includes bypass capacitors for the DUT, each capacitor must be allowed to charge until the average current into or out of the capacitor is stable.

The charging process can take hundreds of milliseconds if the current must stabilize within microamps. Some types of bypass capacitors may even exhibit leakage current greater than the current to be measured. A typical solution to this problem is to connect only a small bypass capacitor (say 0.1 μF) directly to the DUT and then connect a larger capacitor (say 10 μF) through a relay as shown in Figure 3.6. The large bypass capacitor can be disconnected temporarily while the power-down current is measured.

3.4 DC REFERENCES AND REGULATORS

3.4.1 Voltage Regulators

A voltage regulator is one of the most basic analog circuits. The function of a voltage regulator is to provide a well-specified and constant output voltage level from a poorly specified and sometimes fluctuating input voltage. The output of the voltage regulator would then be used as the supply voltage for other circuits in the system. Figure 3.7 illustrates the conversion of a 6- to 12-V ranging power supply to a fixed 5-V output level.

Voltage regulators can be tested using a fairly small number of DC tests. Some of the important parameters for a regulator are output no-load voltage, output voltage or load regulation, input or line regulation, input or ripple rejection, and dropout voltage.

Output no-load voltage is measured by simply connecting a voltmeter to the regulator output with no load current and measuring the output voltage V_O.

Load regulation measures the ability of the regulator to maintain the specified output voltage V_O under different load current conditions I_L. As the output voltage changes with increasing load current, one defines the output voltage regulation as the percentage change in the output voltage (relative to the ideal output voltage, $V_{O,NOM}$) for a specified change in the load current. Load regulation is measured under minimum input voltage conditions

$$\text{load regulation} \equiv 100\% \times \left. \frac{\Delta V_O}{V_{O,\,NOM}} \right|_{\max\{\Delta I_L\},\ \text{minimum } V_I} \tag{3.1}$$

The largest load current change, max (ΔI_L), is created by varying the load current from the minimum rated load current (typically 0 mA) to the maximum rated load current.

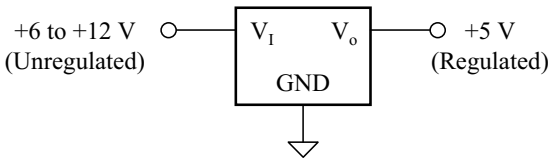
Load regulation is sometimes specified as the absolute change in voltage, ΔV_O, rather than as a percentage change in V_O. The test definition will be obvious from the specification units (i.e. volts or percentage).

Line regulation or *input regulation* measures the ability of the regulator to maintain a steady output voltage over a range of input voltages. Line regulation is specified as the percentage change in the output voltage as the input line voltage changes over its largest allowable range. Like the load regulation test, line regulation is sometimes specified as an absolute voltage change rather than a percentage. Line regulation is measured under maximum load conditions:

$$\text{line regulation} \equiv 100\% \times \left. \frac{\Delta V_O}{V_{O,\,NOM}} \right|_{\max\{\Delta V_I\},\ \text{maximum } I_L} \tag{3.2}$$

For the regulator shown in Figure 3.7, with the appropriate load connected to the regulator output, the line regulation would be computed by first setting the input voltage to 6 V, measuring

Figure 3.7. 5-V DC voltage regulator.



the output voltage, then readjusting the input voltage to 12 V, and again measuring the output voltage to calculate ΔV_O. The line regulation would then be computed using Eq. (3.2).

Input rejection or *ripple rejection* is the ratio of the maximum input voltage variation to the output voltage swing, measured at a particular frequency (commonly 120 Hz) or a range of frequencies. It is a measure of the circuit's ability to reject periodic fluctuations of rectified AC voltage signals applied to the input of the regulator. Input rejection can also be measured at DC using the input voltage range and output voltage swing measured during the line regulation test.

Dropout voltage is the lowest voltage that can be applied between the input and output pins without causing the output to drop below its specified minimum output voltage level. Dropout voltage is tested under maximum current loading conditions. It is possible to search for the exact dropout voltage by adjusting the input voltage until the output reaches its minimum acceptable voltage, but this is a time-consuming test method. In production testing, the input can simply be set to the specified dropout voltage plus the minimum acceptable output voltage. The output is then measured to guarantee that it is equal to or above the minimum acceptable output voltage.

3.4.2 Voltage References

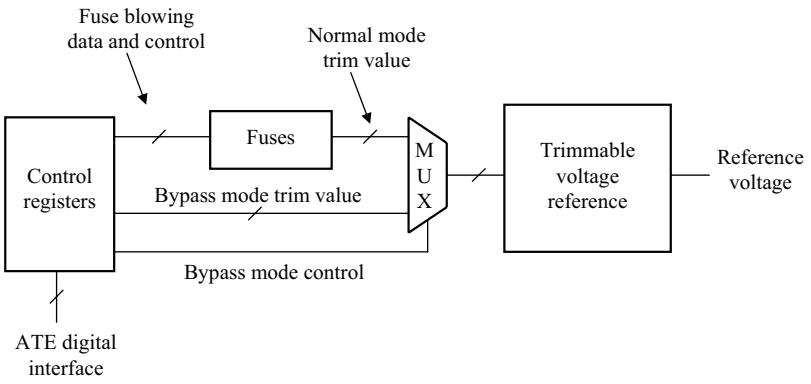
Voltage regulators are commonly used to supply a steady voltage while also supplying a relatively large amount of current. However, many of the DC voltages used in a mixed-signal device do not draw a large amount of current. For example, a 1-V DAC reference does not need to supply 500 mA of current. For this reason, low-power voltage references are often incorporated into mixed-signal devices rather than high-power voltage regulators.

The output of on-chip voltage references may or may not be accessible from the external pins of a DUT. It is common for the test engineer to request a set of test modes so that reference voltages can be measured during production testing. This allows the test program to evaluate the quality of the DC references even if they have no explicit specifications in the data sheet. The design and test engineers can then determine whether failures in the more complicated AC tests may be due to a simple DC voltage error in the reference circuits. DC reference test modes also allow the test program to trim the internal DC references for more precise device operation.

3.4.3 Trimmable References

Many high-performance mixed-signal devices require reference voltages that are trimmed to very exact levels by the ATE tester. DC voltage trimming can be accomplished in a variety of ways. The most common way is to use a programmable reference circuit that can be permanently adjusted to the desired level. One such arrangement is shown in Figure 3.8. The desired level is programmed using fuses, or a nonvolatile digital control mechanism such as EEPROM or flash memory bits. Fuses are blown by forcing a controlled current across each fuse that causes it to vaporize. Fuses can be constructed from either metal or polysilicon. If EEPROM or flash memory is added to a mixed-signal device, then this technology may offer a superior alternative to blown fuses, as EEPROM bits can be rewritten if necessary.

Figure 3.8. Trimmable reference circuit.



There are various algorithms for finding the digital value that minimizes reference voltage error. In the more advanced trimming architectures such as the one in Figure 3.8, the reference can be experimentally adjusted using a bypass trim value rather than permanently blowing the fuses. In this example, the bypass trim value is enabled using a special test mode control signal, bypass mode control. Once the best trim value has been determined by experimental trials, the fuses are permanently blown to set the desired trim value. Then, during normal operation, the bypass trim value is disabled and the programmed fuses are used to control the voltage reference.

Trimming can also be accomplished using a laser trimming technique. In this technique, a laser is used to cut through a portion of an on-chip resistor to increase its resistance to the desired value. The resistance value, in turn, adjusts the DC level of the voltage reference. The laser trimming technique can also be used to trim gains and offsets of analog circuits. Laser trimming is more complex than trimming with fuses or nonvolatile memory. It requires special production equipment linked to the ATE tester.

Laser trimming must be performed while the silicon wafer is still exposed to open air during the probing process. Since metal fuses can produce a conductive sputter when they vaporize, they too are usually trimmed during the wafer probing process. By contrast, polysilicon fuses and EEPROM bits can be blown either before or after the device is packaged.

There is an important advantage to trimming DC levels after the device has been packaged. When plastic is injected around the silicon die, it can place slight mechanical forces on the die. This, in turn, introduces DC offsets. Because of these DC shifts, a device that was correctly trimmed during the wafer probing process may not remain correctly trimmed after it has been encapsulated in plastic. Another potential DC shift problem relates to the photoelectric effect. Since light shining on a bare die introduces photoelectric DC offsets, a bare die must be trimmed in total darkness. Of course, wafer probers are designed with this requirement in mind. They include a black hood or other mechanism to shield bare die from light sources.

3.5 IMPEDANCE MEASUREMENTS

3.5.1 Input Impedance

Input impedance (Z_{IN}), also referred to as *input resistance*, is a common specification for analog inputs. In general, impedance refers to the behavior of both resistive and reactive (capacitive or inductive) components in the circuit. As the discussion in this chapter is restricted to DC, we are assuming that inductors and capacitors do not participate in circuit operation (act as either a short

circuit in the case of an inductor, or an open circuit in the case of a capacitor). Hence, impedance and resistance refer to the same quantity at DC.

Exercises

3.1.	The output of a 5-V voltage regulator varies from 5.10 V under no-load condition to 4.85 V under a 5 mA maximum rated load current. What is its load regulation?	ANS. 5%.
3.2.	The output of a 5-V voltage regulator varies from 5.05 to 4.95 V when the input voltage is changed from 14 to 6 V under a maximum load condition of 10 mA. What is its line regulation?	ANS. 2%.
3.3.	A 9-V voltage regulator is rated to have a load regulation of 3% for a maximum load current of 15 mA. Assuming a no-load output voltage of 9 V, what is the worst-case output voltage at the maximum load current?	ANS. 8.73 V.

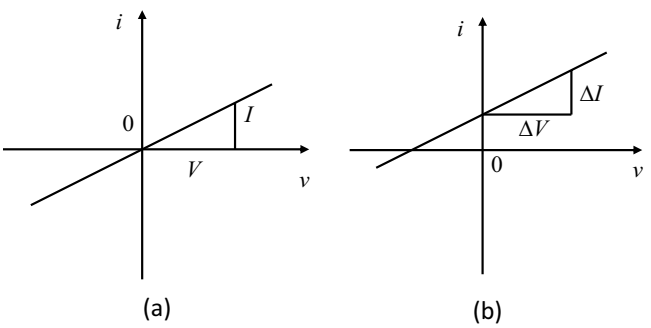
Input impedance is a fairly simple measurement to make. If the input voltage is a linear function of the input current (i.e., if it behaves according to Ohm's law), then one simply forces a voltage V and measures a current I, or vice versa, and computes the input impedance according to

$$Z_{IN} = \frac{V}{I} \tag{3.3}$$

Figure 3.9a illustrates the input i–v relationship of a device satisfying Ohm's law. Here we see that the i–v characteristic is a straight line passing through the origin with a slope equal to $1/Z_{IN}$. In many instances, the i–v characteristic of an input pin is a straight line but does not pass through the origin as shown in Figure 3.9b. Such situations typically arise from biasing considerations where the input terminal of a device is biased by a constant current source such as that shown in Figure 3.10 or has in series with it an unknown voltage source to ground, or in series between two components comprising the input series impedance.

In cases such as these, one cannot use Eq. (3.3) to compute the input impedance, as it will not lead correctly to the slope of the i–v characteristic. Instead, one measures the change in the input

Figure 3.9. Input ***i–v*** characteristic curves resulting in an impedance function with (a) equal DC and AC operation and (b) unequal DC and AC operation.



current (ΔI) that results from a change in the input voltage (ΔV) and computes the input impedance using

$$Z_{IN} = \frac{\Delta V}{\Delta I} \tag{3.4}$$

If the input impedance is so low that it would cause excessive currents to flow into the pin, another approach is needed. The alternative method is to force two controlled currents and measure the resulting voltage difference. This is often referred to as a *force-current/measure-voltage* method. Input impedance is again calculated using Eq. (3.4).

EXAMPLE 3.1

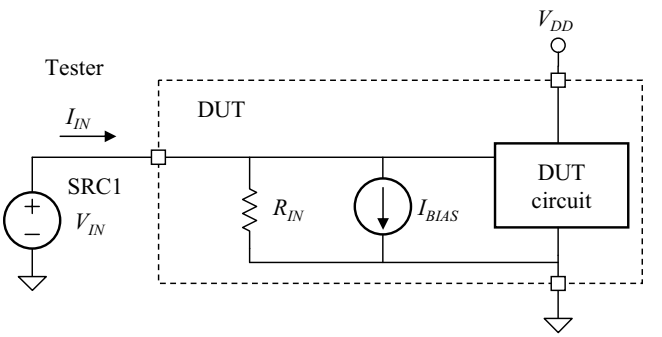
In the input impedance test setup shown in Figure 3.10, voltage source SRC1 is set to 2 V and current flowing into the pin is measured to be 0.055 mA. Then SRC1 is set to 1 V and the input current is measured again to be 0.021 mA. What is the input impedance?

Solution:
Input impedance, Z_{IN}, which is a combination of R_{IN} and the input impedance of the block labeled "DUT Circuit," is calculated using Eq. (3.4) as follows

$$Z_{IN} = \frac{2\,\text{V} - 1\,\text{V}}{0.055\,\text{mA} - 0.021\,\text{mA}} = 29.41\,\text{k}\Omega$$

Note that the impedance could also have been measured by forcing 0.050 and 0.020 mA and measuring the voltage difference. However, the unpredictable value of I_{BIAS} could cause the input voltage to swing beyond the DUT's supply rails. For this reason, the forced-current measurement technique is reserved for low values of resistance.

Figure 3.10. Input impedance test setup.



In Example 3.1, the values of the excitation consisting of 2 and 1 V are somewhat irrelevant. We could just as easily have used 2.25 and 1.75 V. However, the larger the difference in voltage, the easier it is to make an accurate measurement of current change. This is true throughout many types of tests. Large changes in voltages and currents are easier to measure than small ones. The

test engineer should beware of saturating the input of the device with excessive voltages, though. Saturation could lead to extra input current resulting in an inaccurate impedance measurement. The device data sheet should list the acceptable range of input voltages.

3.5.2 Output Impedance

Output impedance (Z_{OUT}) is measured in the same way as input impedance. It is typically much lower than input impedance; so it is usually measured using a force-current/measure-voltage technique. However, in cases where the output impedance is very high, it may be measured using the force-voltage/measure-current method instead.

EXAMPLE 3.2

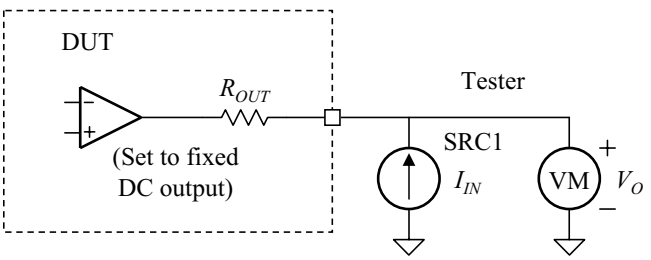
In the output impedance test setup shown in Figure 3.11, current source SRC1 is set to 10 mA and the voltage at the pin is measured, yielding 1.61 V. Then SRC1 is set to –10 mA and the output voltage is measured at 1.42 V. What is the total output impedance (R_{OUT} plus the amplifier's output impedance)?

Solution:

Using Eq. (3.4) with Z_{IN} replaced by Z_{OUT}, we write

$$Z_{OUT} = \frac{1.61\ \text{V} - 1.42\ \text{V}}{10\ \text{mA} - (-10\ \text{mA})} = 9.5\ \Omega$$

Figure 3.11. Output impedance test setup.



3.5.3 Differential Impedance Measurements

Differential impedance is measured by forcing two differential voltages and measuring the differential current change or by forcing two differential currents and measuring the differential voltage change. Example 3.3 illustrates this approach using forcing currents and measuring the resulting differential voltage. Differential input impedance would be measured in a similar manner.

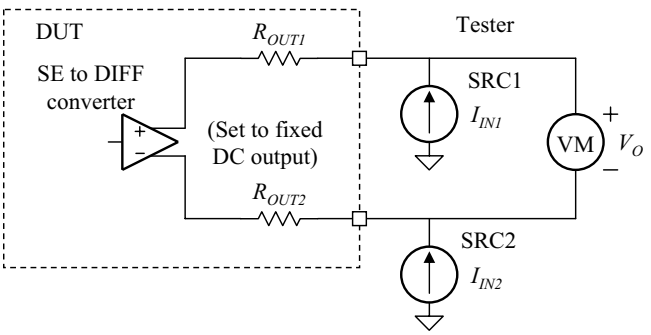
EXAMPLE 3.3

In the differential output impedance test setup shown in Figure 3.12 current source SRC1 is set to 20 mA, SRC2 is set to –20 mA and the differential voltage at the pins is measured at 201 mV. Then SRC1 is set to –20 mA, SRC2 is set to 20 mA, and the output voltage is measured at –199 mV. What is the differential output impedance?

Solution:
The output impedance is found using Eq. (3.4) to be

$$Z_{OUT} = \frac{201\text{ mV} - (-199\text{ mV})}{20\text{ mA} - (-20\text{ mA})} = 10\ \Omega$$

Figure 3.12. Differential output impedance test setup.



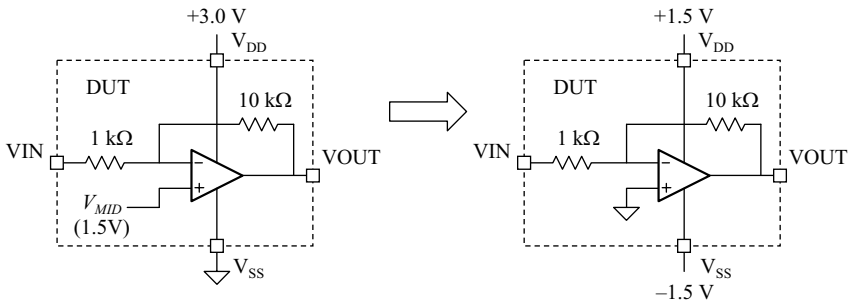
3.6 DC OFFSET MEASUREMENTS

3.6.1 V_{MID} and Analog Ground

Many analog and mixed-signal integrated circuits are designed to operate on a single power supply voltage (V_{DD} and ground) rather than a more familiar bipolar supply (V_{DD}, V_{SS}, and ground). Often these single-supply circuits generate their own low-impedance voltage between V_{DD} and ground that serves as a reference voltage for the analog circuits. This reference voltage, which we will refer to as V_{MID}, may be placed halfway between V_{DD} and ground or it may be placed at some other fixed voltage such as 1.35 V. In some cases, V_{MID} may be generated off-chip and supplied as an input voltage to the DUT.

To simplify the task of circuit analysis, we can define any circuit node to be 0 V and measure all other voltages relative to this node. Therefore, in a single-supply circuit having a V_{DD} of 3 V, a V_{SS} connected to ground, and an internally generated V_{MID} of 1.5 V, we can redefine all voltages relative to the V_{MID} node. Using this definition of 0 V, we can translate our single-supply circuit into a more familiar bipolar configuration with $V_{DD} = +1.5$ V, $V_{MID} = 0$ V, and $V_{SS} = -1.5$ V (Figure 3.13). In order for this approach to be valid, it is assumed that no hidden impedance lies between V_{SS} and ground—a reasonable assumption at low to moderate frequencies, less so at very high frequencies.

Figure 3.13. Redefining V_{MID} as 0 V to simplify circuit analysis.



Several integrated circuit design textbooks refer to this type of V_{MID} reference voltage as analog ground, since it serves as the ground reference in single-supply analog circuits. This is an unfortunate choice of terminology from a test engineering standpoint. Analog ground is a term used in the test and measurement industry to refer to a high-quality ground that is separated from the noisy ground connected to the DUT's digital circuits. In fact, the term "ground" has a definite meaning when working with measurement equipment since it is actually tied to earth ground for safety reasons. In this textbook, we will use the term analog ground to refer to a quiet 0 V voltage for use by analog circuits and use the term V_{MID} to refer to an analog reference voltage (typically generated on-chip) that serves as the IC's analog "ground."

3.6.2 DC Transfer Characteristics (Gain and Offset)

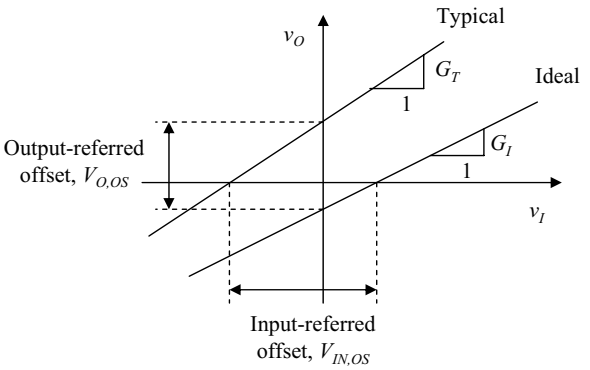
The input–output DC transfer characteristic for an ideal amplifier is shown in Figure 3.14. The input–output variables of interest are voltage, but they could just as easily be replaced by current signals. As the real world is rarely accommodating to IC and system design engineers, the actual transfer characteristic for the amplifier would deviate somewhat from the ideal or expected curve. To illustrate the point, we superimpose another curve on the plot in Figure 3.14 and label it "Typical."

In order to maintain correct system operation, design engineers require some assurance that the amplifier transfer characteristic is within acceptable tolerance limits. Of particular interest to the test engineer are the gain and offset voltages shown in the figure. In this section we shall describe the method to measure offset voltages (which is equally applicable to current signals as well), and the next section will describe several methods used to obtain amplifier gain.

3.6.3 Output Offset Voltage ($V_{0,OS}$)

The output offset ($V_{O,OS}$) of a circuit is simply the difference between its ideal DC output and its actual DC output when the input is set to some fixed reference value, normally analog ground or V_{MID}. Output offset is depicted in Figure 3.14 for an input reference value of 0 V. As long as the output is not noisy and there are no AC signal components riding on the DC level, output offset is a trivial test. If the signal is excessively noisy, the noise component must be removed from the DC level in one of two ways. First, the DC signal can be filtered using a low-pass filter. The output of the filter is measured using a DC voltmeter. ATE testers usually have a low-pass filter built into their DC meter for such applications. The low-pass filter can be bypassed during less demanding measurements in order to minimize the overall settling time. The second method of reducing the effects of noise is to collect multiple readings from the DC meter and then mathematically average the results. This is equivalent to a software low-pass filter.

Figure 3.14. Amplifier input–output transfer characteristics in its linear region.



Sometimes sensitive DUT outputs can be affected by the ATE tester's parasitic loading. Some op amps will become unstable and break into oscillations if their outputs are loaded with the stray capacitance of the tester's meter and its connections to the DUT. An ATE meter may add as much as 200 pF of loading on the output of the DUT, depending on the connection scheme chosen by the test engineer. The design engineer and test engineer should evaluate the possible effects of the tester's stray capacitance on each DUT output. It may be necessary to add a buffer amplifier to the DIB to provide isolation between the DUT output and the tester's instruments.

The input impedance of the tester can also shift DC levels when very high-impedance circuit nodes are tested. Consider the circuit in Figure 3.15 where the DUT is assumed to have an output impedance R_{OUT} of 100 kΩ. The DC meter in this example has an input impedance R_{IN} of 1 MΩ. According to the voltage divider principle with two resistors in series, the voltage that appears across the meter V_{MEAS} with respect to the output $V_{O,OS}$ of the DUT is

$$V_{MEAS} = \frac{R_{IN}}{R_{IN} + R_{OUT}} V_{O,OS} = \frac{1\ \text{M}\Omega}{1\ \text{M}\Omega + 100\ \text{k}\Omega} V_{O,OS}$$
$$= 0.909\, V_{O,OS}$$

It is readily apparent that a relative error of

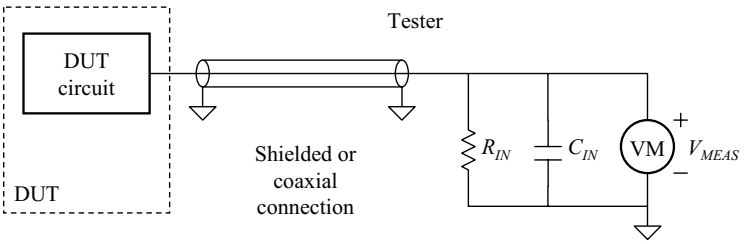
$$\text{relative error} = \frac{V_{O,OS} - V_{MEAS}}{V_{O,OS}} = \frac{(1 - 0.909)}{1} = 0.091$$

or 9.1% is introduced into this measurement. A unity gain buffer amplifier may be necessary to provide better isolation between the DUT and tester instrument.

3.6.4 Single-Ended, Differential, and Common-Mode Offsets

Single-ended output offsets are measured relative to some ideal or expected voltage level when the input is set to some specified reference level. Usually these two quantities are the same and are specified on the data sheet. Differential offset is the difference between two outputs of a differential circuit when the input is set to a stated reference level. For simplicity's sake, we shall use $V_{O,OS}$ to denote the output offset for both the single-ended and differential case. It should be clear from the context which offset is being referred to. The output common-mode voltage $V_{O,CM}$ is defined as

Figure 3.15. Meter impedance loading.



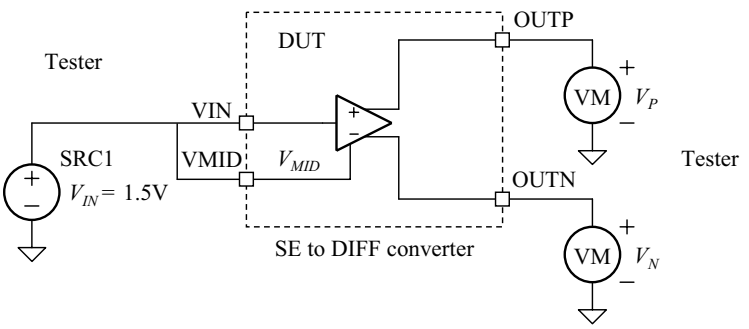
the average voltage level at the two outputs of a differential circuit. Common-mode offset $V_{O,CM,OS}$ is the difference between the output common-mode voltage and the ideal value under specified input conditions.

EXAMPLE 3.4

Consider the single-ended to differential converter shown in Figure 3.16. The two outputs of the circuit are labeled OUTP and OUTN. A 1.5-V reference voltage V_{MID} is applied to the input of the circuit and, ideally, the outputs should both produce V_{MID}. The voltages at OUTP and OUTN, denoted V_P and V_N, respectively, are measured with a meter, producing the following two readings:

$$V_P = 1.507 \text{ V} \quad \text{and} \quad V_N = 1.497 \text{ V}$$

Figure 3.16. Differential output offset test setup.



With an expected output reference level of V_{MID} = 1.50 V, compute the output differential and common-mode offsets.

Solution:

OUTP single-ended offset voltage, $V_{0,P,OS} = V_P - V_{MID} = +7$ mV
OUTN single-ended offset voltage, $V_{0,N,OS} = V_N - V_{MID} = -3$ mV
differential offset, $V_{0,D,OS} = V_P - V_N = +10$ mV
Output common-mode voltage, $V_{0,CM} = (V_P + V_N) / 2 = 1.502$ V
common-mode offset, $V_{0,CM,OS} = V_{0,CM} - V_{MID} = 2$ mV

Exercises

3.4.	An amplifier with a nominal gain of 10 V/V is characterized by $V_{OUT} = 10V_{IN} + 5$. What are its input and output offset voltages?	ANS. +0.5 V (input), 5 V (output).
3.5.	An amplifier with a nominal gain of 10 V/V is characterized by $V_{OUT} = 10V_{IN} - V_{IN}^2 + 5$ over a –5 to +5-V input range. What is its input and output offset voltages?	ANS. +0.477 V (input), 5 V (output).
3.6.	A voltmeter with an input impedance of 100 kΩ is used to measure the DC output of an amplifier with an output impedance of 500 kΩ. What is the expected relative error made by this measurement?	ANS. 83.3%.
3.7.	A differential amplifier has an output OUTP of 3.3 V and an output OUTN of 2.8 V with its input set to a V_{MID} reference level of 3 V. What are the single-ended and differential offsets? The common-mode offset?	ANS. 0.3 V and –0.2V (SE), 0.5 V (DIFF), 50 mV (CM).
3.8.	A perfectly linear amplifier has a measured gain of 5.1 V/V and an output offset of –3.2 V. What is the input offset voltage?	ANS. –0.627 V.

In the preceding example, V_{MID} is provided to the device from a highly accurate external voltage source. But what happens when the V_{MID} reference is generated from an on-chip reference circuit which itself has a DC offset? Typically there is a separate specification for the V_{MID} voltage in such cases; the input of the DUT should be connected to the V_{MID} voltage, if it is possible to do so, and the output offsets are then specified relative to the V_{MID} voltage rather than the ideal value.

Thus the inputs and outputs are treated as if V_{MID} was exactly correct. Any errors in the V_{MID} voltage are evaluated using a separate V_{MID} DC voltage test. In this manner, DC offset errors caused by the single-ended to differential converter can be distinguished from errors in the V_{MID} reference voltage. This extra information may prove to be very useful to design engineers who must decide what needs to be corrected in the design.

3.6.5 Input Offset Voltage ($V_{IN,OS}$)

Input or input-referred offset voltage ($V_{IN,OS}$) refers to the negative of the voltage that must be applied to the input of a circuit in order to restore the output voltage to a desired reference level, that is, analog ground or V_{MID}. If an amplifier requires a +10-mV input to be applied to its input to force the output level to analog ground, then $V_{IN,OS} = -10$ mV. It is common in the literature to find $V_{IN,OS}$ defined as the output offset $V_{O,OS}$ divided by the measured gain G of the circuit:

$$V_{IN,\,OS} = \frac{V_{O,\,OS}}{G} \tag{3.5}$$

If an amplifier has a gain of 10 V/V and its output has an output offset of 100 mV, then its input offset voltage is 10 mV. This will always be true, provided that the values used in Eq. (3.5) are derived from the circuit in its linear region of operation. In high-gain circuits, such as an open-loop op amp, it is not uncommon to find the amplifer in a saturated state when measuring the output offset voltage. As such, Eq. (3.5) is not applicable and one must resort to a different technique, as will be explained shortly.

3.7 DC GAIN MEASUREMENTS

3.7.1 Closed-Loop Gain

Closed-loop DC gain is one of the simplest measurements to make, because the input–output signals are roughly comparable in level. Closed-loop gain, denoted G, is defined as the slope of the amplifier input-output transfer characteristic, as illustrated in Figure 3.14. We refer to this gain as closed-loop because it typically contrived from a set of electronic devices configured in a negative feedback loop. It is computed by simply dividing the change in output level of the amplifier or circuit by the change in its input

$$G = \frac{\Delta V_O}{\Delta V_I} \tag{3.6}$$

DC gain is measured using two DC input levels that fall inside the linear region of the amplifier. This latter point is particularly important, because false gain values are often obtained when the amplifier is unknowingly driven into saturation by poorly chosen input levels. The range of linear operation should be included in the test plan.

Gain can also be expressed in decibels (dB). The conversion from volt-per-volt to decibels is simply

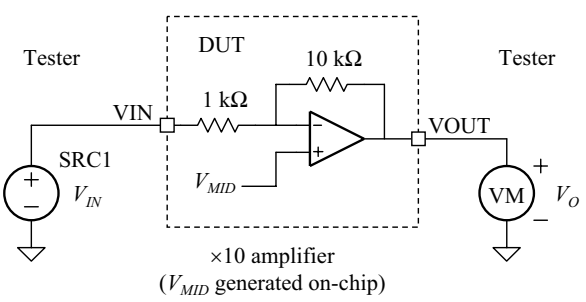
$$G\big|_{\text{dB}} = 20\log_{10}|G| \tag{3.7}$$

The logarithm function in Eq. (3.7) is a base-10 log as opposed to a natural log.

EXAMPLE 3.5

An amplifier with an expected gain of –10 V/V is shown in Figure 3.17. Both the input and output levels are referenced to an internally generated voltage V_{MID} of 1.5 V. SRC1 is set to 1.4 V and an output voltage of 2.51 V is measured with a voltmeter. Then SRC1 is set to 1.6 V and an output voltage of 0.47 V is measured. What is the DC gain of this amplifier in V/V? What is the gain in decibels?

Figure 3.17. A ×10 amplifier gain test setup.



Solution:
The gain of the amplifier is computed using Eq. (3.5) as

$$G = \frac{2.51\ \text{V} - 0.47\ \text{V}}{1.4\ \text{V} - 1.6\ \text{V}} = -10.2\ \text{V/V}$$

or, in terms of decibels

$$G = 20\log_{10}\left|-10.2\right| = 20.172\ \text{dB}$$

Gain may also be specified for circuits with differential inputs and/or outputs. The measurement is basically the same.

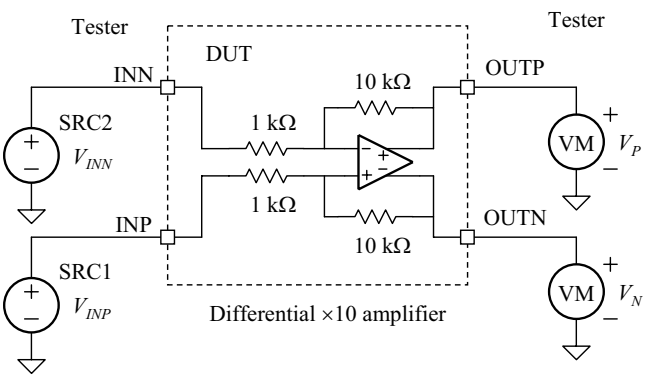
EXAMPLE 3.6

A fully differential amplifier with an expected gain of +10 V/V is shown in Figure 3.18. SRC1 is set to 1.6 V and SRC2 is set to 1.4 V. This results in a differential input of 200 mV. An output voltage of 2.53 V is measured at OUTP, and an output voltage of 0.48 V is measured at OUTN. This results in a differential output of 2.05 V. Then SRC1 is set to 1.4 V and SRC2 is set to 1.6 V. This results in a differential input level of –200 mV. An output voltage of 0.49 V is measured at OUTP, and an output voltage of 2.52 V is measured at OUTN. The differential output voltage is thus –2.03 V. Using the measured data provided, compute the differential gain of this circuit.

Solution:
The differential gain is found using Eq. (3.5) to be

$$G = \frac{2.05\ \text{V} - 2.03\ \text{V}}{200\ \text{mV} - \left(-200\ \text{mV}\right)} = +10.2\ \text{V/V}$$

Figure 3.18. Differential ×10 amplifier gain test setup.



Differential measurements can be made by measuring each of the two output voltages individually and then computing the difference mathematically. Alternatively, a differential voltmeter can be used to directly measure differential voltages. Obviously the differential voltmeter approach will work faster than making two separate measurements. Therefore, the use of a differential voltmeter is the preferred technique in production test programs. Sometimes the differential voltage is very small compared to the DC offset of the two DUT outputs. A differential voltmeter can often give more accurate readings in these cases.

In cases requiring extreme accuracy, it may be necessary to measure the input voltages as well as the output voltages. The DC voltage sources in most ATE testers are well calibrated and stable enough to provide a voltage error no greater than 1 mV in most cases. If this level of error is unacceptable, then it may be necessary to use the tester's high-accuracy voltmeter to measure the exact input voltage levels rather than trusting the sources to produce the desired values. The gain equation in the previous example would then be

$$G = \frac{2.05\ \text{V} - 2.03\ \text{V}}{V_1 - V_2}$$

where V_1 and V_2 are the actual input voltages measured using a differential voltmeter.

Exercises

3.9.	Voltages of 0.8 and 4.1 V appear at the output of a single-ended amplifier when an input of 1.4 and 1.6 V is applied, respectively. What is the gain of the amplifier in V/V? What is the gain in decibels?	ANS. +16.5 V/V, 24.35 dB.
3.10.	An amplifier is characterized by $V_{OUT} = 2.5\ V_{IN} + 1$ over an output voltage range of 0 to 10 V. What is the amplifier output for a 2-V input? Similarly for a 3-V input? What is the corresponding gain of this amplifier in V/V for a 1-V input change? What is the gain in decibels?	ANS. 6 V, 8.5 V, +2.5 V/V, 7.96 dB.
3.11.	An amplifier is characterized by $V_{OUT} = 2.5\ V_{IN} + 0.25\ V_{IN}^2 + 1$ over an output voltage range of 0 to 12 V. What is the amplifier output for a 2-V input? Similarly for a 3-V input? What is the corresponding gain of this amplifier in V/V for a 1-V input change? What is the gain in decibels? Would a 4-V input represent a valid test point?	ANS. 7 V, 10.75 V, +3.75 V/V, 11.48 dB, No—the output would exceed 12 V.

The astute reader may have noticed that the gain and impedance measurements are fairly similar, in that they both involve calculating a slope from a DC transfer characteristic pertaining to the DUT. Moreover, they do not depend on any value for the offsets, only that the appropriate slope is obtained from the linear region of the transfer characteristic.

3.7.2 Open-Loop Gain

Open-loop gain (abbreviated G_{ol}) is a basic parameter of op amps. It is defined as the gain of the amplifier with no feedback path from output to input. Since many op amps have G_{ol} values of 10,000 V/V or more, it is difficult to measure open-loop gain with the straightforward techniques

of the previous examples. It is difficult to apply a voltage directly to the input of an open-loop op amp without causing it to saturate, forcing the output to one power supply rail or the other. For example, if the maximum output level from an op amp is ±5 V and its open-loop gain is equal to 10,000 V/V, then an input-referred offset of only 500 μV will cause the amplifier output to saturate. Since many op amps have input-referred offsets ranging over several millivolts, we cannot predict what input voltage range will result in unsaturated output levels.

We can overcome this problem using a second op amp connected in a feedback path as shown in Figure 3.19. The second amplifier is known as a *nulling amplifier*. The nulling amplifier forces its differential input voltage to zero through a negative feedback loop formed by resistor string R_2 and R_1, together with the DUT op amp. This loop is also known as a servo loop.[2] By doing so, the output of the op amp under test can be forced to a desired output level according to

$$V_{O,DUT} = 2V_{MID} - V_{SRC1} \tag{3.8}$$

where V_{MID} is a DC reference point (grounded in the case of dual-supply op amps, non-grounded for single-supply op amps) and V_{SRC1} is the programmed DC voltage from SRC1. The nulling amplifier and its feedback loop compensate for the input-referred offset of the DUT amplifier. This ensures that the DUT output does not saturate due to its own input-referred offset.

The two matched resistors, R_3, are normally chosen to be around 100 kΩ as a compromise between source loading and op-amp bias-induced offsets. Since the gain around the loop is extremely large, feedback capacitor C is necessary to stabilize the loop. A capacitance value of 1 to 10 nF is usually sufficient. R_{LOAD} provides the specified load resistance for the G_{ol} test.

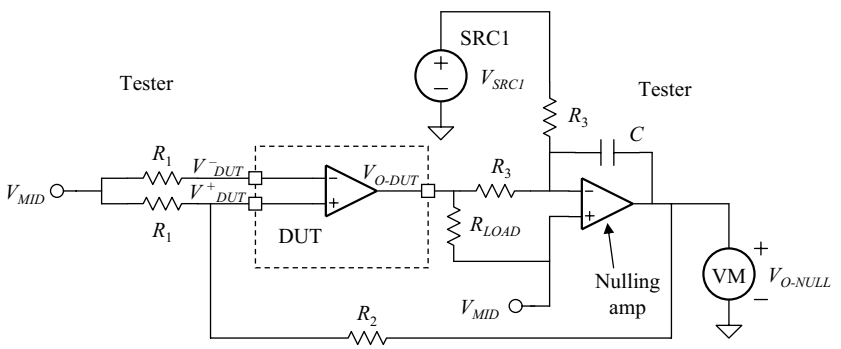
Under steady-state conditions, the signal that is fed back to the input of the DUT amplifier denoted $V_{IN,DUT}$ is directly related to the nulling amplifier output $V_{O\text{-}NULL}$ according to

$$V_{IN,DUT} = V^{+}_{IN,DUT} - V^{-}_{IN,DUT} = \frac{R_1}{R_1 + R_2}\left(V_{O,NULL} - V_{MID}\right) \tag{3.9}$$

where $V^{+}_{IN,DUT}$ and $V^{-}_{IN,DUT}$ are the positive and negative inputs to the DUT amplifier, respectively. Subsequently, the open-loop voltage gain of the DUT amplifier is found from Eqs. (3.6), (3.8), and (3.9) to be given by

$$G_{ol} = \frac{\Delta V_{O,DUT}}{\Delta V_{IN,DUT}} = -\left(\frac{R_1 + R_2}{R_1}\right)\frac{\Delta V_{SRC1}}{\Delta V_{O,NULL}} \tag{3.10}$$

Figure 3.19. Open-loop gain test setup using a nulling amplifier.



The nulling loop method allows the test engineer to force two desired outputs and then indirectly measure the tiny inputs that caused those two outputs. In this manner, very large gains can be measured without measuring tiny voltages. Of course the accuracy of this approach depends on accurately knowing the values of R_1 and R_2, as well as on by selecting the two resistors labeled as R_3 in Figure 3.19 very nearly identical values (i.e., matched conditions).

In order to maximize the signal handling capability of the test setup shown in Figure 3.19, as well as avoid saturating the nulling amplifer, it is a good idea to set the voltage divider ratio to a value approximately equal to the inverse of the expected open-loop gain of the DUT op amp

$$\frac{R_1}{R_1 + R_2} \approx \frac{1}{G_{ol}} \tag{3.11}$$

from which we can write $R_2 \approx G_{ol} R_1$.

EXAMPLE 3.7

For the nulling amplifier setup shown in Figure 3.19 with R_1 = 100 Ω, R_2 = 100 kΩ, and R_3 = 100 kΩ, together with V_{MID} set to a value midway between the two power supply levels (its actual value is not important because all signals will be referenced to it), SRC1 is set to V_{MID} + 1 V and a voltage of V_{MID} + 2.005 V is measured at the nulling amplifier output. SRC1 is set to V_{MID} – 1 V and a voltage of V_{MID} + 4.020 V is measured at the nulling amplifier output. What is the open-loop gain of the amplifier?

Solution:

Open-loop gain is calculated using the following procedure. First the change or swing in the nulling amplifier output $\Delta V_{O,NULL}$ is computed

$$\Delta V_{O,NULL} = 2.005 \text{ V} - 4.020 \text{ V} = -2.015 \text{ V}$$

Then, using Eq. (3.9), the voltage swing at the input of the DUT amplifier, $\Delta V_{IN,DUT}$, is calculated

$$\begin{aligned} \Delta V_{IN,DUT} &= \frac{R_1}{R_1 + R_2} \Delta V_{O,NULL} \\ &= \frac{100}{100 + 100\text{k}} (-2.015 \text{ V}) \\ &= -2.013 \text{ mV} \end{aligned}$$

Making use of the fact that ΔV_{SRC1} is 2 V, which forces $\Delta V_{O,DUT}$ = –2 V, the open-loop gain of the amplifier is found to be

$$G_{ol} = \frac{\Delta V_{O,DUT}}{\Delta V_{IN,DUT}} = \frac{-2 \text{ V}}{-2.013 \text{ mV}} = 993.5 \text{ V/V}$$

If the op amp in the preceding example had an open-loop gain closer to 100 V/V instead of 1000 V/V, then the output of the nulling amplifier would have produced a voltage swing of 20 V instead of 2 V. The nulling amplifier would have been dangerously close to clipping against its output voltage rails (assuming ±15-V power supplies). In fact, if a 5-V op amp were used as the nulling amplifier, it would obviously not be able to produce the 20-V swing.

In the example, the nulling amplifier should have produced two voltages centered around V_{MID}. Instead, it had an average or common-mode offset level of approximately 3 V from this value. A detailed circuit analysis reveals that this offset is caused exclusively by the input-referred offset of the DUT. Hence, the offset that appears at the output of the nulling amplifier, denoted $V_{O,NULL,OS}$, can be used to compute the input-referred offset of the DUT, $V_{IN,DUT,OS}$. Input-referred offset would then be calculated using

$$V_{IN,DUT,OS} = \frac{R_1}{R_1 + R_2} V_{O,NULL,OS} \tag{3.12}$$

Exercises

3.12. For the nulling amplifier setup shown in Figure 3.19 with R_1 = 100 Ω, R_2 = 100 kΩ, and R_3 = 100 kΩ, an SRC1 voltage swing of 1 V results in a 2.3-V swing at the output of the nulling amplifier. What is the open-loop gain in V/V of the DUT amplifier? What is the gain in decibels?

ANS. 435.2 V/V, 52.77 dB.

3.13. For the nulling amplifier setup shown in Figure 3.19 with R_1 = 1 kΩ, R_2 = 100 kΩ, and R_3 = 100 kΩ, an offset of 2.175 V + V_{MID} appears at the output of the nulling op amp when the SRC1 voltage is set to V_{MID}. What is the input offset of the DUT amplifier?

ANS. 21.5 mV.

3.14. For the nulling amplifier setup shown in Figure 3.19 with R_1 = 100 Ω, R_2 = 500 kΩ, and R_3=100 kΩ, and the DUT op amp having an open-loop gain of 4000 V/V, what is the output swing of the nulling amplifier when the SRC1 voltage swings by 1 V?

ANS. 1.25 V.

Because this method involves the same measured data used to compute the open-loop gain, it is a commonly used method to determine the op amp input-referred offset. For the parameters and measurement values described in Example 3.7, the input-referred offset voltage for the DUT is

$$V_{IN,DUT,OS} = \frac{100\ \Omega}{100\ \Omega + 100\ \text{k}\Omega}\left(\frac{4.020\ \text{V} + 2.005\ \text{V}}{2}\right)$$
$$= 3.0\ \text{mV}$$

3.8 DC POWER SUPPLY REJECTION RATIO

3.8.1 DC Power Supply Sensitivity

Power supply sensitivity (PSS) is a measure of the circuit's dependence on a constant supply voltage. Normally it is specified separately with respect to the positive or negative power supply

voltages and denoted PSS^+ and PSS^-. PSS is defined as the change in the output over the change in either power supply voltage with the input held constant

$$PSS^+ \equiv \left.\frac{\Delta V_O}{\Delta V_{PS^+}}\right|_{V_{in}\ \text{constant}} \quad \text{and} \quad PSS^- \equiv \left.\frac{\Delta V_O}{\Delta V_{PS^-}}\right|_{V_{in}\ \text{constant}} \tag{3.13}$$

In effect, PSS is a type of gain test in which the input is one of the power supply levels.

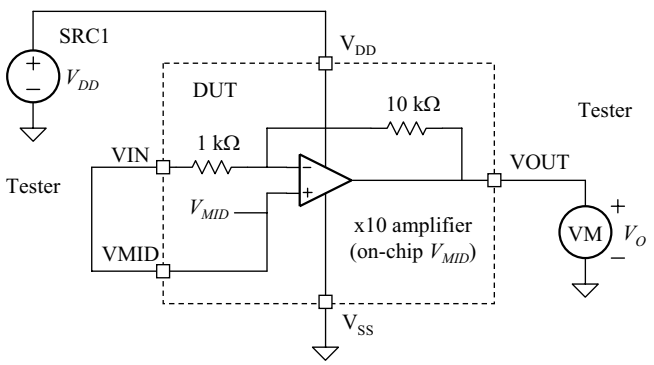
EXAMPLE 3.8

The input of the ×10 amplifier in Figure 3.20 is connected to its own V_{MID} source forcing 1.5 V. The power supply is set to 3.1 V and a voltage of 1.5011 V is measured at the output of the amplifier. The power supply voltage is then changed to 2.9 V and the output measurement changes to 1.4993 V. What is the PSS of the amplifier in V/V? What is the PSS in decibels?

Solution:
As the positive power supply (V_{DD}) is being changed by SRC1, the positive power supply sensitivity is

$$PSS^+ = \frac{\Delta V_0}{\Delta V_{SRC1}} = \frac{1.5011\ \text{V} - 1.4993\ \text{V}}{3.1\ \text{V} - 2.9\ \text{V}} = 9\ \text{mV/V} = -40.92\ \text{dB}$$

Figure 3.20. Power supply sensitivity test setup.



3.8.2 DC Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) is defined as the power supply sensitivity of a circuit divided by the magnitude of the closed-loop gain of the circuit in its normal mode of operation. Normally it is specified separately with respect to each power supply voltage. Mathematically, we write

$$PSRR^+ \equiv \frac{PSS^+}{|G|} \quad \text{and} \quad PSRR^- \equiv \frac{PSS^-}{|G|} \tag{3.14}$$

In Example 3.8, we found $PSS^+ = 0.009$ V/V. In Example 3.5, the DC gain of this same circuit was found to be –10.2 V/V. Hence the $PSRR^+$ would be

$$\text{PSRR}^+ = \frac{\text{PSS}^+}{|G|} = \frac{0.009 \text{ V/V}}{10.2 \text{ V/V}} = 882 \ \mu\text{V/V}$$

Power supply rejection ratio is often converted into decibel units

$$\text{PSRR}^+\big|_{\text{dB}} = 20\log_{10}(882 \ \mu\text{V/V}) = -61.09 \text{ dB}$$

3.9 DC COMMON-MODE REJECTION RATIO

3.9.1 CMRR of Op Amps

Common-mode rejection ratio (CMRR) is a measurement of a differential circuit's ability to reject a common-mode signal $V_{IN,CM}$ at its inputs. It is defined as the magnitude of the common-mode gain G_{CM} divided by the differential gain G_D, given by

$$\text{CMRR} \equiv \left| \frac{G_{CM}}{G_D} \right| \tag{3.15}$$

This expression can be further simplified by substituting for the common-mode gain $G_{CM} = \Delta V_{O,CM} / \Delta V_{IN,CM}$, together with the definition for input-referred offset voltage defined in Eq. (3.5), as follows:

$$\text{CMRR} = \left| \frac{\Delta V_{O,CM} / \Delta V_{IN,CM}}{G_D} \right| = \left| \frac{\Delta V_{O,CM} / G_D}{\Delta V_{IN,CM}} \right| = \left| \frac{\Delta V_{IN,OS}}{\Delta V_{IN,CM}} \right| \tag{3.16}$$

The rightmost expression suggests the simplest procedure to measure CMRR; one simply measures $\Delta V_{IN,OS}$ subject to a change in the input common-mode level $\Delta V_{IN,CM}$. One can measure $\Delta V_{IN,OS}$ directly or indirectly, as the following two examples illustrate.

EXAMPLE 3.9

Figure 3.21 shows a simple CMRR test fixture for an op amp. The test circuit is basically a difference-amplifier configuration with the two inputs tied together. V_{MID} is set to 1.5 V and an input common-mode voltage of 2.5 V is applied using SRC1. An output voltage of 1.501 V is measured at the output of the op amp. Then SRC1 is changed to 0.5 V and the output changes to 1.498 V. What is the CMRR of the op amp?

Solution:

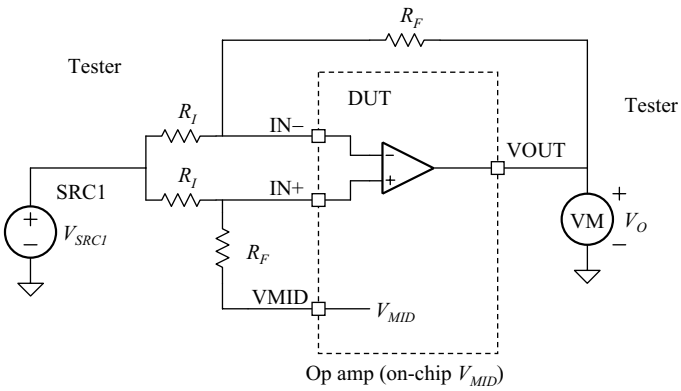
As the measurement was made at the output of the circuit, we need to infer from these results the $\Delta V_{IN,OS}$ for the op amp. This requires a few steps: The first is to find the influence of the op amp

input-referred offset voltage $V_{IN,OS}$ on the test circuit output. As in Section 3.7.2, detailed circuit analysis reveals

$$V_O = \frac{R_I + R_F}{R_I} V_{IN,OS}$$

With all resistors equal and perfectly matched, $V_O = 2\ V_{IN,OS}$. Hence, $\Delta V_O = 2\ \Delta V_{IN,OS}$, or, when re-arranged, $\Delta V_{IN,OS} = 0.5\ \Delta V_O$. Subsequently, substituting measured values $\Delta V_O = 1.501$ V–1.498 V = 3 mV, we find $\Delta V_{IN,OS} = 1.5$ mV. This result can now be substituted into Eq. (3.16), together with $\Delta V_{IN,CM} = \Delta V_{SRC1} = 2.5$ V – 0.5 V = 2.0 V, leading to a CMRR = 750 μV/V or –62.5 dB.

Figure 3.21. Op-amp CMRR test setup.



There is one major problem with this technique for measuring op amp CMRR: The resistors must be known precisely and carefully matched. A CMRR value of –100 dB would require resistor matching to 0.0001%, an impractical value to achieve in practice. A better test circuit setup is the nulling amplifier configuration shown in Figure 3.22. This configuration is very similar to the one used previously to measure the open-loop gain and input offsets of Section 3.7. The basic circuit arrangement is identical, only the excitation and the position of the voltmeter are changed. With this test setup, one can vary the common-mode input to the DUT and measure the differential voltage between the input SRC1 and the nulling amplifier output, which we shall denote as $V_{O,NULL}$. This, in turn, can then be used to deduce the input-referred offset for the DUT amplifier according to

$$V_{IN,DUT,OS} = \frac{R_1}{R_1 + R_2} V_{O,NULL} \tag{3.17}$$

Subsequently, the CMRR of the op amp is given by

$$\text{CMRR} = \frac{R_1}{R_1 + R_2} \left| \frac{\Delta V_{O,NULL}}{\Delta V_{SRC1}} \right| \tag{3.18}$$

EXAMPLE 3.10

For nulling amplifier setup shown in Figure 3.22 with R_1 = 100 Ω, R_2 = 100 k Ω, and R_3 = 100 k Ω, together with V_{MID} set to a value midway between the two power supply levels, SRC1 is set to +2.5 V and a differential voltage of 10 mV is measured between SRC1 and the output of the nulling amplifier. Then SRC1 is set to 0.5 V and the measured voltage changes to –12 mV. What is the CMRR of the op amp?

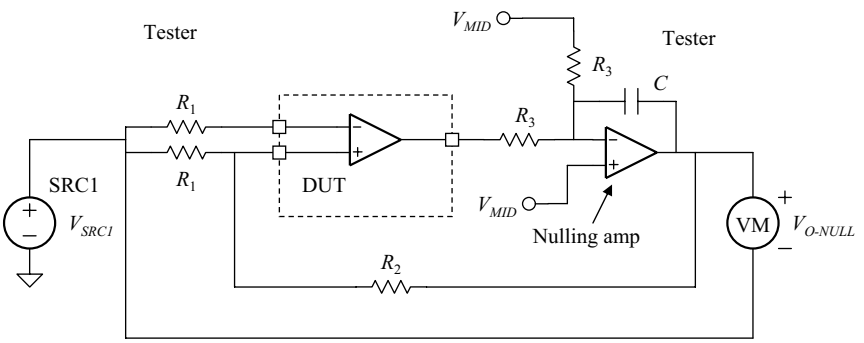
Solution:
Using Eq. (3.17), we deduce

$$\begin{aligned}\Delta V_{IN,DUT,OS} &= \frac{R_1}{R_1 + R_2}\Delta V_{O,NULL} \\ &= \frac{100}{100 + 100\text{k}}\left[10\text{ mV} - (-12\text{ mV})\right] \\ &= 22\ \mu\text{V}\end{aligned}$$

for a corresponding ΔV_{SRC1} = 2.5 V – 0.5 V, or 2.0 V. Thus the CMRR is

$$\text{CMRR} = \frac{22\ \mu\text{V}}{2.0\text{ V}} = 11\frac{\mu\text{V}}{\text{V}} = -99.17\text{ dB}$$

Figure 3.22. Op amp CMRR test setup using nulling amplifier.



3.9.2 CMRR of Differential Gain Stages

Integrated circuits often use op amps as part of a larger circuit such as a differential input amplifier. In these cases, the CMRR of the op amp is not as important as the CMRR of the circuit as a whole. For example, a differential amplifier configuration such as the one in Figure 3.21 may have terrible CMRR if the resistors are poorly matched, even if the op amp itself has a CMRR of –100 dB. The differential input amplifier CMRR specifications include not only the effects of the op amp, but also the effects of on-chip resistor mismatch. As such, we determine the CMRR using the original definition given in Eq. (3.15). Our next example will illustrate this.

EXAMPLE 3.11

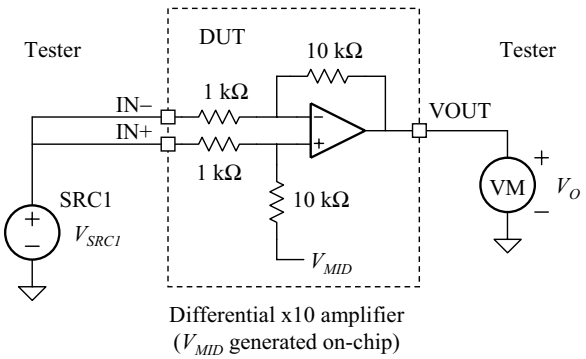
Figure 3.23 illustrates the test setup to measure the CMRR of a differential amplifier having a nominal gain of 10. No assumption about resistor matching is made. Both inputs are connected to a common voltage source SRC1 whose output is set to 2.5 V. A voltage of 1.501 V is measured at the output of the DUT. Then SRC1 is set to 0.5 V and a second voltage of 1.498 V is measured at the DUT output. Next the differential gain of the DUT circuit is measured using the technique described in Section 3.7.1. The gain was found to be 10.2 V/V. What is the CMRR?

Solution:

Since ΔV_O = 1.501 V – 1.498 V = 3 mV corresponding to a $\Delta V_{IN,CM} = \Delta V_{SRC1}$ = 2.0 V, the common-mode gain G_{CM} is calculated to be equal to 0.0015 V/V. In addition, we are told that the differential gain G_D is 10.2 V/V; thus we find the CMRR from the following:

$$\text{CMRR} = \left|\frac{G_{CM}}{G_D}\right| = \left|\frac{0.0015\,\text{V/V}}{10.2\,\text{V/V}}\right| = 0.000147 = -76.65\ \text{dB}$$

Figure 3.23. A ×10 differential amplifier CMRR test setup.



Exercises

3.15. An amplifier has an expected CMRR of –100 dB. For a 1-V change in the input common-mode level, what is the expected change in the input offset voltage of this amplifier?

ANS. 10 μV.

3.16. For the nulling amplifier CMRR setup in Figure 3.22 with R_1 = 100 Ω, R_2 = 500 kΩ, and R_3 = 100 kΩ, SRC1 is set to +3.5 V and a differential voltage of 210 mV is measured between SRC1 and the output of the nulling amplifier. Then SRC1 is set to 0.5 V and the measured voltage changes to –120 mV. What is the CMRR of the op amp in decibels?

ANS. 21.99 μV/V, –93.15 dB.

3.10 COMPARATOR DC TESTS

3.10.1 Input Offset Voltage

Input offset voltage for a comparator is defined as the differential input voltage that causes the comparator to switch from one output logic state to the other. The differential input voltage can be ramped from one voltage to another to find the point at which the comparator changes state. This switching point is, however, dependent on the input common-mode level. One usually tests for the input offset voltage under worst-case conditions as outlined in the device test plan.

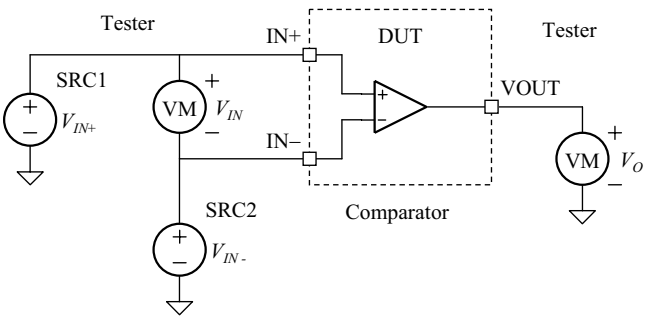
EXAMPLE 3.12

The comparator in Figure 3.24 has a worst-case input offset voltage of ±50 mV and a midsupply voltage of 1.5V. Describe a test setup and procedure with which to obtain its input offset voltage.

Solution:

The comparator in Figure 3.24 is connected to two voltage sources, SRC1 and SRC2. SRC2 is set to 1.5 V and SRC1 is ramped upward from 1.45 to 1.55 V, as the switching point is expected to lie within this range. When the output changes from logic LO to logic HI, the differential input voltage V_{IN} is measured, resulting in an input offset voltage reading of +5 mV. The V_{IN} voltage could be deduced by simply subtracting 1.5 V from the SRC1 voltage, assuming that the DC sources force voltages to an accuracy of a few hundred microvolts. This is usually a questionable assumption, however. It is best to measure small voltages using a voltmeter rather than assume the tester's DC sources are set to exact voltages.

Figure 3.24. Comparator input offset voltage test setup.

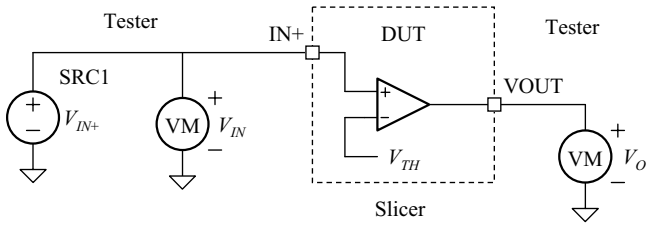


3.10.2 Threshold Voltage

Sometimes a fixed reference voltage is supplied to one input of a comparator, forming a circuit known as a *slicer*. The input offset voltage specification is typically replaced by a single-ended specification, called *threshold voltage*.

The slicer in Figure 3.25 is tested in a manner similar to that of the comparator circuit in the previous example. Assuming that the threshold voltage is expected to fall between 1.45 and 1.55 V, the input voltage from SRC1 is ramped upward from 1.45 to 1.55 V. The output switches states when the input is equal to the slicer's threshold voltage.

Figure 3.25. Slicer threshold voltage test setup.



Notice that threshold voltage will be affected by the accuracy of the on-chip voltage reference, V_{TH}. In theory, the threshold voltage should be equal to the sum of the slicer's reference voltage V_{TH} plus the input offset voltage of the comparator. Threshold voltage error is defined as the difference between the actual and ideal threshold voltages.

3.10.3 Hysteresis

In the comparator input offset voltage example, the output changed when the input voltage reached 5 mV. This occurred on a rising input voltage. On a falling input voltage, the threshold may change to a lower voltage. This characteristic is called *hysteresis*, and it may or may not be an intentional design feature. Hysteresis is defined as the difference in threshold voltage between a rising input test condition and a falling input condition.

EXAMPLE 3.13

The comparator in Figure 3.24 is connected to two voltage sources, SRC1 and SRC2. SRC2 is set to 1.5 V and SRC1 is ramped upward from 1.45 to 1.55 V in 1-mV steps. When the output changes from logic LO to logic HI, the differential input voltage is measured, resulting in an input offset voltage reading of +5 mV relative to SRC1. Then the input is ramped downward from 1.55 to 1.45 V and the output switches when the input voltage reaches –3 mV. What is the hysteresis of this comparator?

Solution:
The hysteresis is equal to the difference of the two input offset voltages

$$5\text{ mV} - (-3\text{ mV}) = 8\text{ mV}$$

It should be noted that input offset voltage and hysteresis may change with different common-mode input voltages. Worst-case test conditions should be determined during the characterization process.

Exercises

3.17.	A comparator has an input offset voltage of 50 mV and its positive terminal is connected to a 1-V level, at what voltage on the negative terminal does the comparator change state?	ANS. 0.950 V.
3.18.	A slicer circuit is connected to a 1.65 V reference V_{TH} and has a comparator input offset voltage of 11 mV. At what voltage level will the slicer change state?	ANS. 1.661 V.
3.19.	A comparator has a measured hysteresis of 9 mV and switches state on a rising input at 2.100 V. At what voltage does the comparator change to a low state on a falling input?	ANS. 2.091 V.

3.11 VOLTAGE SEARCH TECHNIQUES

3.11.1 Binary Searches Versus Step Searches

The technique of ramping input voltage levels until an output condition is met is called a *ramp search*, or *step search*. Step searches are time-consuming and not well suited for production testing. Instead, binary or linear search methods are often used.

To gain a better understanding of these methods, let us consider the general search process. In mathematical terms, let us we denote the input–output behavior of some device under test with some mathematical function, say $y = f(x)$, where x is the input and y the output. Subsequently, to establish the output at some arbitrary level, say $y = D$, we need to find the value of x that satisfies $f(x)–D = 0$. If the inverse of f is known, then we can immediately solve for input as $x = f^{-1}(D)$. Generally, $f(x)$ is not known, since it is specific to each and every device under test. However, through a source-measurement process, the behavior of $y = f(x)$ is encapsulated in the form of a look-up table or by the direct action of a measurement. Consequently, through some search process, we can identify the value of x that satisfies $f(x)–D = 0$. As x is a root of the equation $f(x)–D$, the procedures used to identify the root are known as root-finding algorithms. There are numerous root-finding algorithms, such as bisection (binary), secant (linear), false-position, and Newton-Raphson methods, to name just a few. Any one of these can be adapted to test. Let us begin by describing the binary search method.

To determine an input value such that the output equals a desired target value to within some tolerance, start with two input values. One value is selected such that the output is greater than some desired target value, while the other is selected to obtain an output less than this target value. Let us denote these two output conditions as $output\ @\ input_1$ and $output\ @\ input_2$. Subsequently, the binary search process can be described using the following pseudo code:

```
TARGET = desired value
Measure output @ input1
Measure output @ input2
output @ input3 =1000 # initialization
Do WHILE | output @ input3 - TARGET | ≥ tolerance value
   Set input3=(input1+input2)/2
   Measure output @ input3
   IF output @ input3 –TARGET is of opposite sign to output @ input1 – TARGET Do:
```

```
    Set input1=input1 and input2=input3
  ELSE
    Set input1=input3 and input2=input2
  ENDIF
END Do
```

A binary search can be applied to the comparator input offset voltage test described in the previous section. Instead of ramping the input voltage from 1.45 to 1.55 V, the comparator input is set half-way between to 1.5 V and the output is observed. If the output is high, then the input is increased by one-quarter of the 100-mV search range (25 mV) to try to make the output go low. If, on the other hand, the output is low, then the input is reduced by 25 mV to try to force the output high. Then the output is observed again. This time, the input is adjusted by one-eighth of the search range (12.5 mV). This process is repeated until the desired input adjustment resolution is reached.

The problem with the binary search technique is that it does not work well in the presence of hysteresis. The binary search algorithm assumes that the input offset voltage is the same whether the input voltage is increased or decreased. If the comparator exhibits hysteresis, then there are two different threshold voltages to be measured. To get around this problem without reverting to the time-consuming ramp search technique, a hybrid approach can be used. A binary search can be used to find the approximate threshold voltage quickly. Then a step search can be used with a much smaller search voltage range.

Another solution to the hysteresis problem is to use a modified binary search algorithm in which the output state of the comparator is returned to a known logic state between binary search approximations. This is achieved by forcing the input either well above or well below the threshold voltage. In this way, steps are always taken in one direction, avoiding hysteresis effects. To measure hysteresis, a binary search is used once with the output state forced high between approximations. Then the input offset is measured again with the output state forced low between approximations. The difference in input offset readings is equal to the hysteresis of the comparator.

3.11.2 Linear Searches

Linear circuits can make use of an even faster search technique called a *linear search*. A linear search is similar to the binary search, except that the input approximations are based on a linear interpolation of input–output relationships. For example, if a 0-mV input to a buffer amplifier results in a 10-mV output and a 1-mV input results in a 20-mV output, then a –1-mV input will probably result in a 0-mV output. The linear search algorithm keeps refining its guesses using a simple straight-line approximation $V_{OUT} = M \times V_{IN} + B$ algorithm until the desired accuracy is reached. The following example will help illustrate this method.

EXAMPLE 3.14

Using a linear search algorithm, find the input offset voltage V_{os} for a ×10 amplifier when the output referred offset voltage is 120 mV.

Solution:

The input to a ×10 amplifier is set to 0 V and the output is measured, yielding a reading of 120 mV. The gain M is known to be approximately 10, since this is supposed to be a ×10 amplifier.

The value of offset ***B*** can be approximately determined using the $V_{OUT} = M \times V_{IN} + B$ linear equation, that is,

$$120\ \text{mV} = M \times 0\ \text{mV} + B = 10 \times 0\ \text{mV} + B$$
$$\Rightarrow B = 120\ \text{mV (first-pass guess)}$$

Since 0 mV is the desired output, the next estimate for V_{OS} can be calculated using the linear equation again

$$0\ \text{mV (desired } V_{OUT}) = M \times V_{IN} + B = 10 \times V_{IN} + 120\ \text{mV}$$

Rewriting this equation to solve for V_{IN}, we get

$$V_{IN} = \frac{(0\ \text{mV} - 120\ \text{mV})}{10} = -12\ \text{mV}$$

Applying the best guess of –12 mV to the input, another output measurement is made, resulting in a reading of 8 mV. Now we have two equations in two unknowns

$$120\ \text{mV} = M \times 0\ \text{mV} + B$$
$$8\ \text{mV} = M\,(-12\ \text{mV}) + B$$

from which a more accurate estimate of ***M*** and ***B*** can be made. Solving for the two unknowns

$$M = \frac{120\ \text{mV} - 8\ \text{mV}}{0\ \text{mV} - (-12\ \text{mV})} = 9.333\ \text{V/V}$$
$$B = 10\ \text{mV} - \left[M\,(-12\ \text{mV})\right] = 122\ \text{mV}$$

The next input approximation should be close enough to the input offset voltage to produce an output of 0 mV, that is

$$V_{IN} = \frac{(0\ \text{mV} - \text{B})}{M} = \frac{(0\ \text{mV} - 122\ \text{mV})}{9.333} = -13.1\ \text{mV}$$

The input offset voltage of the ×10 amplifier is therefore +13.1 mV, assuming that the circuit is linear. The sign of the input-referred offset voltage is opposite to that found from the search process on account of the definition of offset voltage. In cases where the input–output relationship is not linear, the linear search technique will still work, but will require more iterations of the above process. For each iteration, two linear interpolations are performed using the two most recent input–output data points. This continues until the process converges to within the desired measurement resolution.

The procedure outline above is an example of the secant root finding method. We can easily generalize the principles described above to one involving the following set of iteration equations with pseudo code:

TARGET = desired value
k=1 # initialize iteration
Measure output @ $input_{k-1}$
Measure output @ $input_k$
output @ $input_{k+1}$ =1000 # initialization
Do WHILE | output @ $input_{k+1}$ – TARGET | ≥ tolerance value

$$Set\ \ input_{k+1} = input_k - (output\ @\ input_k - TARGET) \times \left(\frac{input_k - input_{k-1}}{output\ @\ input_k - output\ @\ input_{k-1}} \right)$$

Measure output @ $input_{k+1}$
k = k + 1
END Do

The reader is encouraged to investigate other root-finding procedures, such as the Newton–Raphson method, to see how well they can be adapted to the search process described above.

EXAMPLE 3.15

For an amplifier characterized by $V_{OUT} = 0.1 + 2.5V_{IN} + 0.01V_{IN}^2 + 0.001V_{IN}^3$ over a 1.0 – 4.0 V output voltage range, determine the input voltage that will establish the output voltage level at 3.00 V using a linear search process. How many search iterations are required for a maximum error of 1 mV? List the input values and corresponding output values as a function of each iteration.

Solution:
We begin by declaring the excitation-measurement process of the DUT as described by the mathematical equation:

$$f = 0.1 + 2.5V_{IN} + 0.01V_{IN}^2 + 0.001V_{IN}^3$$

Next, using a TARGET value of 3.0 V, we perform a linear search on the DUT to find the input voltage level V_{IN} such that the output equals the TARGET value. Beginning with $k = 1$, we declare

$$input_0 = 1.0,\ f(1.0) = 0.1 + 2.5(1.0) + 0.01(1.0)^2 + 0.001(1.0)^2 = 2.611$$

$$input_1 = 4.0,\ f(4.0) = 0.1 + 2.5(4.0) + 0.01(4.0)^2 + 0.001(4.0)^2 = 10.324$$

Next, we find the first update to the input level as follows:

$$\text{input}_2 = \text{input}_1 - \left[f\left(\text{input}_1\right) - \text{TARGET} \right] \times \left(\frac{\text{input}_1 - \text{input}_0}{f\left(\text{input}_1\right) - f\left(\text{input}_0\right)} \right)$$

$$= 4.0 - \left(10.324 - 3.0\right) \times \left(\frac{4.0 - 1.0}{10.324 - 2.611} \right) = 1.1513$$

and obtain the DUT output at this input level,

$$f\left(1.1513\right) = 0.1 + 2.5\left(1.1513\right) + 0.01\left(1.1513\right)^2 + 0.001\left(1.1513\right)^2 = 2.9930$$

As we are about 7 mV away from the target, but need to be less than 1 mV, we shall iterate again and find the next input level from

$$\text{input}_3 = \text{input}_2 - \left[f\left(\text{input}_2\right) - \text{TARGET} \right] \times \left(\frac{\text{input}_2 - \text{input}_1}{f\left(\text{input}_2\right) - f\left(\text{input}_1\right)} \right)$$

$$= 1.1513 - \left(2.9930 - 3.0\right) \times \left(\frac{1.1513 - 4.0}{2.9930 - 10.324} \right) = 1.1540$$

and

$$f\left(1.1540\right) = 0.1 + 2.5\left(1.1540\right) + 0.01\left(1.1540\right)^2 + 0.001\left(1.1540\right)^2 = 2.9998$$

Here we are less than 1 mV away from the targeted value of 3.00 V. Hence we stop the iteration at 2 with an input value of 1.1540 V.

Exercises

3.20. For an amplifier characterized by $V_{OUT} = 10V_{IN} - V_{IN}^2 + 5$ over a ±5 V output voltage range, determine the input offset voltage using a binary search process. The input offset voltage is known to fall between -464 and -496 mV. How many search iterations are required for a maximum error of 1 mV? List the input values and corresponding outputs.

ANS. A 32-mV search range with 2-mV resolution is required, requiring four binary iterations: (1) –480 mV, –30.4 mV; (2) –472 mV, +57 mV; (3) –476 mV, +13.4 mV; (4) –478 mV, –8.5 mV. The final estimate is thus –477 mV ($V_{IN,OS}$ = +477 mV; true answer is +477.2 mV).

3.21. Repeat Exercise 3.20 using a linear search process starting with two points at V_{IN} = –250 mV and –750 mV. How many iterations are required for < 1 mV error in $V_{IN,OS}$?

ANS. Two iterations produce estimates of $V_{IN,OS}$ = +471.6 mV and $V_{IN,OS}$ = +477.1 mV.

3.12 DC TESTS FOR DIGITAL CIRCUITS

3.12.1 I_{IH}/I_{IL}

The data sheet for a mixed-signal device usually lists several DC specifications for digital inputs and outputs. Input leakage currents (I_{IH} and I_{IL}) were discussed in Section 3.2.2. Input leakage is also specified for digital output pins that can be set to a high-impedance state.

3.12.2 V_{IH}/V_{IL}

The input high voltage (V_{IH}) and input low voltage (V_{IL}) specify the threshold voltage for digital inputs. It is possible to search for these voltages using a binary search or step search, but it is more common to simply set the tester to force these levels into the device as a go/no-go test. If the device does not have adequate V_{IH} and V_{IL} thresholds, then the test program will fail one of the digital pattern tests that are used to verify the DUT's digital functionality. To allow a distinction between pattern failures caused by V_{IH}/V_{IL} settings and patterns failing for other reasons, the test engineer may add a second identical pattern test that uses more forgiving levels for V_{IH}/V_{IL}. If the digital pattern test fails with the specified V_{IH}/V_{IL} levels and passes with the less demanding settings, then V_{IH}/V_{IL} thresholds are the likely failure mode.

3.12.3 V_{OH}/V_{OL}

V_{OH} and V_{OL} are the output equivalent of V_{IH} and V_{IL}. V_{OH} is the minimum guaranteed voltage for an output when it is in the high state. V_{OL} is the maximum guaranteed voltage when the output is in the low state. These voltages are usually tested in two ways. First, they are measured at DC with the output pin set to static high/low levels. Sometimes a pin cannot be set to a static output level due poor design for test considerations, so only a dynamic test can be performed. Dynamic V_{OH}/V_{OL} testing is performed by setting the tester to expect high voltages above V_{OH} and low voltages below V_{OL}. The tester's digital electronics are able to verify these voltage levels as the outputs toggle during the digital pattern tests. Dynamic V_{OH}/V_{OL} testing is another go/no-go test approach, since the actual V_{OH}/V_{OL} voltages are verified but not measured.

3.12.4 I_{OH}/I_{OL}

V_{OH} and V_{OL} levels are guaranteed while the outputs are loaded with specified load currents, I_{OH} and I_{OL}. The tester must pull current out of the DUT pin when the output is high. This load current is called I_{OH}. Likewise, the tester forces the I_{OL} current into the pin when the pin is low. These currents are intended to force the digital outputs closer to their V_{OH}/V_{OL} specifications, making the V_{OH}/V_{OL} tests more difficult for the DUT to pass. I_{OH} and I_{OL} are forced using a diode bridge circuit in the tester's digital pin card electronics. The diode bridge circuit is discussed in more detail in Chapter 2, "Tester Hardware."

3.12.5 I_{OSH} and I_{OSL} Short-Circuit Current

Digital outputs often include a current-limiting feature that protects the output pins from damage during short-circuit conditions. If the output pin is shorted directly to ground or to a power supply pin, the protection circuits limit the amount of current flowing into or out of the pin. Short-circuit current is measured by setting the output to a low state and forcing a high voltage (usually V_{DD}) into the pin. The current flowing into the pin (I_{OSL}) is measured with one of the tester's current meters. Then the output is set to a high state and 0 V is forced at the pin. The current flowing out of the pin (I_{OSH}) is again measured with a current meter.

3.13 SUMMARY

This chapter has presented only a few of the many DC tests and techniques that the mixed-signal test engineer will encounter. Several chapters or perhaps even a whole book could be devoted to highly accurate DC test techniques. However, this book is intended to address mixed-signal testing. Hopefully, the limited examples given in this chapter will serve as a solid foundation from which the test engineer can build a more diversified DC measurement skill set.

DC measurements are trivial to define and understand, but they can sometimes be excruciatingly difficult to implement. A DC offset of 100 mV is very easy to measure if the required accuracy is ±10 mV. On the other hand, if 1-μV accuracy is required, the test engineer may find this to be one of the more daunting test challenges in the entire project. The accuracy and repeatability requirements of seemingly simple tests like DC offset can present a far more challenging test problem than much more complicated AC tests.

Accuracy and repeatability of measurements is the subject of Chapter 5, following an introductory chapter on data analysis and probability in Chapter 4. This topic pertains to a wide variety of analog and mixed-signal tests. Much of a test engineer's time is consumed by accuracy and repeatability problems. These problems can be one of the most aggravating aspects of mixed-signal testing. The successful resolution of a perplexing accuracy problem can also be one of the most satisfying parts of the test engineer's day.

PROBLEMS

3.1. The output of a 10-V voltage regulator varies from 9.95 V under no-load condition to 9.34 V under a 10-mA maximum rated load current. What is its load regulation?

3.2. The output of a 5-V voltage regulator varies from 4.86 to 4.32 V when the input voltage is changed from 14 to 6 V under a maximum load condition of 10 mA. What is its line regulation?

3.3. A 9-V voltage regulator is rated to have a load regulation of 0.150 V for a maximum load current of 15 mA. Assuming a no-load output voltage of 8.9 V, what is the expected output voltage at the maximum load current?

3.4. A 6-V voltage regulator is rated to have a load regulation of 2% for a maximum load current of 20 mA. Assuming a no-load output voltage of 5.9 V, what is the worst-case output voltage at the maximum load current?

3.5. A voltage of 1.2 V is dropped across an input pin when a 100-μA current is forced into the pin. Subsequently, a 1.254-V level occurs when the current is increased to 200 μA. What is the input resistance?

3.6. The input pin of a device is characterized by the $i - v$ relationship: $i = 0.001\ v + 100$. What is the resistance seen looking into this pin?

3.7. Voltages of 1.2 and 3.3 V appear at the output of an amplfier when currents of –10 and +10 mA, respectively, are forced into its output. What is the output resistance?

3.8. The no-load output voltage of an amplifier is 4 V. When a 600-Ω load is attached to the output, the voltage drops to 3 V. What is the amplifier's output resistance?

3.9. For a ×10 amplifier characterized by $V_{OUT} = 10V_{IN} - V_{IN}^{\ 2} + 5$ over a ±5-V range, what are its input and output offset voltages?

3.10. A voltmeter introduces a measurement error of –5% while measuring a 1-V offset from an amplifier. What is the actual reading captured by the voltmeter?

3.11. A voltmeter with an input impedance of 500 kΩ is used to measure the DC output of an amplifier with an output impedance of 500 kΩ. What is the expected relative error made by this measurement?

3.12. A differential amplifier has outputs of 2.4 V (OUTP) and 2.7 V (OUTN) with its input set to a V_{MID} reference level of 2.5 V. What are the single-ended and differential offsets? The common-mode offset? (All offsets are to be measured with respect to V_{MID}.)

3.13. A perfectly linear amplifier has a measured gain of 9.8 V/V and an output offset of 1.2 V. What is the input offset voltage?

3.14. Voltages of 1.3 V and 10.3 V appear at the output of a single-ended amplifier when inputs of 110 mV and 1.3 V are applied, respectively. What is the gain of the amplifier in V/V? What is the gain in decibels?

3.15. An amplifier is characterized by $V_{OUT} = 3.5V_{IN} + 1$ over the input voltage range 0 to 5 V. What is the amplifier output for a 2-V input? Similarly for a 3-V input? What is the corresponding gain of this amplifier in V/V to a the 1-V swing centered around 2.5-V? What is the gain in decibels?

3.16. An amplifier is characterized by $V_{OUT} = 1.5V_{IN} + 0.35V_{IN}^2 + 1$ over the input voltage range 0 to 5 V. What is the amplifier output for a 1-V input? Similarly for a 3-V input? What is the corresponding gain of this amplifier in V/V to a signal with a 1-V swing centered at 1-V? What is the gain in decibels?

3.17. For the nulling amplifier setup shown in Figure 3.19 with R_1 = 100 Ω, R_2 = 200 kΩ, and R_3 = 50 kΩ, an SRC1 input swing of 1 V results in a 130-mV swing at the output of the nulling amplifier. What is the open-loop gain of the DUT amplifier in V/V? What is the gain in decibels?

3.18. For the nulling amplifier setup shown in Figure 3.19 with R_1 = 200 Ω, R_2 = 100 kΩ, and R_3 = 100 kΩ, and a V_{MID} of 2.5 V, an offset of 3.175 V (relative to ground) appears at the output of the nulling op amp when the input is set to V_{MID}. What is the input offset of the DUT amplifier?

3.19. For the nulling amplifier setup shown in Figure 3.19 with R_1 = 100 Ω, R_2 = 300 kΩ, and R_3 = 100 kΩ, and the DUT op amp having an open-loop gain of 1000 V/V, what is the output swing of the nulling amplifier when the input swings by 1 V?

3.20. The input of a ×10 amplifier is connected to a voltage source forcing 1.75 V. The power supply is set to 4.9 V and a voltage of 1.700 V is measured at the output of the amplifier. The power supply voltage is then changed to 5.1 V and the output measurement changes to 1.708 V. What is the PSS? What is the PSRR if the measured gain is 9.8 V/V?

3.21. For nulling amplifier CMRR setup shown in Figure 3.22 with R_1 = 100 Ω, R_2 = 300 kΩ, and R_3 = 100 k Ω, SRC1 is set to +3.5 V and a differential voltage of 130 mV is measured between SRC1 and the output of the nulling amplifier. Then SRC1 is set to 1.0 V and the measured voltage changes to –260 mV. What is the CMRR of the op amp in decibels?

3.22. An amplifier has an expected CMRR of −85 dB. For a 1-V change in the input common-mode level, what is the expected change in the input offset voltage of this amplifier?

3.23. A comparator has an input offset voltage of 6 mV and its negative terminal is connected to a 2.5-V level, at what voltage on the positive terminal does the comparator change state?

3.24. A slicer circuit is connected to a 2-V reference and has a threshold voltage error of 20 mV. At what voltage level will the slicer change state?

3.25. If a slicer's 2.5-V reference has an error of +100 mV and the comparator has an input offset of –10 mV, what threshold voltage should we expect?

3.26. A comparator has a measured hysteresis of 10 mV and switches state on a rising input at 2.5 V. At what voltage does the comparator change to a low state on a falling input?

3.27. For an amplifier characterized by $V_{OUT} = 6V_{IN} + 0.5V_{IN}^2 - 2$ over a ±1-V input voltage range, determine the input offset voltage using a linear search process, starting with two points at ±1 V. After how many iterations did the answer change by less than 1 mV? How many iterations would have been required using a binary search from –1 to +1 V?

3.28. For an amplifier characterized by $V_{OUT} = 0.1 + 2.5V_{IN} - 0.8V_{IN}^2$ over a 0.0 to 3.0-V output voltage range, determine the input voltage that will establish the output voltage level at 2.00 V using a linear search process. How many search iterations are required for a maximum error of 1 mV? List the input values and corresponding output as a function of each iteration.

REFERENCES

1. S. Chakravarty and P. J. Thadikaran, *Introduction to IDDQ Testing*, May 1997, Kluwer Academic Publishers, Boston, ISBN 0792399455.
2. Analog Devices application note,* *How to Test Basic Operational Amplifier Parameters*, Analog Devices, Inc., Norwood, MA, July 1982.

*The nulling amplifier/servo loop methods presented in this chapter were adapted from the referenced application note to allow compatiblity with single-supply op amps having a V_{MID} reference voltage. The technique has been presented with permission from Analog Devices, Inc.