Lab 3

Exercise:

1. Using **for** loop, write behavioral Verilog code to convert an N bit grey code into equivalent binary code.
2. Write and simulate the Verilog code for a 4-bit comparator using 2-bit comparators.
3. Write behavioral Verilog code for
    - an 8 to 1 multiplexer using **case** statement
    - a 2 to 1 multiplexer using the **if-else** statement.

Using the above modules write the hierarchical code for a 16 to 1 multiplexer.

Additional exercise:

1. Implement F(a,b,c,d) = a'b + ac' + abd' + bc'd using 8 to 1 multiplexer and write the Verilog code for the same.

Lab 4

Exercise:

1. Write and simulate the Verilog code for a BCD to Excess 3 code converter using 8 to 1 multiplexers and other necessary gates.
2. Write behavioral Verilog code for a 2 to 4 decoder with active low enable input and active high output using **case** statement. Using this, design a 4 to 16 decoder with active low enable input and active high output and write the Verilog code for the same.
3. Write behavioral Verilog code for 16 to 4 priority encoder using **for** loop.

Additional exercise:

1. Write behavioral Verilog code for a 3 to 8 decoder with active-high enable input and active high output using **for** loop. Using the 3 to 8 decoders above, design a 4 to 16 decoder and write the Verilog code for the same.