Lab 1

Exercise:

1. Write Verilog code to describe the following functions
   f1 =ac'+bc+b'c'
   f2 = (a+b'+c)(a+b+c')(a'+b+c')
   Check whether f1 and f2 in question 1 are functionally equivalent or not.
2. Simplify the following functions using K-map and implement the circuit using logic gates. Write Verilog code and simulate the circuit
   a) f(A,B,C,D) = ∑m(1,3,4,9,10,12) + D(0,2,5,11)
   b) f(A,B,C,D) = ∏M(6,9,10,11,12) + D(2,4,7,13)
3. Minimize the following expression using K-map and simulate using only NAND gates.
   f(A,B,C,D)= πM(2,6,8,9,10,11,14)

Additional exercise:

1. Minimize the following expressions using K-map and simulate using only NOR gates.
   f(A,B,C,D)= ∑m(0,1,2,5,8,9,10)

Lab 2

Exercise:

Write behavioral Verilog code to implement the following and simulate

1. Full adder
2. Four-bit adder/ subtractor
3. Single-digit BCD adder using a four-bit adder(s).

Additional exercise:

Write behavioral Verilog code to implement the following and simulate

1. 2-bit multiplier