Lab 5

Exercise:

1. Design and simulate a combinational circuit with external gates and a 4 to 16 decoder built using a decoder tree of 2 to 4 decoders to implement the functions below.
   F= ab'c + a'cd + bcd' , G=acd' + a'b'c and H=a'b'c' + abc + a'cd
2. Design and implement a full adder using 2 to 4 decoder(s) and other gates.
3. Design and simulate the circuit with 3 to 8 decoder(s) and external gates to implement the functions below.
   F(a, b, c, d)= Σm(2,4,7,9) G (a, b, c, d)= Σm (0,3,15) H(a, b, c, d)= Σm(0,2,10,12)

Additional exercise:

1. Design and implement an 8 to 1 multiplexer using 3 to 8 decoder and external gates.

Lab 6

Exercise:

1. Write behavioral Verilog code for a negative edge triggered T FF with asynchronous active low reset.
2. Write behavioral Verilog code for a positive edge-triggered JK FF with synchronous active high reset
3. Design and simulate the following counters
   a) 4-bit ring counter.
   b) 5 bit Johnson counter.