Lab 7

Exercise:

1. Design and simulate the following counters
   a) 4 bit synchronous up counter
   b) 3 bit synchronous up/down counter with a control input up/$\overline{down}$. If up/$\overline{down}$ = 1, then the circuit should behave as an up counter. If up/$\overline{down}$ = 0, then the circuit should behave as a down counter.

Lab 8

Exercise:

1. Write and simulate the Verilog code to swap the contents of two registers using multiplexers.
2. Simulate a simple processor that can perform the following functions:

Operation	**Function performed**
Load *Rx*, *Data*	$Rx \leftarrow Data$
Move *Rx*, *Ry*	$Rx \leftarrow [Ry]$
Add *Rx*, *Ry*	$Rx \leftarrow [Rx] + [Ry]$
Sub *Rx*, *Ry*	$Rx \leftarrow [Rx] - [Ry]$