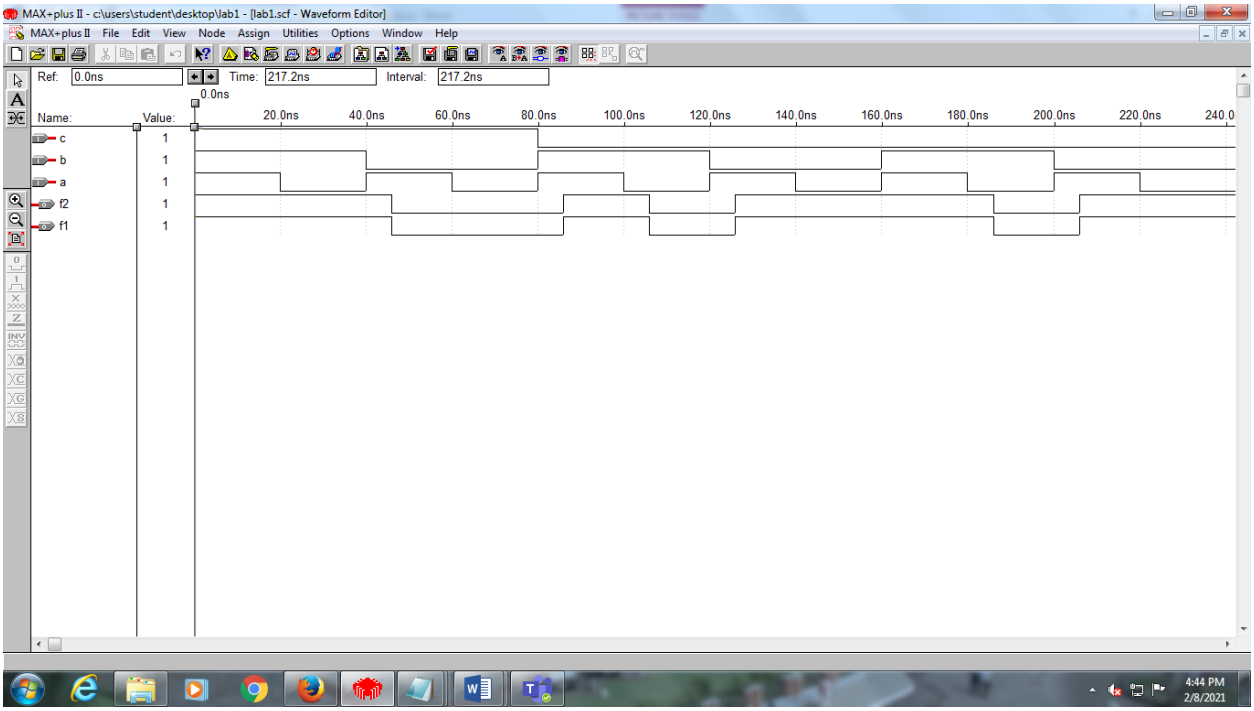
1: Write Verilog code to describe the following functions

f1 =ac'+bc+b'c'
f2 = (a+b'+c)(a+b+c')(a'+b+c')
Check whether f1 and f2 in question 1 are functionally equivalent or not.

Solution:

```
module lab1(a,b,c,f1,f2);
input a,b,c;
output f1,f2;
not(cnot, c);
and(x1,a,cnot);
and(x2,b,c);
not(bnot,b);
and(x3,bnot,cnot);
or(f1,x1,x2,x3);
not(anot,a);
or(y1,a,bnot,c);
or(y2,a,b,cnot);
or(y3,anot,b,cnot);
and(f2,y1,y2,y3);
endmodule
```



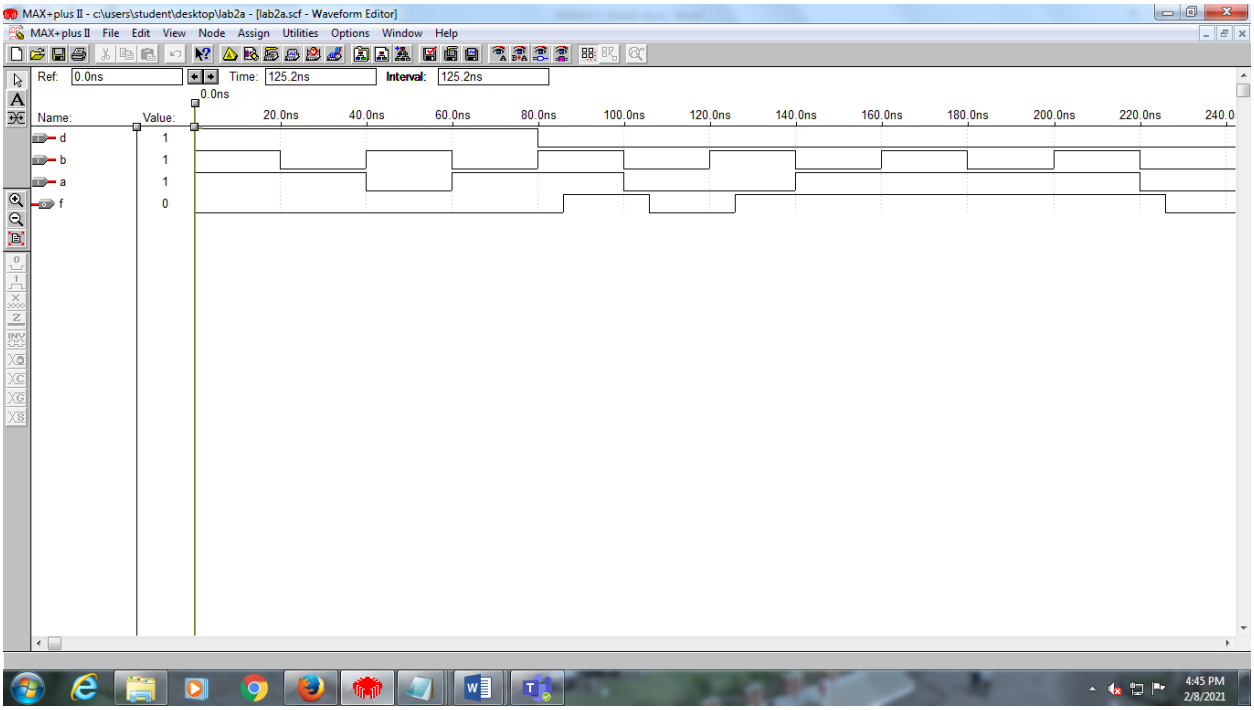

Both f1 and f2 are functionally equal.

2: Simplify the following functions using K-map and implement the circuit using logic gates.

a) f(A,B,C,D) = ∑m(1,3,4,9,10,12) + D(0,2,5,11)

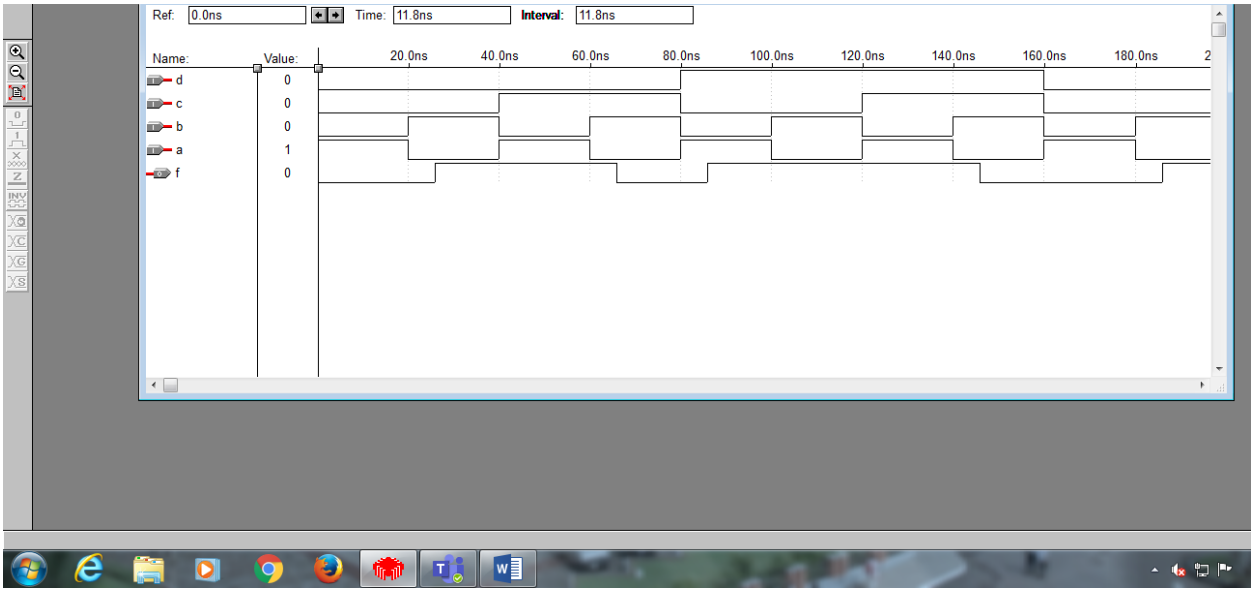
Solution:

```
module lab2a(a,b,d,f);
input a,b,d;
output f;
assign f=(~a&~b&d)|(b&~d)|(a&~d);
endmodule
```




b) f(A,B,C,D) = ∏M(6,9,10,11,12) + D(2,4,7,13)
Solution:

```
module lab2b(a,b,c,d,f);
input a,b,c,d;
output f;
assign f = (~b|~c|~d)&(~a|b|d)&(a|b|c)&(a|b|~d);
endmodule
```


Ref: 0.0ns
Time: 11.8ns
Interval: 11.8ns
Name:
Value:
20.0ns
40.0ns
60.0ns
80.0ns
100.0ns
120.0ns
140.0ns
160.0ns
180.0ns
d 0
c 0
b 0
a 1
f 0

3. Minimize the following expression using K-map and simulate using only NAND gates.
f(A,B,C,D) = πM(2,6,8,9,10,11,14)

Solution:

```
module lab3(a,b,c,d,f);
    input a,b,c,d;
    output f;
    assign f = ~(~(~(a&a)&b)&(~(~(c&c)&d)));
endmodule
```