Capital University of Science and Technology

Department of Computer Science

CS2523 – Computer Organization and Assembly Language

ASSIGNMENT NO. 2: Basics of Computer Organization and Assembly Language, Data Representation

CLO: 1. Define concepts in the design of microprocessor as state machine and designing its data path and its controller. [C1- Remembering]

CLO: 2. Describe how the basic units of the Intel 8088 architecture work together to represent Integer Numbers, Floating Numbers and register representation inside the microprocessor. [C2-Understanding]

Semester: Summer 22 **Max Marks:** 10

Instructor: Ms. Tayyaba Zaheer

Assigned Date: August 12, 2022 **Due Date:** August 17, 2022

Name: **Reg. No.**

Guidelines:

You are required to submit the **screenshots of code and output of the program (where required) and concepts in your own words i.e. must be hand written** in the assignment file (word or pdf – pictures attached must be readable and in portrait mode) as **courseCode_studentReg#_studenName** via Microsoft Teams.

Important Note:

1) Must not copy from other students, so do it all yourself.
2) Assignment should be hand written.

Objectives:

After completion of this Assignment, you will have gained basic knowledge of computer organization and assembly. You will be able to understand the instruction cycle. You will be able to understand the building blocks of assembly language.

Data Representation: Topic: Number Systems, and Conversion between Decimal, Binary, Hexadecimal, and other bases. **Related Reading:** Class Lectures.

Tools/Software Requirement (Optional):

1. Microsoft Word.
2. emu8086.

Important Note:

1) Must not copy from other students, so do it all yourself.

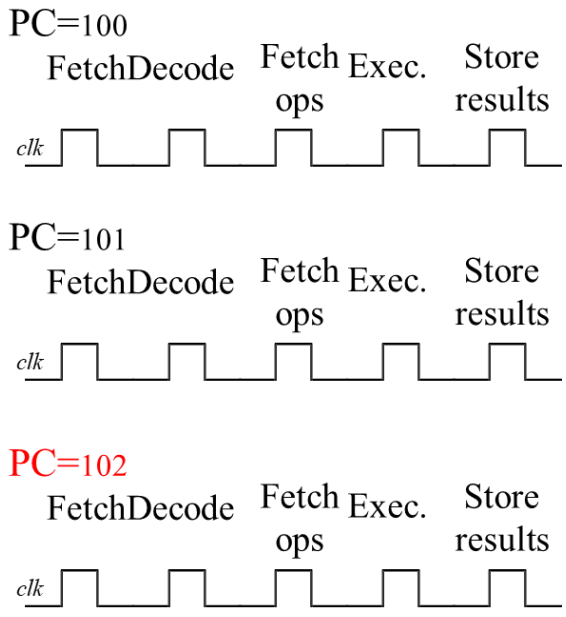
Description:

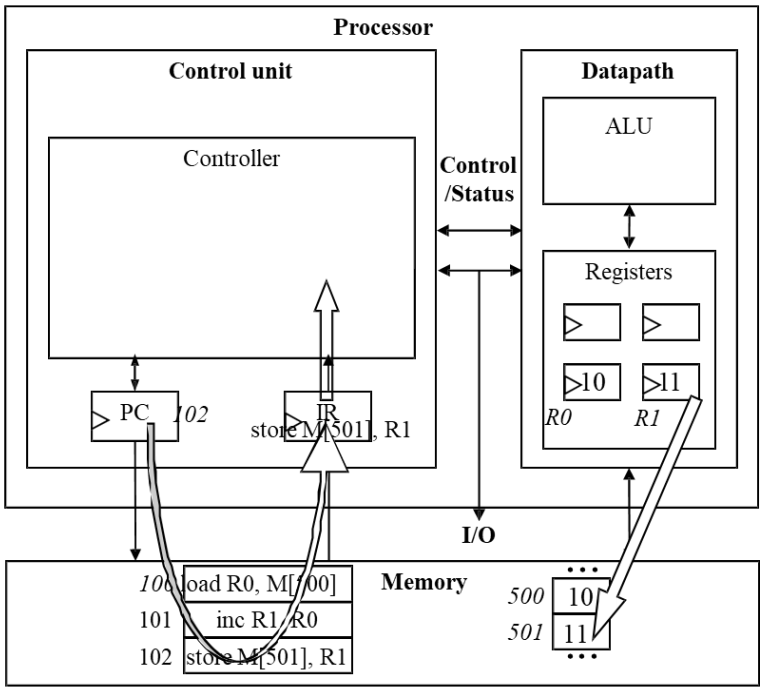
Emu8086 is an 8086-microprocessor emulator and disassembler. Emu8086 permits to assemble, emulate and debug 8086 programs (16bit/DOS).

Tasks:

Task#1: Instruction Cycle: **(02 marks)**

Question: Elaborate 5 sub-operations of the control unit in the given scenario of Instruction Cycle:





Solution:

i. **Fetch:**

Instruction at memory address 102 would be fetched in IR.

ii. **Decode:**

Instruction would be decoded on the basis of opcode.

iii. **Fetch Operands:**

This would not execute for the specified instruction.

iv. **Execute:**

This sub operation would not execute for the specified instruction.

v. **Store:**

Value of register R1 i.e. 11 would be stored in memory at location or address 501 in this sub operation.

Task#2: Data Representation: **(08 marks)**

Question 1 (02 marks): Perform the following operations and elaborate the state of Carry Flag after each operation:

a) **0000 – 0001**
b) **1111 + 0001**
c) **0111 + 0001**
d) **1000 – 0001**

Solution:

After a and b Carry flag is turned on. After c and d Carry flag is turned off [zero].

Question 2 (02 marks): Perform the following operations and elaborate the state of Overflow Flag after each operation:

a) **0100 + 0001**

b) **1100 + 1100**
c) **1000 + 1000**
d) **0100 + 0100**

Solution:
After a and b Overflow flag is turned off. After c and d Overflow flag is turned on.

Question 3 (1.5 marks): Convert -26 into 32-bit floating point representation:

Solution:
Follow procedure same as to convert -17 into 32-bit floating point representation (Given in the lecture slides). Answer should be 11000001110100000000000000000000.

Question 4 (1.5 marks): Convert 32-bit floating point representation 1 10000011 00010000000000000000000 to decimal:

Solution:
Follow procedure same as to convert 11000001110100000000000000000000 to decimal (Given in the lecture slides). Answer should be -17

Question 5 (01 mark): The address of var1 is 00400B20. The address of the next variable after var1 is 0040A06C. How many bytes are used by var1?

Solution:

0040A06C – 00400B20; (Hexadecimal subtraction)

$$\begin{array}{r} 0040A06C \\ -00400B20 \\ \hline 0000954C \end{array}$$

OR

Two's complement of 00400B20;

15 – 0 = 15 = F

15 – 2 = 13 = D

15 – B = 15 – 11 = 4

15 – 0 = F

15 – 0 = F

15 – 4 = 11 = B

15 – 0 = F

15 – 0 = F

FFBFF4DF + 1⇒

$$\begin{array}{r} FFBFF4DF \\ +00000001 \\ \hline FFBFF4E0 \end{array}$$

Two's complement of 00400B20 = $FFBFF4E0$

0040A06C – 00400B20 = 0040A06C + $FFBFF4E0$

$$\begin{array}{r} 0040A06C \\ +FFBFF4E0 \\ \hline 0000954C \end{array}$$