Capital University of Science and Technology
Department of Computer Science

CS 2523 – Computer Organization and Assembly Language

QUIZ NO. 1: Basics of Computer Organization and Assembly Language

Section# 4

CLO: 1. <u>Define</u> concepts in the design of microprocessor as state machine and designing its data path and its controller.

Semester: Fall 22		**Max Marks:** 10
Instructor: Ms. Tayyaba Zaheer	**Date:** October 10, 2022	**Max Time:** 10 Minutes
Name:	**Reg. No.**	

Question No.1 [03 Marks]

Write the following in the correct order of 5 levels of programmer's view of a computer: [You can only write numbers in order like ii, iii, vi…]

   i.   Assembly Language
   ii.   Application Programs High-Level Language
   iii.   Microarchitecture
   iv.   Digital Logic
   v.   Instruction Set Architecture
   vi.   Operating System

Solution:

ii, i, vi, v, iii, iv
ii. Application Programs High-Level Language,
i. Assembly Language,
vi. Operating System,
v. Instruction Set Architecture,
iii. Microarchitecture
iv. Digital Logic

Question No. 2 [03 Marks]

After the execution of the given instruction, the updated value of the ax register would be:

              inc ax, bx;   considering bx=11 and ax=0
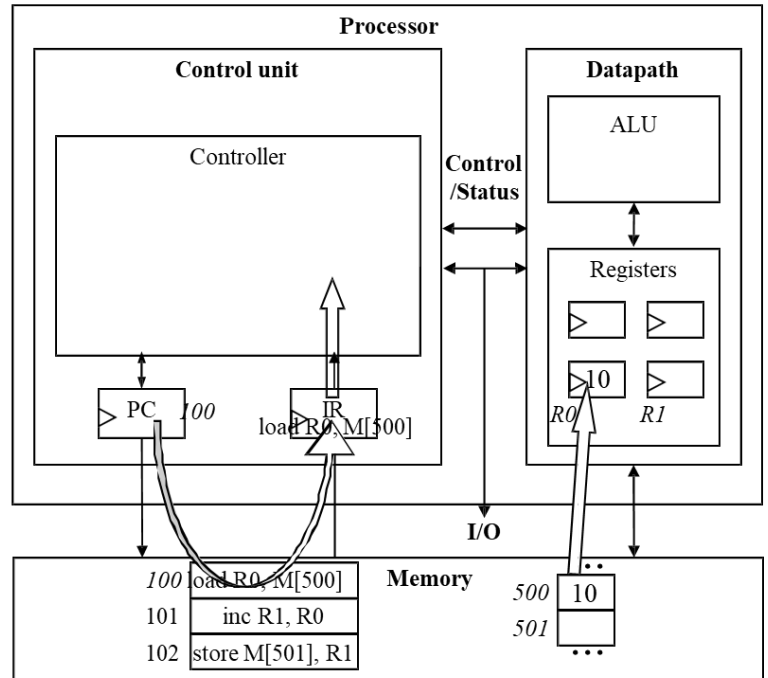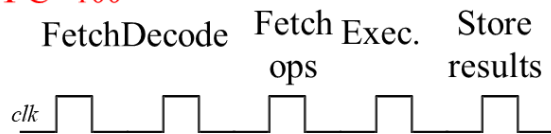
   i.   11
   ii.   10
   iii.   14
   iv.   12

Solution:

iv

Question No. 3 [04 Marks]

Elaborate 5 sub-operations of the control unit in the given scenario of Instruction Cycle:

PC=100

FetchDecode   Fetch   Exec.   Store
                ops   results

clk

Processor

Control unit   **Datapath**

                                        ALU

Controller   Control
                      /Status   Registers

PC   *100*   IR   R0   R1
          load R0, M[500]   10
                                  R0   R1

                        I/O

100 load R0, M[500]   **Memory**   *500* 10
101   inc R1, R0   *501*
102 store M[501], R1

Solution:

1. **Fetch:** Instruction at address 100 would be fetched from memory. Because PC has address of the instruction i.e. 100.
2. **Decode:** Instruction would be decoded by the control unit as per the opcode i.e. load (opcode means load data from memory to register). Control unit would set the controls as per the opcode of the instruction.
3. **Fetch Operands:** This sup operation would fetch data from address of memory 500 i.e. 10 to the register R0.
4. **Execute:** This sub operation would not be executed for this particular instruction as there is nothing to be executed by ALU.

5. **Store:** This sub operation would not be executed for this particular instruction as there is nothing to be stored back to memory in this instruction.