***LAB-1 Basic Circuit Components***

***Inverter Example (Transient analysis with loading c=0.02p) (15%)***

Edit Inverter SPICE, observe waveform, measure Delay time and Power consumption.

MOS transistor:

MP0 Drain Gate Source Body Mode-lname Length Width \*Multi-finger

MP0 outb in vdd vdd **pch**  L=0.1u W=0.5u \*M=2

(finger number: parallel-folded number)

Sizing: Taking inverter as example. We expect the circuit can perform with the same rising time and falling. Since the current driving capability of the PMOS is inferior to that of the NMOS (PMOS is inherently slower than NMOS), the width (W) ratio of the PMOS to the NMOS is usually 2:1. If the circuits are connected in series, the conducting path will become longer. In this case, the width size of the transistor should be increased according to the serial connected number. The width of the two serial connected transistor will be W\*2, the width of the three serial connected transistor will be W\*3, and so on.

Example: (inverter)

.subckt inv in out

mp0 out in vdd vdd pch l=0.1u w=1u

mn0 out in 0 0 nch l=0.1u w=0.5u

.ends

u: micro-meter. 

\*The following five points are the instructions you need for this experiment.

(1) Delay time Instruction: (rise represents for rising edge of signal, fall represents for falling edge of signal)

.meas tran delay trig v(in) val=0.6 rise=1 targ v(out) val=0.6 fall=1



meas: measure, tran: transient analysis, trig: trigger, targ: target, val: value.

(2)Power consumption Instruction:

.meas tran power avg power

(3)Power-Delay-Product instruction:

.meas tran pdp=param('power\*delay')

(4)Instruction to sweep MOS size:

.tran 0.1n 50n sweep w1 2u 25u 1u

w1 is the parameter which need to be swept.

Initial value: 2u, final value: 25u, step: 1u.

Sweep from 2u, 3u, 4u, 5u, 6u, 7u,.................24u, 25u.

Example: (PMOS:NMOS=5:1，sweep size=0.5u, 1u, 1.5u, 2u)

m1 out in vdd vdd pch l=0.1u w='5\*w1'

m2 out in 0 0 nch l=0.1u w=w1

.tran 0.1n 50n sweep w1 0.5u 2u 0.5u

(5)Input signal pattern instruction:

va a 0 pulse(1.2 0 0.1n 0.1n 0.1n 4.9n 10n)

vb b 0 pulse(1.2 0 0.1n 0.1n 0.1n 9.9n 20n)

vc c 0 pulse(1.2 0 0.1n 0.1n 0.1n 19.9n 40n)

vd d 0 pulse(1.2 0 0.1n 0.1n 0.1n 39.9n 80n)

.tran 0.1n 80n

***2-input NAND (Transient Analysis with loading c=0.02p) (20%)***

By following the steps in inverter LAB, try to edit the circuit of 2-input NAND in SPICE. Observe waveform, measure Delay time, Power consumption and Power-Delay-Product.

1. Size: PMOS W/L=2u/0.1 u, NMOS W/L=2u/0.1u (record the experimental data)

2. Sweep NMOS size=2u,3u,4u………20u (W of PMOS: NMOS= 1:1) (By using EXCEL file to analyze the trend of Delay time, Power consumption, and Power-Delay-Product as sizing varies.)

2-input NAND Example:

.subckt nand a b out

mp0 out a vdd vdd pch l=0.1u w=2u

mp1 out b vdd vdd pch l=0.1u w=2u

mn0 out a net 0 nch l=0.1u w=2u

mn1 net b 0 0 nch l=0.1u w=2u

.ends



***2-input NOR (Transient Analysis with loading c=0.02p) (20%)***

By following the steps in inverter LAB, try to edit the circuit of 2-input NAND in SPICE. Observe waveform, measure Delay time, Power consumption and Power-Delay-Product.

1. Size: PMOS W/L=4u/0.1u, NMOS W/L=1u/0.1u (record the experimental data)

2. Sweep NMOS size=2u,3u,4u………20u (W of PMOS: NMOS= 4:1) (By using EXCEL file to analyze the trend of Delay time, Power consumption, and Power-Delay-Product as sizing varies.)

2-input NOR：



**<LAB Experiment Report> (Due: 5/2)**

**SPICE code, waveform, data, Q&A, experience in this LAB.**

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**Questions (45%):**

1. **How to adjust the size of transistors to affect power and delay respectively?**
2. **When will be the minimal Power-Delay-Product in 2-NAND, 2-NOR?**
3. **What the Power and Delay difference between 2-NAND vs. 2-NOR?**