***eLAB-3 Various CMOS Logic Families***

Based on XOR circuit, analyze the circuit characteristics of three different Logic Families:

1. Observe the performance results in terms of power, delay, and pdp when the circuit is faced with different loadings under a fixed size.

2. Observe the performance results of the circuit in terms of power, delay, and pdp using different input frequencies under a fixed loading.

Using the same test pattern:

va a 0 pulse(1.8 0 0.1n 0.1n 0.1n 39.9n 80n)

vb b 0 pulse(1.8 0 0.1n 0.1n 0.1n 79.9n 160n)

vc c 0 pulse(1.8 0 0.1n 0.1n 0.1n 159.9n 320n)

.tran 0.1n 640n

※※When the frequency of input pattern increases, the time when pattern is logic "1" needs to be shortened at the same time.

EX: When the frequency of the input signal Vin is doubled, the time of logic 1 also changes to be half at the same time.

┌Vin in 0 pulse(1.8 0 0.1n 0.1n 0.1n 39.9n 80n) ┐

│ **↓** **↓** │

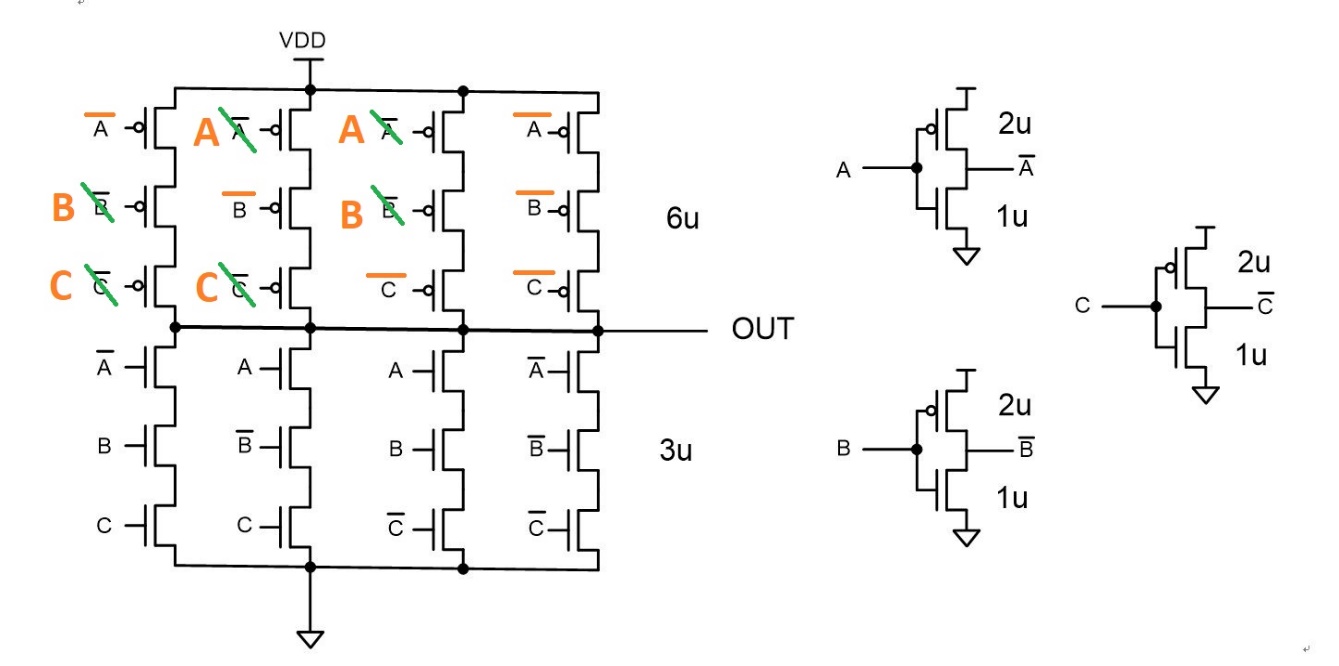
└Vin in 0 pulse(1.8 0 0.1n 0.1n 0.1n 19.9n 40n) ┘

***LAB3-1：Static CMOS 3-input XOR (25%)***

Write 3-input Static CMOS XOR SPICE, observe the waveform and measure Delay time，Power consumption，Power-Delay-Product。

1. Size: L=0.18u, W: Please size it according to the figure below.
2. Please sweep the capacitance loading c=0.05p, 0.1p, 0.15p.....0.5p，observe the waveform and measure Delay time，Power consumption，Power-Delay-Product. (Record the Delay time and Power consumptio according to Loading changes in Excel.)
3. Using fixed loading capacitance c=0.05p，Modify your input pattern with 2 times, 4times ,8 times, and 16times frequency (Record the Delay time and Power consumptio according to Frequency changes in Excel.)

Static CMOS 3-input XOR：



***LAB3-2：Pseudo-NMOS 3-input XOR (25%)***

Write 3-input Pseudo NMOS CMOS XOR SPICE, observe the waveform and measure Delay time，Power consumption，Power-Delay-Product。

1. Size: L=0.18u, W: Please size it according to the figure below.
2. Please sweep the capacitance loading c=0.05p, 0.1p, 0.15p.....0.5p，observe the waveform and measure Delay time，Power consumption，Power-Delay-Product. (Record the Delay time and Power consumptio according to Loading changes in Excel.)
3. Using fixed loading capacitance c=0.05p，Modify your input pattern with 2 times, 4times ,8 times, and 16times frequency (Record the Delay time and Power consumptio according to Frequency changes in Excel.)

Pseudo-NMOS 3-input XOR：



***LAB3-3：Pass-transistor 3-input XOR (25%)***

Write 3-input Pass-transistor CMOS XOR SPICE, observe the waveform and measure Delay time，Power consumption，Power-Delay-Product。

1. Size: L=0.18u, W: Please size it according to the figure below.
2. Please sweep the capacitance loading c=0.05p, 0.1p, 0.15p.....0.5p，observe the waveform and measure Delay time，Power consumption，Power-Delay-Product. (Record the Delay time and Power consumptio according to Loading changes in Excel.)
3. Using fixed loading capacitance c=0.05p，Modify your input pattern with 2 times, 4times ,8 times, and 16times frequency (Record the Delay time and Power consumptio according to Frequency changes in Excel.)

Pass- transistor 3-input XOR：



**Question: (25%) ( 5/10 )**

**1. Analyze the impact of changes in Loading on circuit power and delay? What is the difference in the impact of Logic Family for these 3 different Logic?**

**2. Analyze what impact the change of Pattern frequency has on the power and delay of the circuit? For 3 types of What are the differences in the impacts of different Logic Families?**

**3. Analyze the advantages and disadvantages of 3 different Logic Families**