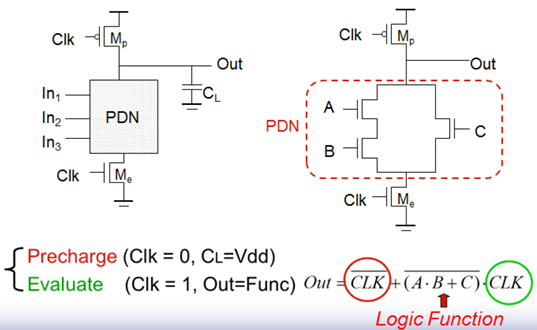
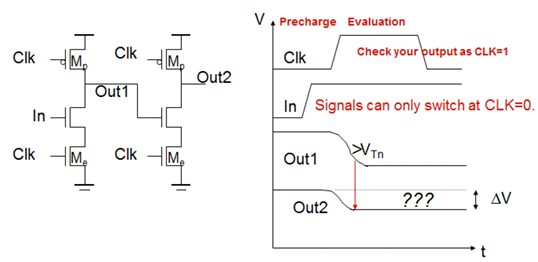
***LAB-4 Dynamic CMOS Logic Circuit***

1. ***3-input XOR Dynamic CMOS Logic Circuit***
2. ***Cascaded Dynamic Domino CMOS Circuit***
3. ***8-bit Manchester Adder***

Dynamic CMOS Logic Circuit



Dynamic circuit operation tips:



***LAB4-1：3-input Dynamic XOR (Loading=0.1p)***

Write 3-input Static CMOS XOR SPICE, observe the waveform and measure Delay time，Power consumption，Power-Delay-Product

1. Size: L=0.18u, W: Please size it according to the figure below.
2. Please sweep the capacitance loading c=0.05p, 0.1p, 0.15p.....0.5p，observe the waveform and measure Delay time，Power consumption，Power-Delay-Product. (Record the Delay time and Power consumptio according to Loading changes in Excel.)
3. Using fixed loading capacitance c=0.1p，Modify your input pattern with 2 times, 4times and 8 times frequency (Record the Delay time and Power consumption according to Frequency changes in Excel.)

VA A 0 pulse(1.8 0 0.1n 0.1n 0.1n 3.9n 8n)

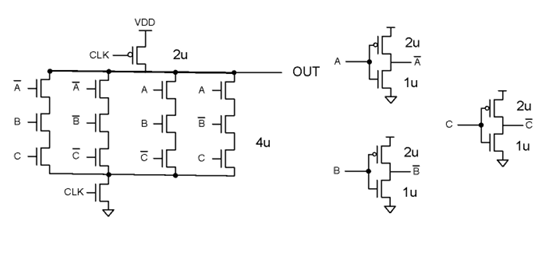
VB B 0 pulse(1.8 0 0.1n 0.1n 0.1n 7.9n 16n)

VV C 0 pulse(1.8 0 0.1n 0.1n 0.1n 15.9n32n)

VCK CK 0 pulse(0 1.8 2.1n 0.1n 0.1n 1.9n 4n)

.tran 0.1n 40n

***3-input Dynamic XOR circuit***

******

**LAB4-2：CascadedDynamicNAND/AND (Loading=0.1p)**

Please cascade the 2-input NAND/AND as following, with fan-out loading c=0.02p.，Please measure Delay time of out1,out2,out3,out4(Record the Delay time with four out in Excel.)

NAND/AND use Wp=1u/0.18u, Wn=1u/0.18u

INV use Wp=1u/0.18u, Wn=0.5u/0.18u

Pattern:

VA A 0 pulse(1.8 0 0.1n 0.1n 0.1n 9.9n 20n)

VB B 0 1.8

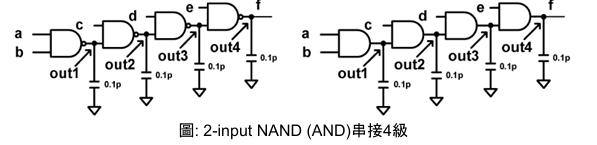
VC C 0 1.8

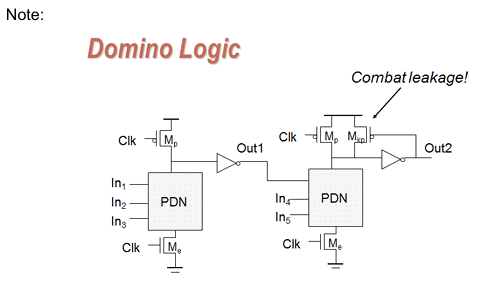
VD D 0 1.8

VE E 0 1.8

VCK CK 0 pulse(0 1.8 2.1n 0.1n 0.1n 1.9n 4n)

.tran 0.1n 40n





***LAB4-3：8-bit Dynamic Manchester Carry-Generation Chain (Loading=0.05p @ C0~C7) G=A and B, P=A XOR B***

The circuit size is freely designed, and the clock frequency is set to 250MHz. Please determine at least 8 groups of patterns, which need to cover one group.

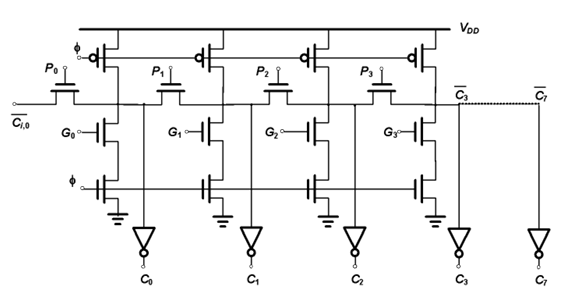
The pattern passes through G0, P1, P2, P3, P4, P5, P6, and P7, and the other seven groups are freely selected. After all functions are verified to be correct,

(Record avg\_power, critical\_delay, waveform, and transistor size.)

<Note>1. Pattern must be at least twice as slow as CLK and down-clocked to an even multiple of the CLK frequency.

2. Pattern must only change when CLK=0, and cannot be switched when CLK=1.

3. For the output logic, please observe the output result when CLK=1.



Question:(5/16)

1. What are the limitations of analyzing Pattern in pre-charge and evaluation?

2. Analyze the impact of Cascade series on circuit power and delay?

3. Explain whether the Domino series circuit is connected and what impact it has on the circuit function?

4. Explain the advantages and disadvantages of dynamic circuits.

5. Explain why dynamic circuits are suitable to be used to implement Manchester Adder?