Chapter – 8
Circuit Layout

8.1 Circuits Boards and PCBs

8.2 Component Placement

8.3 Routing Signal Tracks

8.3.1 Trace Density, Common Impedance, Distribution of signals and Return, Transmission Line Concerns, Trace Impedance and Matching, and Avoiding Crosstalk

8.4 Ground, Returns and Shields

8.5 Cables and Connectors

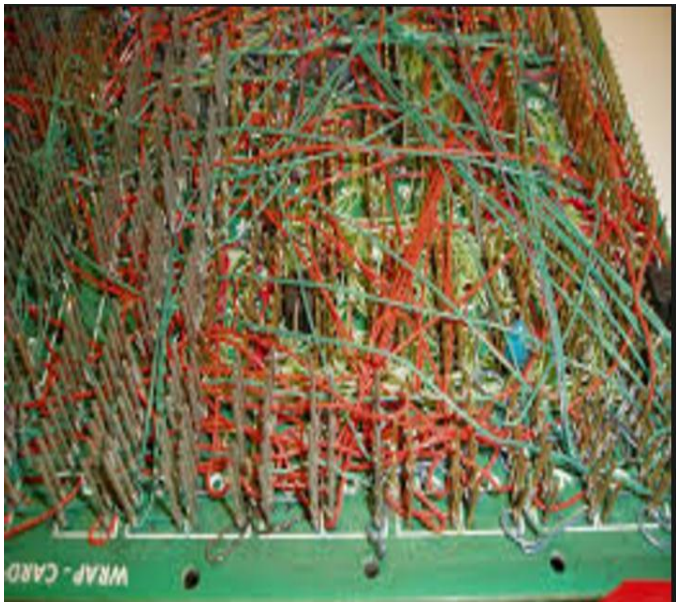
8.6 Testing and Maintenance

Technologies available for connecting components and circuits

- Stitch weld
- Wire wrap
- PCB
- Hybrid and MCM

[PCB= Printed Circuit Board, MCM= Multi Chip Module]

Wire-wrap, Stitch wire



Component Placement

- General rules:
  - Group high current circuit near the connector to isolate stray currents and near the edge of the PCB to remove heat.
  - Group high frequency circuits near the connector to reduce path length, crosstalk and noise.
  - Group low power and low frequency circuits away from high current and high frequency circuits
  - Group analog circuits separately from digital circuits.

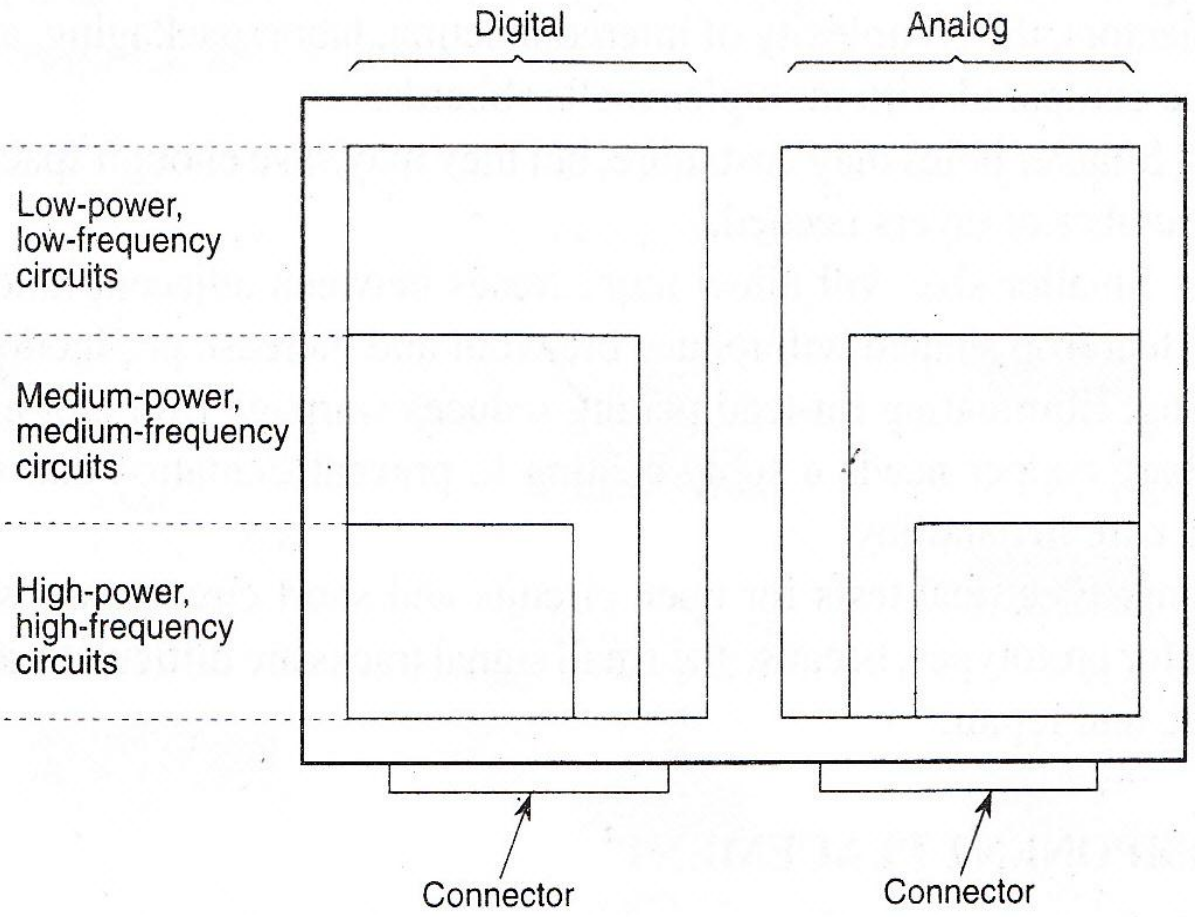


FIG. 8.7 Grouping of components. Arrange high-power and high-frequency circuits near the connector and away from the low-power circuits.

Routing Signal Traces

Important Parameters:

1. **Trace density**
2. **Common Impedance**
3. **Distribute signal and return carefully**
4. **Trace impedance and impedance matching**
5. **Avoiding Crosstalk**

1. Trace density

- As you squeeze signal traces together on a board, you can space components closer and reduce the size of the circuit boards.
- Smaller boards, allowed by higher trace densities, provide flexibility in packaging your product and may reduce the cost of material.

2. Common Impedance

- Common impedance paths cause components to reside at different ground potentials from one another.
- You can reduce the voltage drops, and hence the noise by lowering effective impedance
- Choose IC packaging with low impedance

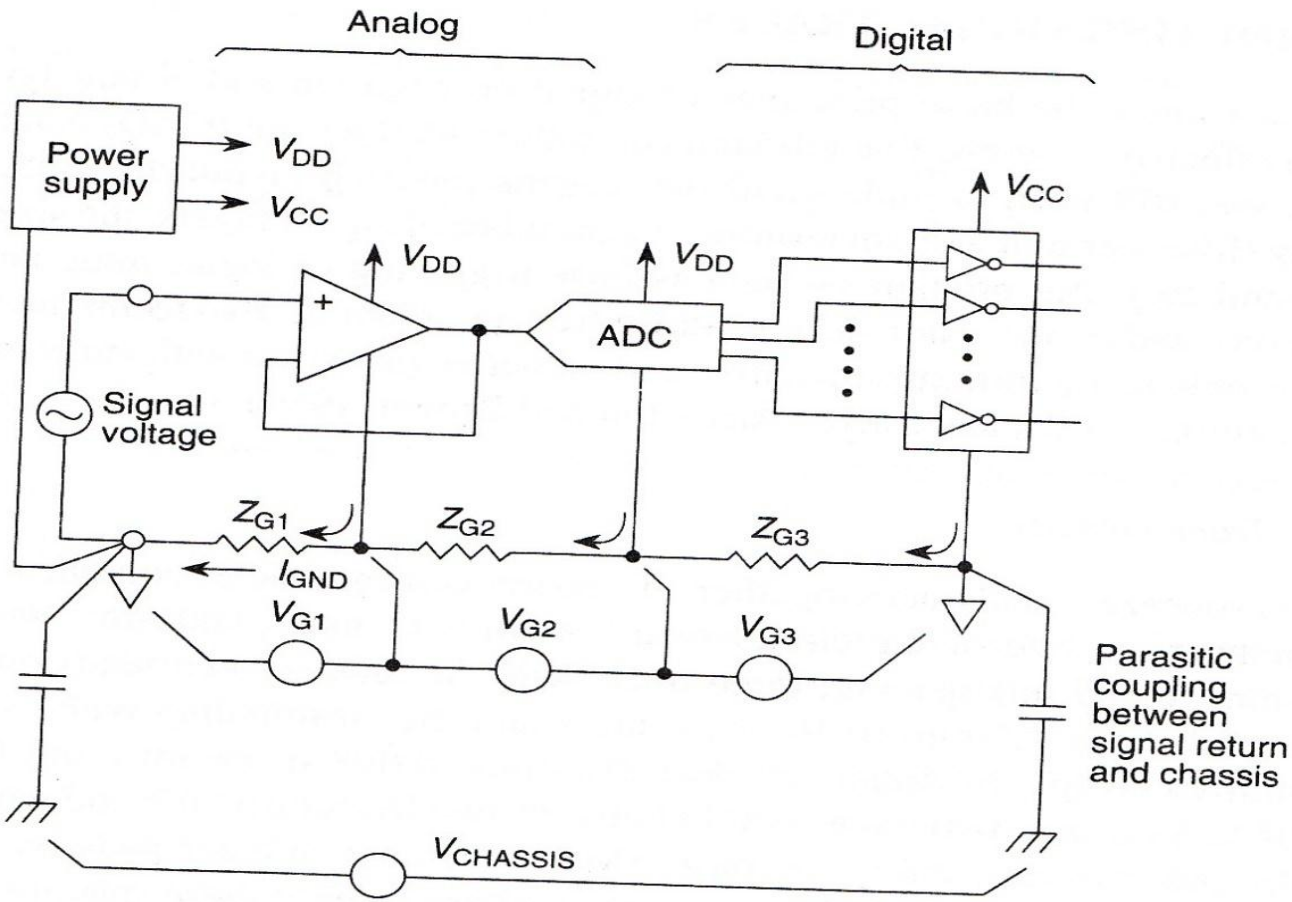
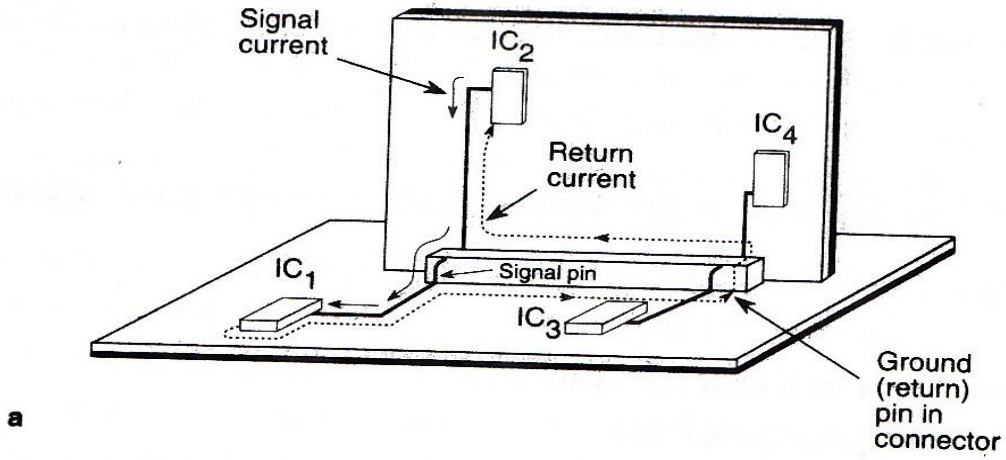


FIG. 8.8 Common impedance. Common-impedance paths cause components to reside at different ground potentials from one another. Larger common impedance will cause larger ground potentials (V_{G1}, V_{G2}, V_{G3}) and coupling to the chassis ($V_{CHASSIS}$); these will bias the signal voltage and introduce error.

3. Distribute signal and return carefully

- Address the issues of return path early in design.
- Long return path can shift the ground potential excessively, decrease noise margin.
- If the return is longer than signal, then the current has high inductance path that cause noise spikes in the ground system.
- Large loops of current have high inductance or impedance and radiated noise is often proportional to return path impedance and loop area.



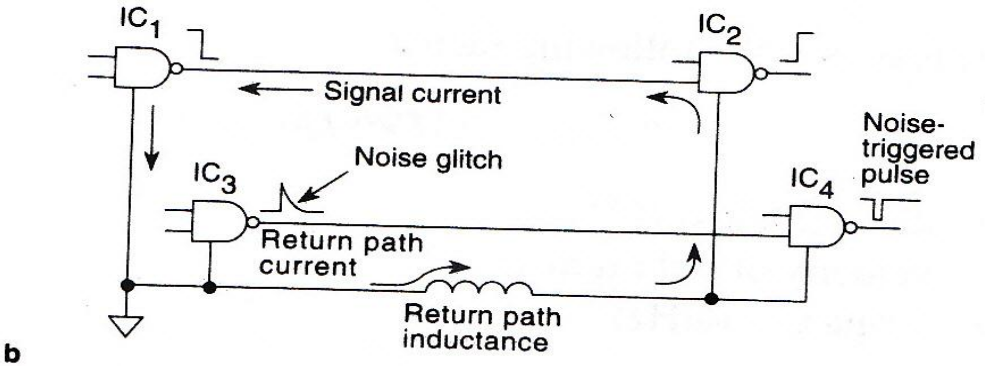


FIG. 8.9 Effect of ground pin placement. Poor placement of ground pins causes long return paths and large loop inductance. (a) The return current follows the path of lowest impedance in the ground under the signal trace, but it makes a long excursion to its connector pin. (b) Schematic representation of a long return path. The voltage across the inductance can cause the output of IC_3 to "glitch" high enough to trigger IC_4.

4. Trace impedance and impedance matching

- Impedance of signal conductors directly affect circuit operation.
- Impedance mismatches lead to reflections that can both delay switching and trigger logic falsely.

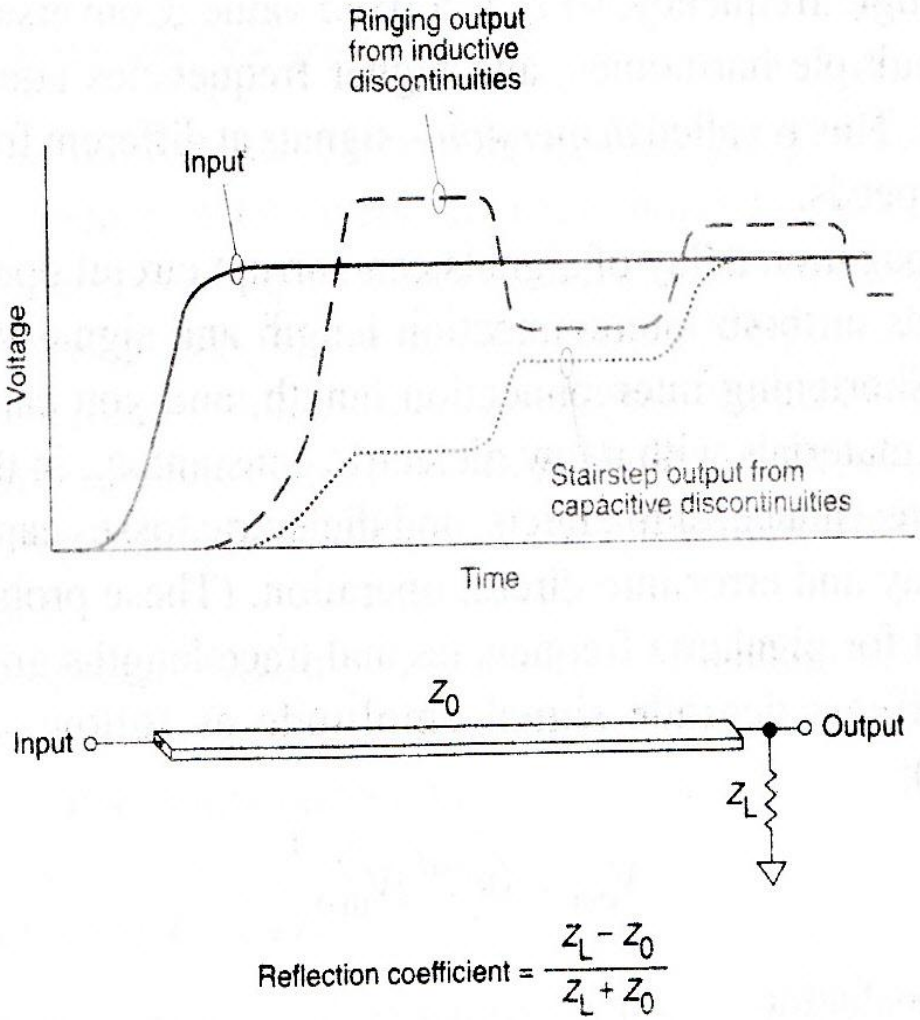


FIG. 8.10 Impedance mismatch and resulting degradation of signals along a printed circuit trace.

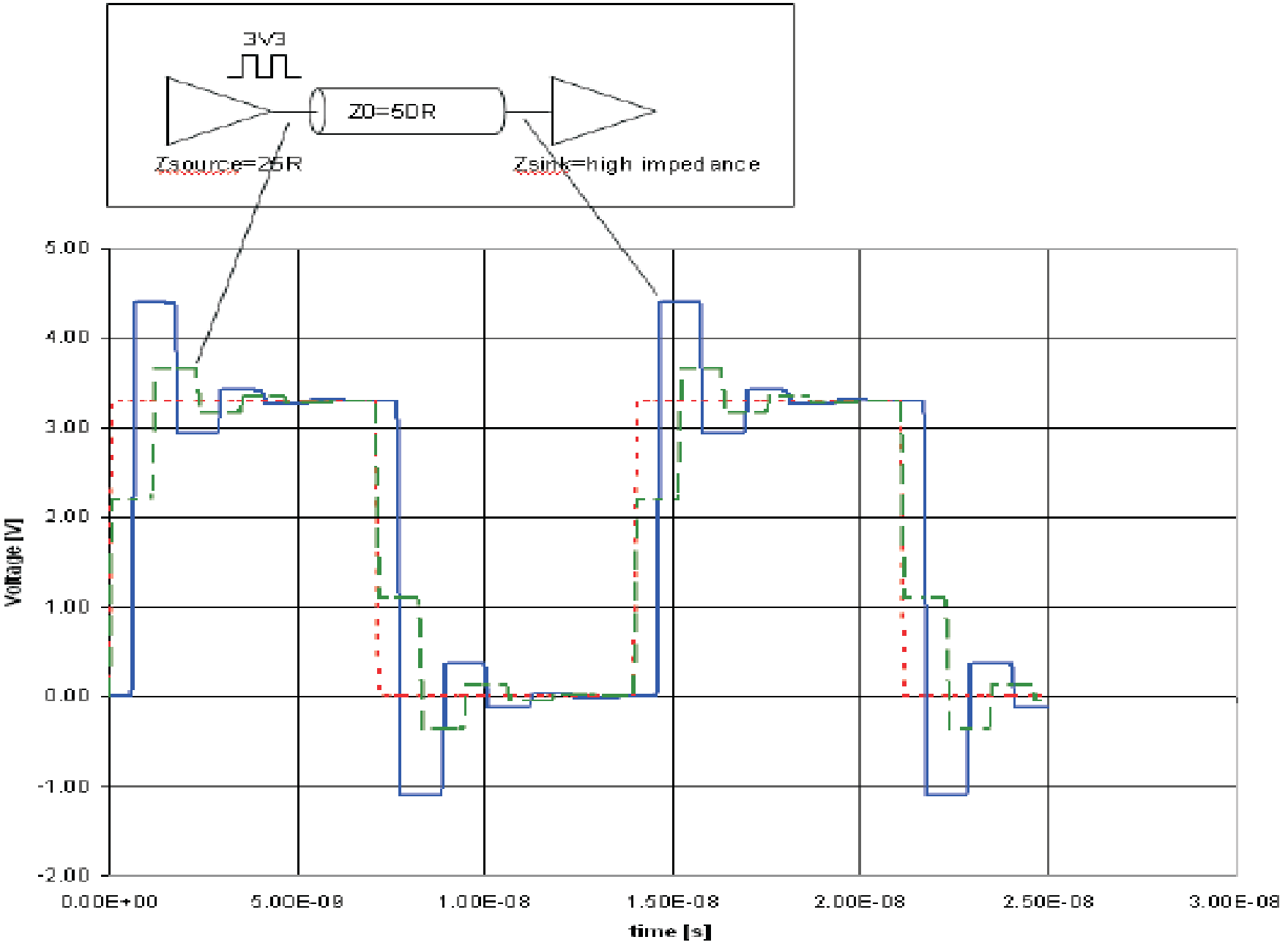


Figure 5. Over- and Undershoots Due to Incorrect Termination

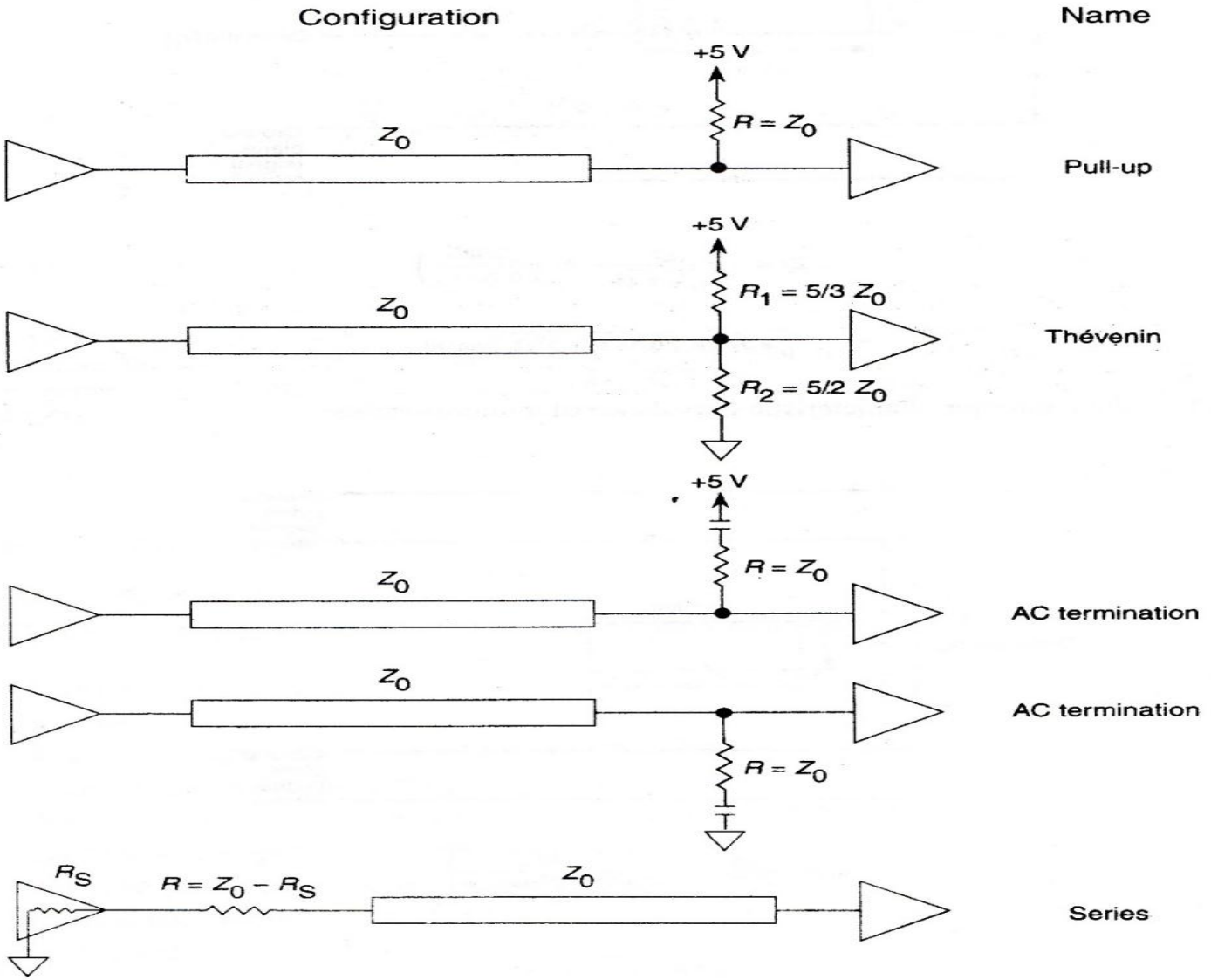


FIG. 8.11 A number of ways to terminate a signal trace.

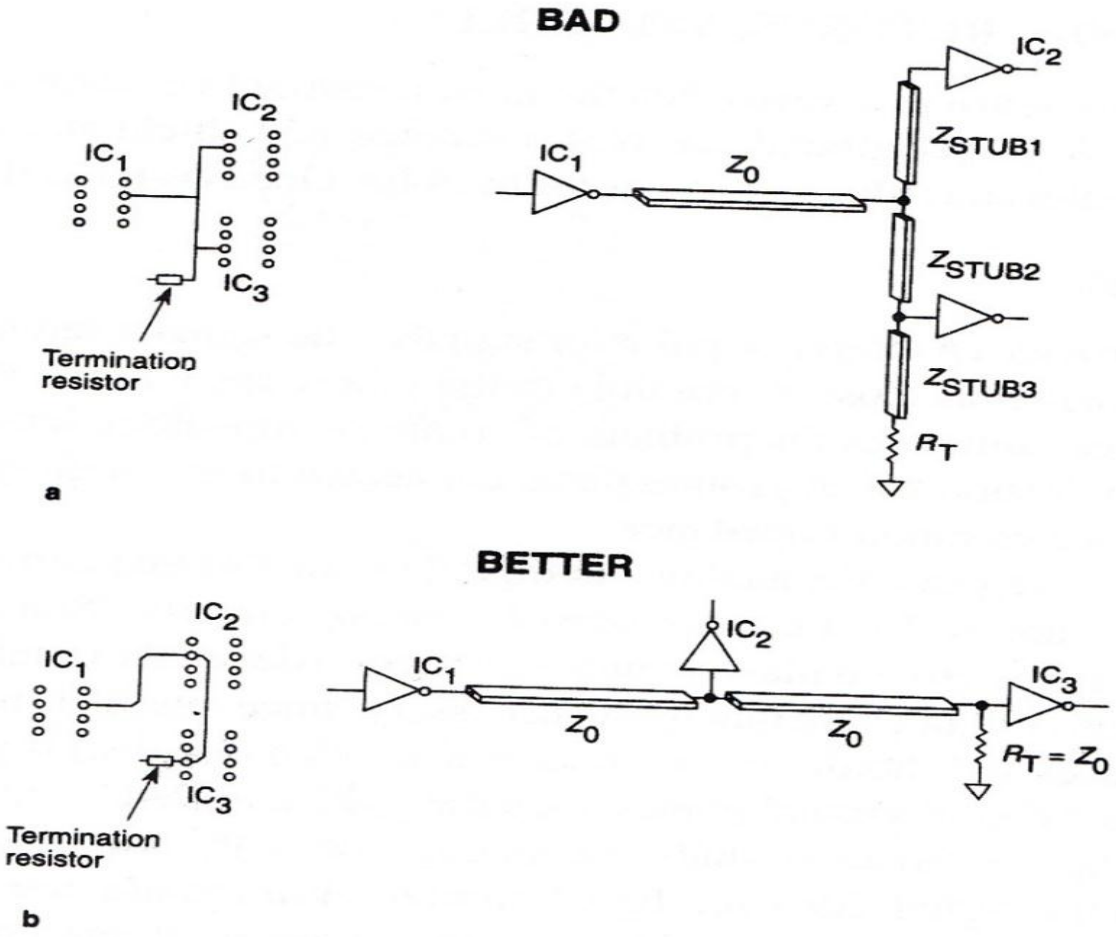


FIG. 8.14 Using a single serpentine trace to connect multiple inputs and eliminate stubs that cause reflections in the signal. (a) Poor layout degrades signal edges at the inputs to IC_2 and IC_3. (b) Using both a serpentine trace and a termination resistor near the last input eliminates stubs and preserves signal integrity.

5. Avoiding Crosstalk

- Simple guidelines when routing signal to a PCB:
  - Don’t run parallel traces for long distances- particularly asynchronous signals.
  - Increase separation between conductors**.(Twice of signal traces)**
  - Reduce magnetic coupling by reducing the loop area of circuits.
  - Sandwich signal lines between return planes
  - Isolate/shield the clock, chip select, chip enable, read and write lines

Avoiding Crosstalk by proper layout of signal traces

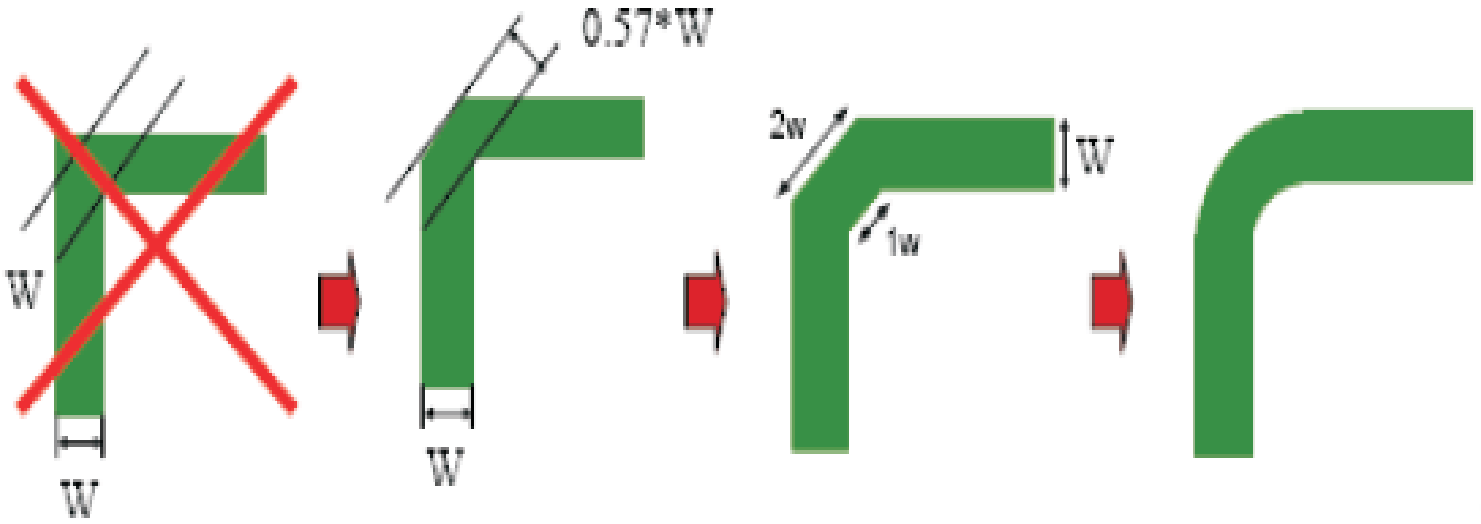
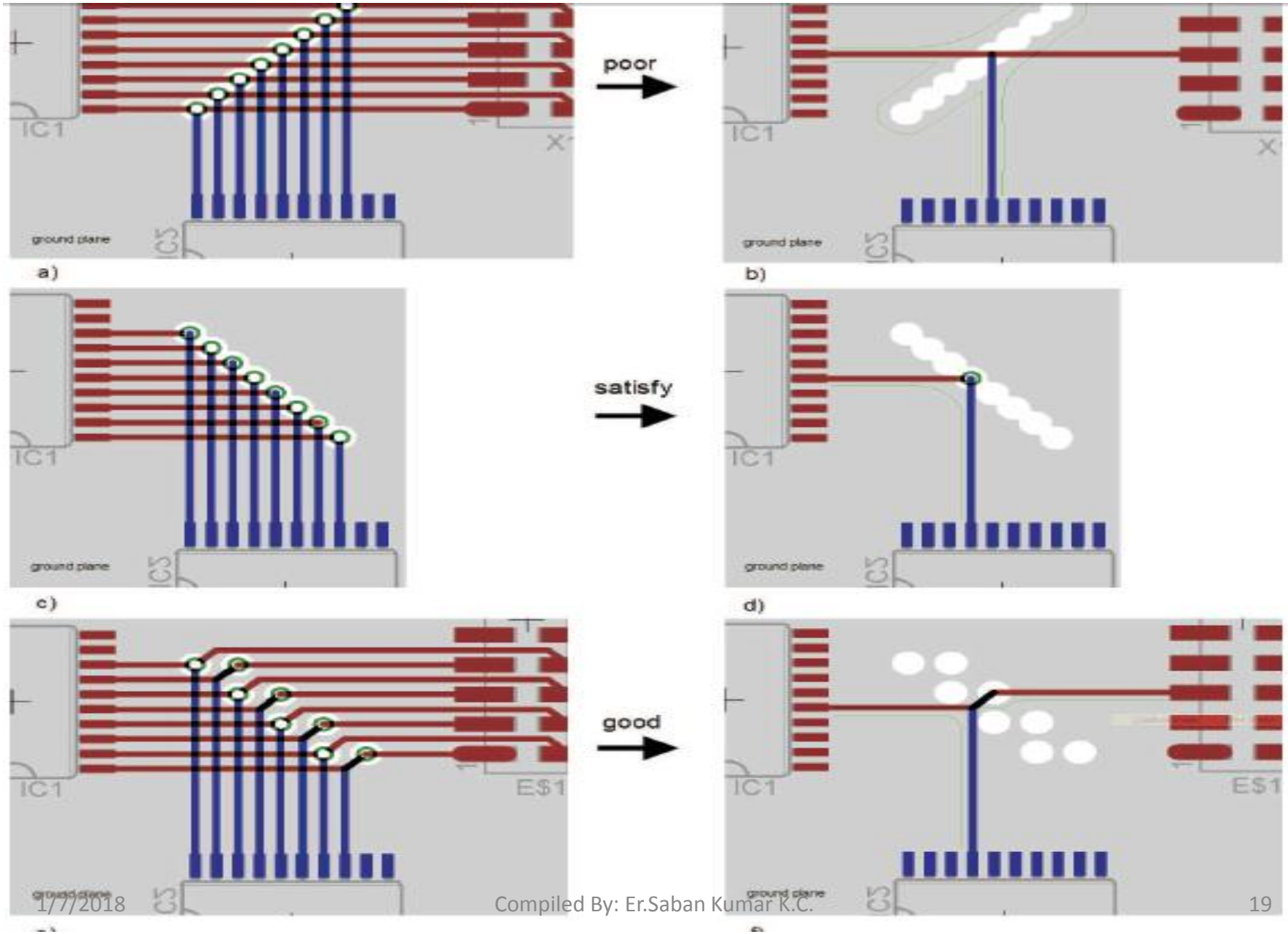


Figure 13. Poor and Good Right Angle Bends

Avoiding Crosstalk by proper layout of signal vias



Grounds, Returns and Shield

- Grounding
  - Provides reference point for signal.
  - Signal reference should be a single point and is as close as possible to the power entry to the PCB.
- Distribute power and return carefully
  - Address the issues of return path early in design.
- Shielding
  - A return plane is the most effective shield for any circuit.

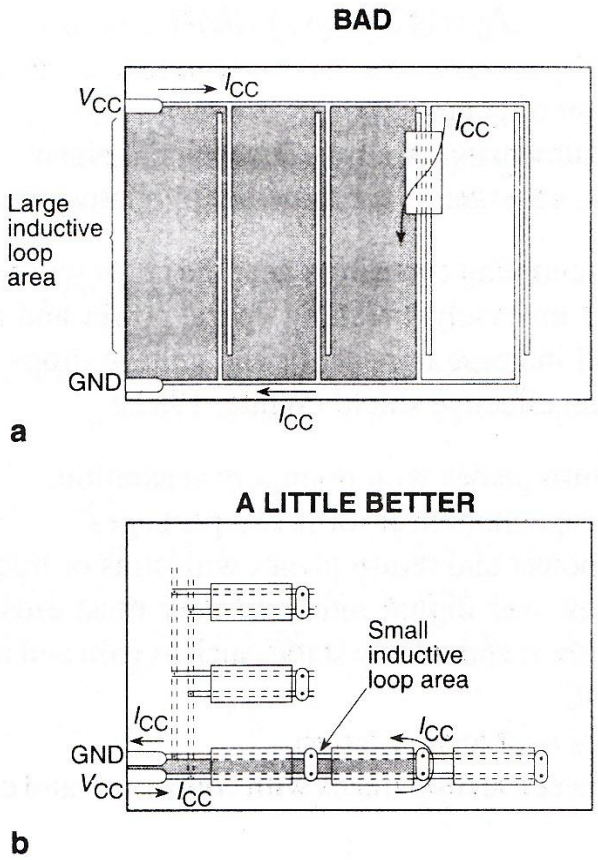


FIG. 8.15 Reducing inductive loop area. Orientation and location of the supply rails are important. (a) Interleaved combs arrangement can create large loops. (b) Running power and return together reduces the loop area. Johnson and Graham (1993) suggest a grid arrangement for the power and return rails to further reduce the loop area of signal currents, but return and power planes are by far the best solution.

Shielding

- Guidelines for effective shield
  - Use power and return planes with minimum separation.
  - Place decoupling capacitors near (or in) IC packages.
  - Don’t disrupt the power and return planes with slots or traces
  - Route digital traces over digital return.
  - Route analog traces over analog return.
  - Fill the regions between analog traces with copper foil and connect to ground.

6. Fill the regions bet...

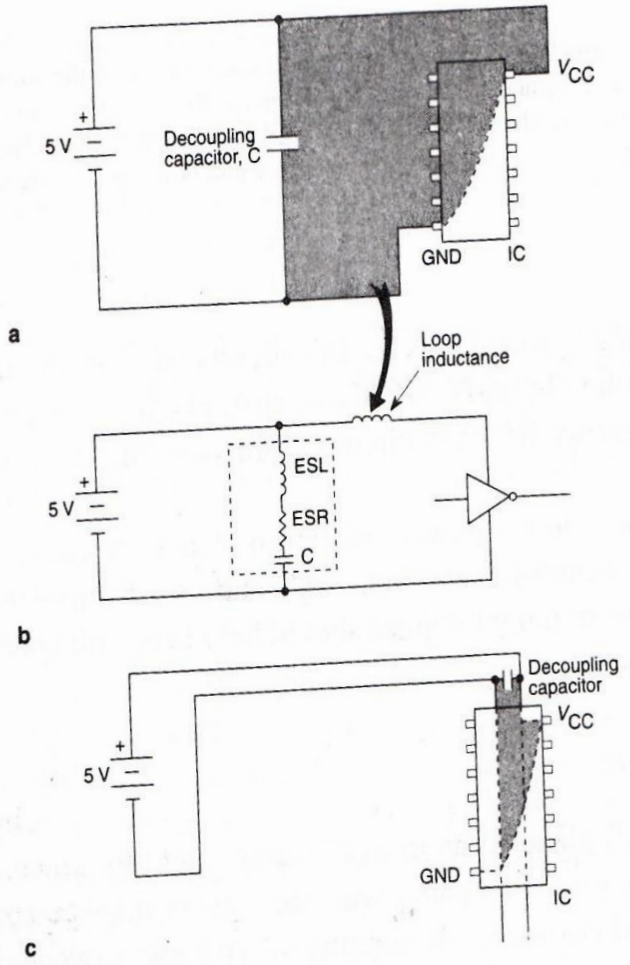


FIG. 8.16 Power supply decoupling. (a) Location of the decoupling capacitor determines the loop area and hence the inductance. (b) Equivalent circuit. (c) Putting the decoupling capacitor near the chip and running power and return together reduces the loop area and inductance.

Connectors and Cables

- Connectors are the mechanical and electrical interface between cable and a circuit board.
- Some guideline for connectors and cables:
  - Pre-assign connector ground pins
  - Distribute and intersperse grounds (return paths)
  - Place clock next to a ground line
  - Minimize I/O
  - Use long rise and fall times to reduce high frequency harmonics
  - Keep current to less than 1 amp per connector pin; otherwise use multiple pins or special pins or special pins with large current capacity.

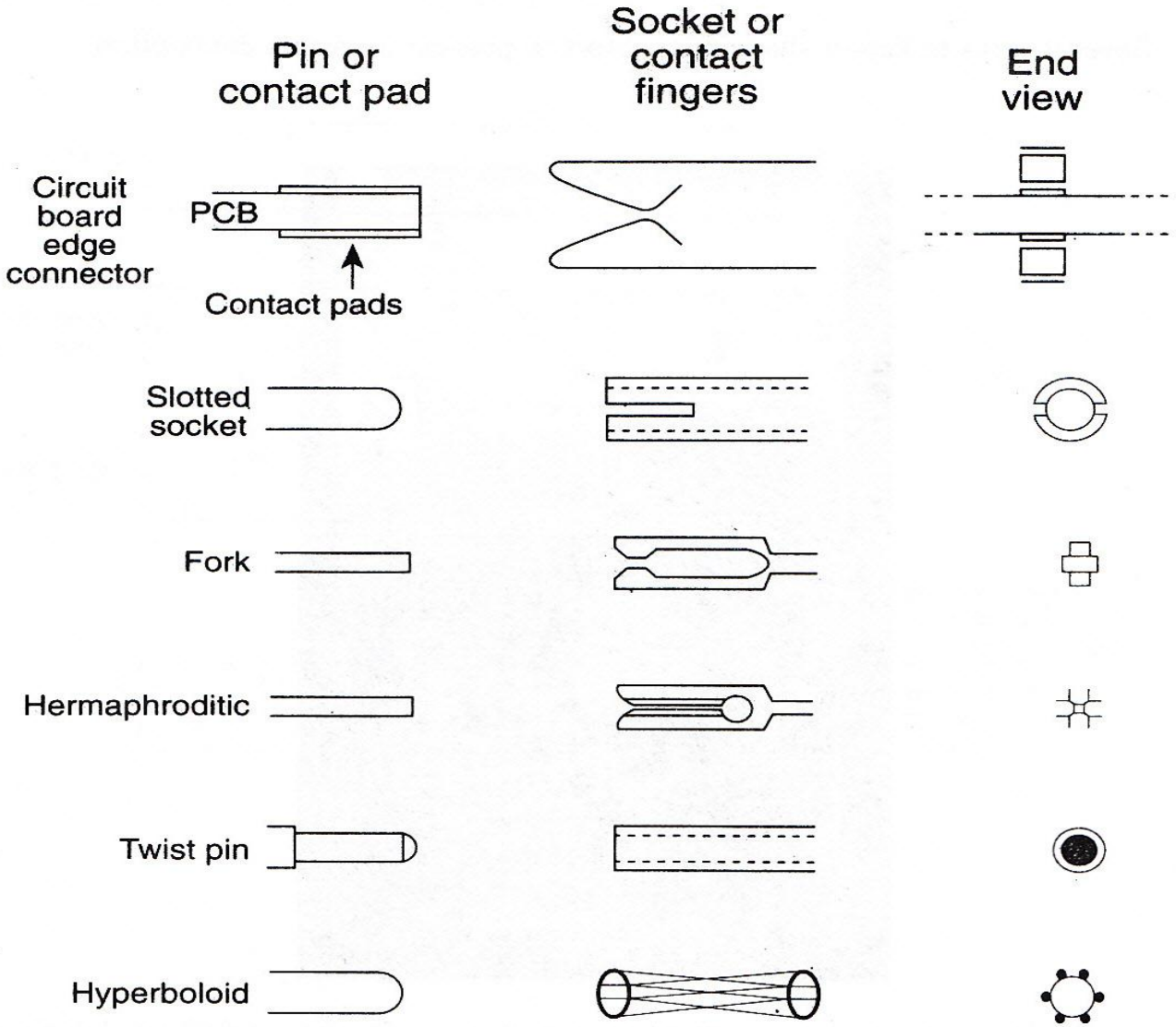


FIG. 8.17 Various configurations for connector pins, sockets, and contact fingers.

References

- K. R.Fowler, Electronic Instrument Design-architecting for the life cycle, Oxford University Press, Inc., 2010.
- H. Aryal, "Instrumentation II," haryal4@gmail.com, Kathmandu, 2010.