Chapter - 7
Circuit Design

7.1 Converting requirement into design

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7.3 High speed design

7.3.1 Bandwidth, Decoupling, ground bounce, cross talk ,Impedance matching and timing

7.4 Low power design

7.5 Reset and power failure detection and interface unit

The block diagram which we find everywhere

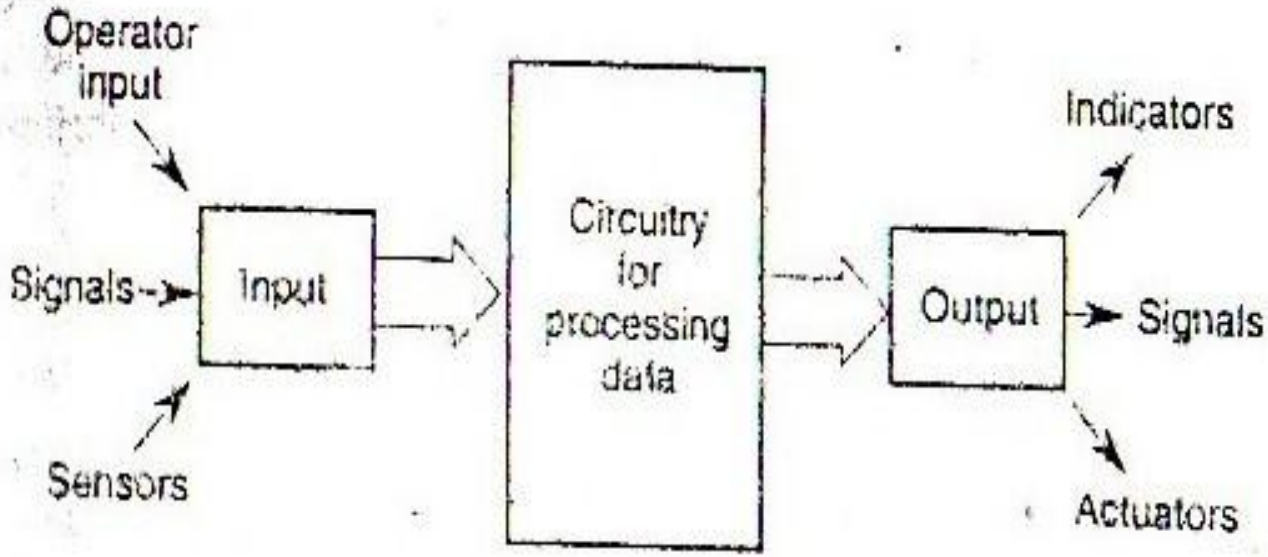


Fig. 7.1 General configuration for the circuits within a system.

Converting requirement into design

- Establishing requirement is the most difficult part of the circuit design.
- Experience is the best guide for setting requirements
- General to specific approach of establishing requirements:
  - Start by defining the desired function in broad term
  - Refine the function with operational concerns
  - Settle on exact regulations and specification

General to specific approach of establishing requirements

Table 7.1 Some requirements that drive design

System concern	Requirement	Parameters
Function	Response times	s, min, hr
	Data rates	Mbytes/s, kbits/s
	I/O drive	A, V
	Reliability—MTBF	hr
Regulations	FCC	
	UL	
	Military specifications	
Environment	Volume	in^3, m^3
	Weight (mass)	lb, kg
	Vibration	g, m/s^2
	Shock	g, m/s^2
Operation	Bandwidth	Hz
	Resolution	%, mV/LSB
	Speed	ns, μs, ms
	Accuracy	%
	Power consumption	mW
	Noise	$nV/\sqrt{Hz}$, SNR

Note: FCC = Federal Communications Commission; LSB = least significant bit; MTBF = mean time between failures; SNR = signal-to-noise ratio; UL = Underwriters Laboratories.

Converting requirement into design Contd..

- Setting specifications is one of the most difficult parts of engineering where good judgment and experience are necessary.
- Requirements often change late in the effort and spoil the design
- Some principles bound the design problem
  - E.g. use of electromagnetic spectrum

use of electromagnetic spectrum

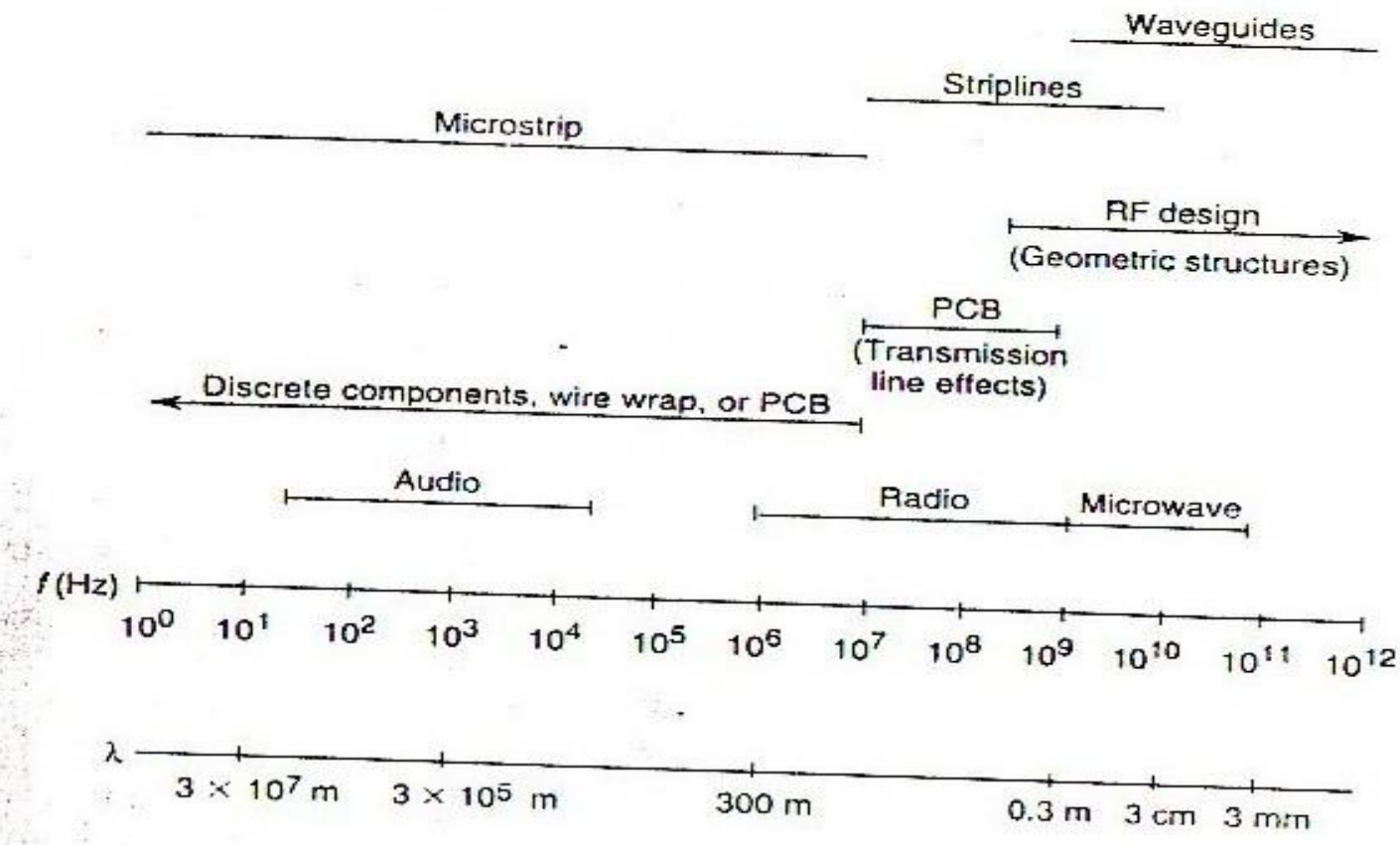


FIG. 7.2 A portion of the electromagnetic spectrum and corresponding technology applications.

Converting requirement into design Contd..

- Time and effort in design increases as the complexity of the function of system increases
- Choice of certain technology and devices are the result of good analysis and may depend on different factors
  - E.g. choice of a microprocessor for a system
  - Choice of A/D and D/A converters

Selection of microprocessor

- Performance
- No . Of peripheral function
- Memory
- Tools support to determine the appropriate processor
- Low power consumption

Performance is determined by:

- Throughput
- Resolution
- Address space and available memory
- Language choice ,code size, speed
- Predominant types of calculation :integer and floating point

No . Of peripheral function

- Math coprocessor
- Graphics accelerator
- Interrupt handler
- Data transfer and communication:DMA,small computer system interface(SCSI), Serial I/O Ports
- Timer
- ADC and DACS
- Power drivers
- Watchdog timing

Memory

- Require minimum size of memory
- Always plan for and specify margin in the requirements for future updates and modifications.
- Size of RAM/ROM Depends on
  - Data array
  - Stack
  - Temporary and permanent variable
  - Compiler overhead
  - I/O buffer

Tools support to determine the appropriate processor

- Hardware simulator: Helps to debug both circuits and code
- Software tools: supports development on the selected processor
- Vendor: good support, good reputation, markedly affected development tools

Complexity vs. Right Technology

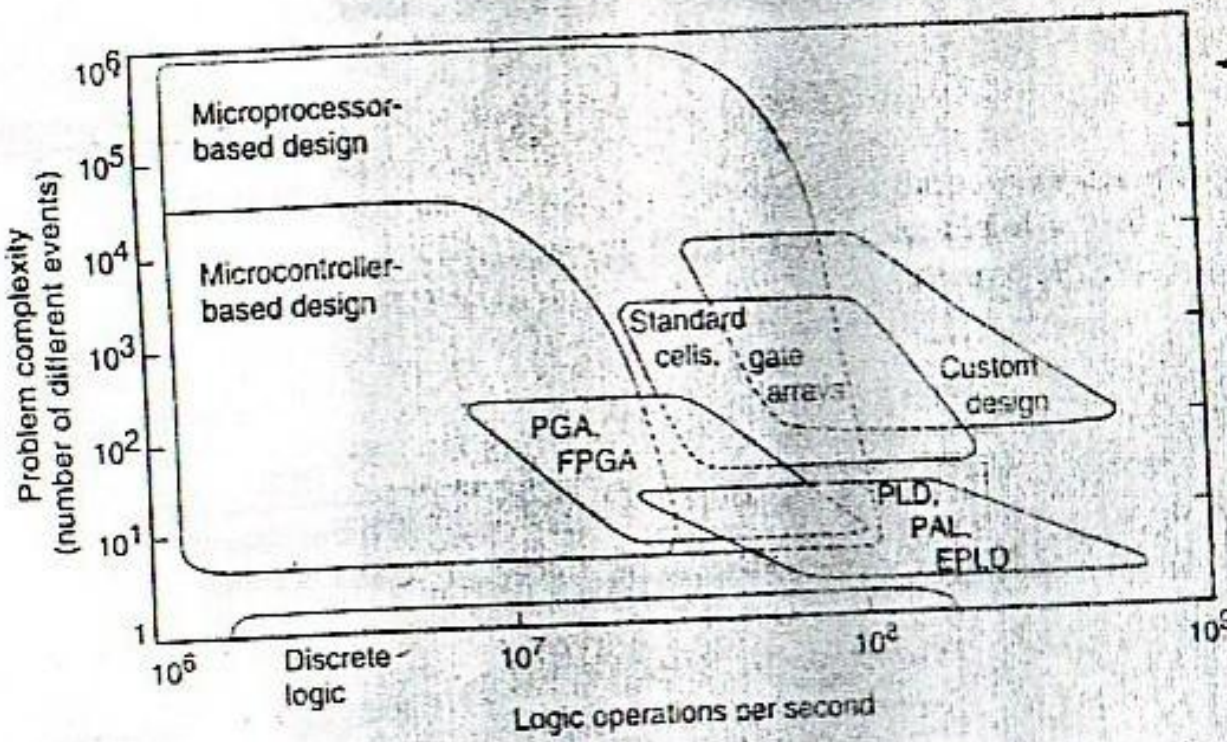


FIG. 7.3 Comparison of the performance of various technologies to the problem complexity handled by the components. (EPLD = electrically programmable logic device; FPGA = field-programmable gate array; PAL = programmable array logic; PGA = programmable gate array; PLD = programmable logic device.)

Design time vs. Complexity

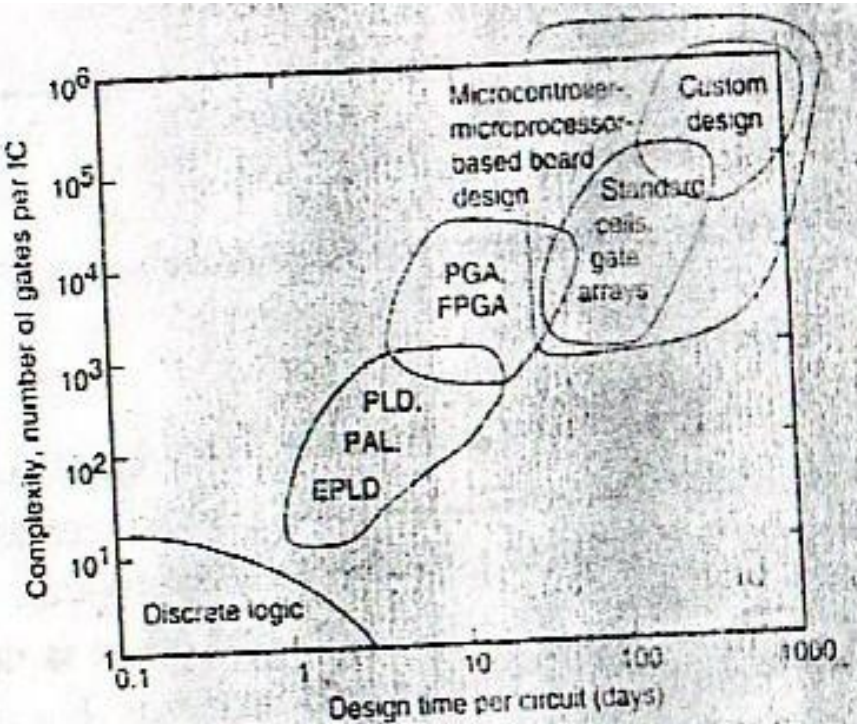


FIG. 7.4 Comparison of the design time required using various technologies versus the complexity of the components.

Reliability, fault tolerance and high speed design

- Reliability
  - How long the product will last?
  - Two factors role in the reliability:-
    - Complexity:- Fewer part better
    - Design margin:- Stressing of components
  - Two methods to measure reliability:-
    - Model prediction:- help update estimates of reliability but are limited and cannot predict every outcome
    - Prototype test:- find out many weaknesses and problems but are time consuming
  - Combination of both is mostly used

Reliability

- The failure rate for a component is a generally a base rate modified by various factors

  $\lambda = \lambda_b \pi_e \pi_q \pi_a$ .....(1)

  Where, λ= failure rate, λ_b= base failure rate

  π_e= environmental factor, π_q= quality factor

  π_a= acceleration factor

- Reliability of a component is a function of failure rate: $R(t) = e^{-\lambda t}$ .....(2)

  Where R(t)=Reliability, λ=failure rate, t = time

- Reliability of a System is a product of all component reliabilities: $R_{System} = \prod_{i=1}^{n} R_i$ ..... (3)

Reliability contd..

- Where R_{system}=reliability of the system, R_i=reliability of component
- Factor affecting on reliability
  - Corrosion
  - Thermal cracks
  - Electro migration
  - Secondary diffusion
  - Ionizing radiation
  - Vibration
  - High voltage breakdown
  - Aging

Fault tolerance

- Defines how the system responses to the fault-abnormal stresses and failures etc
- Reduces the possibility of dysfunction or damage from abnormal stresses and failures
- Allows a measure of continued operation in the event of problem
- Three distinct area
  - Careful design
  - Testable function
  - Redundant Architecture

Careful Design

- Careful design can avoid many failures from abnormal stresses. Some design techniques that can reduce the probability of failure:
  - Reduce overstress from heat with cooling and low dissipation design.
  - Use optoisolation or transformer coupling to stop overvoltage and leakage current
  - Implement ESD protection
  - Mount for shock and vibration
  - Tie down wires and cables, Prevent incorrect hookup

Testable Architecture

- The process of testing and diagnosing failures within a system.
- Two possible configurations of testable architecture:
  - Simple Configuration: Provides Probe points / test points for a technician or instrument to stimulate circuits and record responses. Only the trained personnel must disassemble the system and remove the circuit for testing.
  - Complex Configuration: Dedicated internal circuitry called built in test (BIT) that tests the system and diagnoses problems without disassembly of the equipment so adds complexity and reduces reliability

Redundant Architecture

The most complex and fault tolerant architecture are redundant architectures. They use multiple copies of circuitry and software to self check between functions.

- **Doubly redundant architecture**: merely indicates a failure in one of the subsystems; this allows for quick repair.
- **Triply redundant architecture**: uses voting between the outputs of three identical modules to select the correct value. It can have failure and still operate correctly.
- **Dissimilar redundancy**: compares the output from modules with different software and hardware to select the correct value. It can survive failure and even indicate errors in design if one system is coded correctly and the others are not.

Redundant Architecture contd..

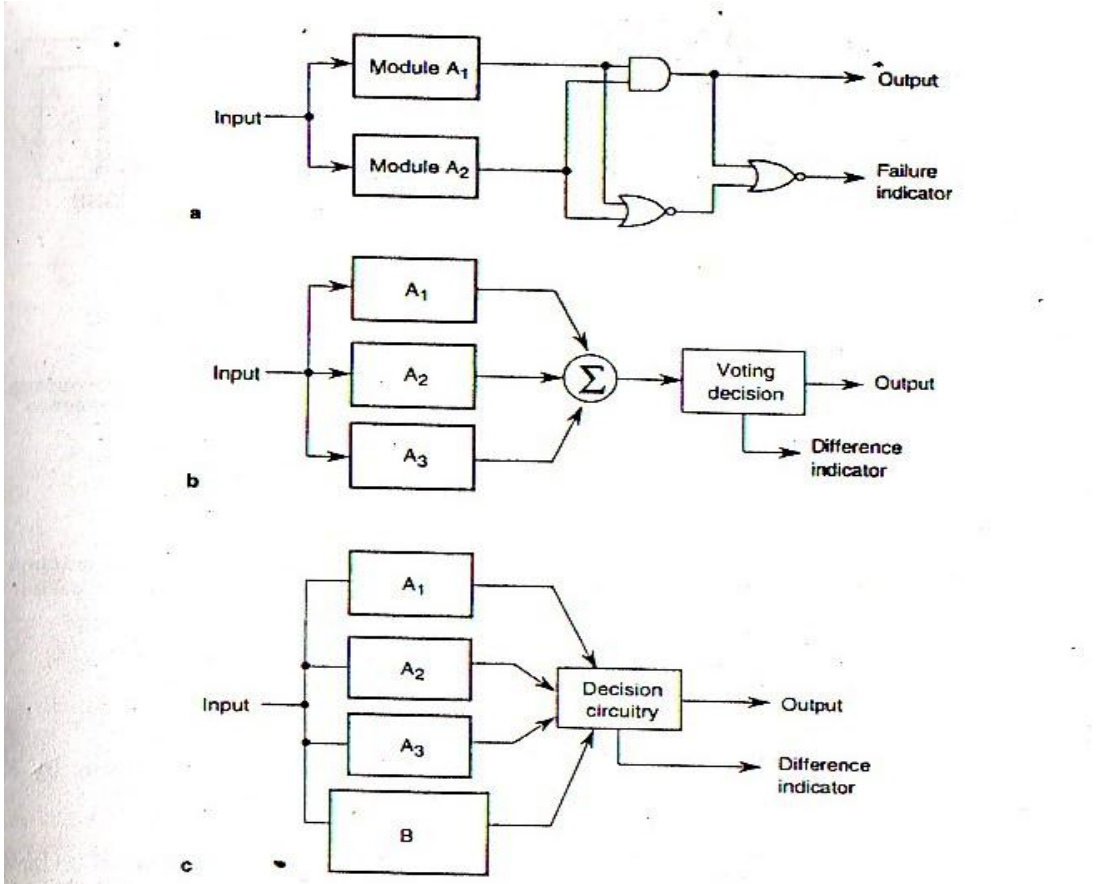


FIG. 7.6 Different configurations for redundant architecture. (a) Doubly redundant architecture ca signal failure. (b) Triply redundant architecture operates in spite of failure. (c) Dissimilar redundanc operates in spite of failure and indicates improper design or operation.

High Speed Design

- We should consider transmission line effect when clock of frequency exceeds 1 MHz in a circuit
- two conservative criteria may be used to estimate when transmission line effect begins
  - **Circuit dimension Vs signal wavelength**: If circuit dimension exceed 5% of the minimum wavelength, then signal path approaches a transmission line i.e. $l=\lambda/20$
  - **Rise time Vs propagation delay**: If the rise time of a signal is less than 4 times the propagation delay of the signal path, then the signal path approximates a transmission line with a characteristic impedance i.e. $t_r=4t_p$
- Transmission line problems:- BW, decoupling, ground debounce, crosstalk, impedance mismatch and timing skew or delay

Bandwidth

- Limiting the bandwidth of the signals within a system is the most effective way to reduce noise, EMI and problems with transmission lines.
- May limit the bandwidth by increasing the rise or fall times of the signal edges or by reducing the clock frequency.
- Selecting the appropriate logic family will set the edge rates and the consequent limit on transmission line concerns.
- Slower edge rates allow longer interconnections between circuits.

Decoupling

- Transient of current on the voltage supply due to switching of digital logic
- Decoupling capacitors are used

- **General recommendation for Decoupling:**
  - Use decoupling capacitor near each chip for two sided board
  - Use a large filter capacitor at the power entry point
  - Use a ferrite bead at the power entry point to the circuit board

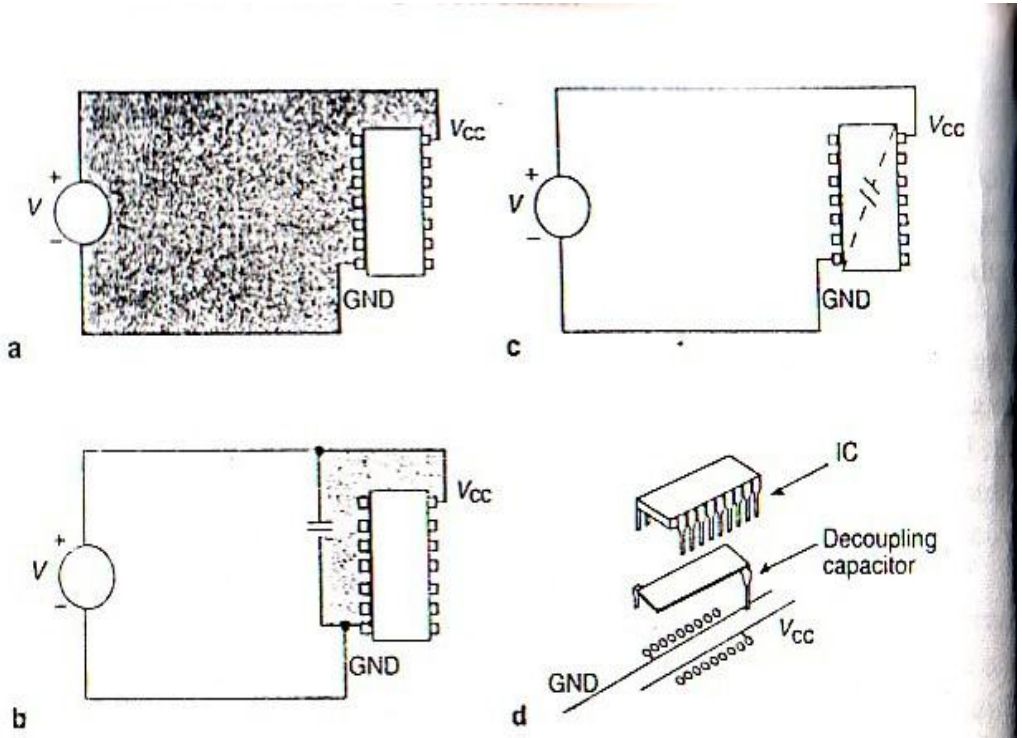


FIG. 7.8 Adding a decoupling capacitator to reduce the power-distribution impedance and consequentl noise. (a) Large inductive loop area without decoupling capacitor. (b) Decoupling capacitor reduce the inductive loop. (c) and (d) Closer to the chip is better.

Ground Bounce

- Voltage surge that couples through GND leads of a chip into non switching o/p and injects glitches onto signal lines.

- Can reduce ground bounce by:
  - Reducing loop inductance
  - Reducing input gate capacitance
  - Choosing logic families that either control the signal transition or have slower fall times.

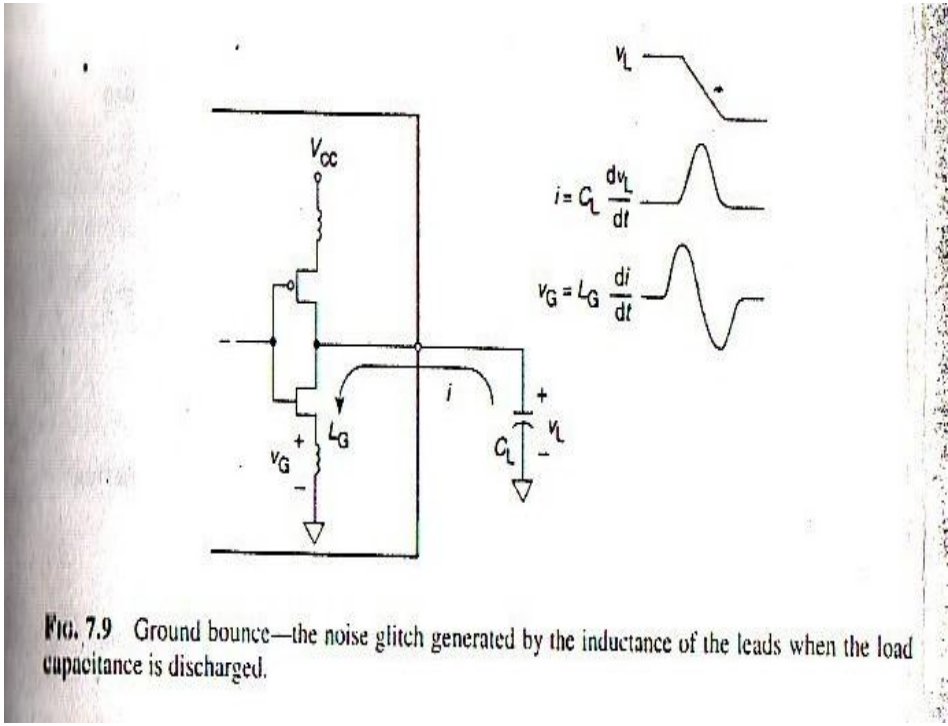


FIG. 7.9 Ground bounce—the noise glitch generated by the inductance of the leads when the load capacitance is discharged.

Crosstalk

- Coupling electromagnetic energy from an active signal to a passive line
- Coupling mechanism:- capacitive or inductive
- Depends on line spacing, length and characteristic impedance, signal rise times
- To reduce crosstalk:
  - Decrease coupling length and characteristic impedance
  - Increase rise time of signal
  - Better layout and design of circuits

Crosstalk contd..

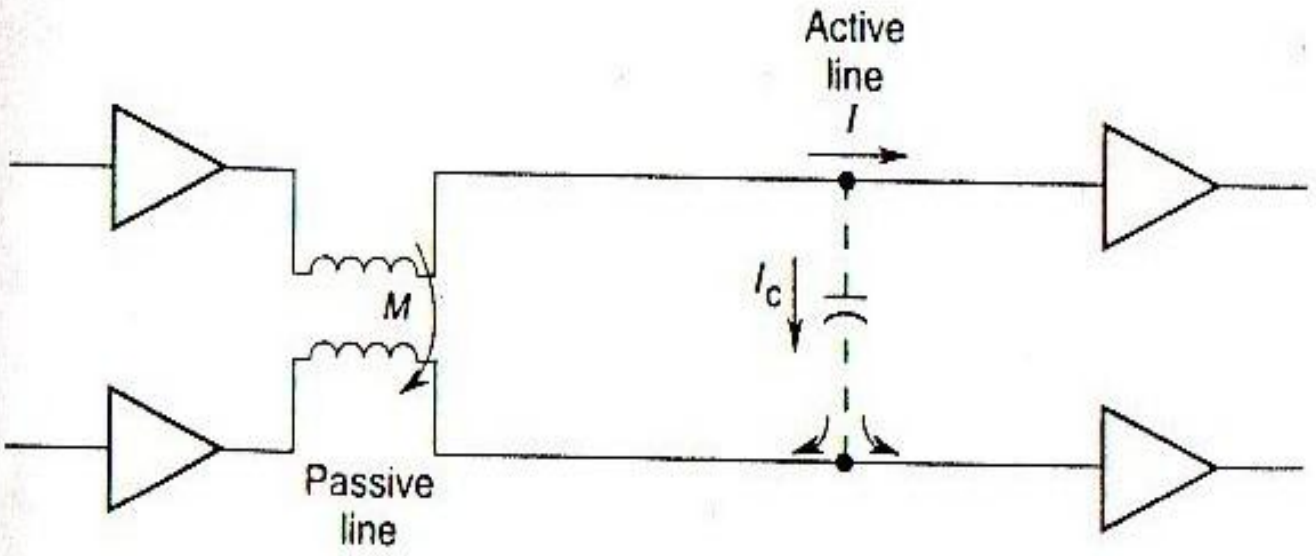


Fig. 7.10 Crosstalk—the inductive and capacitive coupling of signal from an active line to a passive line. (M = mutual inductance; I_c = capacitive current.)

Crosstalk contd..

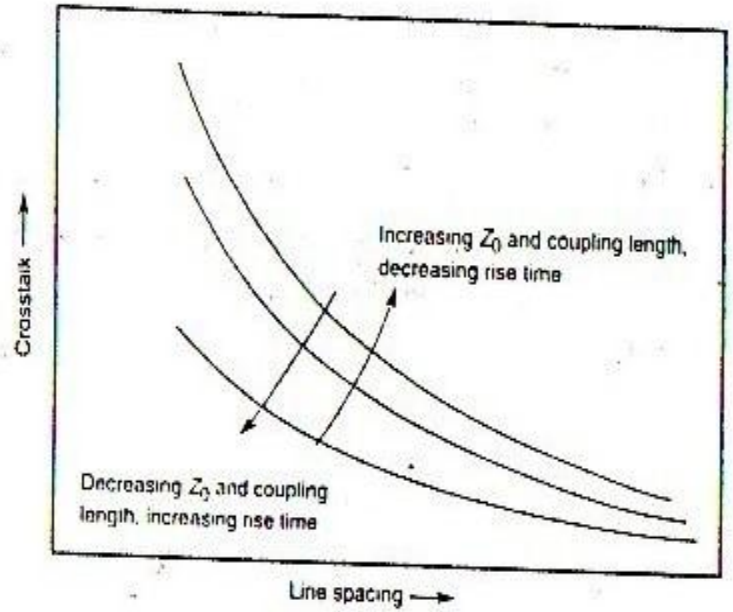


FIG. 7.11 Relationship of crosstalk to line spacing, coupling length, characteristic impedance (Z_0), and signal rise times.

Crosstalk contd...

- Avoiding Crosstalk
  - Don’t run parallel traces for long distances – particularly asynchronous signal
  - Increase separation between conductors
  - Shield clock lines with ground strips
  - Reduce magnetic coupling by reducing the loop area of circuits
  - Sandwich signal lines between return planes
  - Isolate the clock, chip-select, chip-enable, read and write lines

Impedance matching

- The reflection coefficient for a signal passing from medium 1 to medium 2 is given by:

$$\Gamma = \frac{\eta_2 - \eta_1}{\eta_2 + \eta_1} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Where η_i is the intrinsic impedance of medium i and is given by:

$$\eta_i = \sqrt{\frac{\mu_i}{\epsilon_i}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

Impedance matching contd..

- Reflection coefficient will be zero when

$$\eta_1 = \eta_2$$

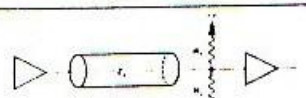
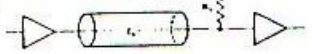
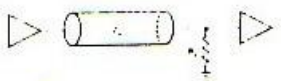
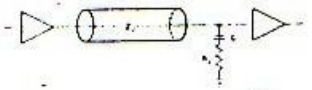
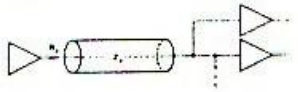
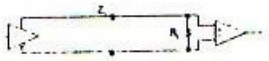
- Impedance matching makes the source and termination impedance equal to the characteristic impedance of the transmission line so that it will eliminate the reflections of signal
- Reflection of signals cause ringing (oscillations), undershoot, and overshoot in the signal pulses.
- Impedance discontinuities occurs in two configurations endpoint and stub.

Impedance matching contd..

- **End point discontinuity**:- the ends of the transmission line don’t match its characteristic impedance
  - Add series resistances at the end until the total impedance equals the line impedance.
  - Terminate the other end of the signal line from driver.

Impedance matching contd..

Table 7.3 Several methods to terminate signal lines by impedance matching, $Z_0 = Z_L$

Terminating configuration	Load impedance, Z_L	Advantages	Disadvantages
	$R_1 \| R_2$, assuming $Z_{receiver} \approx \infty$ otherwise $R_1 \| R_2 \| Z_{receiver}$	Active termination voltage to help a weak driver by speeding transitions. Use with TTL, FAST, and ECL logic.	Constant DC power dissipated through R_1 and R_2. More components required.
	R_2 or $R_1 \| Z_{receiver}$	Reduces DC power dissipation.	Additional load will slow weak drivers.
	R_2 or $R_1 \| Z_{receiver}$	Reduces DC power dissipation	Additional load will slow weak drivers.
	R_2 or $R_1 \| Z_{receiver}$ because $Z_C = 0$	Eliminates DC power dissipation. Use with FACT logic.	More components required.
	Source impedance $Z_S = R_S + Z_{driver}$	Allows branching at load. Eliminates DC power dissipation. Use with FACT and ECL logic.	
	R_1 or $R_1 \| Z_{receiver}$	Use with RS-422 and RS-485.	Constant DC power dissipated through R_L.
	R_1 or $R_1 \| Z_{receiver}$ because $Z_C = 0$	Eliminates DC power dissipation.	Long strings of consecutive 1's or 0's will charge C and cause time jitter in signal transition as C discharges.
	$2R_1$ or $2R_1 \| Z_{receiver}$	Reduces common-mode noise.	Constant DC power dissipated through resistors.

Note: Z_0 = characteristic impedance; Z_S = source impedance; Z_C = capacitive impedance.

Impedance matching contd..

- **Stub discontinuities** cause impedance mismatch by connecting multiple circuits to a single line.
- Each Connection of a stub divides the impedance and splits the power of the signal
- Make them very short to reduce the effect of stub discontinuities
- Good layout and design

Stub

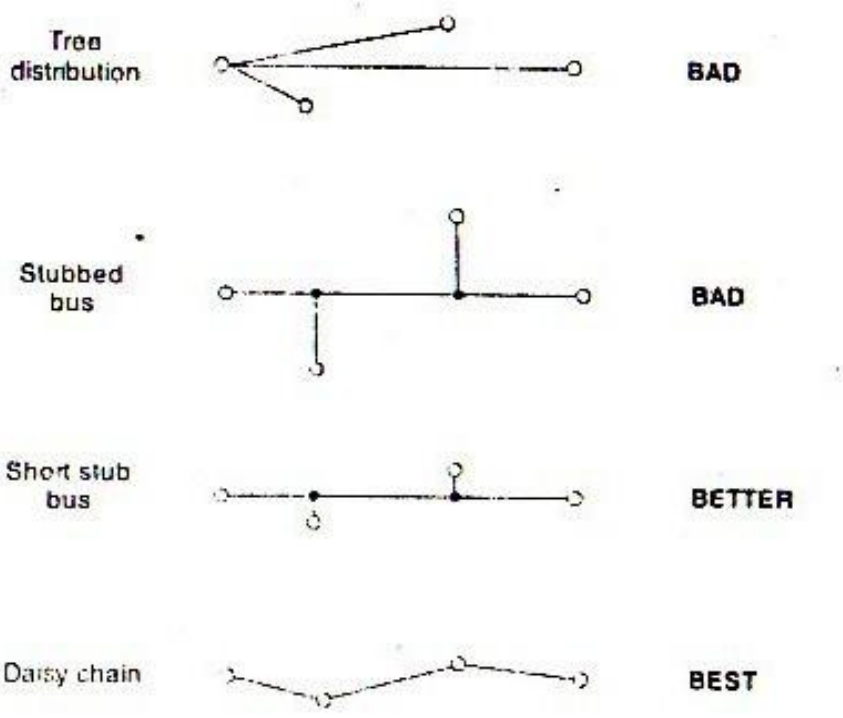


FIG. 7.12 Network geometries. Stubs cause signal reflections on transmission lines that result ringing, overshoot, and undershoot. Reduce the length of stubs and terminate the ends of the transmiss line to eliminate reflections.

Timing

- More prominent in high frequency design
- Clock signal is skewed or arrived at different propagation delays of the clock signal to different destinations
- Differences in propagation delay of rising and falling edges change the duty cycle of the signal or shrink/ expand it.
- Adequate setup and hold time is required to latch data reliably.

Timing contd..

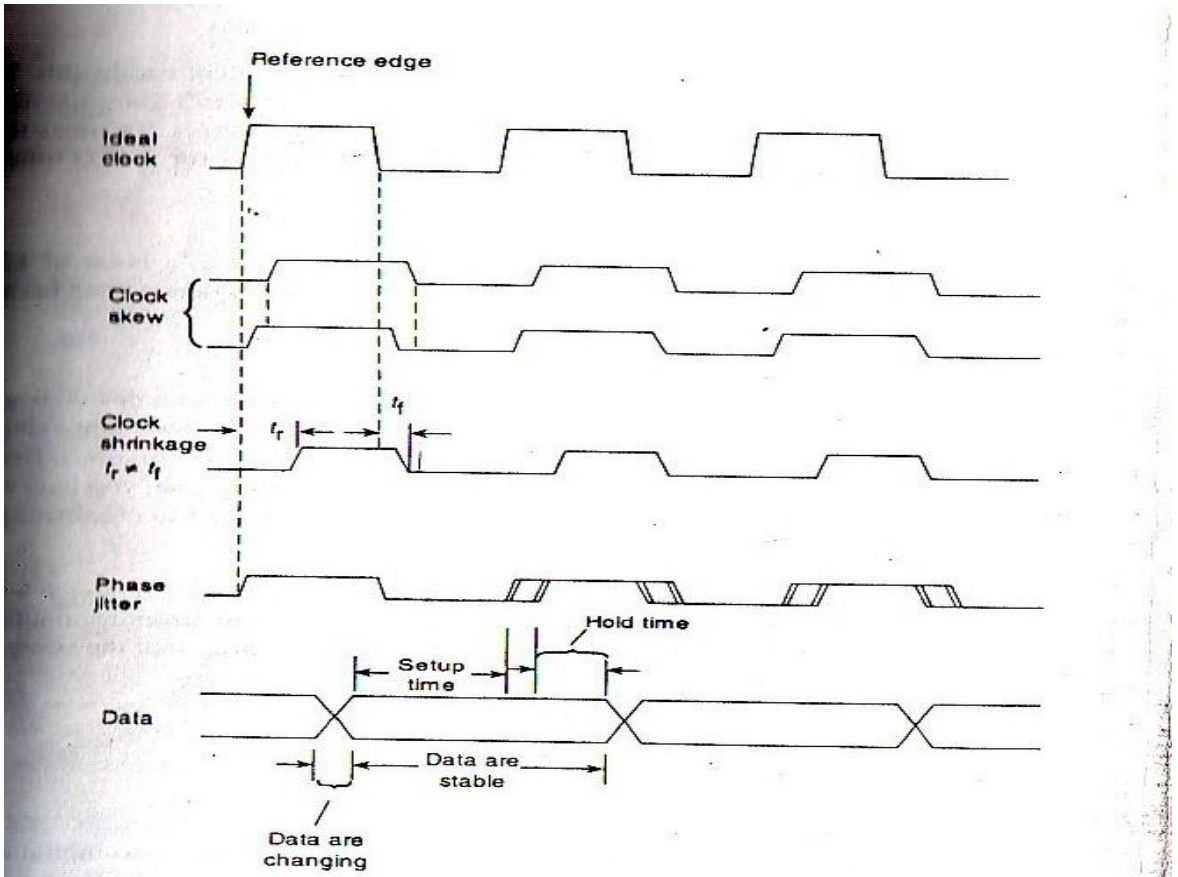


Fig. 7.13 Problems with timing. Adequate margins in the setup and hold times are necessary to account for clock skew, shrinkage, or jitter.

Low-Power Design

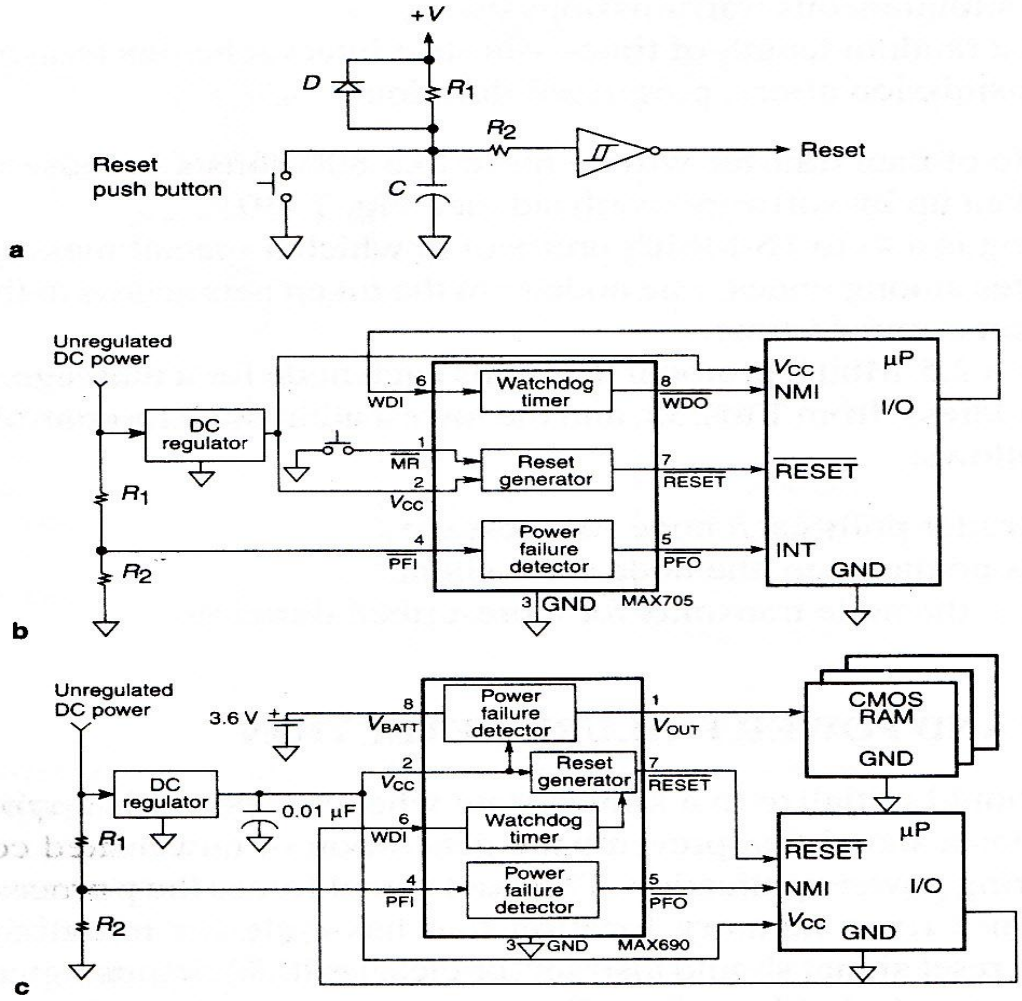
- Design practices that reduce power consumption by at least one order of magnitude; in practice 50% reduction is often acceptable.
- Mobile, TV remote controls ,digital multimeter, video cameras, laptops used low power for
  - Portability
  - Isolation
  - Battery power and low heat dissipation
- ***Active mode power = C * V² * f*** *where C is the load capacitance, V is the supply voltage, and f is the switching frequency*
- Reduce power by reducing
  - Supply voltage
  - Clock frequency
  - Load capacitance
- These seven guidelines in design will minimize power
  1. Lower clock frequency
  2. Lower supply voltage to digital circuit
  3. Shut down unused circuits
  4. Sleep mode in case of not used
  5. Terminate all unused inputs
  6. Avoid slow signal transition
  7. Make normal state use the lowest current ,for instance LEDs should be off

Reset and Power failure detection

- All systems should initialize to a known state whenever power is applied
- Reset circuit generates a signal that prevents the generation of unwanted conditions by the system during power application
- Reset signal
  - Forces the processor to begin execution from a fixed memory location where code for initialing system operation is written.
  - Sets or clears critical output signals to states that don't cause undesirable actions

Reset and Power failure detection contd..

- Reset circuit senses voltage level and generate reset signal when the voltage of power supply goes below the preset values and the reset signal stays active until the voltage of the power supply exceed the preset value.
- E.g. RC network, watchdog timer
- Some system may turn on the battery backup after power failure and also inform the processor through interrupt.


+V
D
R1
R2
Reset
push button
C
Reset
a
Unregulated
DC power
DC
regulator
R1
R2
6
WDI
Watchdog
timer
8
WDO
1
MR
2
VCC
Reset
generator
7
RESET
4
PFI
Power
failure
detector
5
PFO
3 GND
MAX705
VCC
NMI
µP
I/O
RESET
INT
GND
b
Unregulated
DC power
3.6 V
8
VBATT
Power
failure
detector
1
VOUT
CMOS
RAM
GND
2
VCC
Reset
generator
7
RESET
DC
regulator
0.01 µF
R1
6
WDI
Watchdog
timer
µP
RESET
4
PFI
Power
failure
detector
5
PFO
NMI
I/O
R2
3 GND
MAX690
VCC
GND
c

Reset and Power failure detection contd..

- The simple reset circuit as in figure uses the time constants R_1C network to set the desired duration of the reset signal.
- The Schmitt trigger inverter transforms the exponential changing waveform on the input to a signal transition appropriate for logic gates.
- The diode D allows charge to drain off the capacitor if the DC voltage fails, thereby protecting the inverter from an input voltage higher than it's supply voltage.
- When pressed, the manual push button shorts the charge on the capacitor to ground to generate a reset signal so that a user can initialize the operation of the system even while the supply power is stable.

Interface Unit

- The input to all circuit is some sort of electrical signal
- Each signal comes from another circuit, a transducer or a switch.
- Most signals need some preprocessing or conversion before the system can assimilate them
- Eg. switch generate logic transitions that bounce when pressed; there is a series of rapid glitches at the beginning and end of signal pulse.
- It is necessary to design some circuitry to suppress the glitches produced by bounce.
- Also sensors produce continuously changing analog signal that must be converted to digital logic levels for further processing
- You will need to deifne the types of inputs that you expect the system will receive
- Once you know the type of input, you can decide on the necessary circuitry to manipulate the input signals.

References

- K. R.Fowler, Electronic Instrument Design-architecting for the life cycle, Oxford University Press, Inc., 2010.
- H. Aryal, "Instrumentation II," haryal4@gmail.com, Kathmandu, 2010.