CHAPTER 4
INTERFACING A/D AND D/A CONVERTERS

4.1 Introduction
4.2 General terms involved in D/A and A/D converter
4.3 Examples of D/A and A/D Interfacing
4.4 Selection of A/D and D/A converter based on Design Requirements

4.1 Introduction

Even though an analog signal may represent a real physical parameter like temperature, pressure etc, it is difficult to process or store the analog signal for later use without introducing a considerable error. Therefore, in microprocessor based industrial products, it is necessary to translate an analog signal into digital signal. The electronic circuit that translates an analog signal into digital signal is called ADC (Analog to Digital Converter). Similarly a digital signal needs to be translated into an analog signal to represent a physical quantity; this translator is called DAC (Digital to Analog Converter).

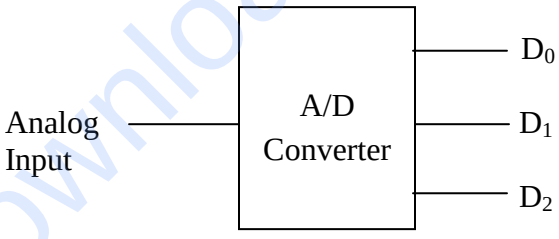
Analog to Digital Converter

The A/D converter is a quantizing process whereby an analog signal is represented by equivalent binary states. ADC can be classified into two general groups based on conversion technique.

- One technique involves comparing a given analog signal with the internally generated equivalent signal. This includes successive approximation, counter and flash type converters.
- Second technique involves a changing an analog signal into time or frequency and comparing these new parameters to known values. This group includes integrator converters and voltage to frequency converters.

The successive approximation and the flash type are faster but generally less accurate than integrator and voltage to frequency converters. The flash type is expensive and difficult to design for high accuracy.

Fig. 4.1.a shows a block diagram of a 3-bit A/D converter, it has one input line for an analog signal and three output lines for digital signals. Fig. 4.1.b shows the graph of the analog input voltage (0-1 V) and the corresponding digital output signal. It shows 8 (2^3) discrete output states from 000 to 111 each state being 1/8V apart. This is defined as the resolution of the converter.



(a)

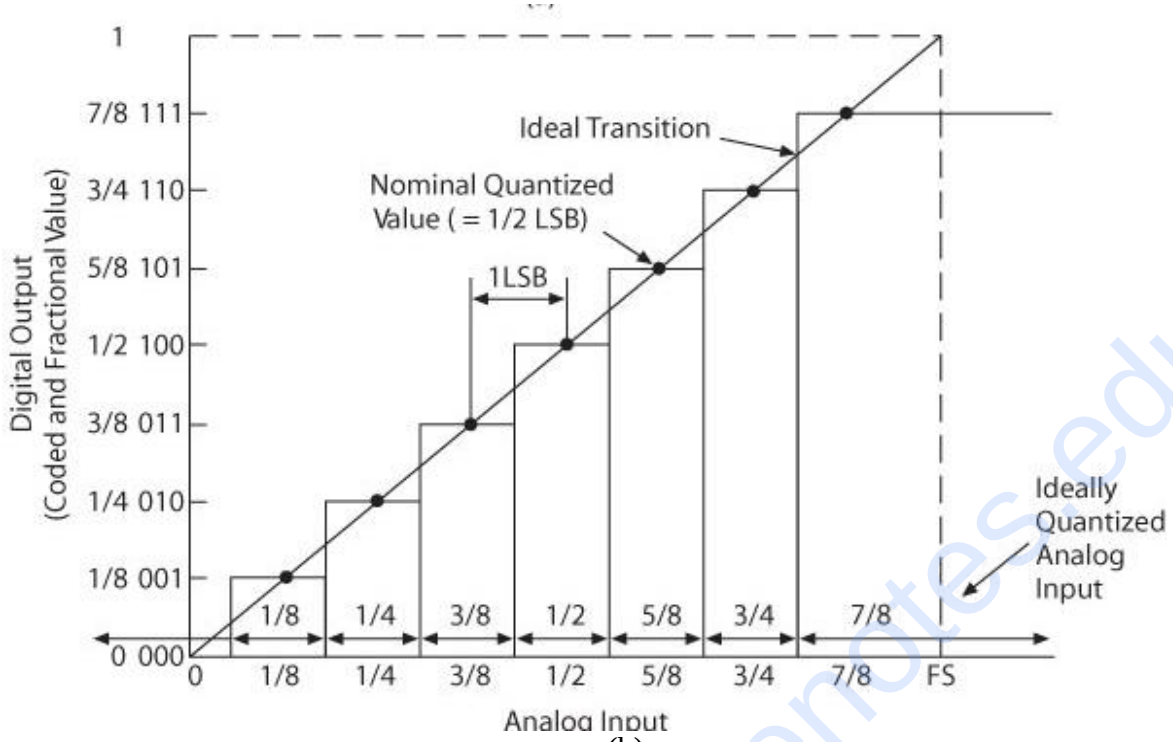


Fig. 4.1: a) A 3-bit ADC block diagram b) Analog input versus digital output

Parameters (Characteristics) of ADC

- **Resolution**
  In ADC, the original analog signal has essentially an infinite resolution as the signal is continuous. The digital representation of this signal would of course reduce this resolution as digital quantities are discrete and vary in equal steps. The resolution of an ADC is smallest change that can be distinguished in the analog input.
  Resolution = FSR (Full Scale Range) / 2^n
- **Conversion Time**
  The A/D conversion another critical parameter is conversion time. This is defined as the total time required converting an analog signal into its digital output.
- **Accuracy**
  It is the comparison of the actual output and the expected output.
- **Linearity**
  The output should be the linear function of input.
- **Full scale output value**
  The maximum bit output achieved from the respective input.

Types of ADC

1. Successive Approximation A/D Converter

It is one of the most used ADC.
Conversion time is faster than Dual slope but slower than Flash.
It has fixed conversion time for any value of analog input.

Successive approximation register generates a series of bit and DAC convert it into analog value which is compared with output. For 4-bit ADC, 1000 is generated and the analog value of 1000 is compared with the output. If it is greater, 1 is flipped to 0 otherwise retained. Then in next clock cycle the second bit is changed to 1 and the whole cycle continues till every bit is flipped and checked.

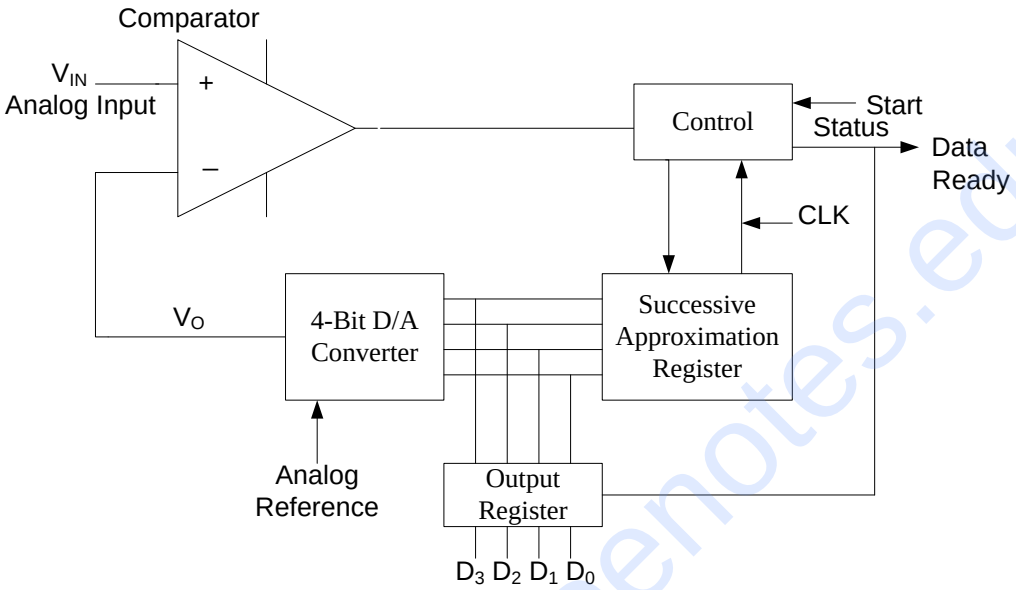


Fig. 4.2: Block diagram of successive approximation A/D converter

It includes three major elements: the A/D converter, the successive approximation register (SAR) and the comparator. The conversion technique involves comparing the output of the D/A converter V_O with the analog input signal V_{in}. When the DAC output matches the analog signal, the input to the DAC is the equivalent digital signal. In the case of a 4-bit A/D converter, bit D_3 is turned on first and the output of the DAC is compared with an analog signal. If the comparator changes the state, indicating that the output generated by D_3 is larger than the analog signal, bit D_3 is turned off in the SAR and bit D_2 is turned on. The process continues until the input reaches bit D_0.

2. The Counter type ADC

The analog input is the V^+ input to the comparator. As long as it is greater than V^- input, the AND gate is enabled and clock pulses are passed to the counter. The digital output of the counter is converted to an analog voltage by the DAC and that voltage is the other input to the comparator. Thus the counter counts up until its output has a value equal to the analog input. At that time, comparator switches low inhibiting the clock pulses and counting ceases. The count it reached is the digital output proportionate to the analog input. Control circuitry shown in fig 4.3 is used to latch the output and reset the counter. This scheme uses long time for conversion.

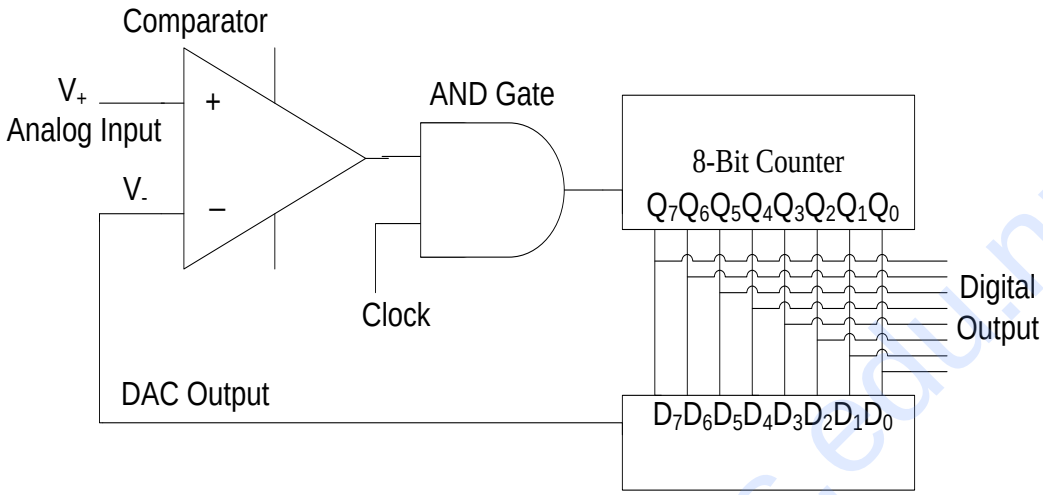


Fig. 4.3: Block diagram of an 8-bit counter type ADC

3. Parallel Comparator ADC (Flash Type ADC)

- The Flash Type ADC (Simultaneous ADC) is the fastest ADC that utilizes comparators that compares reference voltage with input analog voltage.
- A priority encoder is used to convert the output of comparator into digital output.
- For n-bit ADC 2n-1 comparators are required, so this is very expensive.
- It's conversion time is less and can even digitize video signal.

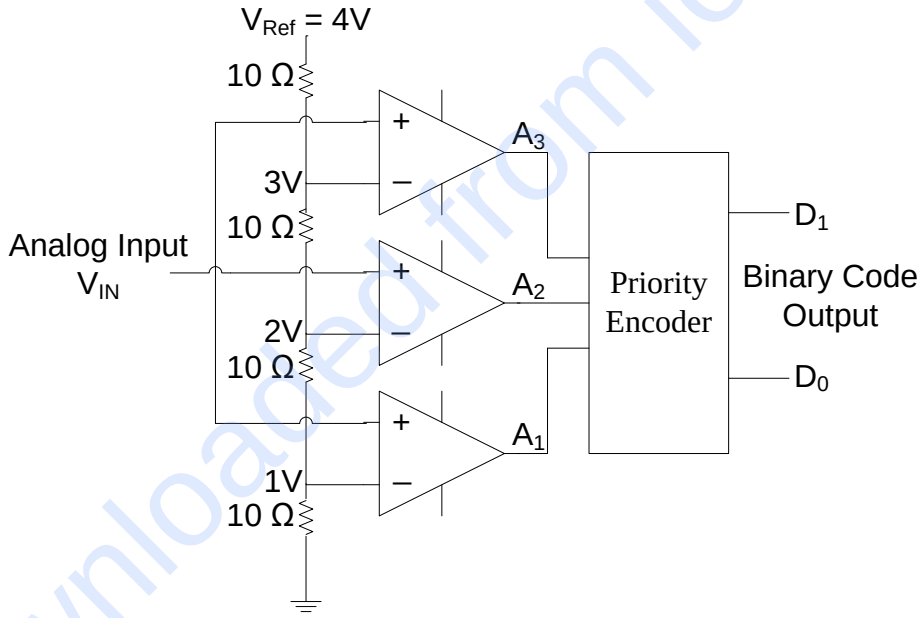


Fig. 4.4: Parallel Comparator ADC

Advantages: Very Fast, Clocks not required. **Disadvantages:** Expensive, Consume high power, Complexity doubles for each additional bit.

Fig. 4.4 shows a circuit for 2-bit ADC using parallel comparators. A voltage divider sets reference voltage on the inverting input's of each of the comparator. The voltage at the top of the divider chain represents the full scale value for the converter. The voltage to be converted is

applied to the non-inverting inputs of all the comparators in parallel. If the input voltage on a comparator is greater than the reference voltage on the inverting input, the output of the comparator will go high. The outputs of the comparators then give us a digital representation of the voltage level of the input signal.

V_{IN}	A_3	A_2	A_1	D_1	D_2
$0 \le V_{IN} \le 1$	0	0	0	0	0
$1 \le V_{IN} \le 2$	0	0	1	0	1
$2 \le V_{IN} \le 3$	0	1	1	1	0
$3 \le V_{IN} \le 4$	1	1	1	1	1

For an example, with an input voltage of 2.6 V, the output of comparators A1 and A2 will be high. A priority encoder produces a binary output corresponding to the input having the highest priority. In this case, the one representing the largest voltage level equal to or less than analog input. Thus, the binary output closely represents the analog input voltage. Although it is expensive, the conversion time is fast.

4. Ramp ADC / Dual slope ramp ADC

Conversion from analog to digital form inherently involves comparator action where the value of the analog voltage at some point in time is compared with some standard. A common way to do that is to apply the analog voltage to one terminal of a comparator and trigger a binary counter which drives a DAC. The output of the DAC is applied to the other terminal of the comparator. Since the output of the DAC is increasing with the counter, it will trigger the comparator at some point when its voltage exceeds the analog input. The transition of the comparator stops the binary counter, which at that point holds the digital value corresponding to the analog voltage. This has the advantage that a slow comparator cannot be disturbed by fast input changes.

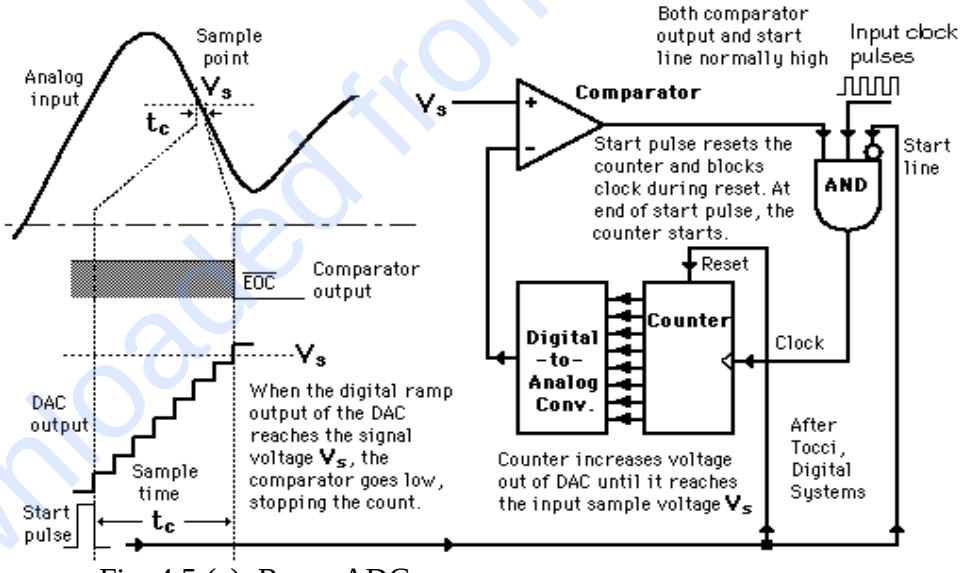


Fig. 4.5 (a): Ramp ADC

Dual Slope ADC is used in the Digital Voltmeter and other type of measuring instruments because of its large resolution and low cost.

A ramp generator (integrator) is used to produce the dual slope characteristics.

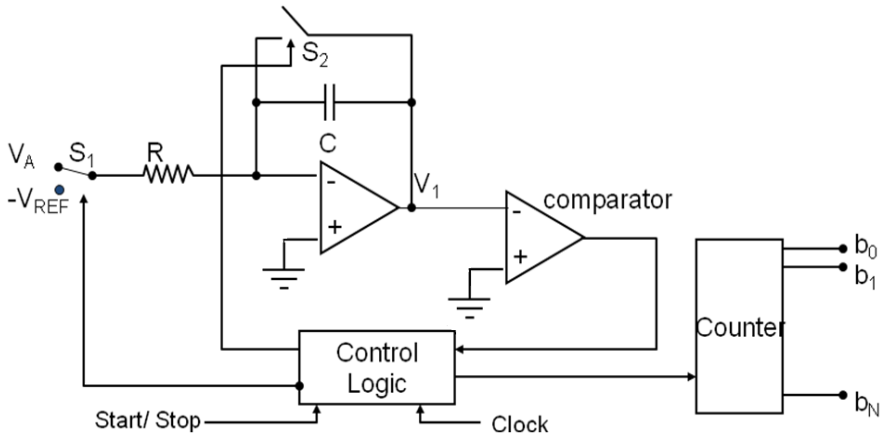
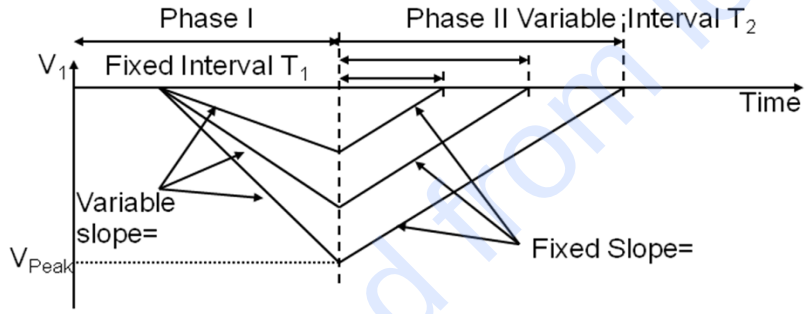


Fig. 4.5 (b): Dual Slope Ramp ADC

Operation:

- First of all capacitor is reset (i.e. Vo is made zero)
- For positive Vin we need negative Vref.
- During time T1, the capacitor is charged by the Vin for fixed time interval which is controlled by the control unit with a fixed current (I = Va/R).
- After time T1, the control unit switches the connection from Vin to –Vref through which the capacitor is discharged. This discharge through the fixed slope until it
- becomes zero which is sensed by the comparator. The reading of the counter is the output for the input.



5. Integrator ADC

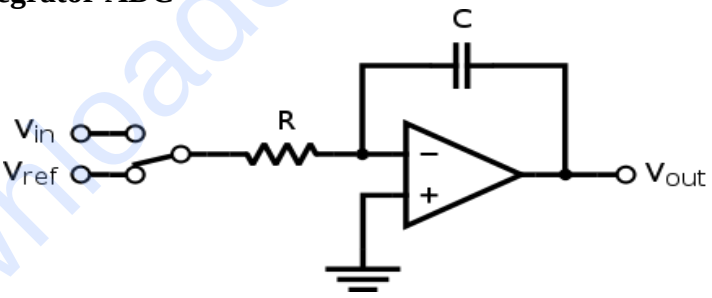


Fig. 4.6: Integrator ADC

The basic integrating ADC circuit consists of the op-amp integrator and a switch to select between the voltage to be measured and the reference voltage. Depending on the implementation, a switch may also be present in parallel with the integrator capacitor to allow the integrator to be reset (by discharging the integrator capacitor). The switches will be controlled electrically by means of the converter's controller (a microprocessor or dedicated

control logic). Inputs to the controller include a clock (used to measure time) and the output of a comparator used to detect when the integrator's output reaches zero.
The conversion takes place in two phases: the run-up phase, where the input to the integrator is the voltage to be measured, and the run-down phase, where the input to the integrator is a known reference voltage. During the run-up phase, the switch selects the measured voltage as the input to the integrator. The integrator is allowed to ramp for a fixed period of time to allow a charge to build on the integrator capacitor. During the run-down phase, the switch selects the reference voltage as the input to the integrator. The time that it takes for the integrator's output to return to zero is measured during this phase.

Q. Calculate the maximum conversion time of a successive approximation ADC and an 8-bit staircase ramp ADC, if the clock rate is 2MHz.
For a 8-bit successive approximation ADC, the conversion time is constant and equal to

$$T_c = \frac{n}{f} = \frac{8}{2\times10^6} = 4\times10^{-6}s = 4\mu s$$

For a 8-bit staircase ramp ADC, the maximum number of count is

$n_c = 2^8 = 256$

Therefore, the maximum conversion time is

$$T_c = \frac{n_c}{f} = \frac{256}{2\times10^6} = 128\times10^{-6}s = 128\mu s$$

It can be noted that the conversion speed of successive approximation ADC is much faster than the staircase ramp type.

Interfacing an 8-Bit ADC using Status Check

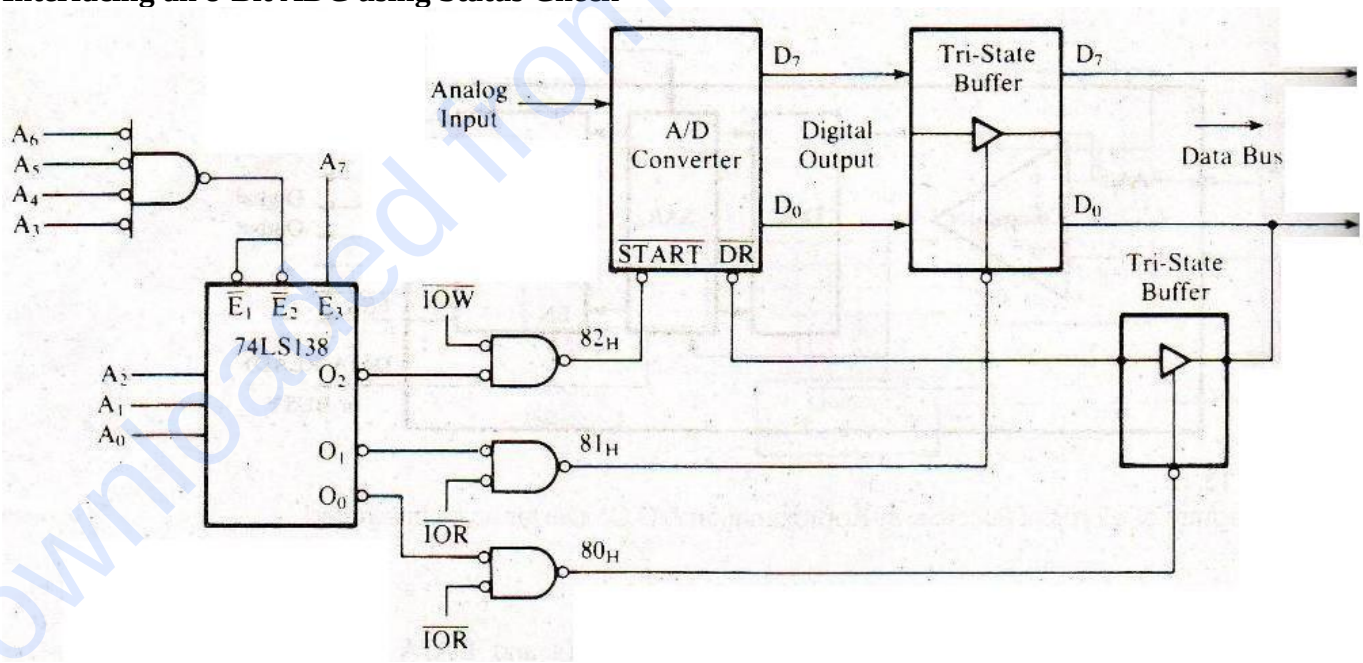
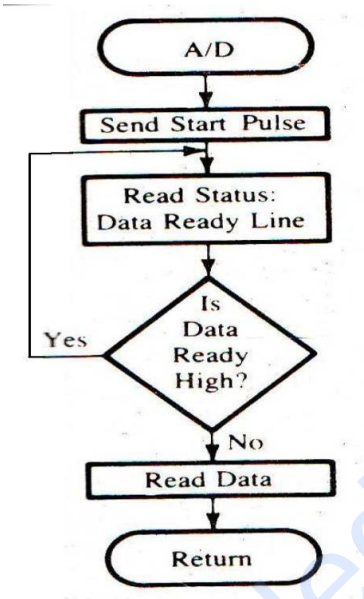


Fig: Interfacing an ADC using Status Check

- Above figure shows a schematic of interfacing a typical ADC using status check.
- ADC has one input line for analog signal and eight output lines for converted digital signals.
- Typically, analog signal can range from 0 to 10V or ±5V.
- When an active low pulse is sent to the $\overline{START}$ pin, the $\overline{DR}$ goes high and the output lines go into high impedance state.
- The $\overline{START}$ pulse initiates conversion.
- When the conversion is complete, the $\overline{DR}$ goes low and data are made available on the output lines that can be read by the microprocessor.
- To interface A/D converter, we need one output port to and a $\overline{START}$ pulse and two input ports one to check the status of $\overline{DR}$ line and the other to read the output of the converter.
- The subroutine instructions to initiate the conversion and to read output data, and the flowchart are shown below.




```
        OUT 82H; Start conversion
Test:   IN 80H; Read data ready status
        RAR; Rotate D0 into carry

        JC TEST; If D0=1, conversion is not yet complete,
                 ; go back and check

        IN 81 H; read output and save it in accumulator
        RET
```

Fig: Flowchart of ADC Process

Interfacing an 8-Bit ADC using Interrupt

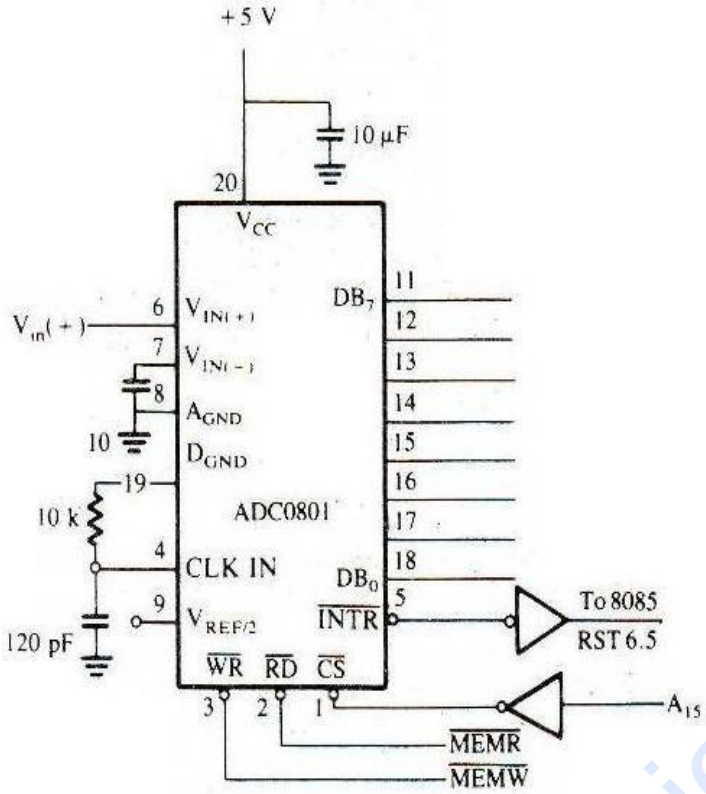


Fig: Interfacing ADC 0801 using Interrupt

- In ADC interfacing using status check, we need external ports to access data and monitor the data ready signal. In this configuration using Interrupt, the necessary logic is built inside the chip.
- The converter requires a clock at CLK IN; the frequency range can be from 100 KHZ to 800 KHZ.
- The user has two options; either to connect an external clock at CLK IN or to use the built in internal clock by connecting a register and a capacitor externally at pins 19 & 4 respectively.
- The frequency is calculated by using the formula F = 1 / 1.1 RC.
- The ADC0801 is designed to be microprocessor compatible. It has three control signals: $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ that are used for interfacing. To start conversion, the $\overline{CS}$ and $\overline{WR}$ signals are asserted low.
- When $\overline{WR}$ goes low, the internal SAR is reset and the output lines go into the high impedance state. When $\overline{WR}$ makes transition from low to high, the conversion begins.
- When the conversion is completed, the $\overline{INTR}$ is asserted low and the data are placed on the output lines. $\overline{INTR}$ signal can be used to interrupt the processor.
- When the processor reads the data by asserting $\overline{RD}$, the $\overline{INTR}$ is set.
- When Vcc is +5V, the input voltage can range from 0V to 5V and the corresponding output will be from 00H to FFH.

- However, the full-scale output can be restricted to the lower range of inputs by using pin 9 (Vref/2). For example, if we connect a 0.5V DC source at pin 9, we can obtain full scale output FFH for a 1V input signal.

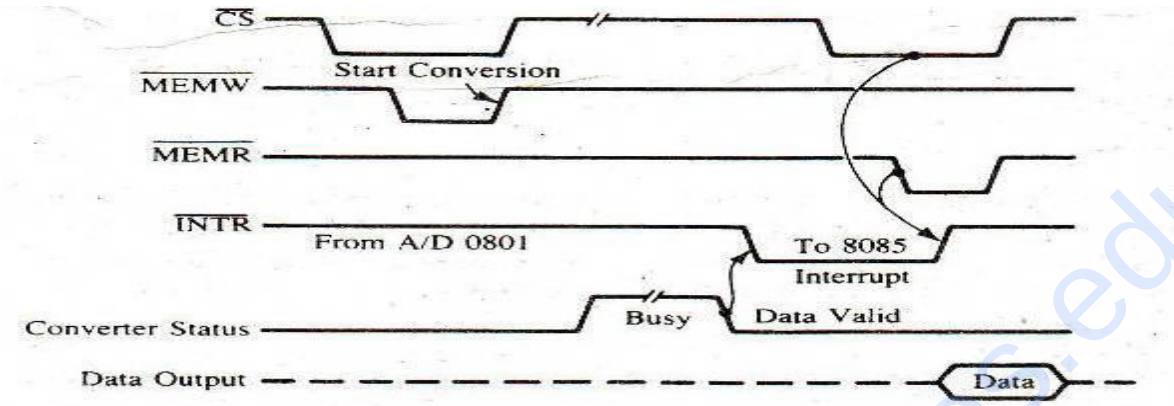


Fig: Timing diagram for Reading Data from ADC

Service Routine:

```
LDA 8000H;   Read data
MOV M, A ;   store data in memory
INX H;       Next  memory location
DCR B;       Next count
STA 8000H;   start next conversion
EI;          Enable interrupt again
RNZ;         Go back to main if counter not equal to zero
HLT
```

Sample and Hold Circuit:

A Sample and Hold circuit is used before analog signal is fed to ADC, so that the value of analog input can be kept constant and conversion can be done with constant value. Start/ EOC signals are used for interfacing.

The result of sampling process is identical to multiplying the analog signal by a train of pulses of unit magnitude. Sample and hold circuit is used when it is necessary to hold the sampled value of input signal for specified period of time. Sample and hold circuit is used in order to avoid the use of very fast and expensive A/D converters.

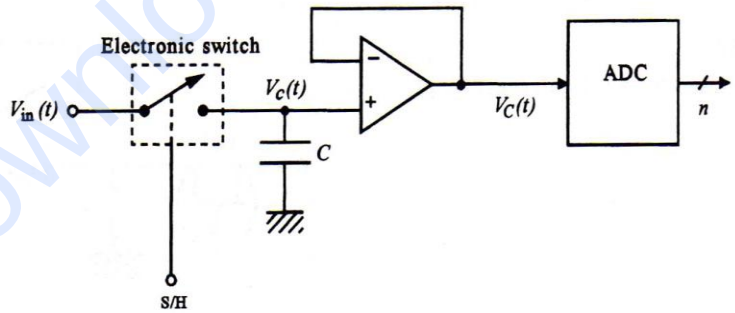


Fig.: Sample and Hold Circuit

- When the conversion is needed the switch is opened, isolating the capacitor from the input
- The capacitor will hold the voltage when switch is opened
- The capacitor will not discharge due to the high impedance of the voltage follower

Quantization

It is the process of converting an input function having continuous values to an output having only discrete values.

Binary Coding

It is the method of assigning a binary equivalent number to each discrete level.

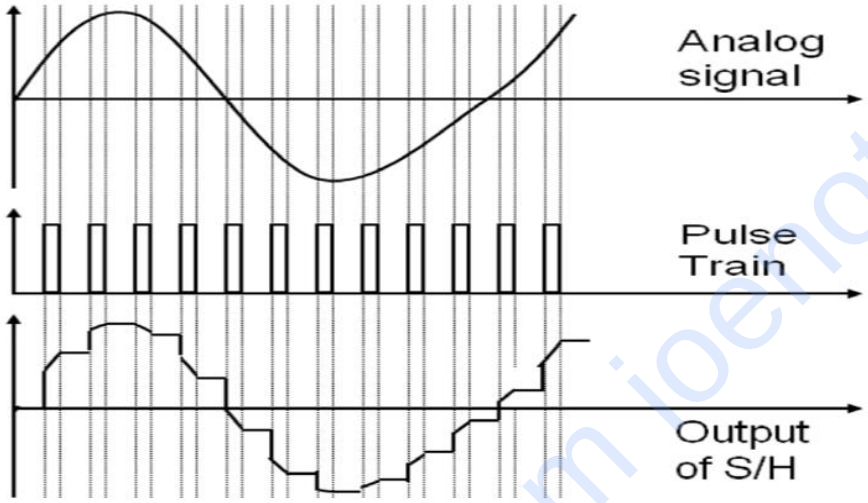


Fig: Sampling of Signal

Sampling Rate:

The Analog Signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called the Sampling Rate or Sampling Frequency of the converter. A continuously varying band limited signal can be sampled and then the original signal can be exactly reproduced from the discrete-time values by an interpolation formula. The accuracy is limited by quantization error. However, this faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal. This is essentially what is embodied in the Shannon-Nyquist Sampling Theorem.

Since a practical ADC cannot make an instantaneous conversion, the input value must necessarily be held constant during the time that the converter performs a conversion (called the Conversion Time). An input circuit called a Sample and Hold performs this task in most cases by using a capacitor to store the analog voltage at the input, and using an electronic switch or gate to disconnect the capacitor from the input. Many ADC integrated circuits include the sample and hold subsystem internally.

Aliasing:

If the digital values produced by the ADC are converted back to analog values by a DAC, it is desirable that the output of the DAC be an exact replica of the original signal. If the input signal is changing much faster than the sample rate, then this will not be the case, and spurious signals (false) called aliases will be produced at the output of the DAC. For example, a 2 kHz sine wave being sampled at 1.5 kHz would be reconstructed as a 500 Hz sine wave. This problem is called aliasing. To avoid aliasing, the input to an ADC must be low-pass filtered to remove frequencies above half the sampling rate. This filter is called an Anti-aliasing Filter, and is essential for a practical ADC system that is applied to analog signals with higher frequency content.

Dither:

In ADC, performance can usually be improved using dither. This is a very small amount of random noise (white noise), which is added to the input before conversion. The result is an accurate representation of the signal over time. A suitable filter at the output of the system can thus recover this small signal variation. An audio signal of very low level (with respect to the bit depth of the ADC) sampled without dither sounds extremely distorted and unpleasant. Without dither the low level may cause the least significant bit to "stick" at 0 or 1. With dithering, the true level of the audio may be calculated by averaging the actual quantized sample with a series of other samples (the dither) that are recorded over time.

Sampling Theorem (Nyquist sampling theorem)

The theorem is commonly called the Nyquist sampling theorem, is a fundamental result in the field of information theory, in particular telecommunications and signal processing. Sampling is the process of converting a signal (for example, a function of continuous time or space) into a discrete sequence (a function of discrete time or space). Sampling theorem states: If a function $x(t)$ contains no frequencies higher than B hertz, it is completely determined by giving its ordinates at a series of points spaced $1/(2B)$ seconds apart.

In other way; a continuous time signal may be completely represented in its samples and recovered back if the sampling frequency fs ≥ 2fm. Here, fs is the sampling frequency and fm is the maximum frequency present in the signal.

A signal or function is band limited if it contains no energy at frequencies higher than some band limit or bandwidth B. A signal that is band limited is constrained in how rapidly it changes in time, and therefore how much detail it can convey in an interval of time. The sampling theorem asserts that the uniformly spaced discrete samples are a complete representation of the signal if this bandwidth is less than half the sampling rate. To formalize these concepts, let $x(t)$ represent a continuous-time signal and $X(f)$ be the continuous Fourier transform of that signal:

$$X(f) \ \stackrel{\text{def}}{=} \ \int_{-\infty}^{\infty} x(t)\ e^{-i2\pi ft}\ dt.$$

The signal $x(t)$ is said to be band limited to a one-sided baseband bandwidth, B, if:

$$X(f) = 0 \ \text{ for all } \ |f| > B$$

or, equivalently, supp(X)[2] $\subseteq$ $[-B, B]$. Then the sufficient condition for exact reconstructability from samples at a uniform sampling rate f_s(in samples per unit time) is:

$$f_s > 2B,$$

or equivalently:

$$B < \frac{f_s}{2}.$$

2*B* is called the *Nyquist rate* and is a property of the band limited signal, while f_s / 2 is called the *Nyquist frequency* and is a property of this sampling system.

The time interval between successive samples is referred to as the *sampling interval*:

$$T \stackrel{\text{def}}{=} \frac{1}{f_s},$$

and the samples of *x*(*t*) are denoted by:

$x[n] = x(nT) \quad n \in \mathbb{Z}$ (integers).

The sampling theorem leads to a procedure for reconstructing the original *x*(*t*) from the samples and states sufficient conditions for such a reconstruction to be exact.

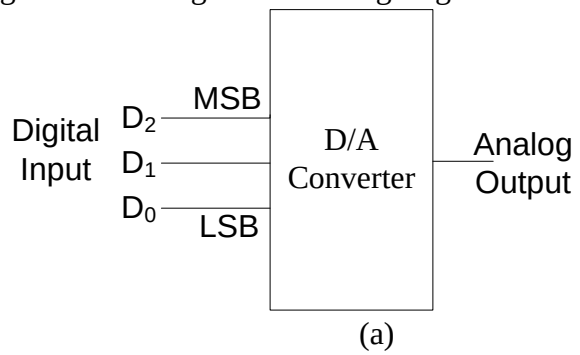
What happens if we sample the signal at a frequency that is lower that the Nyquist rate? When the signal is converted back into a continuous time signal, it will exhibit a phenomenon called aliasing. Aliasing is the presence of unwanted components in the reconstructed signal. These components were not present when the original signal was sampled. In addition, some of the frequencies in the original signal may be lost in the reconstructed signal. Aliasing occurs because signal frequencies can overlap if the sampling frequency is too low. Frequencies "fold" around half the sampling frequency - which is why this frequency is often referred to as the folding frequency.

Sometimes the highest frequency components of a signal are simply noise, or do not contain useful information. To prevent aliasing of these frequencies, we can filter out these components before sampling the signal. Because we are filtering out high frequency components and letting lower frequency components through, this is known as low-pass filtering.

Digital-to-Analog Converter (DAC)

DAC converts straight binary to analog voltage or current proportional to the digital value. DAC can be broadly classified in three categories: Current Output, Voltage Output and Multiplying Type.

Voltage output DAC is comparatively slower than Current output DAC because of the delay in converting the current signal into voltage signal.



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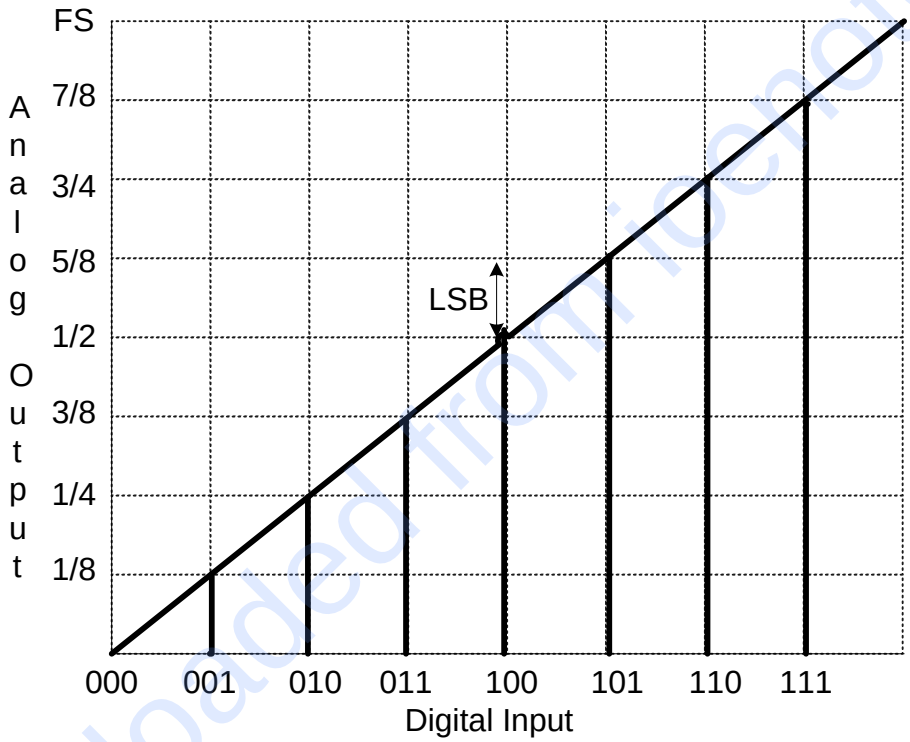


Fig. : A 3-bit D/A converter

- The three input lines D_2, D_1 and D_0 can assume 8 input combinations from 000 to 111.
- If the full scale analog voltage is 1V, the smallest unit or the LSB (Least Significat Bit) 001_2 is equivalent to $1/2^n$ of 1V. This is defined as resolution. Here, LSB $(001)_2$ = 1/8 V.
- The MSB (Most Significat Bit) represents half of the full scale value. Here, MSB $(100)_2$ = 1/2 V.

- For the maximum input signal $(111)_2$, the output signal is equal to the value of the full scale input signal minus the value of 1 LSB input signal. Here, maximum input signal $(111)_2$ represents $(1 – 1 / 8) = 7 / 8$ V.

Parameters (Characteristics) of DAC

- **Resolution**
  It is determined by the number of bits in the input binary word. A 12-bit converter has a resolution of 1 part in 2^{12}.

- **Full scale output voltage**
  The maximum output voltage of a converter (when all input are 1) will always have a value 1 LSB less than the named value.

- **Accuracy**
  The actual output voltage of a DAC is different from the ideal value; the factors that contribute to the lack of linearity also contribute to the lack of accuracy. The accuracy of a DAC is the measure of difference between actual output voltage and the expected output voltage. For an example, a DAC with ±0.2% accuracy and full scale (maximum) output voltage of 10V will produce a maximum error for an output voltage is of 20 mV. [0.2/100 * 10V = 0.002*10 V = 20mV]

- **Linearity**
  An ideal DAC should be linear i.e. the output voltage should be a linear function of the input code. All DAC depart somewhat from the ideal linearity. Typical factors responsible for introducing non-linearity are non-exact value of resistors and non-ideal electronic switches that introduce extra resistance to the circuit. The non-linearity (linearity error) is the amount by which the actual output differs from the ideal straight line output.

- **Settling time**
  When the output of DAC changes from one value to another, it typically overshoots the new value and may oscillate briefly around that new value before it settles to a constant value. It is the time interval between the instant when the analog input passes a specified value and the time instant when the analog output enters for the last time a specified error band about its final value.

- **Monotonicity**
  A converter is said to be monotonic if its output voltage value continuous to increase with a continuously increasing input value.

- **Temperature Coefficient**
  It is defined as the degree of inaccuracy that the temperature change can cause in any of the parameter of the DAC.

Types of DAC:

1) DAC with Binary Weighted Resistor Network (WRN):

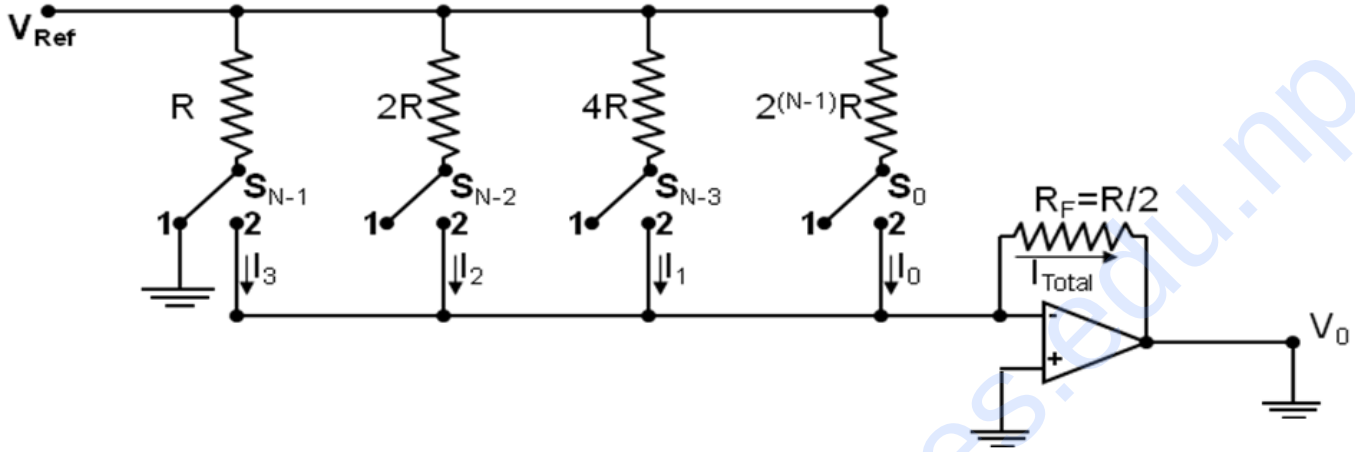


Fig: DAC with Binary Weighted Resistor Network

WRN DAC circuit consists of

- Reference voltage VRef
- N Binary weighted resistors R, 2R, 4R,…. 2N-1R
- Single Pole Double Throw (SPDT) Switches S0, S1, S2…. SN-1
- Op Amp with feedback resistance RF=R/2

Switches controlled N-bit digital input word

$$I_{Total} = \frac{V_{Ref}}{R} b_{N-1} + \frac{V_{Ref}}{2R} b_{N-2} + \ldots + \frac{V_{Ref}}{2^{N-1}R} b_0$$

$$I_{Total} = \frac{2V_{Ref}}{R}\left(\frac{b_{N-1}}{2^1} + \frac{b_{N-2}}{2^2} + \ldots + \frac{b_0}{2^N}\right) = \frac{2V_{Ref}}{2^N R} D$$

$$V_o = -I_{Total} R_F = -\frac{V_{Ref}}{2^N} D$$

$$\therefore V_o = -\frac{V_{Ref}}{2^N} D$$

Accuracy of Binary Weighted DAC depends critically on

- ✓ Accuracy of VRef
- ✓ Precision of Binary weighted resistors
- ✓ Perfection of switches

Drawbacks of Binary Weighted DAC:

Large spread between smallest and largest resistance for higher no. of bits
Precise resistor values not available
Impractical for large number of bits.

2) R-2R Ladder Network

It uses only two resistor values R and 2R. Hence, its implementation in IC form is much easier than the weighted resistor converted.

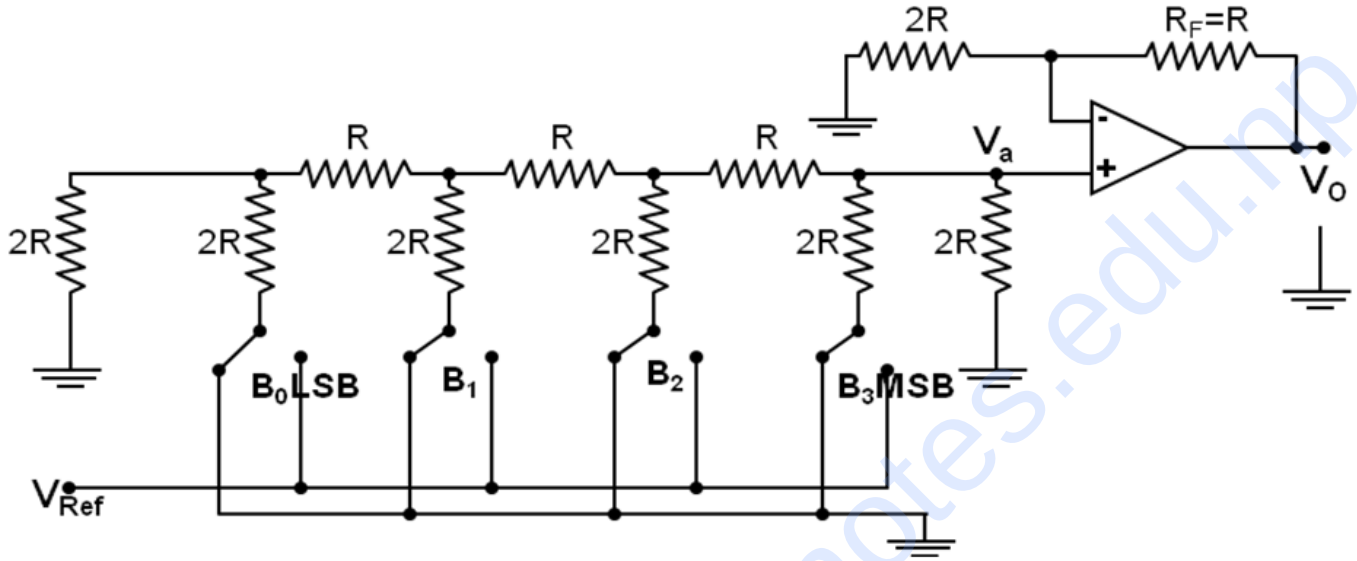


Fig: R-2R Ladder (Voltage Mode)

Working:

When MSB high (1) and all others low (0)

$$I = \frac{V_{Ref}}{(2R//2R)+2R} = \frac{V_{Ref}}{3R}$$

$$V_a = I \times R = \frac{V_{Ref}}{3}$$

$$V_o = \left(1+\frac{R}{2R}\right)V_a = \frac{V_{Ref}}{2}$$

When next MSB bit high (1) and others low (0)

$$V_o = \frac{V_{Ref}}{2^2}$$

Similarly when only LSB is high

$$V_o = \frac{V_{Ref}}{2^n}$$

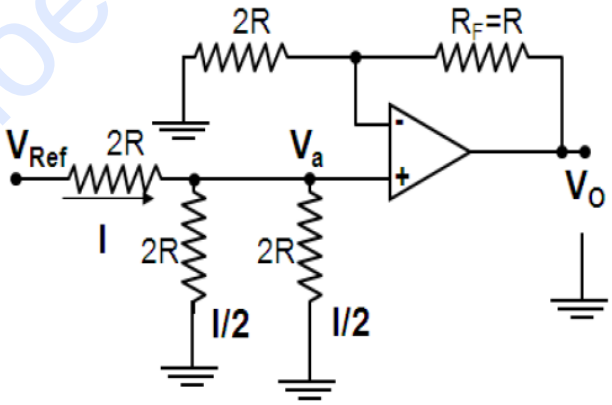


Fig: When MSB High, Other Low

Interfacing 8-Bit DAC with 8085

Q. Design an output port with address FFH to interface the 1408 DAC that is calibrated for 0 to 10 V range.

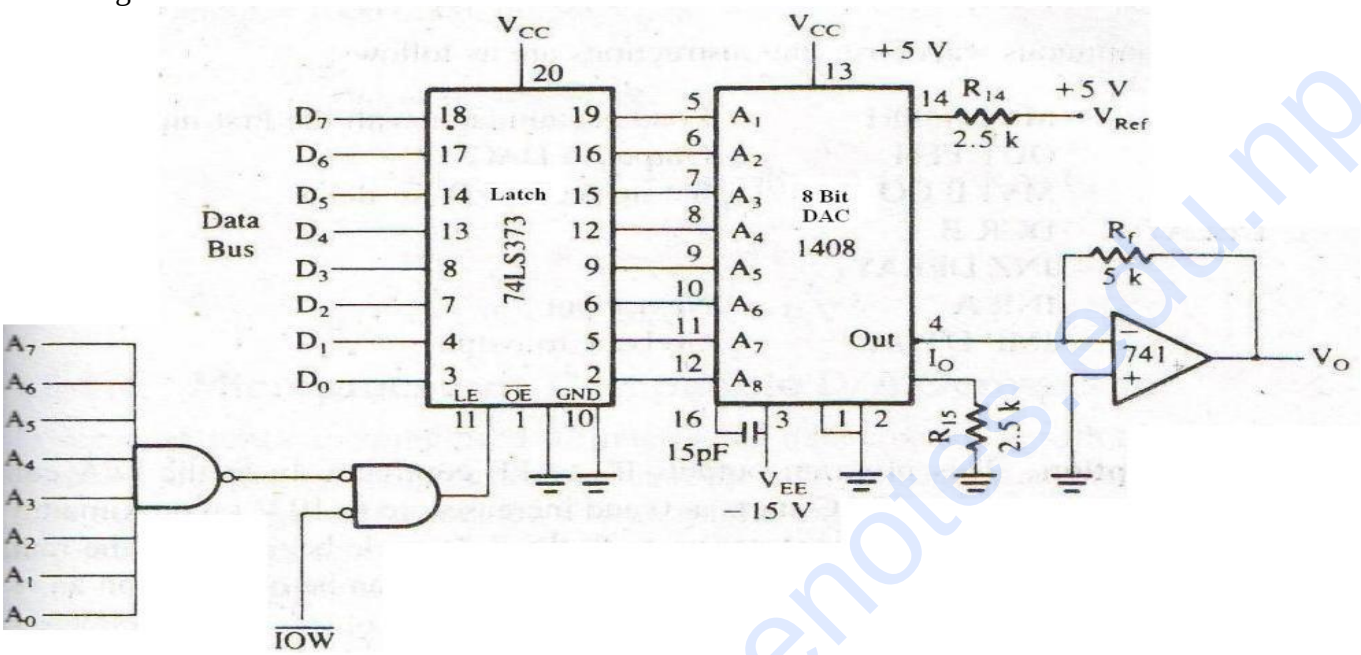


Fig: Interfacing 1408 DAC in Unipolar Range

This includes an 8-input NAND gate and a NOR gate as the address decoding logic, the 74LS373 as a latch, and a 1408 DAC. Address lines (A_7-A_0) are decoded using the 8-input NAND gate and its output is combined with the control signal $\overline{IOW}$. When the microprocessor sends the address FFH, the output of the negative AND gate enables the latch, and the data bits are placed on the input lines of the converter for conversion.

The total reference current source is determined by the resistor R_{14} and the voltage V_{Ref}. The resistor R_{15} is generally equal to R_{14} to match the input impedance of the reference source. The output I_O is calculated as:

$$I_O = V_{Ref}/R_{14}\,(A_1/2 + A_2/4 + A_3/8 + A_4/16 + A_5/32 + A_6/64 + A_7/128 + A_8/256)$$

For full scale input,

I_O = 5V/2.5K (1/2 + ¼ + 1/8 + 1/16 + 1/32 + 1/64 + 1/128 + 1/256)
= 2mA (255/256)
= 1.992mA

Output voltage,

$V_O = I_O * R_F$
= 2mA (255/256) * 5K
= 9.961V

Q. WAP to generate a continuous ramp waveform (8085).

```
        MVI A,00H       ; Load accumulator with the first input
DTOA:   OUT FFH         ; Output to DAC (FF is port address)
        MVI B,COUNT     ; Setup register B for delay
DELAY:  DCR B
        JNZ DELAY
        INR A           ; Next input
        JMP DTOA        ; Go back to output
```

This program outputs 00 to FF continuously to the DAC. Analog output of DAC starts at 0 and increases approximately up to 10V as ramp. Slope of the ramp can be varied by changing the delay.

Q. Explain the operation of the 1408 which is calibrated for a bipolar range ±5V. Calculate output voltage V_O if the input is 10000000_2.

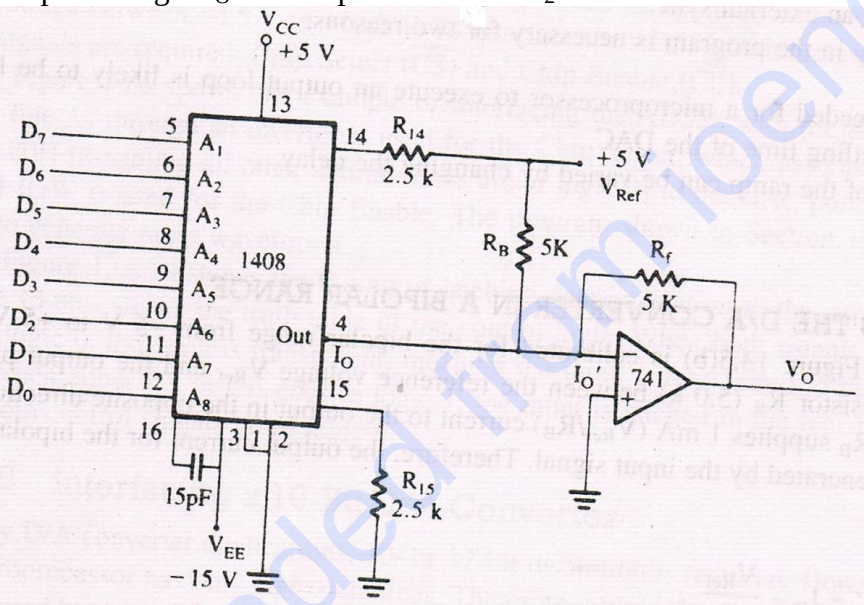


Fig: Interfacing 1408 DAC in Bipolar Range

The 1408 is calibrated for the bipolar range from -5V to +5V by adding the resistor R_B (5.0K) between the reference voltage V_{Ref} and the output pin 4. R_B supplies 1mA (V_{Ref}/R_B) current to the output in the opposite direction of the current generated by input signal.

Here, $I_O' = I_O - V_{Ref}/R_B$

When input signal is zero,

$V_O = I_O' R_F$

$= (I_O - V_{Ref}/R_B) R_F$

$= (0 - 5V/5K) 5K$

$= -5V$

When the input = 1000 0000, output V_O is

$V_O = I_O' R_F$

$= (I_O - V_{Ref}/R_B) R_F$

$= (V_{Ref}/R_{14} * A_1/2 - V_{Ref}/R_B) R_F$ $[A_8\text{-}A_2 = 0]$

$= (5V/2.5K * 1/2 - 5V/5K) 5K$

$= (1mA\text{-}1mA) 5K$

$= 0V$

Microprocessor Compatible DAC

In response to the growing need for interfacing DAC with the microprocessor, specially designed microprocessor-compatible DAC are available. These DAC generally include a latch on the chip, thus eliminating the need for an external latch.

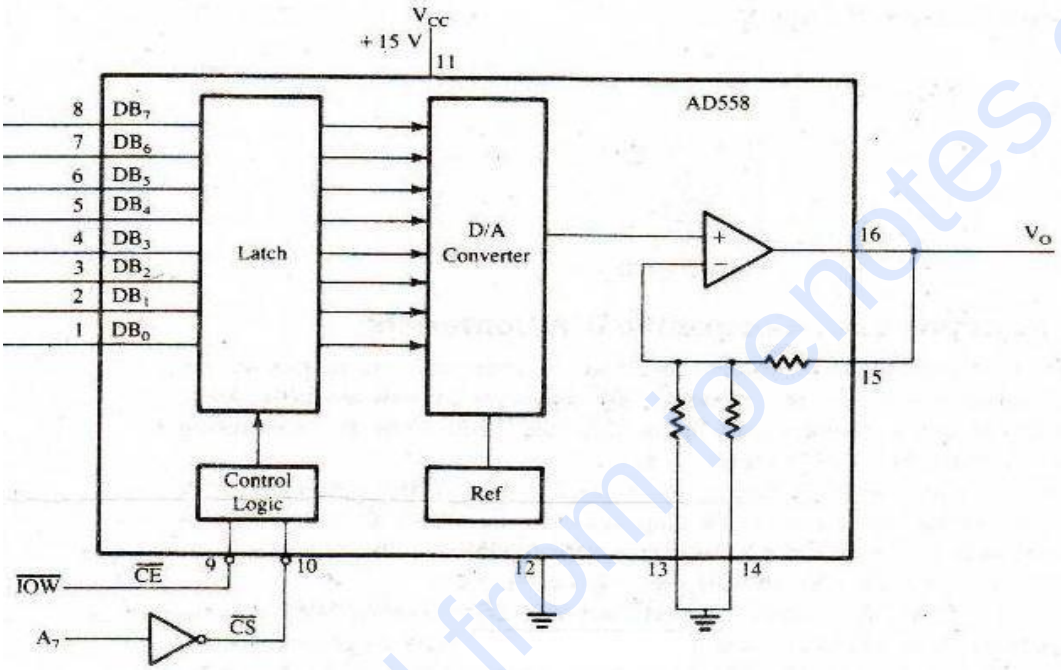


Fig: Block Diagram of Analog Device along with latch and output Op-Amp internal to the Chip

To interface a device with the microprocessor, two signals are required: Chip Select ($\overline{CS}$) and Chip Enable ($\overline{CE}$). In the figure shown above, the address line A7 through inverter is used for Chip Select, which assigns port address 80H (assuming all other address lines 0) to the DAC port.

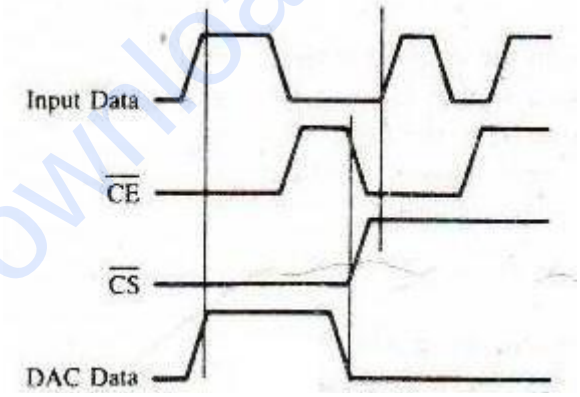


Fig: Timing Diagram: Control Signals and Data Transfer

Figure above shows the timing of latching data in relation to the control signals. When both signals $\overline{CS}$ and $\overline{CE}$ are at logic 0, the latch is transparent, meaning the input is transferred to the DAC. When either $\overline{CS}$ or $\overline{CE}$ goes logic 1, input is latched in the register and held until both control signals go to logic 0.

Interfacing 10-Bit DAC with 8085

In many DAC applications, 10 or 12-bit resolution is required. But microprocessor has only 8-bit data lines. One method is to use two output ports on time shared basis; one for first eight bits and second for the remaining bits. A disadvantage of this method is that the DAC input assumes on intermediate value between two input operations. The solution to this difficulty can be using a double buffer DAC.

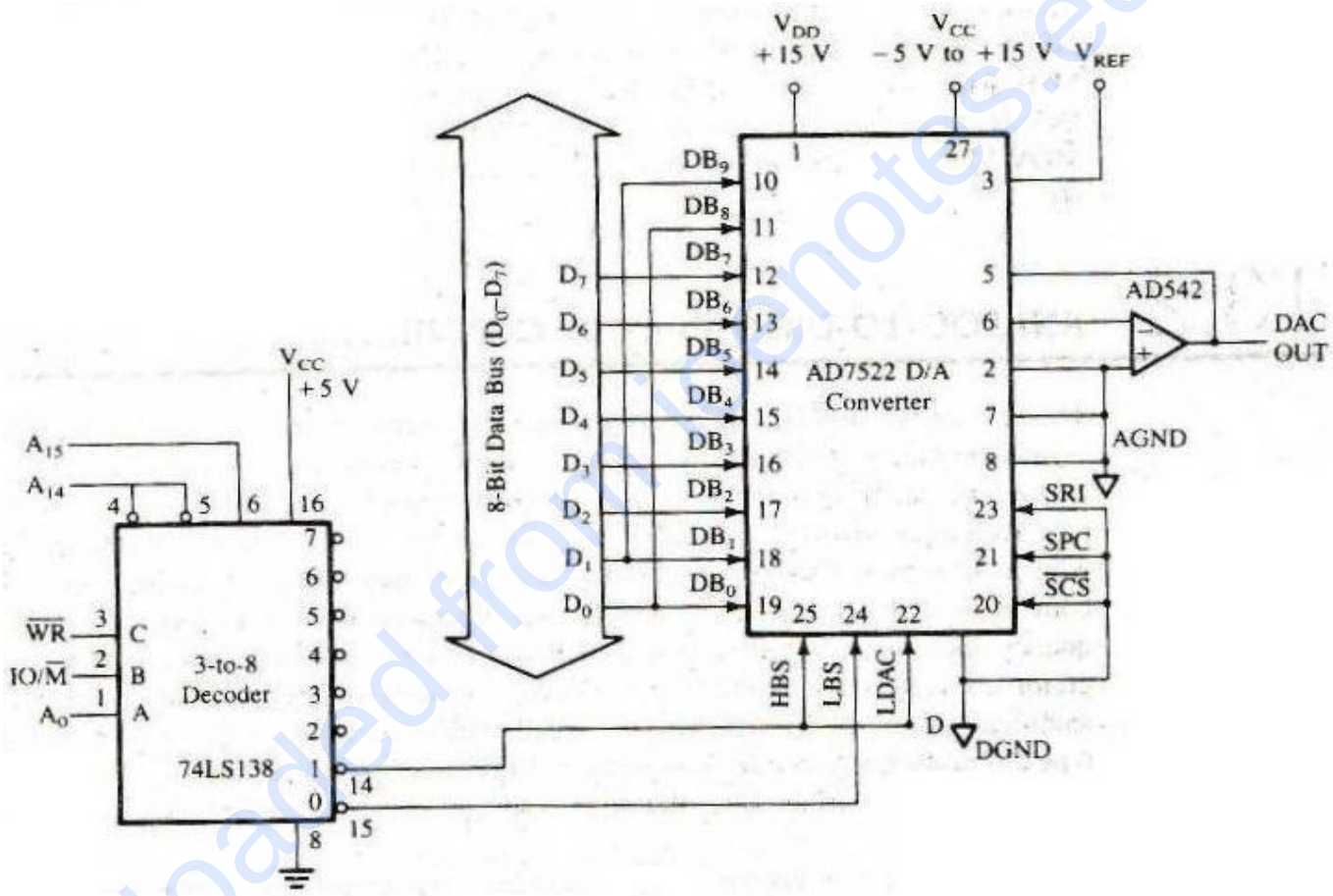


Fig: Interfacing 10-Bit DAC with 8085

- AD7522 is a CMOS 10-bit DAC consists of an input buffer and a holding register. 10 bits are loaded into the input register in two steps using two output ports.
- The low-order 8-bits are loaded with the control line LBS and remaining 2-bits are loaded with the control line HBS. Then all 10-bits are switched into a holding register for conversion by enabling LDAC line.
- When a data byte is sent to the port address 8000H in a memory map I/O, the $\overline{WR}$ and IO/$\overline{M}$ signals go low along with A_0 and the line LBS is enabled. Similarly, the address 8001H enables lines HBS and LDAC.

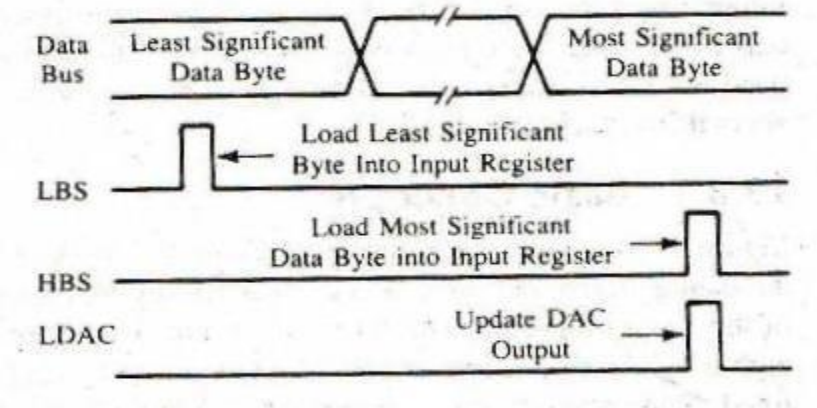


Fig: Timing Diagram

- The following instructions illustrate how to load the maximum input of 10-bits all 1's into the DAC.

```
LXI B, 03FFH;    Load 10-bit at logic 1 in BC register
LXI H, 8000H;    Load HL with port address for lower 8-bits
MOV M, C;        Load 8-bits D7-D0 in the DAC
INX H;           Point to port address 8001H
MOV M, B;        Load two bits D9 and D8 and switch all ten bits for conversion
HLT
```

Interfacing 12-bit DAC to 8-bit Data Bus

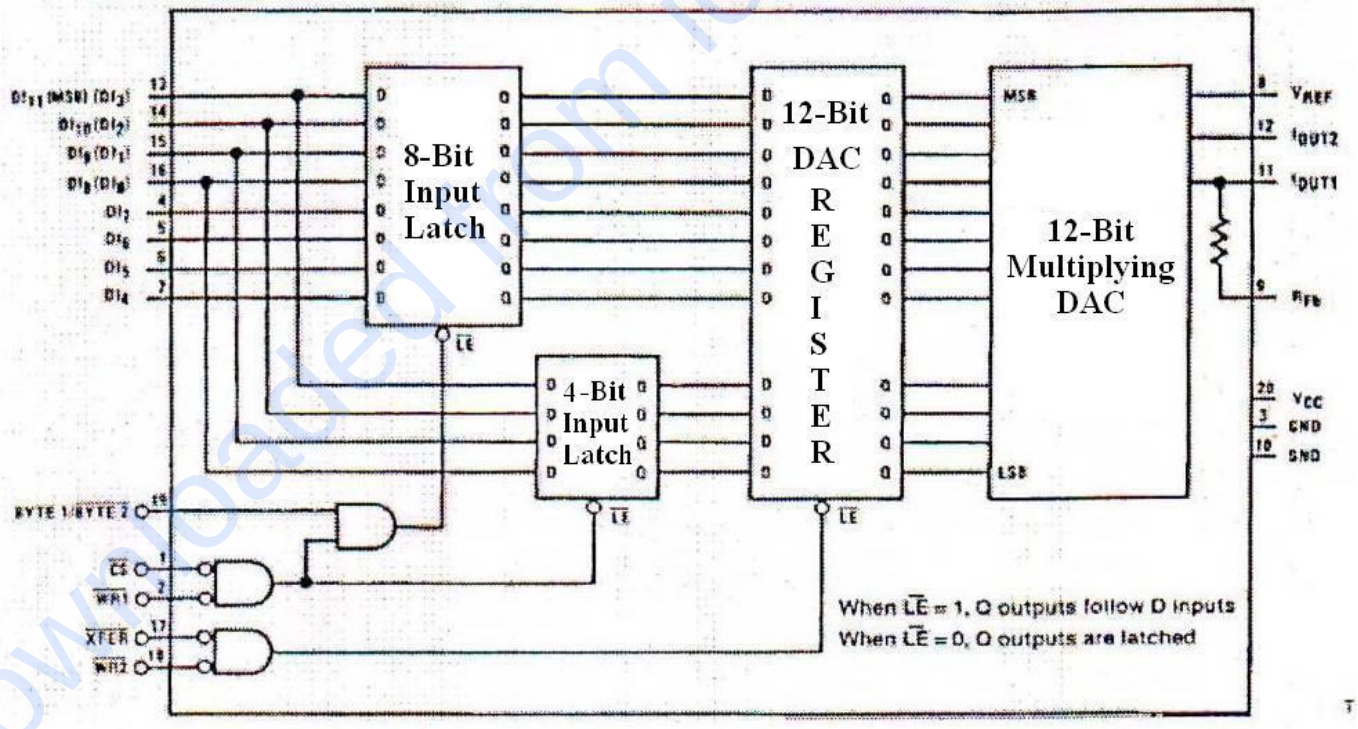


Fig: Interfacing 12-bit DAC to 8-bit Data Bus

Selection of DAC or ADC (Design Requirements)

- Resolution
- Linearity
- DAC: Settling Time
- ADC: Conversion Time
- Accuracy
- Codes Used
- Cost

Errors in ADC and DAC

1. Dynamic Errors

A. Conversion Time

It is the elapsed time between the command to perform a conversion and the appearance at the converter output of the complete digital representation of the analog input value.

B. Delay Time

It is the time interval between the instant when the digital input changes and the instant when the analog output passes a specified value that is close to its initial value.

C. Settling Time

When the output of DAC changes from one value to another, it typically overshoots the new value and may oscillate briefly around that new value before it settles to a constant value. It is the time interval between the instant when the analog output passes a specified value and the instant when the analog output enters for a last time a specified error band about its final value.

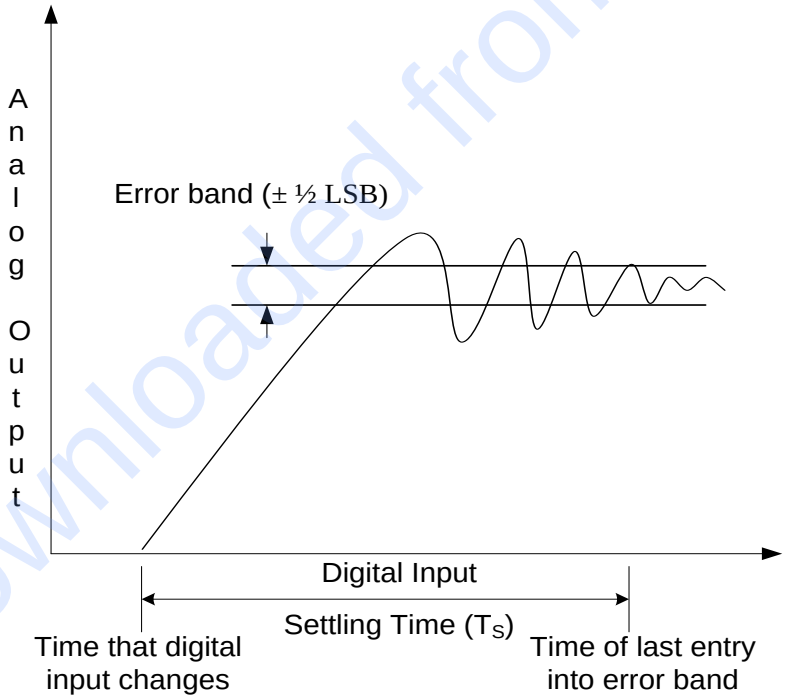


Fig: Settling Time

2. Static Errors

A. Differential Linearity

It is a measure of the separation between adjacent levels. Differential linearity measures the bit-to-bit deviations from ideal output steps rather than entire output range. If V_S is the ideal change and V_{CX} is the actual change, then the differential linearity can be expressed as: $[(V_{CX}-V_S)/V_S]*100\%$

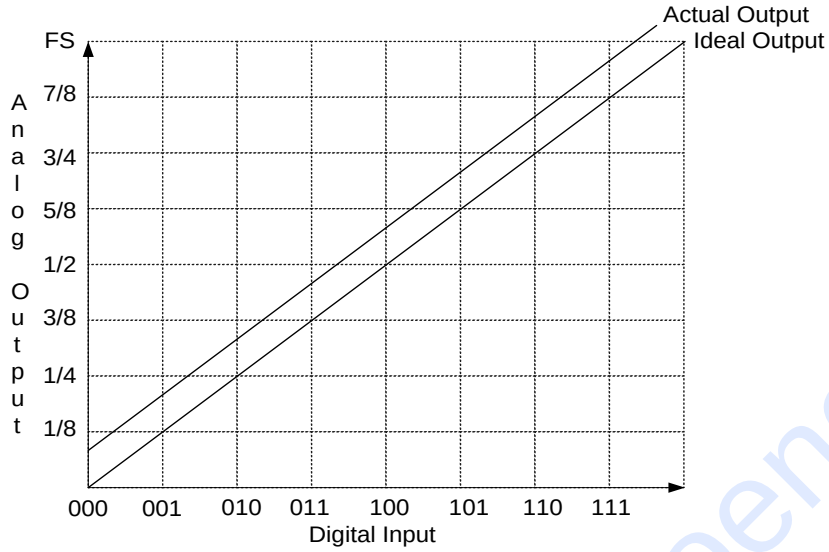


Fig: Differential Linearity Error

B. Monotonicity

In a D/A converter; means that as the digital input to the converter increases over its full scale range, the analog output never exhibit a decrease between one conversion step and next.

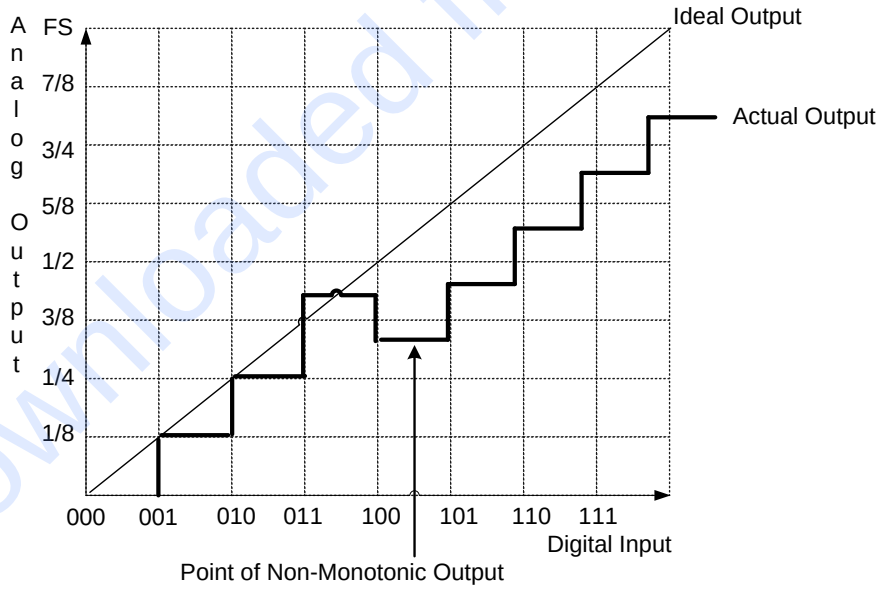


Fig: Non-Monotonic transfer function

C. Integral Linearity

It is the maximum deviation of the output of a D/A for any given input code from a straight line drawn from its ideal minimum to its ideal maximum.

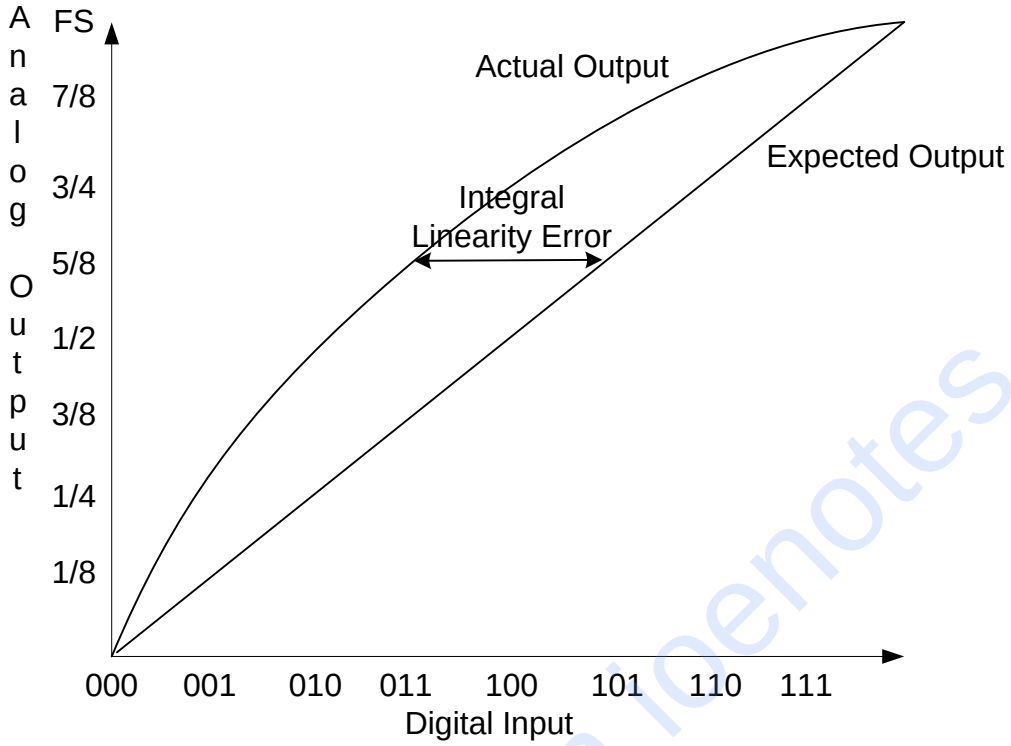


Fig: Integral Linearity error

I. Absolute Linearity

It is measured by assuming that the output of a D/A will begin at zero and end at full scale. The actual outputs are compared with a line drawn through these two points.

a. Zero Error

It is the difference between the actual output and zero when the digital word for a zero output is applied.

b. Full Scale Error

It is the difference between the actual and the ideal voltage when the digital word for a full scale output is applied.

i. Gain Error (Scale Factor Non-Linearity)

It is the difference between the gains of the actual static and ideal input output characteristics.

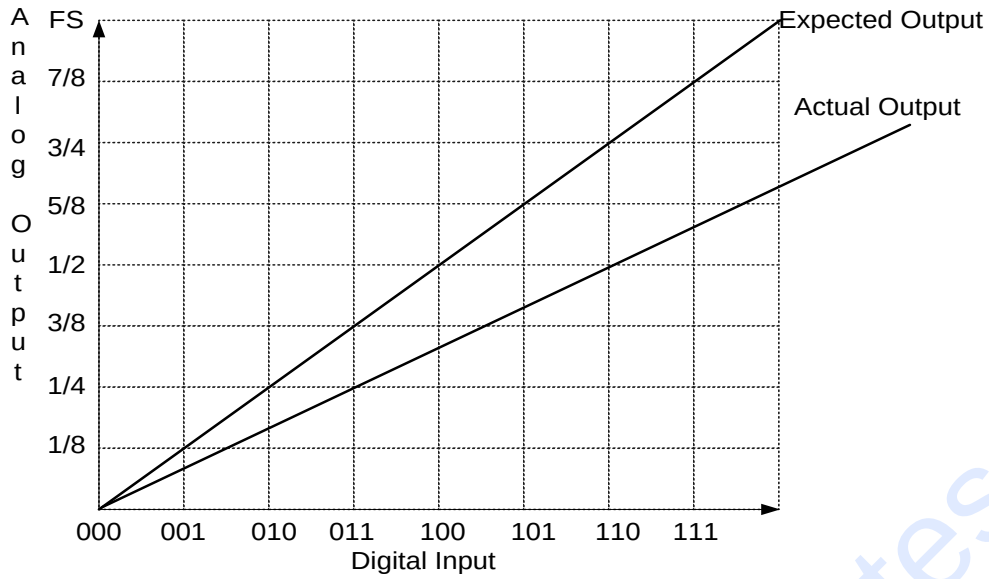


Fig: Gain error

ii. Offset Error

Offset error adds a constant value to output.

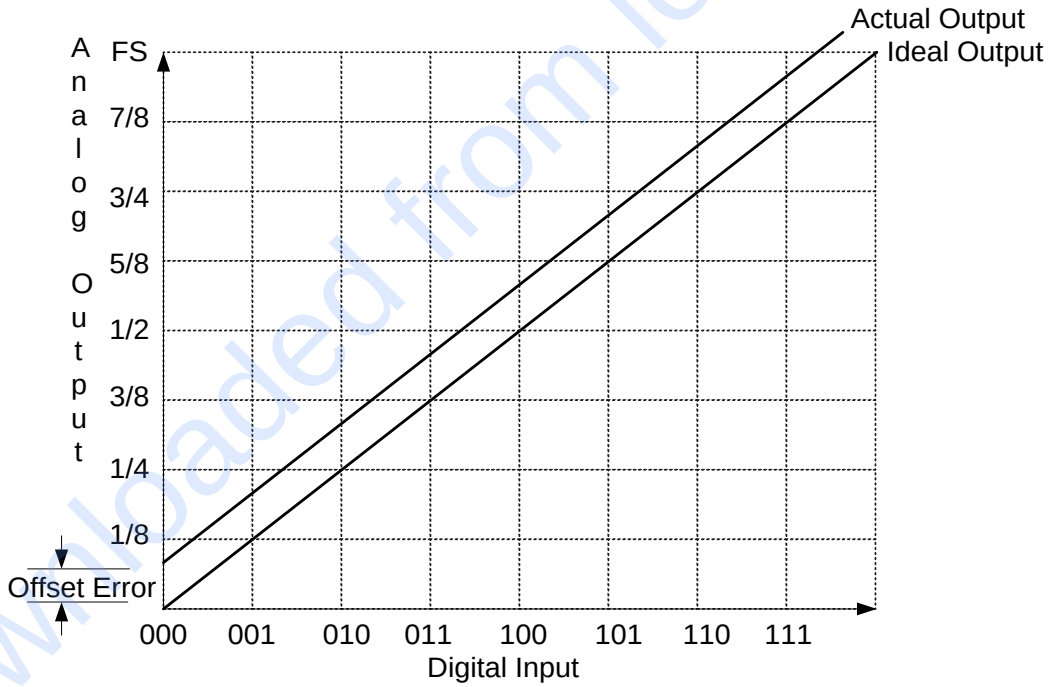


Fig: Offset error

II. Best Straight Line Linearity

It depicts the accuracy of a D/A in terms of the deviation from the ideal output range without regard to zero or full scale errors.

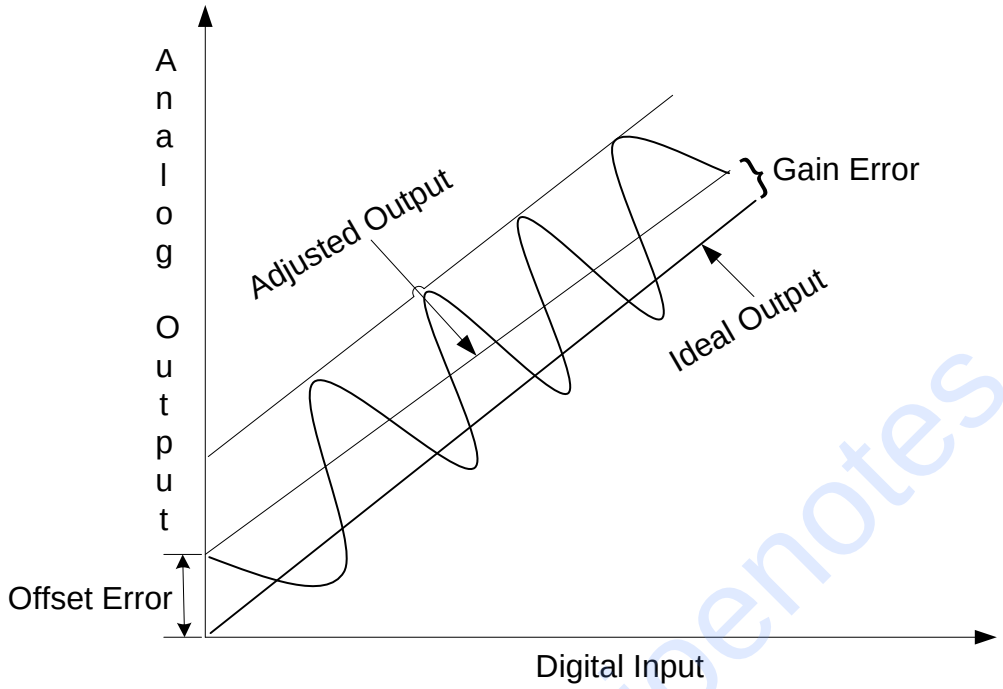


Fig: Best straight line error

III. End Point Linearity

It uses a straight line through the actual end points instead of the ideal points.

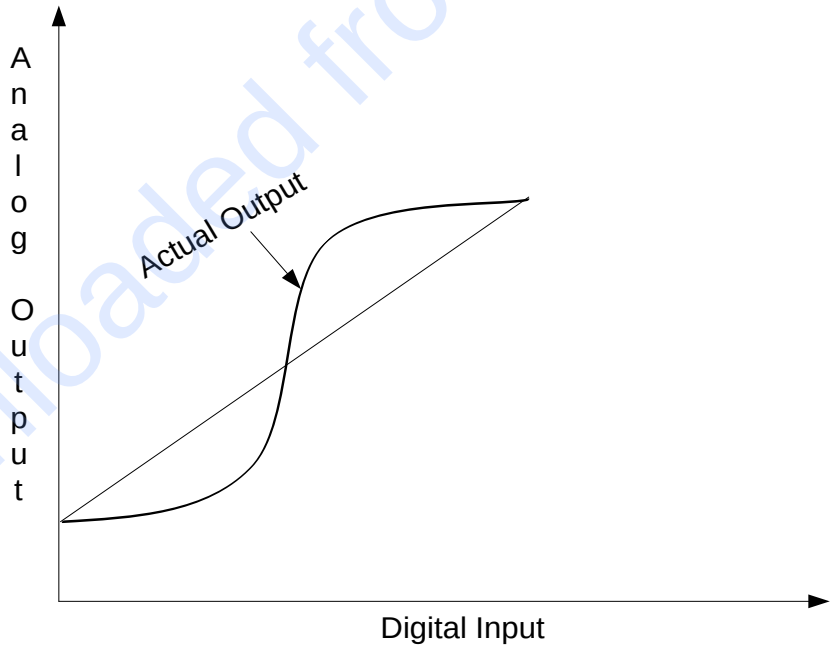
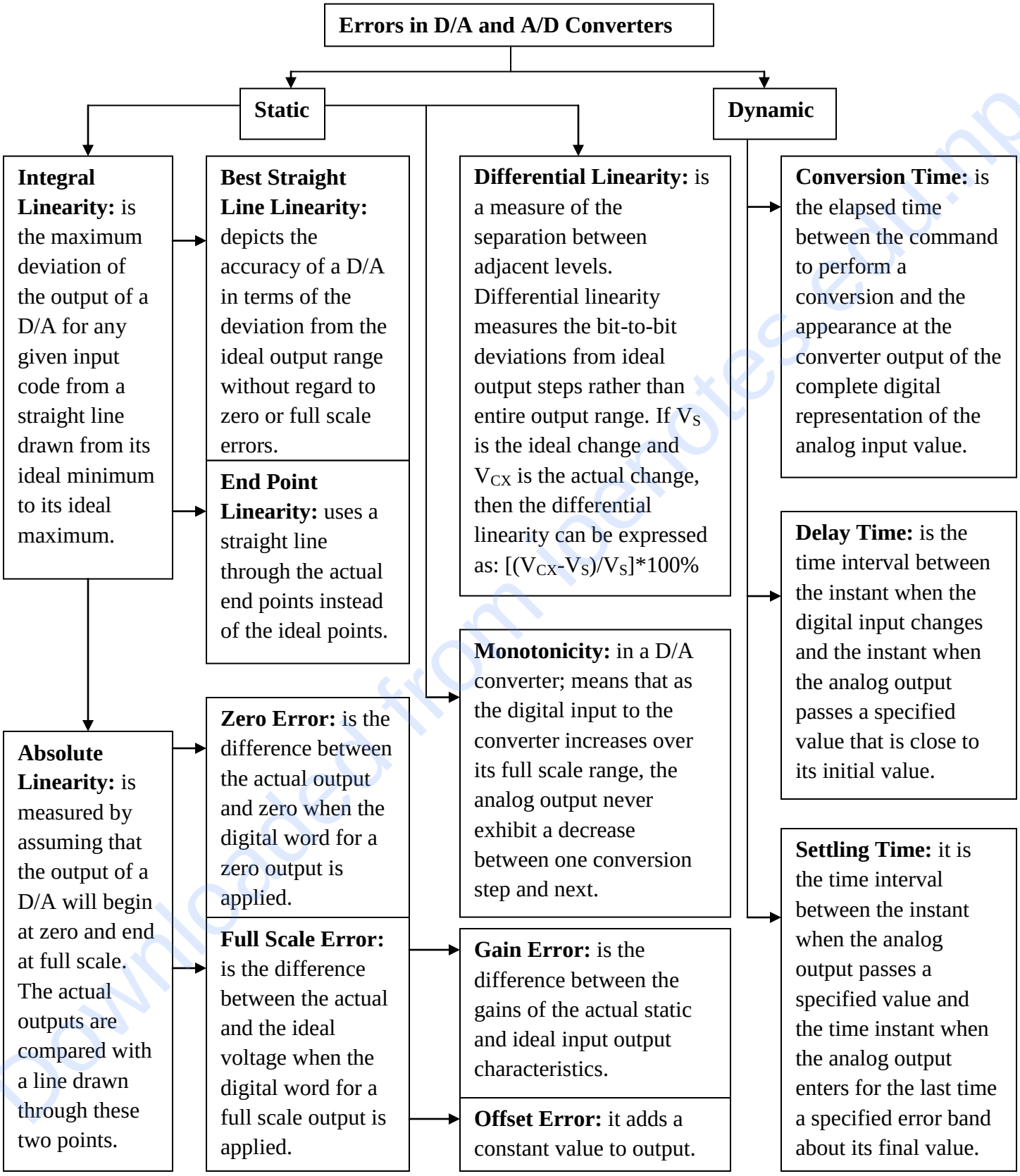
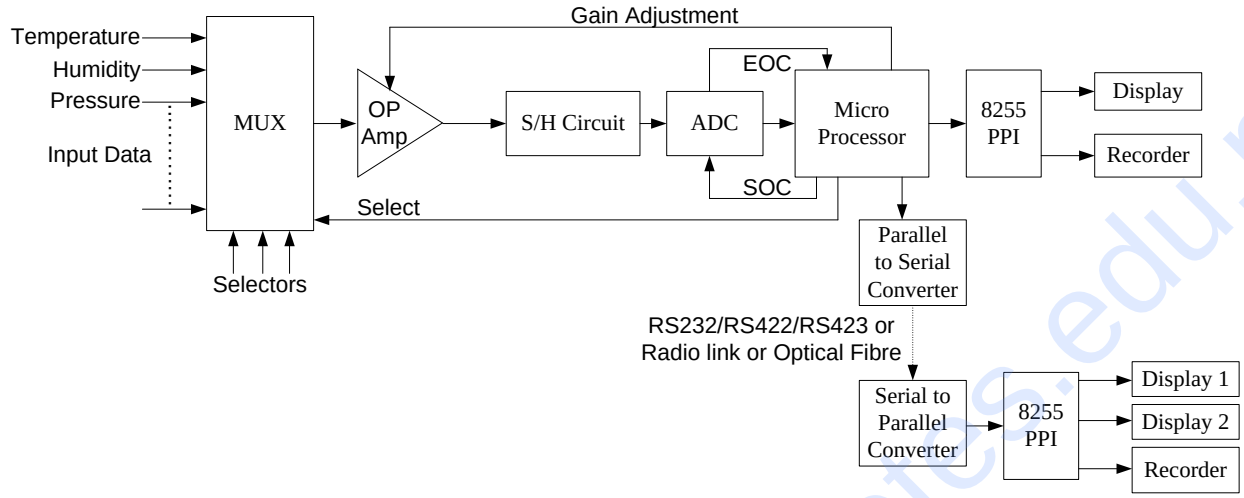


Fig.: End Point Linearity Error



Designing the embedded system with ADC, MUX, S/H circuit for transmitting data in long distance.



- A typical system that converts signals from analog to digital and back to analog includes:
  - A transducer that converts non-electrical signals into electrical signals
  - An A/D converter that converts analog signals into digital signals
  - A digital processor that processes digital data (signals)
  - A D/A converter that converts digital signals into equivalent analog signals
  - A transducer that converts electrical signals into real life non-electrical signals (sound, pressure, and video)