CSE 371 HW 2

Memories

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1. Problem 1

Specify the minimum size (i.e., number of words and number of bits per word) of separate ROMs that will accommodate the truth tables for the following combinational circuit components. Assume the output will be as wide as is needed to represent the largest possible result (no truncation).

(a) A binary multiplier that multiplies two 4-bit binary words.

> Multiplying two 4-bit binary words requires a word size of 8 bits. We need $2^8 = 256$ words to account for each possibility.

(b) A 3-bit adder-subtractor.

> Adding or subtracting two 3-bit numbers results in a range of $[0000 - 1110]$ for our outputs, which requires 4 bits to represent. We need $2^7 = 128$ words to account for each possibility.

2. Problem 2

(a) How many 4 Mi × 16 RAM chips are needed to provide a total memory capacity of 64 Mi-bytes?

> 4 Mi x $16 = 2^2 \cdot 2^{20} \cdot 2^4 = 2^{26} = 64$ Mi bits $= 8$ MiB. We need 64 MiB / 8 MiB $= 8$ chips.

(b) How many address bits are needed for our larger, 64 Mi-byte-memory assuming the same word size as the individual chips?

> We need $\log_2(64$ MiB / $16) = \log_2(2^{29} / 2^4) = 25$ bits.

(c) How many of the address bits are connected to each RAM chip?

> Each RAM chip should have $\log_2(4$ Mi x $16) = 22$ address bits.

(d) How many of the address bits must be decoded for the chip select (i.e., how many are needed for us to know which RAM chip we need to access)? Specify the size of the decoder.

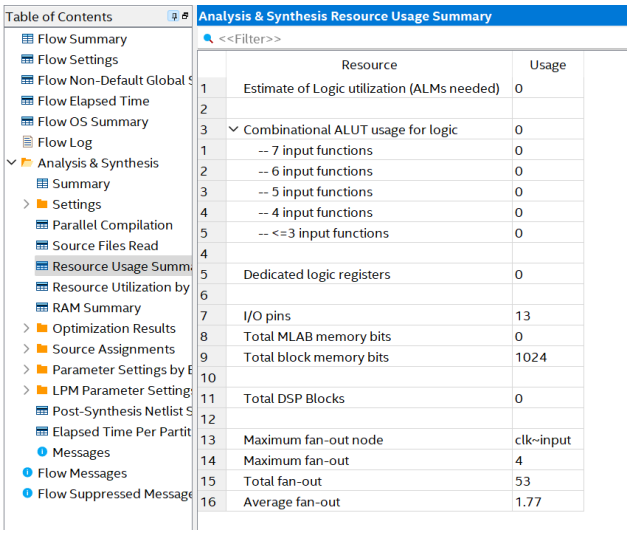
> To know which of the 8 chips we need to access, we need $\log_2(8) = 3$ decoder bits.

3. Problem 3

3.4. Resource Usage

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	5
2		
3	⌄ Combinational ALUT usage for logic	9
1	-- 7 input functions	0
2	-- 6 input functions	1
3	-- 5 input functions	0
4	-- 4 input functions	3
5	-- <=3 input functions	5
4		
5	Dedicated logic registers	0
6		
7	I/O pins	12
8		
9	Total DSP Blocks	0
10		
11	Maximum fan-out node	always0~0
12	Maximum fan-out	4
13	Total fan-out	48
14	Average fan-out	1.45

Figure 1: sign_mag_add



	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	0
2		
3	⌄ Combinational ALUT usage for logic	0
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	0
4		
5	Dedicated logic registers	0
6		
7	I/O pins	13
8	Total MLAB memory bits	0
9	Total block memory bits	1024
10		
11	Total DSP Blocks	0
12		
13	Maximum fan-out node	clk~input
14	Maximum fan-out	4
15	Total fan-out	53
16	Average fan-out	1.77

Figure 2: sync_rom

4. Problem 4

(a) Memory diagram for an implementation of the 4×4 RAM as a register file. The en inputs to the registers are enable signals (i.e., the register will update when en=1 and remain the same when en=0).

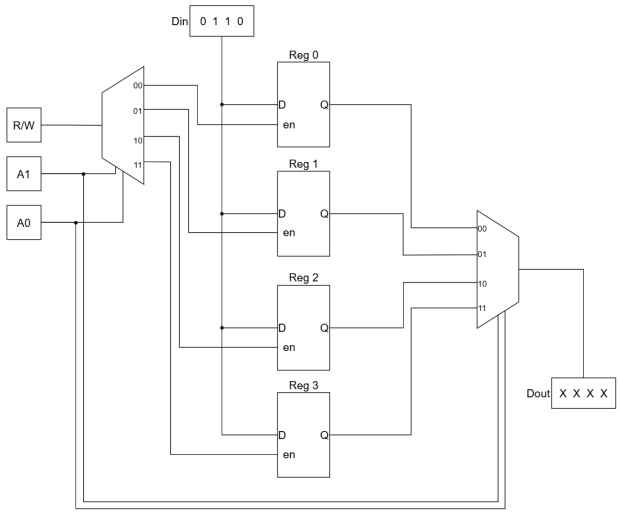


Figure 3: 4x4 RAM diagram

(b) Construct an 8×8 memory diagram using the given 4×4 RAM as a building block. Hint: how will the inputs and outputs differ for a 8×8 RAM compared to the 4×4 RAM block diagram shown above?

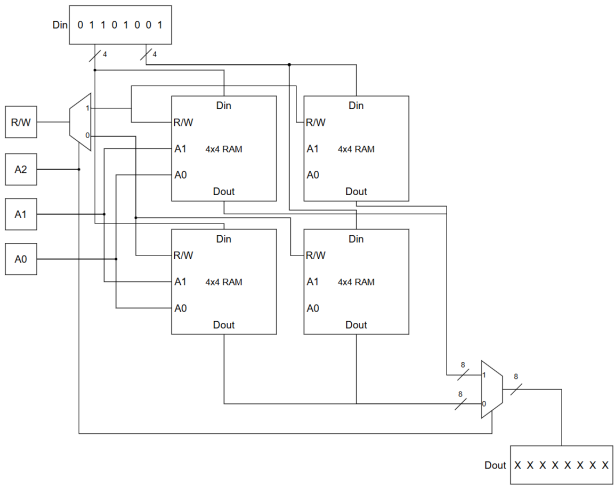


Figure 4: 8x8 RAM diagram using 4x4 blocks

5. Misc.

Time spent: 5 hours
Rating: Moderate