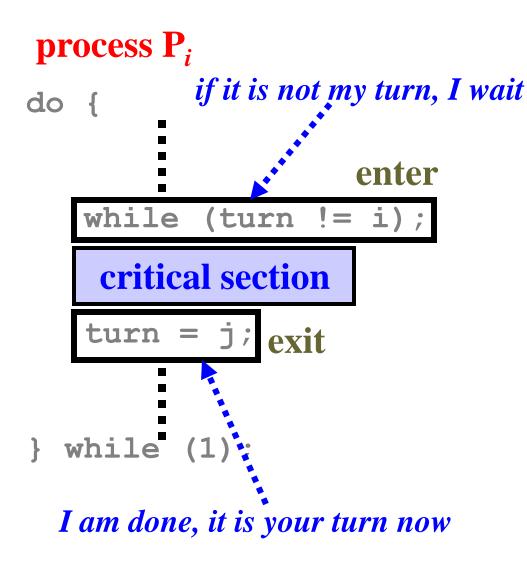
Part III Synchronization Software and Hardware Solutions

Computers are useless. They can only give answers.

Software Solutions for Two Processes

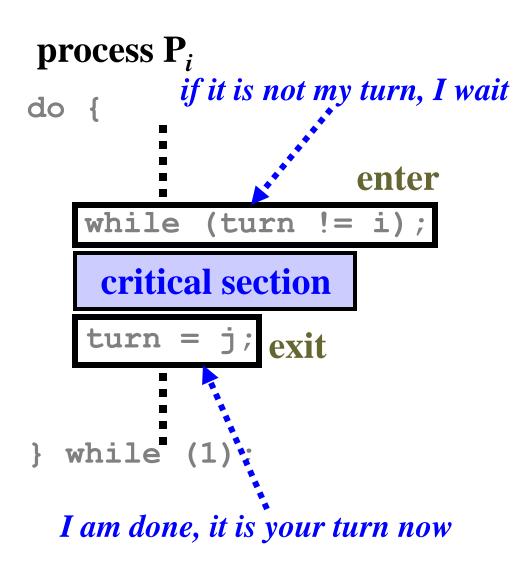
- Suppose we have two processes P_0 and P_1 .
- Let one process be P_i and the other be P_j , where j = 1 i. Thus, if i = 0, then j = 1 and if i = 1, then j = 0.
- We wish to design an enter-exit protocol for a critical section to ensure mutual exclusion.
- We will go through a few unsuccessful attempts and finally obtain a correct one.
- These solutions are pure software-based.

Attempt I: 1/3



- Shared variable turn controls who can enter the critical section.
- Since turn is either 0 or 1, only one can enter.
- However, processes are forced to run in an alternating way.
- Not good!

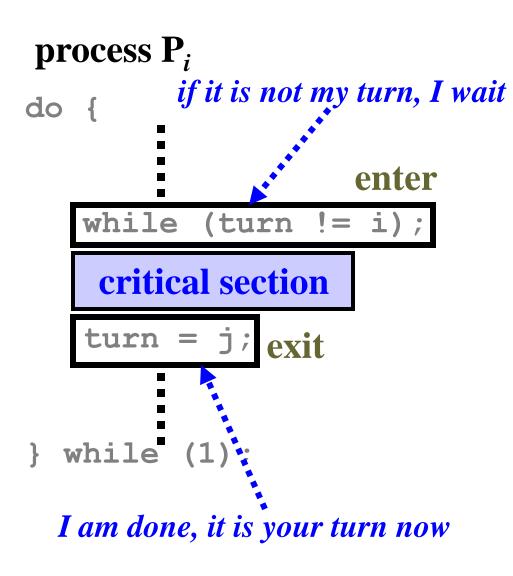
Attempt I: 2/3



Mutual Exclusion

- P_0 in its CS if turn=0.
- P_1 in its CS if turn=1.
- If P₀ and P₁ are BOTH in their CS, then turn=0 and turn=1 must BOTH be true.
- This is absurd, because a variable can only hold one and only one value (i.e., cannot hold both 0 and 1).

Attempt I: 3/3



Progress

- If P_i sets turn to j and never uses the critical section again, P_j can enter but cannot enter again.
- Thus, an irrelevant process blocks other processes from entering a critical section. Not good!
- Does bounded waiting hold? Exercise!

Attempt II: 1/5

```
bool
       flag[2];
        I am interested
do {
              wait for you
                     enter
    flag[i] = TRUE;
    while (flag[j]
     critical section
                       exit
                FALSE;
          I am not interested
```

- Shared variable flag[i] is the "state" of process P_i: interested or not-interested.
- P_i indicates its intention to enter, waits for P_j to exit, enters its section, and, finally, changes to "I am out" upon exit.

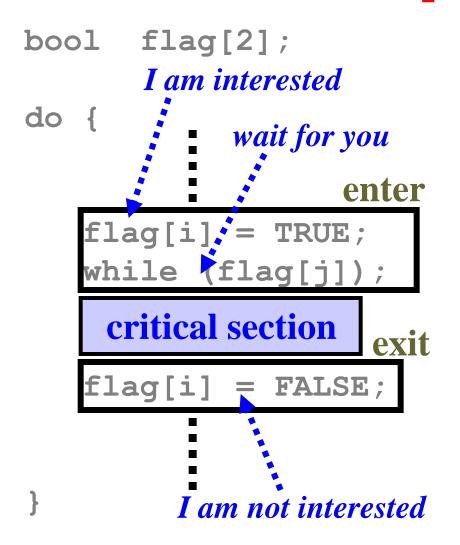
Attempt II: 2/5

```
bool
        flag[2];
        I am interested
do {
              wait for you
                     enter
    flag[i] = TRUE;
    while {flag[j]
     critical section
                       exit
                 FALSE;
          I am not interested
```

Mutual Exclusion

- P₀ is in CS if flag[0] is TRUE AND flag[1] is FALSE.
- P₁ is in CS if flag[1] is TRUE AND flag[0] is FALSE.
- If both are in their CS, flag[0] must be both TRUE and FALSE.
- This is absurd.

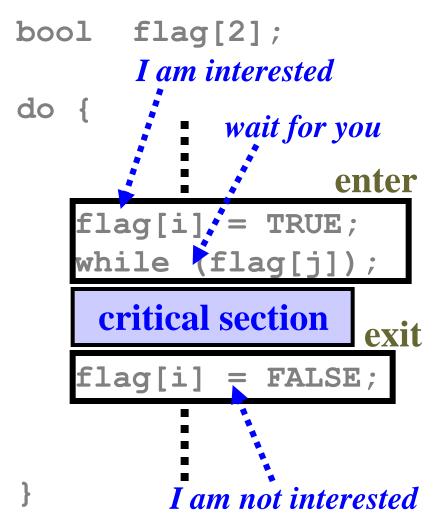
Attempt II: 3/5



Progress

- If both P₀ and P₁ set flag [0] and flag [1] to TRUE at the same time, then both will loop at the while forever and no one can enter.
- A decision cannot be made in finite time.

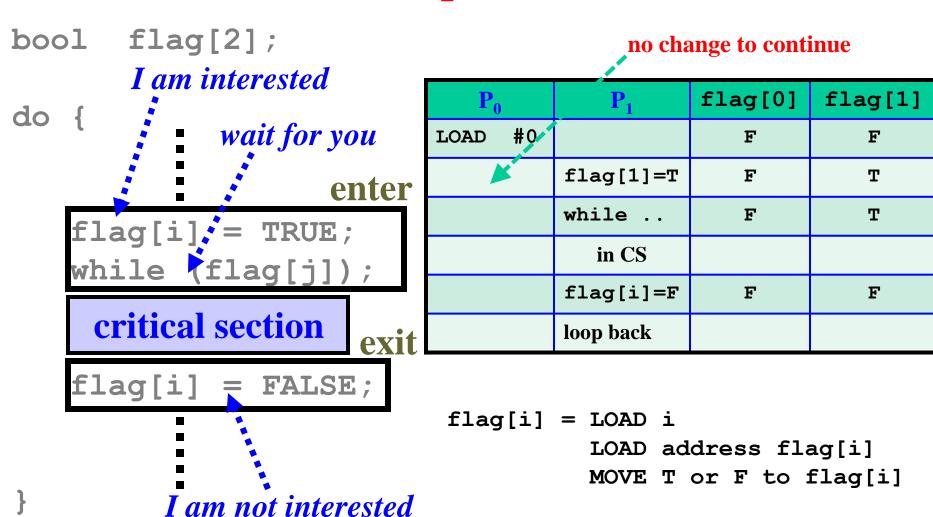
Attempt II: 4/5



Bounded Waiting

- P₀ is in the enter section but switched out before setting flag[0] to TRUE.
- P₁ reaches its CS and sees flag[0] being not
 TRUE. P₁ enters.
- P₁ can enter and exit in this way repeatedly. Thus,
 P₀ cannot enter forever (i.e., unbounded).

Attempt II: 5/5



Attempt III/A Combination: 1/12 Peterson's Algorithm

```
bool flag[2] = FALSE; // process P_i
           int
                 turn;
                        I am interested
                                          yield to you first
          do
                        = TRUE
                                                      enter
                       (flag[j
                                   2.2
I am done
                critical section
                                            wait while you are
                                            interested and it is
                        = FALSE;
                                            your turn.
                                                          11
```

Attempt III: Mutual Exclusion 2/12

 $\begin{array}{ll} \text{process } P_i & \text{process } P_j \\ \\ \text{flag[i] = TRUE;} & \text{flag[j] = TRUE;} \\ \text{turn = j;} & \text{turn = i;} \\ \text{while (flag[j] && turn == j);} & \text{while (flag[i] && turn == i);} \\ \end{array}$

- If P_i is in its critical section, then it sets
 - flag[i] to TRUE
 - \Rightarrow turn to j (but turn may not be j after this point because P_i may set it to i later).
 - *and waits until flag[j] && turn == j
 becomes FALSE

Attempt III: Mutual Exclusion 3/12

 $\begin{array}{ll} \text{process } P_i & \text{process } P_j \\ \\ \text{flag[i] = TRUE;} & \text{flag[j] = TRUE;} \\ \text{turn = j;} & \text{turn = i;} \\ \text{while (flag[j] && turn == j);} & \text{while (flag[i] && turn == i);} \\ \end{array}$

- If P_j is in its critical section, then it sets
 - flag[j] to TRUE
 - \diamond turn to i (but turn may not be i after this point because P_i may set it to j later).
 - *and waits until flag[i] && turn == i
 becomes FALSE

Attempt III: Mutual Exclusion 4/12

```
\begin{array}{ll} \text{process } P_i & \text{process } P_j \\ \\ \text{flag[i] = TRUE;} & \text{flag[j] = TRUE;} \\ \text{turn = j;} & \text{turn = i;} \\ \text{while (flag[j] && turn == j);} & \text{while (flag[i] && turn == i);} \\ \end{array}
```

If processes P_i and P_j are both in their critical sections, then we have:

they are both TRUE

```
#flag[i] and flag[j] are both TRUE.
#flag[i] && turn == i and flag[j] &&
turn == j are both FALSE.
```

❖Therefore, turn == i and turn == j must both be FALSE.

Attempt III: Mutual Exclusion 5/12

 $\frac{1}{\text{process } \mathbf{P}_i}$

```
flag[i] = TRUE;
turn = j;
while (flag[j] && turn == j);
flag[j] = TRUE;
turn = i;
while (flag[i] && turn == i);
```

- Since turn == i and turn == j are both FALSE and since turn is set to j (by P_i) or i (by P_j) before entering the critical section, only one of turn == i and turn == j can be FALSE but not both.
- Therefore, we have a contradiction.
- Of course, mutual exclusion holds.

Attempt III: Mutual Exclusion 6/12

- We normally use the proof by contradiction technique to establish the mutual exclusion condition.
- To do so, follow the procedure below:
 - \bullet Find the condition C_0 for P_0 to enter its CS
 - \bullet Find the condition C_1 for P_1 to enter its CS
 - **If** \mathbf{P}_0 and \mathbf{P}_1 are in their critical sections, \mathbf{C}_0 and \mathbf{C}_1 will both be true.
 - **Trom** C_0 and C_1 being true, we should be able to derive an absurd result.
 - *Therefore, mutual exclusion holds.

Attempt III: Mutual Exclusion 7/12

- We care about the conditions C_0 and C_1 . The way of reaching these conditions via instruction execution is un-important.
- Never use an execution sequence to prove mutual exclusion. In doing so, you make a serious mistake, which is usually referred to as proof by example.
- You may use a single example to show a proposition being false. But, you cannot use a single example to show a proposition being true. That is, $3^2 + 4^2 = 5^2$ cannot be used to prove $a^2 + b^2 = c^2$ for a right triangles.

Attempt III: Progress 8/12

$\begin{array}{lll} & & & & & & & & & & & \\ \text{flag[i]} = & & & & & & & \\ \text{flag[j]} = & & & & & & \\ \text{turn} = & & & & & \\ \text{while (flag[j] && turn} == & &); & \text{while (flag[i] && turn} == & i); \\ \end{array}$

- If P_i and P_j are both waiting to enter their critical sections, since the value of turn can only be i or j but not both, one process can pass its while loop (i.e., decision time is finite).
- Suppose P_i is waiting and P_j is not in its CS:
 - Since P_j is not interested in entering, flag[j] was set to FALSE when P_j exits and P_i enters.
 - *Thus, the process that is not entering does not influence the decision.

Attempt III: Bounded Waiting 9/12

$\begin{array}{ll} \text{process } P_i & \text{process } P_j \\ \\ \text{flag[i] = TRUE;} & \text{flag[j] = TRUE;} \\ \text{turn = j;} & \text{turn = i;} \\ \text{while (flag[j] && turn == j);} & \text{while (flag[i] && turn == i);} \\ \end{array}$

- If P_i wishes to enter, we have three cases:
 - 1. P_i is *outside* of its critical section.
 - 2. P_i is *in* its critical section.
 - 3. P_i is in the entry section.

Attempt III: Bounded Waiting 10/12

```
\begin{array}{lll} & & & & & & & & & & \\ & & & & & & & \\ & & & & & \\ & & & & & \\ & & & & \\ & & & & \\ & & & & \\ & & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\
```

- CASE I: If P_j is *outside* of its critical section, P_j sets flag[j] to FALSE when it exits its critical section, and P_i may enter.
- In this case, P_i does not wait.

Attempt III: Bounded Waiting 11/12

```
\begin{array}{lll} & & & & & & & & & & \\ \text{flag[i]} = & & & & & & & \\ \text{flag[j]} = & & & & & & \\ \text{turn} = & & & & & \\ \text{while (flag[j] && turn} == & & ); & & \\ \text{while (flag[i] && turn} == & i); & & \\ \end{array}
```

- CASE 2: If P_j is in the entry section, depending on the value of turn, we have two cases:
 - If turn is i (e.g., P_i sets turn to j before P_j sets turn to i), P_i enters immediately.
 - **Otherwise,** P_j enters and P_i stays in the while loop, and we have **CASE 3**.

Attempt III: Bounded Waiting 12/12

process P_i process P_j

```
flag[i] = TRUE;
turn = j;
while (flag[j] && turn == j);
flag[j] = TRUE;
turn = i;
while (flag[i] && turn == i);
```

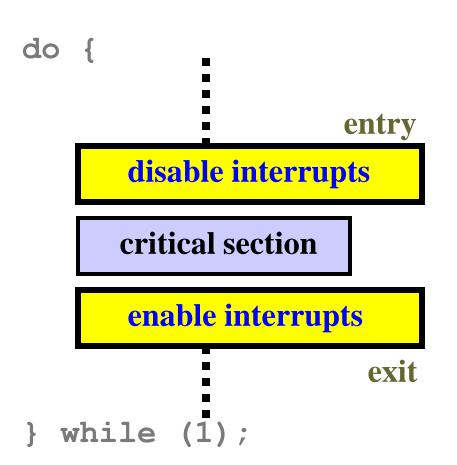
CASE 3: If P_j is *in* its critical section, turn must be j and P_i waits for at most one round.

P_i	P_{j}	flag[i]	flag[j]	turn	Comments
flag[i]=T	flag[j]=T	TRUE	TRUE	?	
while ()		TRUE	TRUE	j	P_j enters
	Critical Sec				P_j in CS
	flag[j]=F	TRUE	FALSE	j	P_j exits
	flag[j]=T	TRUE	TRUE	j	\mathbf{P}_j returns
	turn = i	TRUE	TRUE	i	P_j yields
	while ()	TRUE	TRUE	i	P_j loops
Critical Sec					P. enters

Hardware Support

- There are two types of hardware synchronization supports:
 - *Disabling/Enabling interrupts: This is slow and difficult to implement on multiprocessor systems.
 - **❖**Special *privileged*, actually *atomic*, machine instructions:
 - **✓** Test and set (TS)
 - **√**Swap
 - **✓** Compare and Swap (CS)

Interrupt Disabling



- Because interrupts are disabled, no context switch can occur in a critical section (why?).
- Infeasible in a multiprocessor system because all CPUs/cores must be informed.
- Some features that depend on interrupts (e.g., clock) may not work properly.

Test-and-Set Instruction: 1/2

```
bool TS(bool *key)
{
   bool save = *key;
   *key = TRUE;
   return save;
}
```

- **TS** is atomic.
- Mutual exclusion is met as the TS instruction is atomic. See next slide.
- However, bounded waiting may not be satisfied. Progress?

```
lock = FALSE;
bool
do {
                    entry
          (TS(&lock));
      critical section
    lock = FALSE;
                     exit
  while (1);
```

Test-and-Set Instruction: 2/2

- A process is in its critical section if the TS instruction returns FALSE.
- If two processes P_0 and P_1 are in their critical sections, they both got the FALSE return value from TS.
- P₀ and P₁ cannot execute their TS instructions at the same time because TS is atomic.
- Hence, one of them, say P_0 , executes the TS instruction before the other.
- Once P₀ finishes its TS, the value of lock becomes TRUE.
- P₁ cannot get a FALSE return value and cannot enter its CS.
- We have a contradiction!

```
bool
      lock = FALSE;
do {
   while (TS(&lock));
      critical section
   lock = FALSE;
  while (1);
```

Problems with Software and Hardware Solutions

- All of these solutions use busy waiting.
- Busy waiting means a process waits by executing a tight loop to check the status/value of a variable.
- Busy waiting may be needed on a multiprocessor system; however, it wastes CPU cycles that some other processes may use productively.
- Even though some systems may allow users to use some atomic instructions, unless the system is lightly loaded, CPU and system performance can be low, although a programmer may "think" his/her program looks more efficient.
- So, we need better solutions.

The End