CHAPTER 15

Semiconductor Microwave and Power Devices

In previous chapters, we have discussed the basic physics, operation, and characteristics of diodes and transistors. We have analyzed the frequency response as well as the current–voltage characteristics of these semiconductor devices. However, we have not specifically considered the generation of microwave signals using semiconductor devices or the power capabilities of semiconductor transistors.

In this chapter, we first consider three semiconductor devices that are used to generate microwave signals. These devices include the tunnel diode, GUNN diode, and IMPATT diode. A basic principle of oscillators is that a region of negative differential resistance must exist. We consider the process by which a region of negative differential resistance is created in each device and discuss the basic operation of these devices.

Second, we discuss three specialized semiconductor power devices, including power bipolar transistors and power MOSFETs. We have considered the basic physics of these devices in previous chapters, and analyzed the current–voltage characteristics without specifically considering the current or voltage limitations or the power dissipation within the devices. In this chapter, we discuss the limitations in current and voltage, and the power capabilities of the devices. Finally, we discuss the operation and characteristics of a four-layered structure called a thyristor. ■

15.0 | PREVIEW

In this chapter, we will:

- Discuss the concept of negative differential resistance in a tunnel diode and derive an expression for the maximum resistance cutoff frequency.
- Discuss the concept of negative differential mobility in GaAs and discuss the process by which this characteristic can lead to microwave oscillations in a GUNN diode.
- Discuss the operation of an IMPATT diode oscillator and determine the process by which a dynamic negative resistance is created.

- Present the basic geometry and electrical characteristics of a power bipolar transistor. The limiting current and voltage factors will be analyzed, and the safe operating area of the BJT will be considered.
- Present the basic geometry and electrical characteristics of a power MOSFET. The limiting current and voltage factors will be analyzed, and the safe operating area of the MOSFET will be considered.
- Discuss the operation of a four-layer switching device that is generally referred to as a Thyristor. The operation of several structures will be analyzed.

15.1 | TUNNEL DIODE

The tunnel diode, also known as the Esaki diode, has been briefly discussed in Section 8.5 of the book. Recall that the device is a pn junction in which both the n and p regions are degenerately doped. With the very high doping concentrations, the space charge region width is very narrow ($W \approx 0.5 \times 10^{-6}$ cm $= 50$ Å).

The forward-bias current–voltage characteristics are again shown in Figure 15.1a. For small forward-bias voltages ($V < V_p$), electrons in the conduction band on the n side are directly opposite empty states in the valence band of the p region (see Figure 8.29). Electrons tunnel through the potential barrier into the empty states producing a tunneling current. For forward-bias voltages in the range $V_p < V < V_v$, the number of electrons on the n side directly opposite empty states on the p side decreases so that the tunneling current decreases. For $V > V_v$, the normal diode diffusion currents dominate.

A decrease in current with an increase in voltage produces a region of negative differential resistance in the range $V_p < V < V_v$. A negative differential resistance phenomenon is necessary for oscillators.

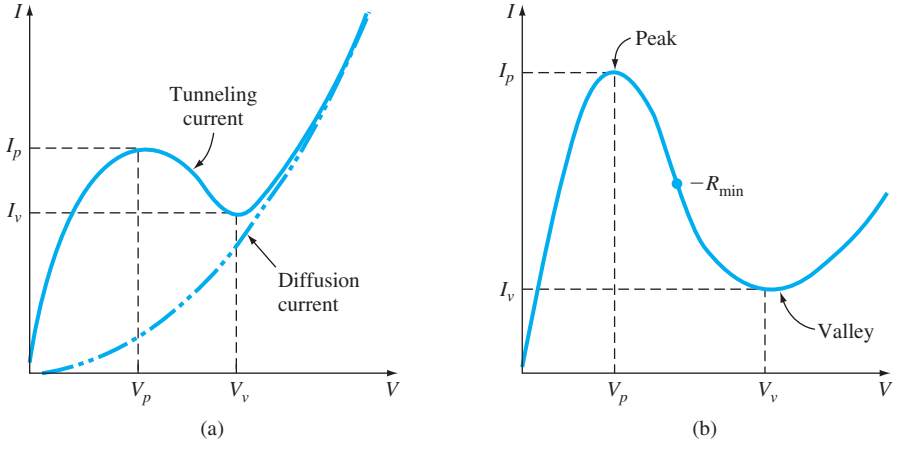

Figure 15.1 | (a) Forward-bias current–voltage characteristics of a tunnel diode. (b) Expanded plot of *I–V* characteristics.

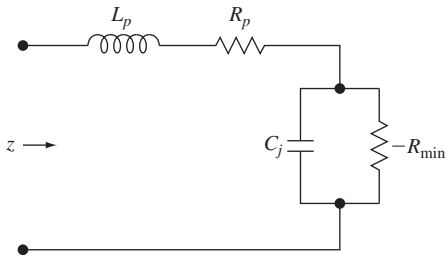

Figure 15.2 | Equivalent circuit of the tunnel diode.

Figure 15.1b shows an expanded plot of the *I–V* characteristics in the tunneling range. A point is shown on the curve where the minimum value of negative resistance occurs. (Note that $R_{\min}$ is a positive quantity.) The equivalent circuit of the tunnel diode for the case when the diode is biased at the $-R_{\min}$ point is shown in Figure 15.2. The parameter C_j is the junction capacitance, and the parameters L_p and R_p are the parasitic or interconnect line inductance and resistance, respectively.

The small signal input impedance can be written as

$$Z = \left[R_p - \frac{R_{\min}}{1 + \omega^2 R_{\min}^2 C_j^2}\right] + j\omega\left[L_p - \frac{\omega R_{\min}^2 C_j}{1 + \omega^2 R_{\min}^2 C_j^2}\right] \tag{15.1}$$

The resistive part of the impedance goes to zero at a frequency of

$$f_r = \frac{1}{2\pi R_{\min} C_j}\sqrt{\frac{R_{\min}}{R_p} - 1} \tag{15.2}$$

For frequencies $f > f_r$, the resistive part of the impedance becomes positive so that the diode loses its negative differential resistance characteristic. The operating frequency must then occur at $f_o < f_r$. The frequency f_r is referred to as the *maximum resistive cutoff frequency*.

The tunneling process is a majority carrier effect so the diode does not exhibit time delays due to minority carrier diffusion, which means that the diode is capable of operating at microwave frequencies. However, due to the relatively small voltage range in which the diode exhibits the negative resistance characteristic, the tunnel diode is not used extensively.

15.2 | GUNN DIODE

Another negative differential resistance device is the GUNN diode, or **T**ransferred-**E**lectron **D**evice (TED). The transferred-electron phenomenon is demonstrated in a few semiconductors in which conduction electrons in a high-mobility band are scattered to a low-mobility band by a high electric field. In Chapter 5, we discussed the drift velocity of electrons in GaAs versus electric field. Figure 15.3 again shows a plot of this characteristic. InP also shows this same characteristic.

Figure 15.4 shows an expanded plot of the energy-band structure in GaAs that is given in Figure 5.8. For small electric fields, essentially all of the electrons in the

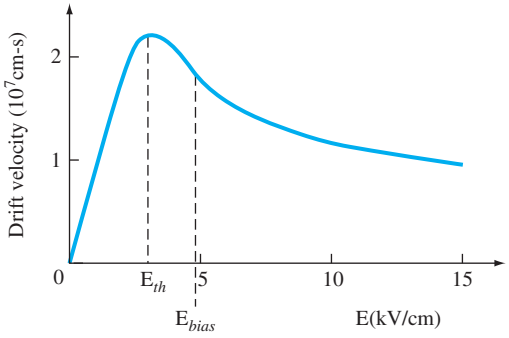

Figure 15.3 | Electron drift velocity versus electric field for GaAs.

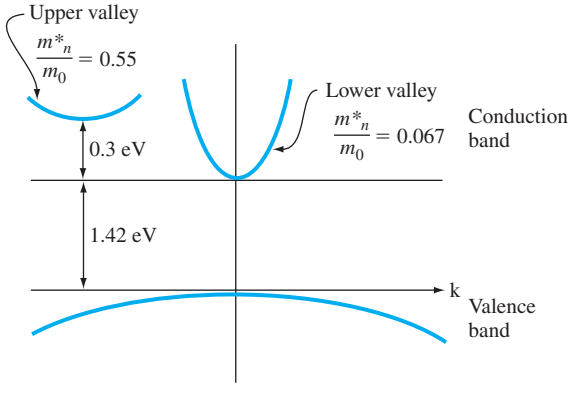

Figure 15.4 | Energy-band structure of GaAs showing the lower valley and upper valley in the conduction band.

conduction band exist in the lower valley of the E versus k diagram, where the density of states electron effective mass is small. A small effective mass leads to a large mobility value.

As the electric field increases above a threshold or critical value, E_{th}, the electrons gain more than the 0.3 eV energy separating the two valleys so that electrons can be scattered into the upper valley, where the density of states electron effective mass is much larger. The larger effective mass yields a smaller mobility. The intervalley transfer mechanism with a change in mobility results in a decreasing average drift velocity of electrons with electric field, or a negative differential electron mobility. The maximum negative differential electron mobility in GaAs is approximately -2400 cm^2/V-s.

Consider a two-terminal n-type GaAs device with ohmic contacts at the ends that is biased in the negative mobility region ($E_{bias} > E_{th}$) as shown in Figure 15.5a. A small space charge region may develop in the material near the cathode as shown in Figure 15.5b. As a result, the electric field increases in this region as shown in Figure 15.5c. (Special device structures can be fabricated to ensure that the space charge fluctuations are generated near the cathode.)

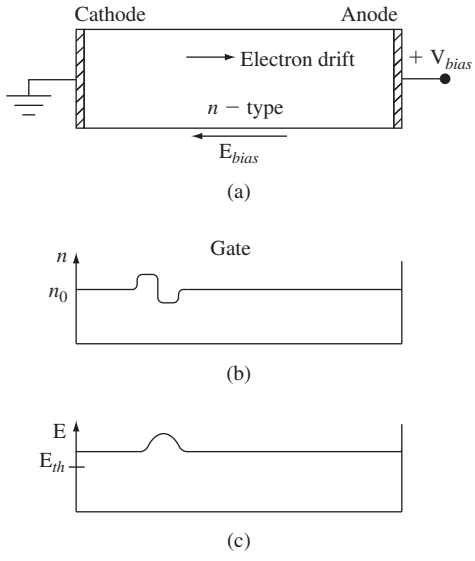

Figure 15.5 | (a) A simplified two-terminal GaAs device. (b) Electron concentration versus distance showing a space charge formation. (c) Electric field versus distance.

In discussing excess carrier behavior in Chapter 6, we found the time behavior of a net charge density in a semiconductor to be given by

$$\delta Q(t) = \delta Q(0)e^{-t/\tau_d} \tag{15.3}$$

where τ_d is the dielectric relaxation time constant and is on the order of a picosecond. Normally, a small space charge region would be quickly neutralized. The dielectric relaxation time constant is given by $\tau_d = \epsilon/\sigma$, where σ is the semiconductor conductivity. If the GaAs is biased in the negative mobility region, then the conductivity is negative and the exponent in Equation (15.3) becomes positive, so the space charge region, now called a *domain,* can actually build up as it drifts toward the anode. As the domain grows (Figure 15.6a), the electric field in this region increases which means that the electric field in the remaining material decreases. The E field in the material outside of the domain can drop below the critical value, as indicated in Figure 15.6b, while the E field within the domain remains above the critical value. For this reason, only one domain will normally be established in the material at any given time.

As the domain reaches the anode, a current pulse is induced in the external circuit. After the domain reaches the anode, another domain may form near the cathode and the process repeats itself. Thus, a series of current pulses may be generated as shown in Figure 15.7. The time between current pulses is the time for the domain to drift through the device. The oscillation frequency is given by

$$f = 1/\tau = v_d/L \tag{15.4}$$

where v_d is the average drift velocity and L is the length of the drift region.

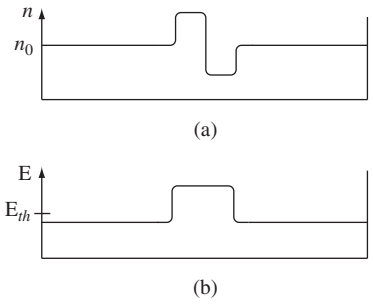

Figure 15.6 | (a) Electron concentration versus distance showing a domain. (b) Electric field versus distance.

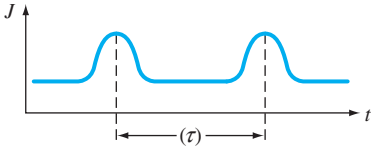

Figure 15.7 | Current pulses versus time in the GaAs device.

The oscillation mechanism just described is called the transit-time mode. More complex modes of operation are possible. Studies have shown that the efficiency of the transit-time device is largest when the product $n_0 L$ is a few times 10^{12} cm^{-2}. For this case, the domain fills about one-half of the drift region length and produces a current output that is nearly sinusoidal. The maximum dc-to-rf conversion efficiency is approximately 10 percent.

Oscillations in the frequency range of 1 to 100 GHz or higher can be obtained. If the device is operated in a pulsed mode, a peak output power in the range of hundreds of watts can be produced. Transferred-electron devices are now used as the microwave source in many radar systems.

15.3 | IMPATT DIODE

The term IMPATT stands for **IMP**act ionization **A**valanche **T**ransit-**T**ime. The IMPATT diode consists of a high-field avalanche region and a drift region that produces a dynamic negative resistance at microwave frequencies. The negative resistance characteristic produced in this device is a result of a time delay so that the ac current and voltage components are out of phase, and is a different phenomenon compared to the tunnel diode, for example. The tunnel diode has a negative dI/dV region in the I–V characteristic.

One example of an IMPATT diode is a p^+-n-i-n^+ structure as shown in Figure 15.8a. Typical doping concentrations (magnitudes) are shown in Figure 15.8b. The device is reverse biased so that the n and intrinsic regions are completely depleted. The electric field in the device is shown in Figure 15.8c. We may note that $\int E dx = V_B$ where V_B is the applied reverse-biased voltage. The value of V_B is very close to the breakdown voltage. The avalanche region is localized near the pn junction. The electric field in the intrinsic region is nearly constant and the intrinsic layer provides the drift region.

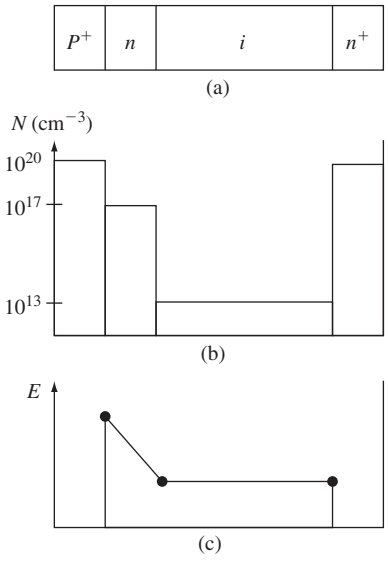

Figure 15.8 | (a) An IMPATT diode structure. (b) Typical doping concentrations in the IMPATT diode. (c) Electric field versus distance through the IMPATT diode.

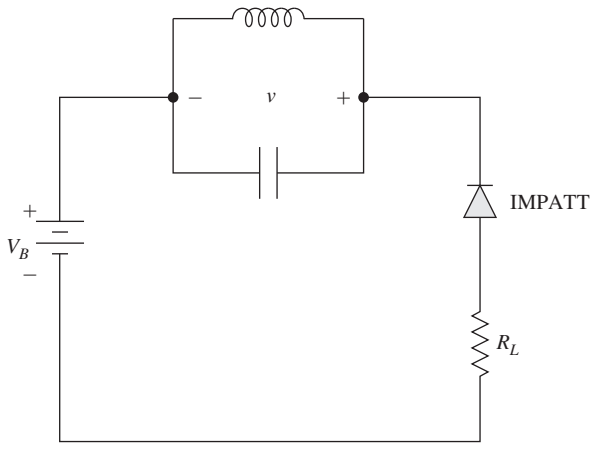

Figure 15.9 | Circuit for an IMPATT diode oscillator.

Figure 15.9 shows the circuit for an IMPATT diode oscillator. An LC resonant circuit is required for the oscillator operation. During the positive ac voltage across the LC circuit as shown in the figure, the diode goes into breakdown and electron–hole pairs are generated at the p^+n junction. The generated electrons flow back into the p^+ region, while the holes start drifting through the depleted intrinsic region. In general, the holes will travel at their saturation velocity. During the negative ac voltage, the device operates below the breakdown voltage so electron–hole pairs are no longer produced.

There is an inherent $\pi/2$ phase shift between the peak value of the avalanche voltage at the p^+n junction and the injection of the holes into the intrinsic drift region due to the finite buildup time of the avalanche generated electron–hole pairs. A further delay of $\pi/2$ is then required during the drift process to provide the total 180 degrees of phase shift between the current and voltage at the output terminal. The transit time of the holes is $\tau = L/v_s$, where L is the length of the drift region and v_s is the saturation velocity of the holes. The LC circuit resonant frequency must be designed to be equal to the device resonant frequency, which is given by

$$f = \frac{1}{2\tau} = \frac{v_s}{2L} \tag{15.5}$$

When the holes reach the n^+ cathode, the current is at a maximum value and the voltage is at its minimum value. The ac current and ac voltage are 180 degrees out of phase with respect to each other producing the dynamic negative resistance.

Devices can be designed to operate in the 100 GHz or higher frequency range and produce power outputs of a few watts. The efficiency of these devices is in the range of 10 to 15 percent, and these devices provide the highest continuous output power of all the semiconductor microwave devices. As with most semiconductor device designs, other structures can be fabricated to provide specialized output characteristics.

15.4 | POWER BIPOLAR TRANSISTORS

In our previous discussions, we have ignored any physical transistor limitations in terms of maximum current, voltage, and power. We implicitly assumed that the transistors are capable of handling the current and voltage, and could handle the power dissipated within the device without suffering any damage.

However, with power transistors, we must be concerned with various transistor limitations. The limitations involve maximum rated current (on the order of amperes), maximum rated voltage (on the order of 100 V), and maximum rated power (on the order of watts or tens of watts).[1]

15.4.1 Vertical Power Transistor Structure

Figure 15.10 shows the structure of a vertical npn power transistor. We have considered vertical npn bipolar transistors previously. However, with small switching devices, the collector terminal is still formed at the surface. In the vertical configuration for the power bipolar transistor, the collector terminal is at the "bottom" of the device. This configuration is preferred since it maximizes the cross-sectional area through which current is flowing in the device. In addition, the doping concentrations

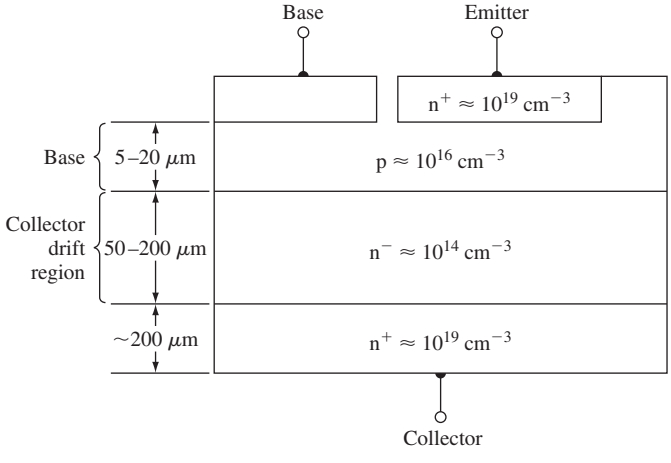

Figure 15.10 | Cross section of typical vertical npn power BJT.

[1]We must note that, in general, the maximum rated current and maximum rated voltage cannot occur at the same time.

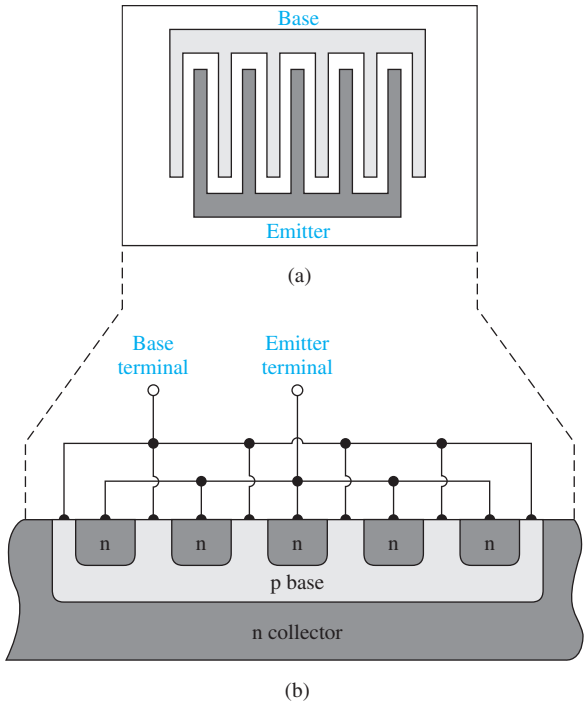

Figure 15.11 | An interdigitated bipolar transistor structure showing the top view and cross-sectional view.

and dimensions are not the same as we have encountered in small switching transistors. The primary collector region has a low-doped impurity concentration so that a large base–collector voltage can be applied without initiating breakdown. Another n region, with a higher doping concentration, reduces collector resistance and makes contact with the external collector terminal. The base region is also much wider than normally encountered in small devices. A large base–collector voltage implies a relatively large space charge width being induced in both the collector and base regions. A relatively large base width is required to prevent punch-through breakdown.

Power transistors must also be large-area devices in order to handle large currents. We have previously considered the interdigitated structure that is repeated in Figure 15.11. Relatively small emitter widths are required to prevent the emitter current crowding effects that were discussed in Section 12.4.4.

15.4.2 Power Transistor Characteristics

The relatively wide base width implies a much smaller current gain β for power transistors compared to small switching transistors, and large area device implies a larger junction capacitance and hence lower cutoff frequency for a power transistor compared to a small switching transistor. Table 15.1 compares the parameters of a

Table 15.1 | Comparison of the characteristics and maximum ratings of small-signal and power BJTs

Parameter	Small-signal BJT (2N2222A)	Power BJT (2N3055)	Power BJT (2N6078)
V_{CE} (max) (V)	40	60	250
T_C (max) (A)	0.8	15	7
P_D (max) (W) (at $T = 25°C$)	1.2	115	45
β	35–100	5–20	12–70
f_T (MHz)	300	0.8	1

general-purpose small-signal BJT to those of two power BJTs. The current gain is generally smaller in the power transistors, typically in the range of 20 to 100, and may be a strong function of collector current and temperature. Figure 15.12 shows typical current gain versus collector current characteristics for the 2N3055 power BJT at various temperatures.

The *maximum rated collector current* $I_{C,\max}$ may be related to the maximum current that the wires connecting the semiconductor to the external terminals can handle, the collector current at which the current gain falls below a minimum specified value, or the current that leads to the maximum power dissipation when the transistor is biased in saturation.

The *maximum rated voltage* in a BJT is generally associated with avalanche breakdown in the reverse-biased base–collector junction. In the common-emitter configuration, the breakdown voltage mechanism also involves the transistor gain, as well as the breakdown phenomenon in the pn junction. This is discussed in Section 12.4.6. Typical I_C versus V_{CE} characteristics are shown in Figure 15.13.

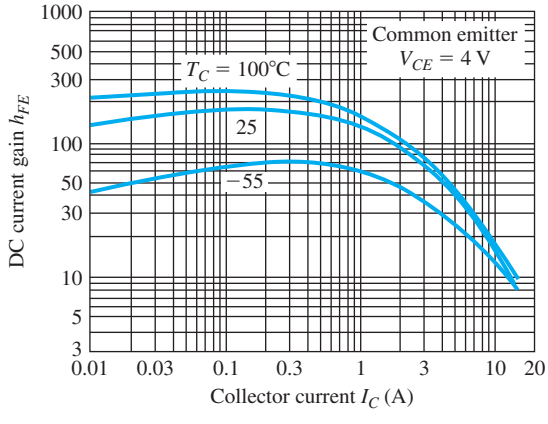

Figure 15.12 | Typical dc beta characteristics (h_{FE} versus I_C) for 2N3055.

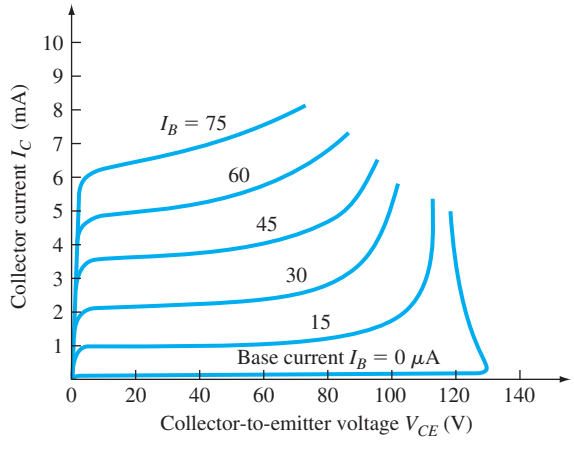

Figure 15.13 | Typical collector current versus collector–emitter voltage characteristics of a bipolar transistor, showing breakdown effects.

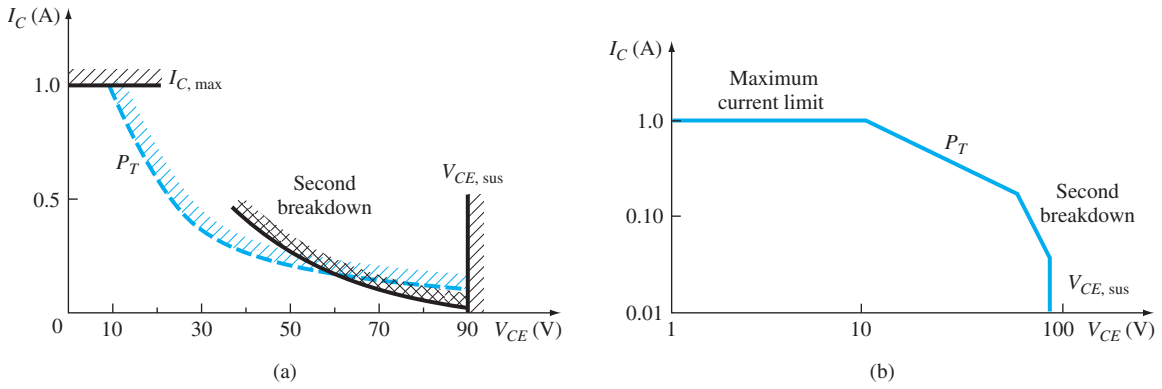

Figure 15.14 | The safe operating area (SOA) of a bipolar transistor plotted on (a) linear scales and (b) logarithmic scales.

When the transistor is biased in the forward-active mode, the collector current begins to increase significantly before the actual breakdown voltage is reached. All the curves tend to merge to the same collector–emitter voltage once breakdown has occurred. This voltage, $V_{CE,\,sus}$, is the minimum voltage necessary to sustain the transistor in breakdown.

Another breakdown effect is called *second breakdown,* which occurs in a BJT operating at high voltage and high current. Slight nonuniformities in current density produce local regions of increased heating that increases the minority carrier concentrations in the semiconductor material, which in turn increases the current in these regions. This effect results in positive feedback, and the current continues to increase, producing a further increase in temperature, until the semiconductor material may actually melt, creating a short circuit between the collector and emitter.

The average power dissipated in a BJT must be kept below a specified maximum value, to ensure that the temperature of the device remains below a maximum value. If we assume the collector current and collector–emitter voltage are dc values, then at the *maximum rated power* P_T for the transistor, we can write

$$P_T = V_{CE} I_C \tag{15.6}$$

Equation (15.6) neglects the $V_{BE} I_B$ component of power dissipation in the transistor.

The maximum current, voltage, and power limitations can be illustrated on the I_C versus V_{CE} characteristics as shown in Figure 15.14. The average power limitation, P_T, is a hyperbola described by Equation (15.6). The region where the transistor can be operated safely is known as the safe operating area (SOA) and is bounded by $I_{C,\max}$, $V_{CE,\,sus}$, P_T, and the transistor's second breakdown characteristic curve. Figure 15.14a shows the safe operating area using linear current and voltage scales. Figure 15.14b shows the same characteristics using log scales.

EXAMPLE 15.1

Objective: Determine the required current, voltage, and power rating of a power BJT.

Consider the common-emitter circuit in Figure 15.15. The parameters are $R_L = 10\ \Omega$ and $V_{CC} = 35$ V.

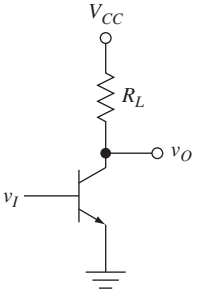

Figure 15.15 | Bipolar common-emitter circuit.

■ Solution

For $V_{CE} \approx 0$, the maximum collector current is

$$I_C\,(\text{max}) = \frac{V_{CC}}{R_L} = \frac{35}{10} = 3.5\ \text{A}$$

For $I_C = 0$, the maximum collector–emitter voltage is

$$V_{CE}\,(\text{max}) = V_{CC} = 35\ \text{V}$$

The load line is given by

$$V_{CE} = V_{CC} - I_C R_L$$

and must remain within the SOA, as shown in Figure 15.16.

The transistor power dissipation is

$$P_T = V_{CE} I_C = (V_{CC} - I_C R_L) I_C = V_{CC} I_C - I_C^2 R_L$$

The current at which the maximum power occurs is found by setting the derivative of this equation equal to zero as follows:

$$\frac{dP_T}{dI_C} = 0 = V_{CC} - 2 I_C R_L$$

which yields

$$I_C = \frac{V_{CC}}{2R_L} = \frac{35}{2(10)} = 1.75\ \text{A}$$

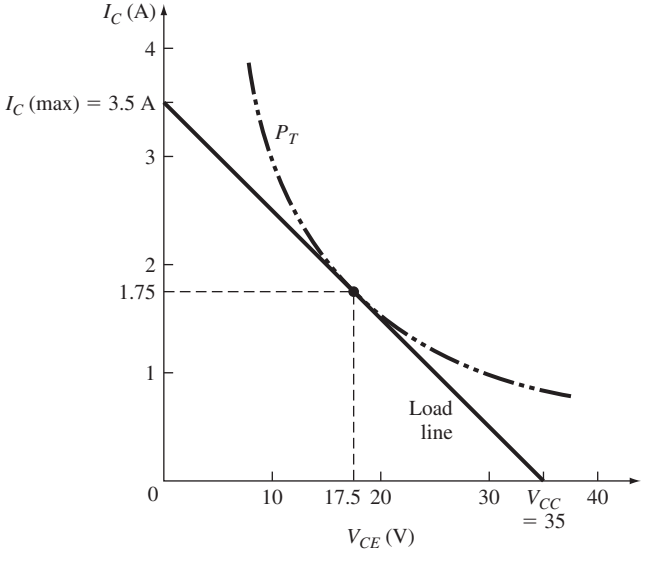

Figure 15.16 | Load line and maximum power curve for Example 15.1.

The collector–emitter voltage at this maximum power point is

$$V_{CE} = V_{CC} - I_C R_L = 35 - (1.75)(10) = 17.5 \text{ V}$$

The maximum power dissipated in the transistor occurs at the center of the load line. The maximum transistor power dissipation is therefore

$$P_T = V_{CE} I_C = (17.5)(1.75) = 30.6 \text{ W}$$

Comment

To find a transistor for a given application, safety factors are normally used. For this example, a transistor with a current rating greater than 3.5 A, a voltage rating greater than 35 V, and a power rating greater than 30.6 W would be required for the application just described.

EXERCISE PROBLEM

Ex 15.1 Assume the BJT in the common-emitter circuit shown in Figure 15.15 has limiting factors of $I_{C,\max} = 5\text{A}$, $V_{CE,\text{sus}} = 75$ V, and $P_T = 30$ *W*. Neglecting second breakdown effects, determine the minimum value of R_L such that the Q-point of the transistor always stays within the safe operating area for (*a*) $V_{CC} = 60$ V, (*b*) $V_{CC} = 40$ V, and (*c*) $V_{CC} = 20$ V. In each case, determine the maximum collector current and maximum transistor power dissipation.

[Ans. (*a*) $R_L = 30\ \Omega$, $I_{C(\max)} = 2$ A, $P_{(\max)} = 30$ W; (*b*) $R_L = 13.3\ \Omega$, $I_{C(\max)} = 3$ A, $P_{(\max)} = 30$ W; (*c*) $R_L = 4\ \Omega$, $I_{C(\max)} = 5$ A, $P_{(\max)} = 25$ W]

15.4.3 Darlington Pair Configuration

As mentioned, the base width of a power BJT is relatively wide so that the current gain is then relatively small. One method that is used to increase the effective current gain is to use a Darlington pair such as shown in Figure 15.17. Considering the currents, we see that

$$i_C = i_{CA} + i_{CB} = \beta_A i_B + \beta_B i_{EA} = \beta_A i_B + \beta_B (1 + \beta_A) i_B \tag{15.7}$$

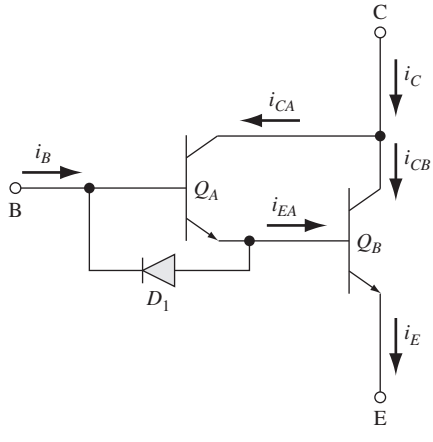

Figure 15.17 | An npn Darlington pair configuration.

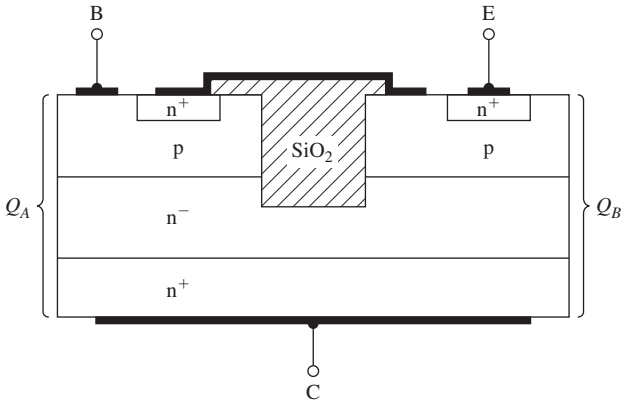

Figure 15.18 | An integrated circuit implementation of the npn Darlington pair configuration.

The overall common-emitter current gain is then

$$\frac{i_C}{i_B} = \beta_A\beta_B + \beta_A + \beta_B \tag{15.8}$$

Thus, if the gain of each individual transistor is $\beta_A = \beta_B = 15$, then the overall gain of the Darlington pair is $i_C/i_B = 255$. This overall gain is then substantially larger than that of the individual device. A diode may be incorporated as shown in Figure 15.17 to aid in turning off the transistor Q_B. A reverse current out of the base of Q_B through the diode will pull charge out of the base of this transistor and turn the device off faster than when no diode is used.

The Darlington pair shown in Figure 15.17 is typically used in the output stage of a power amplifier when an npn bipolar transistor is required. A pnp Darlington pair may also be used to increase the effective current gain of a power pnp device.

The integrated circuit configuration of the npn Darlington pair may be as shown in Figure 15.18. The silicon dioxide that is shown completely penetrates through the p-type base region so that the base regions of the two transistors are isolated.

TEST YOUR UNDERSTANDING

TYU 15.1 Consider the vertical power silicon BJT shown in Figure 15.10. Assume that a reverse-biased voltage of 200 V is applied to the base–collector junction. Calculate the space charge width that extends into the (*a*) collector region and (*b*) base region.

[Ans. (*a*) $x_d(n) = 0.506\ \mu m$; (*b*) $x_d(p) = 0.950\ \mu m$]

TYU 15.2 For the emitter–follower circuit in Figure 15.19, the parameters are $V_{CC} = 10$ V and $R_E = 200\ \Omega$. The transistor current gain is $\beta = 150$, and the current and voltage limitations are $I_{C,\max} = 200$ mA and $V_{CE,\text{sus}} = 50$ V. Determine the minimum transistor power rating such that the transistor Q-point is always inside the safe operating area.

(Ans. $P_{\max} = 0.5$ W)

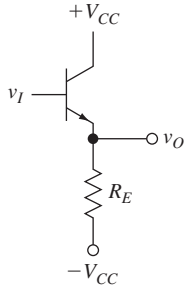

Figure 15.19 | Figure for Exercise TYU 15.2.

15.5 | POWER MOSFETs

The basic operation of the power MOSFET is the same as that of any MOSFET. However, the current handling capability of these devices is usually in the ampere range, and the drain-to-source blocking voltage may be in the range of 50 to 100 volts or even higher. One big advantage that a power MOSFET has over a bipolar power device is that the control signal is applied to the gate whose input impedance is extremely large. Even during switching between on and off states, the gate current is small, so that relatively large currents can be switched with very small control currents.

15.5.1 Power Transistor Structures

Large currents can be obtained in a MOSFET with a very large channel width. To achieve a large channel width device with good characteristics, power MOSFETs are fabricated with a repetitive pattern of small cells operating in parallel. To achieve a large blocking voltage, a vertical structure is used. There are two basic power MOSFET structures. The first is called a *DMOS* device and is shown in Figure 15.20. The DMOS device uses a double diffusion process: The p-base or the p-substrate region and the n^+ source contact are diffused through a common window defined by the edge of the gate. The p-base region is diffused deeper than the n^+ source, and the difference in the lateral diffusion distance between the p-base and the n^+ source defines the surface channel length.

Electrons enter the source terminal and flow laterally through the inversion layer under the gate to the n-drift region. The electrons then flow vertically through the n-drift region to the drain terminal. The conventional current direction is from the drain to the source. The n-drift region must be moderately doped so that the drain breakdown voltage is sufficiently large. However, the thickness of the n-drift region should also be as thin as possible to minimize drain resistance.

The second power MOSFET structure, shown in Figure 15.21, is a *VMOS* structure. The vertical channel or VMOS power device is a nonplanar structure that requires a different type of fabrication process. In this case, a p-base or p-"substrate" diffusion

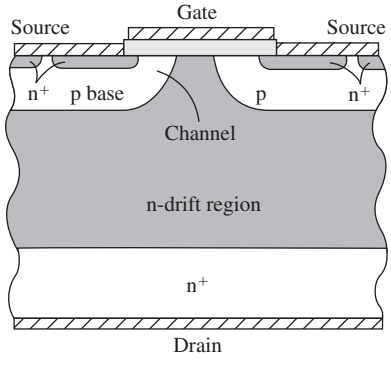

Figure 15.20 | Cross section of a double-diffused MOS (DMOS) transistor.

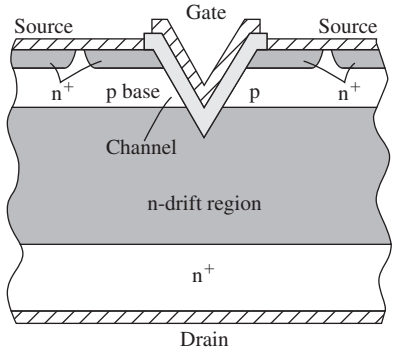

Figure 15.21 | Cross section of a vertical channel MOS (VMOS) transistor.

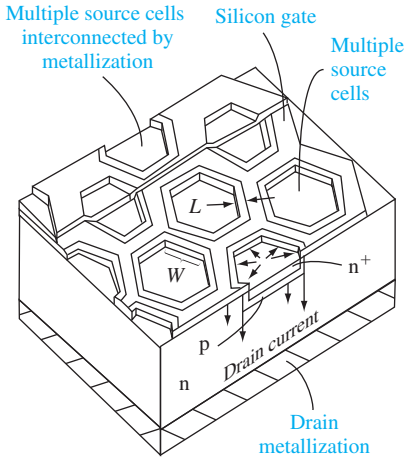

Figure 15.22 | A HEXFET structure.

is performed over the entire surface followed by the n^+ source diffusion. A V-shaped groove is then formed, extending through the n-drift region. It has been found that certain chemical solutions etch the (111) planes in silicon at a much slower rate than the other planes. If (100) oriented silicon is etched through a window at the surface, these chemical etches will create a V-shaped groove. A gate oxide is then grown in the V-shaped groove and the metal gate material is deposited. An electron inversion layer is formed in the base or substrate so that current is again essentially a vertical current between the source and the drain. The relatively low-doped n-drift region supports the drain voltage since the depletion region extends mainly into this low-doped region.

We mentioned that many individual MOSFET cells are connected in parallel to fabricate a power MOSFET with the proper width-to-length ratio. Figure 15.22 shows a HEXFET structure. Each cell is a DMOS device with an n^+ polysilicon gate. The HEXFET has a very high packing density—it may be on the order of 10^5 cells per cm^2. In the VMOS structure, the anisotropic etching of the grooves must be along the [110] direction on the (100) surface. This constraint limits the design options available for this type of device.

15.5.2 Power MOSFET Characteristics

Table 15.2 lists the basic parameters of two n-channel power MOSFETs. The drain currents are in the ampere range and the breakdown voltages are in the hundreds of volts range.

An important parameter of a power MOSFET is the *on resistance,* which can be written as

$$R_{on} = R_S + R_{CH} + R_D \tag{15.9}$$

where R_S is the resistance associated with the source contact, R_{CH} is the channel resistance, and R_D is the resistance associated with the drain contact. The R_S and R_D

Table 15.2 | Characteristics of two power MOSFETs

Parameter	2N6757	2N6792
V_{DS}(max) (V)	150	400
I_D(max) (at $T = 25°C$)	8	2
P_D(W)	75	20

resistance values are not necessarily negligible in power MOSFETs since small resistances and high currents can produce considerable power dissipation.

In the linear region of operation, we may write the channel resistance as

$$R_{CH} = \frac{L}{W\mu_n C_{ox}(V_{GS} - V_T)} \tag{15.10}$$

We have noted in previous chapters that mobility decreases with increasing temperature. The threshold voltage varies only slightly with temperature so that, as current in a device increases and produces additional power dissipation, the temperature of the device increases, the carrier mobility decreases, and R_{CH} increases, which inherently limits the channel current. The resistances R_S and R_D are proportional to semiconductor resistivity and so are also inversely proportional to mobility and have the same temperature characteristics as R_{CH}. Figure 15.23 shows a typical "on-resistance" characteristic as a function of drain current.

The increase in resistance with temperature provides stability for the power MOSFET. If the current in any particular cell begins to increase, the resulting temperature rise will increase the resistance, thus limiting the current. With this particular characteristic, the total current in a power MOSFET tends to be evenly distributed among the parallel cells, not concentrated in any single cell, a condition that can cause burnout.

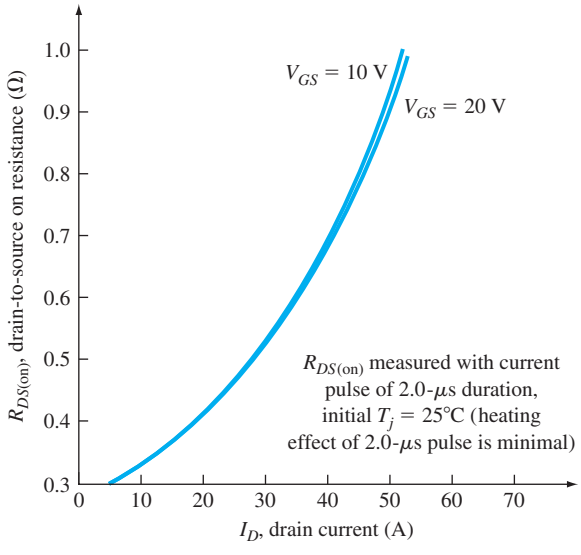

Figure 15.23 | Typical drain-to-source resistance versus drain current characteristics of a MOSFET.

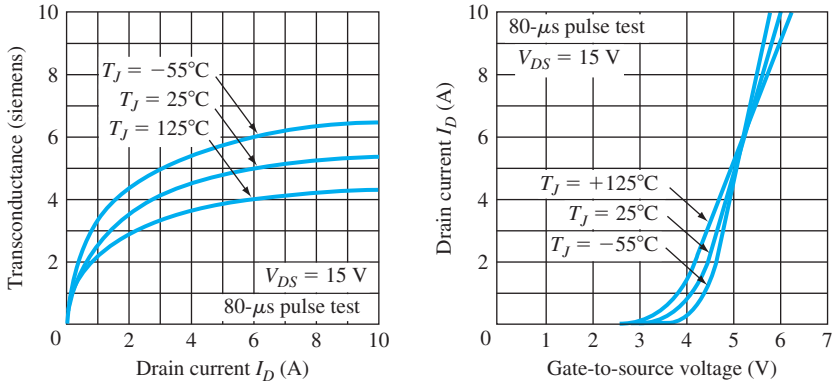

Figure 15.24 | Typical characteristics for high-power MOSFETs at various temperatures: (a) transconductance versus drain current; (b) drain current versus gate-to-source voltage.

Power MOSFETs differ from bipolar power transistors in both operating principles and performance. The superior performance characteristics of power MOSFETs are faster switching times, no second breakdown, and stable gain and response time over a wide temperature range. Figure 15.24a shows the transconductance of the 2N6757 versus temperature. The variation with temperature of the MOSFET transconductance is less than the variation in the BJT current gain that is shown in Figure 15.12. Figure 15.24b is a plot of drain current versus gate-to-source voltage at three different temperatures. We may note that at high current, the current decreases with temperature at a constant gate-to-source voltage, providing the stability that has been discussed.

Power MOSFETs must operate in a SOA. As with power BJTs, the SOA is defined by three factors: the maximum drain current, $I_{D,\max}$, rated breakdown voltage, BV_{DSS}, and the maximum power dissipation given by $P_T = V_{DS}I_D$. The SOA is shown in Figure 15.25a in which the current and voltage are plotted on linear scales. The

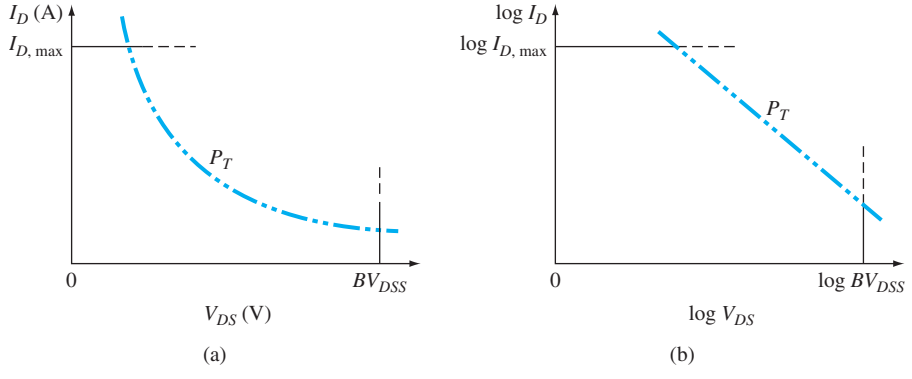

Figure 15.25 | The safe operating area (SOA) of a MOSFET plotted on (a) linear scales and (b) logarithmic scales.

same SOA curve is shown in Figure 15.25b in which the current and voltage are plotted on log scales.

EXAMPLE 15.2

Objective: Find the optimum drain resistor in a MOSFET inverter circuit.

A MOSFET inverter circuit is shown in Figure 15.26. Two different MOSFETs are being considered for use in the circuit. The parameters for devices *A* and *B* are given.

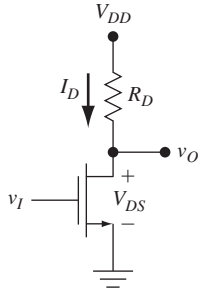

Figure 15.26 | A MOSFET inverter circuit.

Device A	Device B
$BV_{DSS} = 35$ V	$BV_{DSS} = 35$ V
$P_T = 30$ W	$P_T = 30$ W
$I_{D,\max} = 6$ A	$I_{D,\max} = 4$ A

■ Solution

The SOA curves for the two devices are shown in Figure 15.27.

The load line for the inverter circuit using device A is shown as curve A. The load line intersects the voltage axis at $V_{DD} = 24$ V. This curve is tangent to the maximum power curve and intersects the current axis at $I_D = 5$ A. Note that, if we had wanted the load line to intersect the maximum rated current of $I_{D,\max} = 6$ A, the load line would have gone outside of the SOA.

For the load line *A*, the drain resistance is

$$R_D = \frac{V_{DD}}{I_D} = \frac{24}{5} = 4.8\ \Omega$$

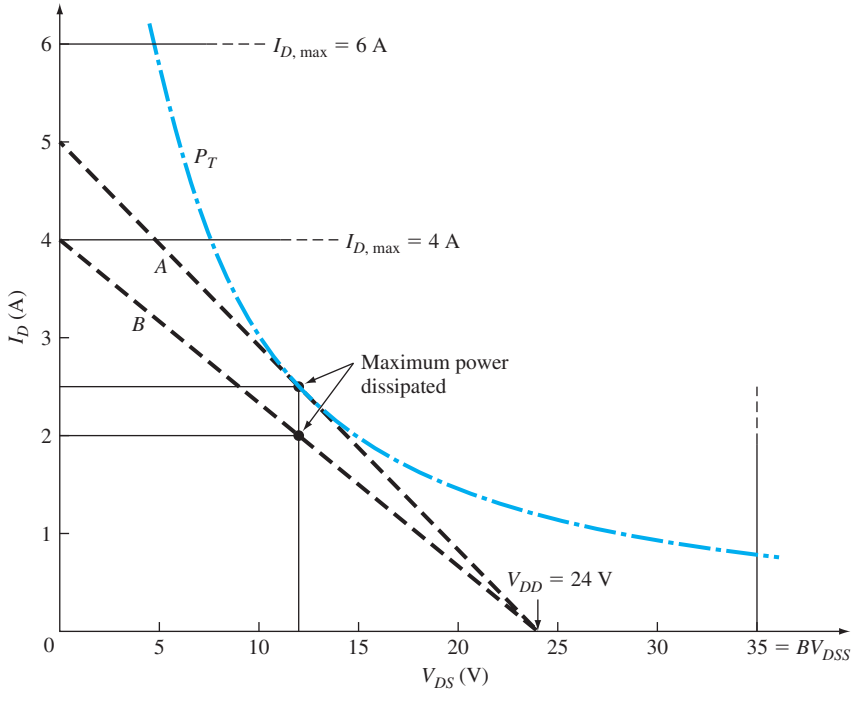

Figure 15.27 | Safe operating area and load lines for devices in Example 15.2.

The current at the maximum power point (using the results from Example 15.1) is

$$I_D = \frac{V_{DD}}{2R_D} = \frac{24}{2(4.8)} = 2.5 \text{ A}$$

and the corresponding drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D = 24 - (2.5)(4.8) = 12 \text{ V}$$

The maximum power that may be dissipated in the transistor is $P = V_{DS} I_D = (12)(2.5) = 30 \text{ W} = P_T$, which corresponds to the maximum rated power. This point is shown on the curve.

The load line for the inverter circuit using device B is shown as curve B. The load line intersects the voltage axis at $V_{DD} = 24$ V as before. This curve can now intersect the current axis at the maximum rated drain current of $I_{D,\max} = 4$ A. We see that the load line falls within the SOA of the transistor.

For load line B, the drain resistance is

$$R_D = \frac{V_{DD}}{I_D} = \frac{24}{4} = 6 \ \Omega$$

The current at the maximum power point is

$$I_D = \frac{V_{DD}}{2R_D} = \frac{24}{2(6)} = 2 \text{ A}$$

and the corresponding drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D = 24 - (2)(6) = 12 \text{ V}$$

The maximum power that may be dissipated in the transistor is $P = V_{DD} I_D = (12)(2) = 24$ W, which is less than the maximum rated power. This point is also shown on the curve.

Conclusion

We see that if device A is used, the drain resistor is determined by the maximum power. However, if device B is used, the drain resistor is determined by the maximum rated current of the device.

EXERCISE PROBLEM

Ex 15.2 Consider the common-source circuit shown in Figure 15.26. Determine the required current, voltage, and power ratings of the MOSFET for (*a*) $R_D = 12 \ \Omega$, $V_{DD} = 24$ V and (*b*) $R_D = 8 \ \Omega$, $V_{DD} = 40$ V.

[Ans. (*a*) $BV_{DSS} = 24$ V, $I_{D,\max} = 2$ A, $P_T = 12$ W; (*b*) $BV_{DSS} = 40$ V, $I_{D,\max} = 5$ A, $P_T = 50$ W]

15.5.3 Parasitic BJT

The MOSFET has a parasitic BJT as an inherent part of its structure. The parasitic BJT may be seen in both the DMOS and VMOS structures shown in Figures 15.20 and 15.21. The source terminal corresponds to the n-type emitter, the p-type base or substrate region corresponds to the p-type base, and the n-type drain corresponds to the n-type collector. This is also shown schematically in Figure 15.28. The channel length of the MOSFET corresponds to the base width of the parasitic BJT. Since this length is normally quite small, the current gain β of the BJT can be larger than unity.