then formed between the source and drain contacts. The forward-bias gate voltage must not be too large or an undesirable gate current will be present in the device.

## EXERCISE PROBLEM

**Ex 13.6** An n-channel GaAs MESFET has a gate barrier height of $\phi_{Bn} = 0.89$ V. The channel doping concentration is $N_d = 10^{16}$ cm$^{-3}$. What channel thickness is required to yield a threshold voltage of $V_T = 0.25$ V?

(Ans. $a = 0.280\ \mu m$)

Ideally, the *I–V* characteristics of the enhancement mode device are the same as the depletion mode device—the only real difference is the relative values of the internal pinchoff voltage. The current in the saturation region is given by Equation (13.35) as

$$I_{D1} = I_{D1}(\text{sat}) = I_{P1}\left\{1 - 3\left(\frac{V_{bi} - V_{GS}}{V_{p0}}\right)\left[1 - \frac{2}{3}\sqrt{\frac{V_{bi} - V_{GS}}{V_{p0}}}\right]\right\}$$

The threshold voltage for the n-channel device is defined in Equation (13.42) as $V_T = V_{bi} - V_{p0}$, so we can also write

$$V_{bi} = V_T + V_{p0} \tag{13.43}$$

Substituting this expression for $V_{bi}$ into Equation (13.35), we obtain

$$I_{D1}(\text{sat}) = I_{P1}\left\{1 - 3\left[1 - \left(\frac{V_{GS} - V_T}{V_{p0}}\right)\right] + 2\left[1 - \left(\frac{V_{GS} - V_T}{V_{p0}}\right)\right]^{3/2}\right\} \tag{13.44}$$

Equation (13.44) is valid for $V_{GS} \geq V_T$.

When the transistor first turns on, we have $(V_{GS} - V_T) \ll V_{p0}$. Equation (13.44) can then be expanded into a Taylor series and we obtain

$$I_{D1}(\text{sat}) \approx I_{P1}\left[\frac{3}{4}\left(\frac{V_{GS} - V_T}{V_{p0}}\right)\right]^2 \tag{13.45}$$

Substituting the expressions for $I_{P1}$ and $V_{p0}$, Equation (13.45) becomes

$$I_{D1}(\text{sat}) = \frac{\mu_n \epsilon_s W}{2aL}(V_{GS} - V_T)^2 \quad \text{for } V_{GS} \geq V_T \tag{13.46}$$

We can now write Equation (13.46) as

$$\boxed{I_{D1}(\text{sat}) = k_n(V_{GS} - V_T)^2} \tag{13.47}$$

where

$$\boxed{k_n = \frac{\mu_n \epsilon_s W}{2aL}} \tag{13.48}$$

The factor $k_n$ is called a *conduction parameter*. The form of Equation (13.47) is the same as for a MOSFET.

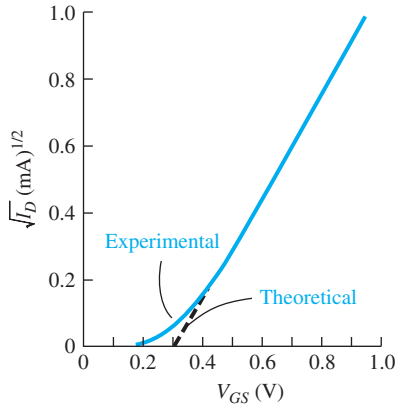


**Figure 13.14** | Experimental and theoretical $\sqrt{I_D}$ versus $V_{GS}$ characteristics of an enhancement mode JFET.

The square root of Equation (13.47), or $\sqrt{I_{D1}(\text{sat})}$ versus $V_{GS}$, is plotted as the ideal dotted curve shown in Figure 13.14. The ideal curve intersects the voltage axis at the threshold voltage, $V_T$. The solid line shows an experimental plot. Equation (13.46) does not describe the experimental results well near the threshold voltage. The ideal current–voltage relationship is derived assuming an abrupt depletion approximation for the pn junction. However, when the depletion region extends almost through the channel, a more accurate model of the space charge region must be used to more accurately predict the drain current characteristics near threshold. We consider the subthreshold conduction in Section 13.3.3.

**DESIGN EXAMPLE 13.7**

Objective: Design the channel width of an n-channel GaAs enhancement-mode pn JFET to produce a specified current for a given bias.

Consider the GaAs JFET described in Example 13.6. In addition, assume $\mu_n = 8000\ \text{cm}^2/\text{V-s}$ and $L = 1.2\ \mu\text{m}$. Design the width such that $I_{D1} = 75\ \mu\text{A}$ with an applied voltage of $V_{GS} = 0.5\ \text{V}$.

### ■ Solution

In the saturation region, the current is given by

$$I_{D1} = k_n(V_{GS} - V_T)^2$$

or

$$75 \times 10^{-6} = k_n(0.5 - 0.24)^2$$

The conduction parameter is then

$$k_n = 1.109\ \text{mA/V}^2$$

The conduction parameter, from Equation (13.48), is given by

$$k_n = \frac{\mu_n \epsilon_s W}{2aL}$$

or

$$1.109 \times 10^{-3} = \frac{(8000)(13.1)(8.85 \times 10^{-14})(W)}{2(0.70 \times 10^{-4})(1.2 \times 10^{-4})}$$

The required channel width is then

$$W = 20.1\ \mu\text{m}$$

### Comment

The saturation current will obviously increase if $V_{GS}$ is increased or if the width of the transistor is increased.

### EXERCISE PROBLEM

**Ex 13.7** Consider the GaAs MESFET described in Exercise Problem Ex 13.5. In addition, assume $\mu_n = 7000\ \text{cm}^2/\text{V-s}$, $L = 0.8\ \mu\text{m}$, and $W = 25\ \mu\text{m}$. Calculate the conduction parameter $k_n$ and the current $I_{D1}(\text{sat})$ for $V_{GS} = 0.50$ V.
[Ans. $k_n = 3.17\ \text{mA/V}^2$, $I_{D1}(\text{sat}) = 0.325\ \text{mA}$]

The transconductance of the enhancement mode device operating in the saturation region can also be derived. Using Equation (13.47), we can write

$$g_{ms} = \frac{\partial I_{D1}(\text{sat})}{\partial V_{GS}} = 2k_n(V_{GS} - V_T) \tag{13.49}$$

The transconductance increases as $V_{GS}$ increases for the enhancement mode device as it did for the depletion mode device.

### TEST YOUR UNDERSTANDING

**TYU 13.1** Consider a GaAs pn junction n-channel FET. The $p^+$ gate doping concentration is $N_a = 5 \times 10^{18}\ \text{cm}^{-3}$ and the n-channel doping concentration is $N_d = 5 \times 10^{15}\ \text{cm}^{-3}$. The zero-bias depletion width is to be $1.2a$; that is, the channel is completely depleted at zero bias. Determine the value of $a$ and the pinchoff voltage.
(Ans. $a = 0.513\ \mu\text{m}$, $V_p = +0.397\ \text{V}$)

**TYU 13.2** The pinchoff current $I_{P1}$ given by Equation (13.28) and the pinchoff voltage given by Equation (13.26c) also apply to a p-channel JFET in which $\mu_n$ is replaced by $\mu_p$ and $N_d$ is replaced by $N_a$. Assume a p-channel silicon JFET has the following parameters: $N_d = 5 \times 10^{18}\ \text{cm}^{-3}$, $N_a = 2 \times 10^{16}\ \text{cm}^{-3}$, $a = 0.50\ \mu\text{m}$, $L = 5\ \mu\text{m}$, $W = 40\ \mu\text{m}$, and $\mu_p = 400\ \text{cm}^2/\text{V-s}$. Calculate the pinchoff current $I_{P1}$ and the maximum drain current $I_{D1}(\text{sat})$ for $V_{GS} = 0$.
[Ans. $I_{P1} = 0.659\ \text{mA}$, $I_{D1}(\text{sat}) = 0.256\ \text{mA}$]

## *13.3 | NONIDEAL EFFECTS

As with any semiconductor device, there are nonideal effects that will change the ideal device characteristics. In all of the previous discussions, we have considered an ideal transistor with a constant channel length and constant mobility; we have also

neglected gate currents. However, when a JFET is biased in the saturation region, the effective electrical channel length is a function of $V_{DS}$. This nonideal effect is called channel length modulation. In addition, when a transistor is biased near or in the saturation region, the electric field in the channel can become large enough so that the majority carriers reach their saturation velocity. At this point, the mobility is no longer a constant. The magnitude of the gate current will affect the input impedance, which may need to be taken into account in a circuit design.

### 13.3.1 Channel Length Modulation

The expression for the drain current is inversely proportional to the channel length $L$ as given, for example, by Equation (13.27). In deriving the current equations, we have implicitly assumed that the channel length was constant. However, the effective channel length can change. Figure 13.5 shows the space charge region in the channel when the transistor is biased in the saturation region. The neutral n-channel length decreases as $V_{DS}$ increases; thus, the drain current will increase. The change in the effective channel length and the corresponding change in drain current is called channel length modulation.

The pinchoff current, Equation (13.28), is modified by the channel length modulation and can be written as

$$I'_{P1} = \frac{\mu_n (eN_d)^2 W a^3}{6\epsilon_s L'} \tag{13.50}$$

where

$$L' \approx L - \frac{1}{2}\Delta L \tag{13.51}$$

If we assume the channel depletion region shown in Figure 13.5 extends equally into the channel and drain regions, then as a first approximation, we will include the factor $\frac{1}{2}$ in the expression for $L'$.

The drain current can be written as

$$I'_{D1} = I_{D1} \cdot \frac{I'_{P1}}{I_{P1}} = I_{D1}\left(\frac{L}{L - \frac{1}{2}\Delta L}\right) \tag{13.52}$$

where $I_{D1}$ is the ideal drain current predicted by Equation (13.35). Another form of the current–voltage characteristic in the saturation region is given by

$$I'_{D1}(\text{sat}) = I_{D1}(\text{sat})(1 + \lambda V_{DS}) \tag{13.53}$$

The effective channel length $L'$ supports the $V_{DS}(\text{sat})$ voltage, and the space charge region length $\Delta L$ in the channel supports the drain voltage beyond the saturation value. Neglecting charges in the space charge region due to current flow, the depletion length $\Delta L$ is then, to a first approximation, given by

$$\Delta L = \left[\frac{2\epsilon_s (V_{DS} - V_{DS}(\text{sat}))}{eN_d}\right]^{1/2} \tag{13.54}$$

Since the effective channel length changes with $V_{DS}$, the drain current is now a function of $V_{DS}$. The small-signal output impedance at the drain terminal can be defined as

$$r_{ds} = \frac{\partial V_{DS}}{\partial I'_{D1}} \approx \frac{\Delta V_{DS}}{\Delta I'_{D1}} \tag{13.55}$$

**EXAMPLE 13.8**

Objective: Calculate the small-signal output resistance at the drain terminal due to channel length modulation effects.

Consider an n-channel depletion mode silicon JFET with a channel doping of $N_d = 3 \times 10^{15}$ cm$^{-3}$. Calculate $r_{ds}$ for the case when $V_{DS}$ changes from $V_{DS}(1) = V_{DS}(\text{sat}) + 2.0$ to $V_{DS}(2) = V_{DS}(\text{sat}) + 2.5$. Assume $L = 10\ \mu$m and $I_{D1} = 4.0$ mA.

### ■ Solution

We have that

$$r_{ds} = \frac{\Delta V_{DS}}{\Delta I'_{D1}} = \frac{V_{DS}(2) - V_{DS}(1)}{\Delta I'_{D1}(2) - I'_{D1}(1)}$$

We can calculate the change in the channel length for the two voltages as

$$\Delta L(2) = \left[\frac{2\epsilon_s(V_{DS}(2) - V_{DS}(\text{sat}))}{eN_d}\right]^{1/2} = \left[\frac{2(11.7)(8.85 \times 10^{-14})(2.5)}{(1.6 \times 10^{-19})(3 \times 10^{15})}\right]^{1/2} = 1.04\ \mu\text{m}$$

and

$$\Delta L(1) = \left[\frac{2(11.7)(8.85 \times 10^{-14})(2.0)}{(1.6 \times 10^{-19})(3 \times 10^{15})}\right]^{1/2} = 0.929\ \mu\text{m}$$

The drain currents are then

$$I'_{D1}(2) = I_{D1}\left(\frac{L}{L - \frac{1}{2}\Delta L(2)}\right) = 4.0\left(\frac{10}{9.48}\right)$$

and

$$I'_{D1}(1) = I_{D1}\left(\frac{L}{L - \frac{1}{2}\Delta L(1)}\right) = 4.0\left(\frac{10}{9.54}\right)$$

The output resistance can be calculated as

$$r_{ds} = \frac{2.5 - 2.0}{4\left(\frac{10}{9.48}\right) - 4\left(\frac{10}{9.54}\right)} = 18.9\ \text{k}\Omega$$

### ■ Comment

This value of output resistance is significantly less than the ideal value of infinity.

### ■ EXERCISE PROBLEM

**Ex 13.8** Repeat Example 13.8 if the channel doping concentration increases to $N_d = 10^{16}$ cm$^{-3}$. All other parameters remain the same.

(Ans. $r_{ds} = 39.4\text{k}\Omega$)

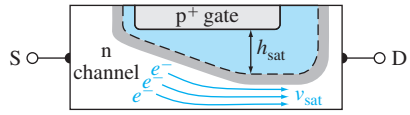


**Figure 13.15** | Cross section of JFET showing carrier velocity and space charge width saturation effects.

For high-frequency MESFETs, typical channel lengths are on the order of 1 $\mu$m. Channel length modulation and other effects become very important in short-channel devices.

### 13.3.2 Velocity Saturation Effects

We have seen that the drift velocity of a carrier in silicon saturates with increasing electric field. This velocity saturation effect implies that the mobility is not a constant. For very short channels, the carriers can easily reach their saturation velocity, which changes the *I–V* characteristics of the JFET.

Figure 13.15 shows the channel region with an applied drain voltage. As the channel narrows at the drain terminal, the velocity of the carriers increases since the current through the channel is constant. The carriers first saturate at the drain end of the channel. The depletion region will reach a saturation thickness, so we can write

$$I_{D1}(\text{sat}) = eN_d v_{\text{sat}}(a - h_{\text{sat}})W \tag{13.56}$$

where $v_{\text{sat}}$ is the saturation velocity and $h_{\text{sat}}$ is the saturation depletion width. This saturation effect occurs at a drain voltage smaller than the $V_{DS}(\text{sat})$ value determined previously. Both $I_{DS}(\text{sat})$ and $V_{DS}(\text{sat})$ will be smaller than previously calculated.

Figure 13.16 shows normalized plots of $I_D$ versus $V_{DS}$. Figure 13.16a is for the case of a constant mobility and Figure 13.16b is for the case of velocity saturation. Since the *I–V* characteristics change when velocity saturation occurs, the transconductance will also change—the transconductance will become smaller; hence, the effective gain of the transistor decreases when velocity saturation occurs.

### 13.3.3 Subthreshold and Gate Current Effects

The subthreshold current is the drain current in the JFET that exists when the gate voltage is below the pinchoff or threshold value. The subthreshold conduction is shown in Figure 13.14. When the JFET is biased in the saturation region, the drain current varies quadratically with gate-to-source voltage. When $V_{GS}$ is below the threshold value, the drain current varies exponentially with gate-to-source voltage. Near threshold, the abrupt depletion approximation does not accurately model the channel region: A more detailed potential profile in the space charge region must be used. However, these calculations are beyond the scope of this chapter.

When the gate voltage is approximately 0.5 to 1.0 V below threshold in an n-channel MESFET, the drain current reaches a minimum value and then slowly increases as the gate voltage decreases. The drain current in this region is the gate leakage current. Figure 13.17 is a plot of the drain current versus $V_{GS}$ for the three regions

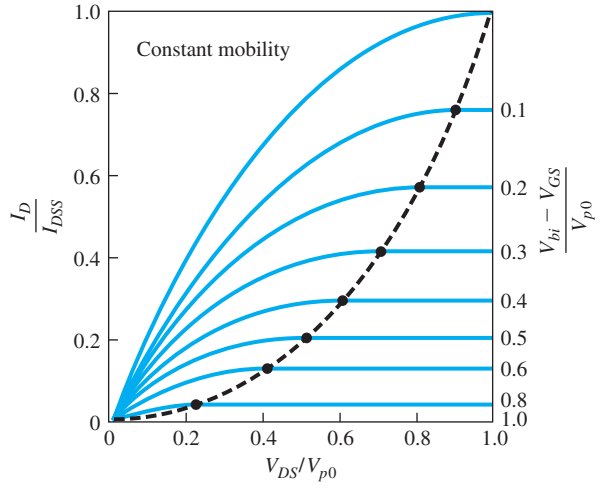


**Figure 13.16** | Normalized $I_D$ versus $V_{DS}$ plots for a constant mobility and field-dependent mobility.
*(From Sze [19].)*

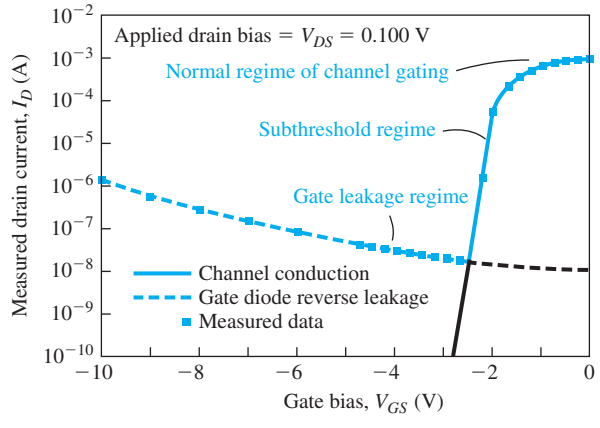


**Figure 13.17** | Measured drain current versus $V_{GS}$ for a GaAs MESFET showing the normal drain current, subthreshold current, and gate leakage current.
*(From Daring [2].)*

of gate voltage. The curve illustrates that the drain current becomes small below threshold, but is not zero. The minimum drain current may need to be accounted for in low-power circuit applications.

## *13.4 | EQUIVALENT CIRCUIT AND FREQUENCY LIMITATIONS

In order to analyze a transistor circuit, one needs a mathematical model or equivalent circuit of the transistor. One of the most useful models is the small-signal equivalent circuit, which applies to transistors used in linear amplifier circuits. This equivalent circuit will introduce frequency effects in the transistor through the equivalent capacitor–resistor circuits. The various physical factors in the JFET affecting the frequency limitations are considered here and a transistor cutoff frequency, which is a figure of merit, is then defined.

### 13.4.1 Small-Signal Equivalent Circuit

The cross section of an n-channel pn JFET is shown in Figure 13.18, including source and drain series resistances. The substrate may be semi-insulating gallium arsenide or it may be a $p^+$ type substrate.

Figure 13.19 shows a small-signal equivalent circuit for the JFET. The voltage $V_{g's'}$ is the internal gate-to-source voltage that controls the drain current. The $r_{gs}$ and $C_{gs}$ parameters are the gate-to-source diffusion resistance and junction capacitance, respectively. The gate-to-source junction is reverse biased for depletion mode devices and has only a small forward-bias voltage for enhancement mode devices, so that normally $r_{gs}$ is large. The parameters $r_{gd}$ and $C_{gd}$ are the gate-to-drain resistance and capacitance, respectively. The resistance $r_{ds}$ is the finite drain resistance, which is a function of the channel length modulation effect. The $C_{ds}$ capacitance is mainly a drain-to-source parasitic capacitance and $C_s$ is the drain-to-substrate capacitance.

The ideal small-signal equivalent circuit is shown in Figure 13.20a. All diffusion resistances are infinite, the series resistances are zero, and at low frequency the

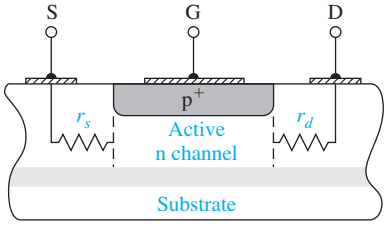


**Figure 13.18** | Cross section of JFET with source and drain series resistance.

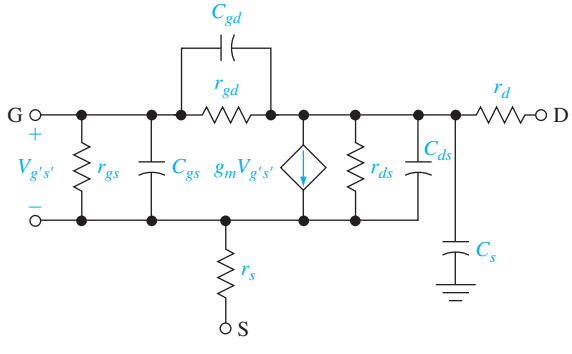


**Figure 13.19** | Small-signal equivalent circuit of JFET.

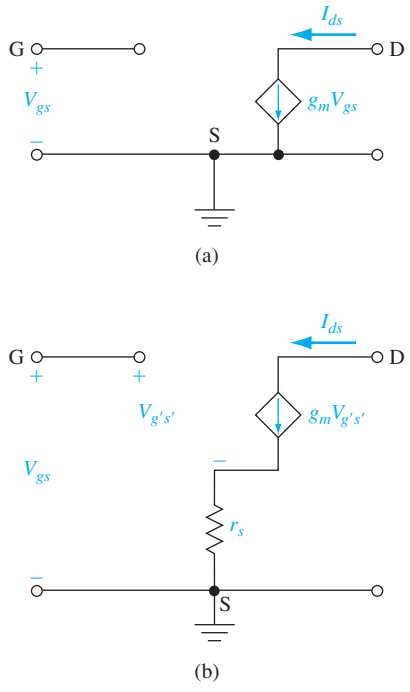


**Figure 13.20** | (a) Ideal low-frequency small-signal equivalent circuit. (b) Ideal equivalent circuit including $r_s$.

capacitances become open circuits. The small-signal drain current is now

$$I_{ds} = g_m V_{gs} \tag{13.57}$$

which is a function only of the transconductance and the input-signal voltage.

The effect of the source series resistance can be determined using Figure 13.20b. We have

$$I_{ds} = g_m V_{g's'} \tag{13.58}$$

The relation between $V_{gs}$ and $V_{g's'}$ can be found from

$$V_{gs} = V_{g's'} + (g_m V_{g's'}) r_s = (1 + g_m r_s) V_{g's'} \tag{13.59}$$

Equation (13.58) can then be written as

$$I_{ds} = \left(\frac{g_m}{1 + g_m r_s}\right) V_{gs} = g'_m V_{gs} \tag{13.60}$$

The effect of the source resistance is to reduce the effective transconductance or transistor gain.

Recall that $g_m$ is a function of the dc gate-to-source voltage, so $g'_m$ will also be a function of $V_{GS}$. Equation (13.41b) is the relation between $g_m$ and $V_{GS}$ when the

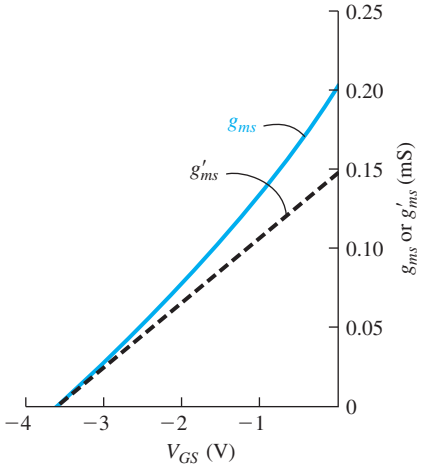


**Figure 13.21** | JFET transconductance versus $V_{GS}$ (a) without and (b) with a source series resistance.

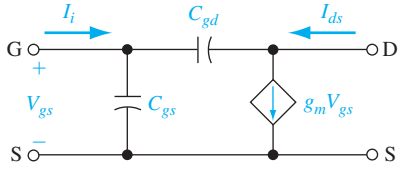


**Figure 13.22** | A small-signal equivalent circuit with capacitance.

transistor is biased in the saturation region. Figure 13.21 shows a comparison between the theoretical and experimental transconductance values using the parameters from Example 13.4 and letting $r_s = 2000\ \Omega$. (A value of $r_s = 2000\ \Omega$ may seem excessive, but keep in mind that the active thickness of the semiconductor may be on the order of 1 $\mu$m or less; thus, a large series resistance may result if special care is not taken.)

### 13.4.2 Frequency Limitation Factors and Cutoff Frequency

There are two frequency limitation factors in a JFET. The first is the channel transit time. If we assume a channel length of 1 $\mu$m and assume carriers are traveling at their saturation velocity, then the transit time is on the order of

$$\tau_t = \frac{L}{v_s} = \frac{1 \times 10^{-4}}{1 \times 10^{+7}} = 10 \text{ ps} \tag{13.61}$$

The channel transit time is normally not the limiting factor except in very high frequency devices.

The second frequency limitation factor is the capacitance charging time. Figure 13.22 is a simplified equivalent circuit that includes the primary capacitances and ignores the diffusion resistances. The output current will be the short-circuit current. As the frequency of the input-signal voltage $V_{gs}$ increases, the impedance of $C_{gd}$ and $C_{gs}$ decreases so the current through $C_{gd}$ will increase. For a constant $g_m V_{gs}$, the $I_{ds}$ current will then decrease. The output current then becomes a function of frequency.

If the capacitance charging time is the limiting factor, then the cutoff frequency $f_T$ is defined as the frequency at which the magnitude of the input current $I_i$ is equal to the magnitude of the ideal output current $g_m V_{gs}$ of the intrinsic transistor. We have,

when the output is short-circuited,

$$I_i = j\omega\,(C_{gs} + C_{gd})V_{gs} \tag{13.62}$$

If we let $C_G = C_{gs} + C_{gd}$, then at the cutoff frequency

$$|I_i| = 2\pi f_T C_G V_{gs} = g_m V_{gs} \tag{13.63}$$

or

$$f_T = \frac{g_m}{2\pi C_g} \tag{13.64}$$

From Equation (13.41b), the maximum possible transconductance is

$$g_{ms}\,(\max) = G_{01} = \frac{e\mu_n N_d W a}{L} \tag{13.65}$$

and the minimum gate capacitance is

$$C_G\,(\min) = \frac{\epsilon_s W L}{a} \tag{13.66}$$

where $a$ is the maximum space charge width. The maximum cutoff frequency can be written as

$$\boxed{f_T = \frac{e\mu_n N_d a^2}{2\pi\epsilon_s L^2}} \tag{13.67}$$

**EXAMPLE 13.9**

Objective: Calculate the cutoff frequency of a silicon JFET.

Consider a silicon JFET with the following parameters:

$$\mu_n = 1000\ \text{cm}^2/\text{V-s} \qquad a = 0.60\ \mu\text{m}$$

$$N_d = 10^{16}\ \text{cm}^{-3} \qquad L = 5\ \mu\text{m}$$

### Solution

Substituting the parameters into Equation (13.67), we have

$$f_T = \frac{e\mu_n N_d a^2}{2\pi\epsilon_s L^2} = \frac{(1.6\times10^{-19})(1000)(10^{16})\,(0.6\times10^{-4})^2}{2\pi(11.7)(8.85\times10^{-14})(5\times10^{-4})^2} = 3.54\ \text{GHz}$$

### Comment

This example shows that even silicon JFETs can have relatively large cutoff frequencies.

### EXERCISE PROBLEM

**Ex 13.9** The parameters of an n-channel silicon JFET are $\mu_n = 1000\ \text{cm}^2/\text{V-s}$, $N_d = 5\times10^{15}\ \text{cm}^{-3}$, $a = 0.50\ \mu\text{m}$, and $L = 2\ \mu\text{m}$. Determine the cutoff frequency.

(Ans. $f_T = 7.69$ GHz)

For gallium arsenide JFETs or MESFETs with very small geometries, the cutoff frequency is even larger. The channel transit time may also become a factor in very high frequency devices, in which case the expression for cutoff frequency would need to be modified.

One application of GaAs FETs is in ultrafast digital integrated circuits. Conventional GaAs MESFET logic gates can achieve propagation delay times in the sub nanosecond range. These delay times are at least comparable to, if not shorter than, fast ECL, but the power dissipation is three orders of magnitude smaller than in the ECL circuits. Enhancement mode GaAs JFETs have been used as drivers in logic circuits, and depletion mode devices may be used as loads. Propagation delay times of as low as 45 ps have been observed. Special JFET structures may be used to further increase the speed. These structures include the modulation-doped field-effect transistor, which is discussed in the following section.

### TEST YOUR UNDERSTANDING

**TYU 13.3** Consider a p-channel silicon JFET that has parameters $a = 0.50\ \mu$m, $\mu_p = 400\ \text{cm}^2/\text{V-s}$, $N_a = 2 \times 10^{16}\ \text{cm}^{-3}$, and $L = 4\ \mu$m. Calculate the cutoff frequency.

(Ans. $f_T = 3.07\ \text{GHz}$)

**TYU 13.4** An n-channel GaAs pn JFET has parameters $a = 0.50\ \mu$m, $L = 1\ \mu$m, $N_d = 3 \times 10^{15}\ \text{cm}^{-3}$, and $\mu_n = 6500\ \text{cm}^2/\text{V-s}$. Determine the cutoff frequency.

(Ans. $f_T = 107\ \text{GHz}$)

## *13.5 | HIGH ELECTRON MOBILITY TRANSISTOR

As frequency needs, power capacity, and low noise performance requirements increase, the gallium arsenide MESFET is pushed to its limit of design and performance. These requirements imply a very small FET with a short channel length, large saturation current, and large transconductance. These requirements are generally achieved by increasing the channel doping under the gate. In all of the devices we have considered, the channel region is in a doped layer of bulk semiconductor with the majority carriers and doping impurities in the same region. The majority carriers experience ionized impurity scattering, which reduces carrier mobility and degrades device performance.

The degradation in mobility and peak velocity in GaAs due to increased doping can be minimized by separating the majority carriers from the ionized impurities. This separation can be achieved in a heterostructure that has an abrupt discontinuity in conduction and valence bands. We considered the basic heterojunction properties in Chapter 9. Figure 13.23 shows the conduction-band energy relative to the Fermi energy of an N-AlGaAs-intrinsic GaAs heterojunction in thermal equilibrium. Thermal equilibrium is achieved when electrons from the wide-bandgap AlGaAs flow into the GaAs and are confined to the potential well. However, the electrons are free to move parallel to the heterojunction interface. In this structure, the majority carrier

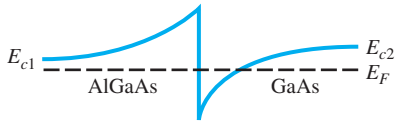


**Figure 13.23 |** Conduction-band edges for N-AlGaAs–intrinsic GaAs abrupt heterojunction.

electrons in the potential well are now separated from the impurity dopant atoms in the AlGaAs; thus, impurity scattering tends to be minimized.

The FETs fabricated from these heterojunctions are known by several names. The term used here is the **h**igh **e**lectron **m**obility **t**ransistor (HEMT). Other names include **mo**dulation-**d**oped **f**ield-**e**ffect **t**ransistor (MODFET), **s**electively **d**oped **h**etero junction field-effect **t**ransistor (SDHT), and **t**wo-dimensional **e**lectron **g**as **f**ield-**e**ffect **t**ransistor (TEGFET).

### 13.5.1 Quantum Well Structures

Figure 13.23 shows the conduction-band energy of an N-AlGaAs–intrinsic GaAs heterojunction. A two-dimensional surface channel layer of electrons is formed in the thin potential well (~80Å) in the undoped GaAs. Electron sheet carrier densities on the order of $10^{12}$ cm$^{-2}$ have been obtained. An improvement in the low-field mobility of the carriers moving parallel to the heterojunction is observed since the impurity-scattering effects are reduced. At 300 K, mobilities have been reported in the range of 8500–9000 cm$^2$/V-s, whereas GaAs MESFETs doped to $N_d = 10^{17}$ cm$^{-3}$ have low-field mobilities of less than 5000 cm$^2$/V-s. The electron mobility in the heterojunction now tends to be dominated by lattice or phonon scattering, so that as the temperature is reduced, the mobility increases rapidly.

Impurity-scattering effects can be further reduced by increasing the separation of the electrons and ionized donor impurities. The electrons in the potential well of the abrupt heterojunction shown in Figure 13.23 are separated from the donor atoms, but are still close enough to be subjected to a coulomb attraction. A thin spacer layer of undoped AlGaAs can be placed between the doped AlGaAs and the undoped GaAs. Figure 13.24 shows the energy-band diagram for this structure. Increasing the

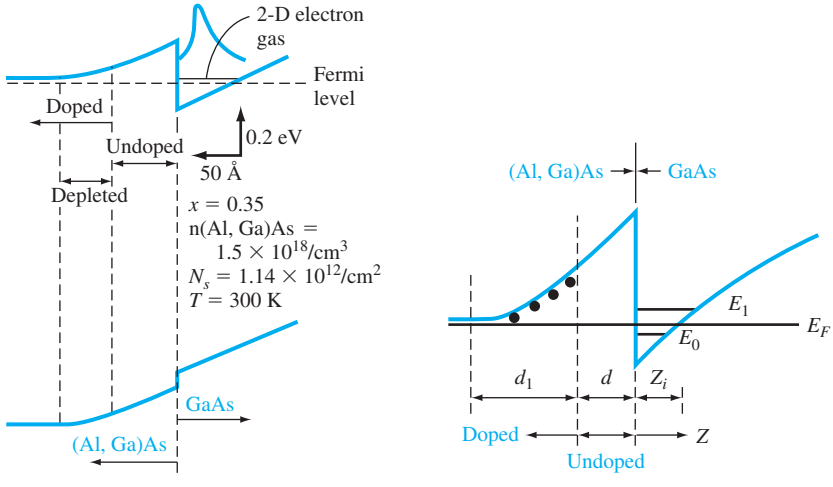


**Figure 13.24** | Conduction-band edges for N-AlGaAs–undoped AlGaAs–undoped GaAs heterojunction.
*(From Shur [13].)*

separation between the carriers and ionized donors increases further the electron mobility, since there is even less coulomb interaction. One disadvantage of this graded heterojunction is that the electron density in the potential well tends to be smaller than in the abrupt junction.

The molecular beam epitaxial process allows the growth of very thin layers of specific semiconductor materials with specific dopings. In particular, a multilayer modulation–doped heterostructure can be formed, as shown in Figure 13.25. Several surface channel layers of electrons are formed in parallel. This structure would be equivalent to increasing the channel electron density, which would increase the current capability of the FET.

### 13.5.2 Transistor Performance

A typical HEMT structure is shown in Figure 13.26. The N-AlGaAs is separated from the undoped GaAs by an undoped AlGaAs spacer. A Schottky contact to the N-AlGaAs forms the gate of the transistor. This structure is a "normal" MODFET. An "inverted" structure is shown in Figure 13.27. In this case the Schottky contact is made to the undoped GaAs layer. The inverted MODFET has been investigated less than the normal structure because the normal structure has yielded superior results.

The density of electrons in the two-dimensional electron gas layer in the potential well can be controlled by the gate voltage. The electric field of the Schottky gate depletes the two-dimensional electron gas layer in the potential well when a

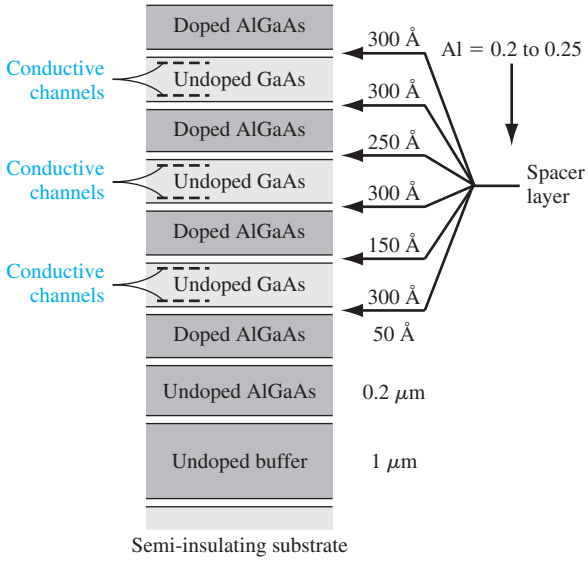


**Figure 13.25** | Multilayer modulation–doped heterostructure.

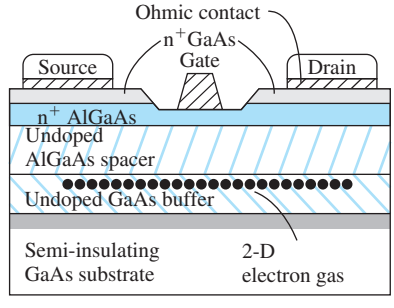


**Figure 13.26** | A "normal" AlGaAs–GaAs HEMT.

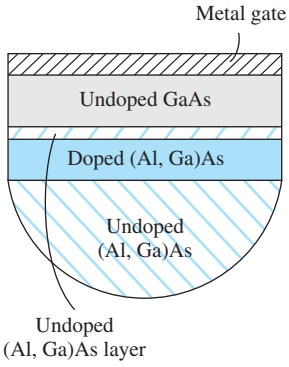


**Figure 13.27** | An "inverted" GaAs–AlGaAs HEMT. (*From Shur* [*13*].)

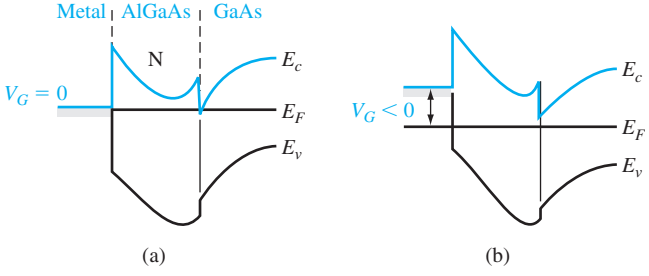


**Figure 13.28** | Energy-band diagram of a normal HEMT (a) with zero gate bias and (b) with a negative gate bias.

sufficiently large negative voltage is applied to the gate. Figure 13.28 shows the energy-band diagrams of the metal–AlGaAs–GaAs structure under zero bias and with a reverse bias applied to the gate. With zero bias, the conduction-band edge in the GaAs is below the Fermi level, implying a large density of the two-dimensional electron gas. With a negative voltage applied to the gate, the conduction-band edge in the GaAs is above the Fermi level, implying that the density of the two-dimensional electron gas is very small and the current in an FET would be essentially zero.

The Schottky barrier depletes the AlGaAs layer from the surface, and the heterojunction depletes the AlGaAs layer from the heterojunction interface. Ideally the device should be designed so that the two depletion regions just overlap to prevent electron conduction through the AlGaAs layer. For depletion mode devices, the depletion layer from the Schottky gate should extend only to the heterojunction depletion layer. For enhancement mode devices, the thickness of the doped AlGaAs layer is smaller and the Schottky gate built-in potential barrier will completely

deplete the AlGaAs layer and the two-dimensional electron gas channel. A positive voltage applied to the gate of the enhancement mode device will turn on the device.

The density of the two-dimensional electron gas in a normal structure can be described using a charge control model. We may write

$$n_s = \frac{\epsilon_N}{q\,(d + \Delta d)}(V_g - V_{\text{off}}) \tag{13.68}$$

where $\epsilon_N$ is the permittivity of the N-AlGaAs, $d = d_d + d_i$ is the thickness of the doped-plus-undoped AlGaAs layer, and $\Delta d$ is a correction factor given by

$$\Delta d = \frac{\epsilon_N a}{q} \approx 80 \text{ Å} \tag{13.69}$$

The threshold voltage $V_{\text{off}}$ is given by

$$V_{\text{off}} = \phi_B - \frac{\Delta E_c}{q} - V_{p2} \tag{13.70}$$

where $\phi_B$ is the Schottky barrier height and $V_{p2}$ is

$$V_{p2} = \frac{qN_d d_d^2}{2\epsilon_N} \tag{13.71}$$

A negative gate bias will reduce the two-dimensional electron gas concentration. If a positive gate voltage is applied, the density of the two-dimensional electron gas will increase. Increasing the gate voltage will increase the two-dimensional electron gas density until the conduction band of the AlGaAs crosses the Fermi level of the electron gas. Figure 13.29 shows this effect. At this point the gate loses control over the electron gas since a parallel conduction path in the AlGaAs has been formed.

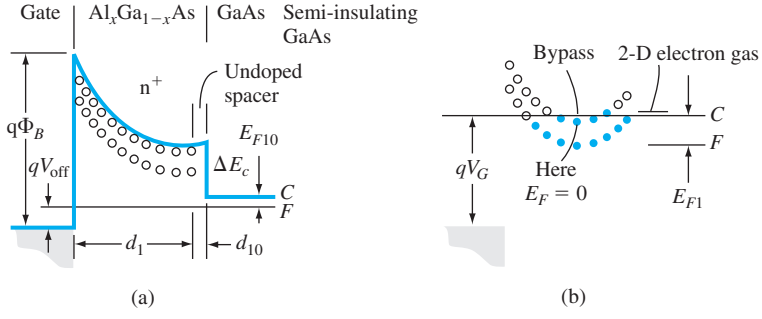


**Figure 13.29** | Energy-band diagram of an enhancement mode HEMT (a) with a slight forward gate voltage, and (b) with a larger forward gate voltage that creates a conduction channel in the AlGaAs. *(From Fritzsche [5].)*

**EXAMPLE 13.10**

Objective: Determine the two-dimensional electron concentration for an N–AlGaAs–intrinsic GaAs heterojunction.

Consider an N-$Al_{0.3}Ga_{0.7}As$ layer doped to $10^{18}$ cm$^{-3}$ and having a thickness of 500 Å. Assume an undoped spacer layer of 20 Å. Let $\phi_B = 0.85$ V and $\Delta E_c/q = 0.22$ V. The relative dielectric constant of $Al_{0.3}Ga_{0.7}As$ is $\epsilon_N = 12.2$.

### ■ Solution

The parameter $V_{p2}$ is found as

$$V_{p2} = \frac{qN_d d_d^2}{2\epsilon_N} = \frac{(1.6 \times 10^{-19})(10^{18})(500 \times 10^{-8})^2}{2(12.2)(8.85 \times 10^{-14})} = 1.85 \text{ V}$$

Then the threshold voltage is

$$V_{\text{off}} = \phi_B - \frac{\Delta E_c}{q} - V_{p2} = 0.85 - 0.22 - 1.85 = -1.22 \text{ V}$$

The channel electron concentration for $V_g = 0$ is found from Equation (13.68) to be

$$n_s = \frac{(12.2)(8.85 \times 10^{-14})}{(1.6 \times 10^{-19})(500 + 20 + 80) \times 10^{-8}}[-(-1.22)] = 1.37 \times 10^{12} \text{ cm}^{-2}$$

### ■ Comment

The threshold voltage $V_{\text{off}}$ is negative, making this device a depletion mode MODFET; applying a negative gate voltage will turn off the device. A value of $n_s \approx 10^{12}$ cm$^{-2}$ is a typical channel concentration.

The current–voltage characteristics of the MODFET can be found using the charge control model and the gradual channel approximation. The channel carrier concentration can be written as

$$n_s(x) = \frac{\epsilon_N}{q(d + \Delta d)}[V_g - V_{\text{off}} - V(x)] \tag{13.72}$$

where $V(x)$ is the potential along the channel due to the drain-to-source voltage. The drain current is

$$I_D = qn_s\, v(\text{E})W \tag{13.73}$$

where $v$(E) is the carrier drift velocity and $W$ is the channel width. This analysis is very similar to that for the pn JFET in Section 13.2.2.

If we assume a constant mobility, then for low $V_{DS}$ values, we have

$$I_D = \frac{\epsilon_N \mu W}{2L(d + \Delta d)}\left[2(V_g - V_{\text{off}})\, V_{DS} - V_{DS}^2\right] \tag{13.74}$$

The form of this equation is the same as that for the pn JFET or MESFET operating in the nonsaturation region. If $V_{DS}$ increases so that the carriers reach the saturation velocity, then

$$I_D(\text{sat}) = \frac{\epsilon_N W}{(d + \Delta d)}(V_g - V_{\text{off}} - V_0)v_{\text{sat}} \tag{13.75}$$

where $v_{\text{sat}}$ is the saturation velocity and $V_0 = \text{E}_s L$ with $\text{E}_s$ being the electric field in the channel that produces the saturation velocity.

Various velocity versus electric field models can be used to derive different *I–V* expressions. However, Equations (13.74) and (13.75) yield satisfactory results for most situations. Figure 13.30 shows a comparison between experimental and calculated *I–V* characteristics. As observed in the figure, the current in these heterojunction devices can be quite large. The transconductance of the MODFET is defined as it was for the pn JFET and MESFET. Typical measured values at $T = 300$ K are in the range of 250 mS/mm. Higher values have been reported. These transconductance values are significantly larger than for either the pn JFET or the MESFET.

HEMTs may also be fabricated with multiple heterojunction layers. This device type is shown in Figure 13.31. A single heterojunction for an AlGaAs–GaAs interface has a maximum two-dimensional electron sheet density on the order of $1 \times 10^{12}$ cm$^{-2}$. This concentration can be increased by fabricating two or more AlGaAs–GaAs interfaces in the same epitaxial layer. The device current capacity is increased, and power performance is improved. The multichannel HEMT behaves as multiple single-channel HEMTs connected in parallel and modulated by the same gate but with slightly different threshold voltages. The maximum transconductance will not scale directly with the number of channels because of the change in threshold voltage with each channel. In addition, the effective channel length increases as the distance between the gate and channel increases.

HEMTs can be used in high-speed logic circuits. They have been used in flip-flop circuits operating at clock frequencies of 5.5 GHz at $T = 300$ K; the clock frequency can be increased at lower temperatures. Small-signal, high-frequency amplifiers have also been investigated. HEMTs showing low noise and reasonable gains have been operated at 35 GHz. The maximum frequency increases as the channel length decreases. Cutoff frequencies on the order of 100 GHz have been measured with channel lengths of 0.25 $\mu$m.

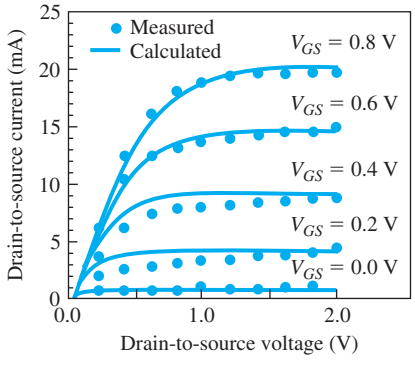


**Figure 13.30** | Current–voltage characteristics of an enhancement mode HEMT, in which solid curves are numerical calculations and dots are measured points.
*(From Shur [13].)*

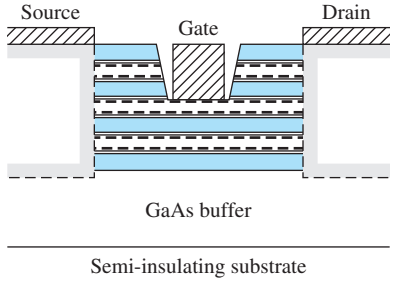


**Figure 13.31** | A multilayer HEMT.

It seems clear that HEMTs are inherently superior to other FET technologies in terms of achieving higher speeds of operation, lower power dissipation, and lower noise. These advantages derive directly from the superior transport properties obtained by using undoped GaAs as the channel layer for the FET. One way to achieve an adequate carrier concentration in an undoped channel is to accumulate the carriers at a semiconductor heterojunction interface, as we have seen. The disadvantage of the HEMT is that the fabrication processes for the heterojunction are more complicated.

## 13.6 | SUMMARY

- The physics, characteristics, and operation of the junction field-effect transistor are considered in this chapter.
- The current in a JFET is controlled by an electric field applied perpendicular to the direction of current. The current is in the channel region between the source and drain contacts. In a pn JFET, the channel forms one side of a pn junction that is used to modulate the channel conductance.
- Two primary parameters of the JFET are the internal pinchoff voltage $V_{p0}$ and the pinchoff voltage $V_p$. The internal pinchoff voltage is defined as a positive quantity and is the total gate-to-channel potential that causes the junction space charge layer to completely fill the channel region. The pinchoff voltage is defined as the gate voltage that must be applied to achieve the pinchoff condition.
- The ideal current–voltage relationship is derived. The transconductance, or transistor gain, is the rate of change of drain current with respect to the corresponding change in gate-to-source voltage.
- Three nonideal effects are considered; channel-length modulation, velocity saturation, and subthreshold current. Each of these effects changes the ideal current–voltage relationship.
- A small-signal equivalent circuit of the JFET is developed. The equivalent circuit includes capacitances that introduce frequency effects in the transistor. Two physical factors affect the frequency limitation; channel transit time and capacitance charging time. The capacitance charging time constant is normally the limiting factor in short channel devices.
- The high-electron mobility transistor (HEMT) structure utilizes a heterojunction. A two-dimensional electron gas is confined to a potential well at the heterojunction interface. However, the electrons are free to move parallel to the interface. These electrons are separated from the ionized donors so that ionized impurity scattering effects are minimized, resulting in a high mobility.

## GLOSSARY OF IMPORTANT TERMS

**capacitance charging time** The time associated with charging or discharging the input gate capacitance with a change in the input gate signal.

**channel conductance** The ratio of a differential change in drain current to the corresponding differential change in drain-to-source voltage in the limit as the drain-to-source voltage approaches zero.

**channel conductance modulation** The process whereby the channel conductance changes with gate voltage; this is the basic field-effect transistor action.

**channel length modulation** The change in effective channel length with drain-to-source voltage with the JFET biased in the saturation region.

**conduction parameter** The multiplying factor $k_n$ in the expression for drain current versus gate-to-source voltage for the enhancement mode MESFET.

**cutoff frequency** A figure of merit for the transistor defined to be the frequency at which the ratio of the small-signal input gate current to small-signal drain current is equal to unity.

**depletion mode JFET** A JFET in which a gate-to-source voltage must be applied to create pinchoff and turn the device off.

**enhancement mode JFET** A JFET in which pinchoff exists at zero gate voltage and a gate-to-source voltage must be applied to induce a channel, turning the device on.

**internal pinchoff voltage** The total potential drop across the gate junction at pinchoff.

**output resistance** The ratio of a differential change in drain-to-source voltage to the corresponding differential change in drain current at a constant gate-to-source voltage.

**pinchoff** The condition whereby the gate junction space charge region extends completely through the channel so that the channel is completely depleted of free carriers.

## CHECKPOINT

After studying this chapter, the reader should have the ability to:

- Describe the basic operation of the pn JFET and MESFET.
- Discuss how current is contained in the channel region of a GaAs MESFET with a semi-insulating substrate.
- Sketch the *I–V* characteristics of a depletion mode JFET.
- Discuss how the internal pinchoff voltage is defined and how the pinchoff voltage is defined.
- Define transconductance for a JFET.
- Discuss the concept of an enhancement mode MESFET.
- Discuss three nonideal effects in a JFET including channel-length modulation, velocity saturation effects, and subthreshold effects.
- Sketch the small-signal equivalent circuit of a JFET.
- Discuss the frequency limitation factors and define the cutoff frequency.
- Sketch the cross section of a simple HEMT.
- Describe the advantages of a HEMT compared to a MESFET.

## REVIEW QUESTIONS

1. Sketch the cross section of a p-channel pn JFET and indicate voltage polarities for device operation.
2. Sketch cross sections of a p-channel pn JFET showing the depletion regions when biased in the nonsaturation region and in the saturation region.
3. What is the mechanism of current saturation in a pn JFET?
4. Sketch the cross section of an n-channel GaAs MESFET.
5. What is the mechanism of current saturation in a MESFET?
6. Define internal pinchoff voltage and pinchoff voltage for a pn JFET.

7. Define threshold voltage for a MESFET.
8. Sketch the small-signal equivalent circuit of a JFET.
9. Define two frequency limitation factors for a JFET. Define the condition for cutoff frequency.
10. Sketch the cross section of an AlGaAs–GaAs HEMT. Sketch the conduction energy band across the heterojunction.
11. What is the principal advantage of a HEMT compared to a MESFET?

# PROBLEMS

(*Note:* Assume $T = 300$ K for the following problems unless otherwise stated.)

## Section 13.1 JFET Concepts

**13.1** (*a*) Draw the structure of a p-channel JFET similar to the structure shown in Figure 13.2. (*b*) Qualitatively discuss the *I–V* characteristics, including current directions and voltage polarities, similar to those shown in Figures 13.3 and 13.4.

**13.2** Consider the n-channel JFET in Figure P13.2. The p-type substrate is connected to the n-type source terminal. Sketch the space charge regions for various $V_{GS}$ values when $V_{DS} = 0$ and for various $V_{DS}$ values when $V_{GS} = 0$.

## Section 13.2 The Device Characteristics

**13.3** An n-channel GaAs pn JFET at $T = 300$ K has parameters $N_d = 3 \times 10^{16}$ cm$^{-3}$, $N_a = 2 \times 10^{18}$ cm$^{-3}$, and $a = 0.40$ $\mu$m. (*a*) Calculate the (*i*) internal pinchoff voltage $V_{po}$ and (*ii*) pinchoff voltage $V_p$. (*b*) Determine the minimum undepleted channel thickness, $a - h$, for $V_{GS} = -0.5$ V and for (*i*) $V_{DS} = 0$, (*ii*) $V_{DS} = 0.5$ V, and (*iii*) $V_{DS} = 2.5$ V. (*c*) Find $V_{DS}$(sat) for (*i*) $V_{GS} = 0$ and (*ii*) $V_{GS} = -1.0$ V.

**13.4** Repeat Problem 13.3 for an n-channel silicon pn JFET with the same geometrical and electrical parameters.

**13.5** Consider a p-channel GaAs pn JFET at $T = 300$ K. The parameters are $N_d = 10^{18}$ cm$^{-3}$ and $a = 0.65$ $\mu$m. (*a*) Determine the channel doping concentration such that the internal pinchoff voltage is $V_{po} = 2.75$ V. (*b*) Using the results of part (*a*), what is the pinchoff voltage $V_p$? (*c*) For $V_{SD} = 0$, determine the value of $V_{GS}$ such that the minimum undepleted channel thickness is 0.15 $\mu$m. (*d*) For $V_{GS} = 0$, find the value of $V_{SD}$ such that the channel is just pinched off at the drain terminal.

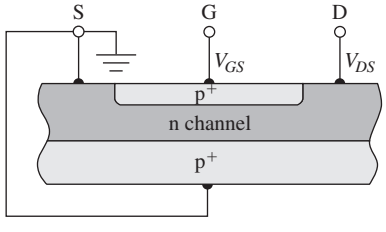


**Figure P13.2** | Figure for Problem 13.2.