CHAPTER 13

The Junction Field-Effect Transistor

The Junction Field-Effect Transistor (JFET) is a separate class of field-effect transistors. The MOSFET has been considered in Chapters 10 and 11. In this chapter, we cover the physics and properties of the JFET. Although we have discussed the MOS and bipolar transistors in previous chapters, the material in this chapter only presumes a knowledge of semiconductor material properties and the characteristics of pn and Schottky barrier junctions.

As with the transistors considered in previous chapters, the JFET, in conjunction with other circuit elements, is capable of voltage gain and signal power gain. Again, the basic transistor action is the control of current at one terminal by the voltage across the other two terminals of the device.

There are two general categories of JFETs. The first is the pn junction FET, or pn JFET, and the second is the **ME**tal-**S**emiconductor **F**ield-**E**ffect **T**ransistor, or MESFET. The pn JFET is fabricated with a pn junction and the MESFET is fabricated with a Schottky barrier rectifying junction. ■

13.0 | PREVIEW

In this chapter, we will:

- Present the geometry and discuss the basic operation of the pn JFET and MESFET devices.
- Analyze the modulation of the channel conductance of the JFET by an electric field perpendicular to the channel. The modulating electric field is induced in the space charge region of a reverse-biased pn junction or reverse-biased Schottky barrier junction.
- Derive the ideal current–voltage characteristics of the JFET in terms of the semiconductor material and geometrical properties of the device.

- Consider the transistor gain, or transconductance, of the JFET.
- Discuss a few nonideal effects in JFETs, including channel-length modulation and velocity saturation effects.
- Develop a small-signal equivalent circuit of the JFET that is used to relate small-signal currents and voltages in the device.
- Examine various physical factors affecting the frequency response and limitations of JFETs, and derive an expression for the cutoff frequency.
- Present the geometry and characteristics of a specialized JFET called HEMT.

13.1 | JFET CONCEPTS

The concept of the field-effect phenomenon was the basis for the first proposed solid-state transistor. Patents filed in the 1920s and 1930s conceived and investigated the transistor shown in Figure 13.1. A voltage applied to the metal plate modulated the conductance of the semiconductor under the metal and controlled the current between the ohmic contacts. Good semiconductor materials and processing technology were not available at that time, so the device was not seriously considered again until the 1950s.

The phenomenon of modulating the conductance of a semiconductor by an electric field applied perpendicular to the surface of a semiconductor is called field effect. This type of transistor has also been called the unipolar transistor, to emphasize that only one type of carrier, the majority carrier, is involved in the operation. We will qualitatively discuss the basic operation of the two types of JFETs in this section, and introduce some of the JFET terminology.

13.1.1 Basic pn JFET Operation

The first type of field-effect transistor is the pn junction field-effect transistor, or pn JFET. A simplified cross section of a symmetrical device is shown in Figure 13.2. The n region between the two p regions is known as the channel and, in this n-channel

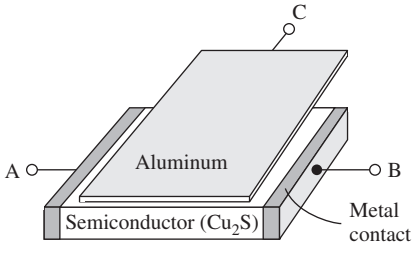

Figure 13.1 | Idealization of the Lilienfeld transistor.
(From Pierret [10].)

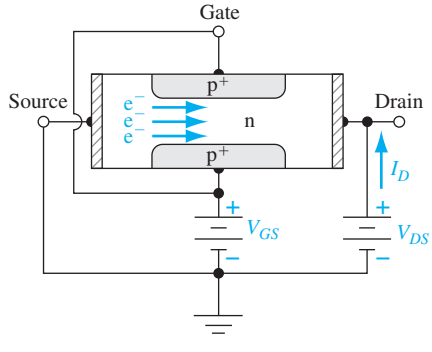

Figure 13.2 | Cross section of a symmetrical n-channel pn junction FET.

device, majority carrier electrons flow between the source and drain terminals. The source is the terminal from which carriers enter the channel from the external circuit, the drain is the terminal where carriers leave, or are drained from, the device, and the gate is the control terminal. The two gate terminals shown in Figure 13.2 are tied together to form a single gate connection. Since majority carrier electrons are primarily involved in the conduction in this n-channel transistor, the JFET is a majority-carrier device.

A complementary p-channel JFET can also be fabricated in which the p and n regions are reversed from those of the n-channel device. Holes will flow in the p-type channel between source and drain and the source terminal will now be the source of the holes. The current direction and voltage polarities in the p-channel JFET are the reverse of those in the n-channel device. The p-channel JFET is generally a lower frequency device than the n-channel JFET due to the lower hole mobility.

Figure 13.3a shows an n-channel pn JFET with zero volts applied to the gate. If the source is at ground potential, and if a small positive drain voltage is applied, a drain current I_D is produced between the source and drain terminals. The n channel is essentially a resistance so the I_D versus V_{DS} characteristic, for small V_{DS} values, is approximately linear, as shown in the figure.

When we apply a voltage to the gate of a pn JFET with respect to the source and drain, we alter the channel conductance. If a negative voltage is applied to the gate of the n-channel pn JFET shown in Figure 13.3, the gate-to-channel pn junction becomes reverse biased. The space charge region now widens so the channel region becomes narrower and the resistance of the n channel increases. The slope of the I_D versus V_{DS} curve, for small V_{DS}, decreases. These effects are shown in Figure 13.3b. If a larger negative gate voltage is applied, the condition shown in Figure 13.3c can be achieved. The reverse-biased gate-to-channel space charge region has completely filled the channel region. This condition is known as *pinchoff*. The drain current at pinchoff is essentially zero, since the depletion region isolates the source and drain terminals. Figure 13.3c shows the I_D versus V_{DS} curve for this case, as well as the other two cases.

The current in the channel is controlled by the gate voltage. The control of the current in one part of the device by a voltage in another part of the device is the basic transistor action. This device is a normally on or *depletion mode* device, which means that a voltage must be applied to the gate terminal to turn the device off.

Now consider the situation in which the gate voltage is held at zero volts, $V_{GS} = 0$, and the drain voltage changes. Figure 13.4a is a replica of Figure 13.3a for zero gate voltage and a small drain voltage. As the drain voltage increases (positive), the gate-to-channel pn junction becomes reverse biased near the drain terminal so that the space charge region extends further into the channel. The channel is essentially a resistor, and the effective channel resistance increases as the space charge region widens; therefore, the slope of the I_D versus V_{DS} characteristic decreases as shown in Figure 13.4b. The effective channel resistance now varies along the channel length and, since the channel current must be constant, the voltage drop through the channel becomes dependent on position.

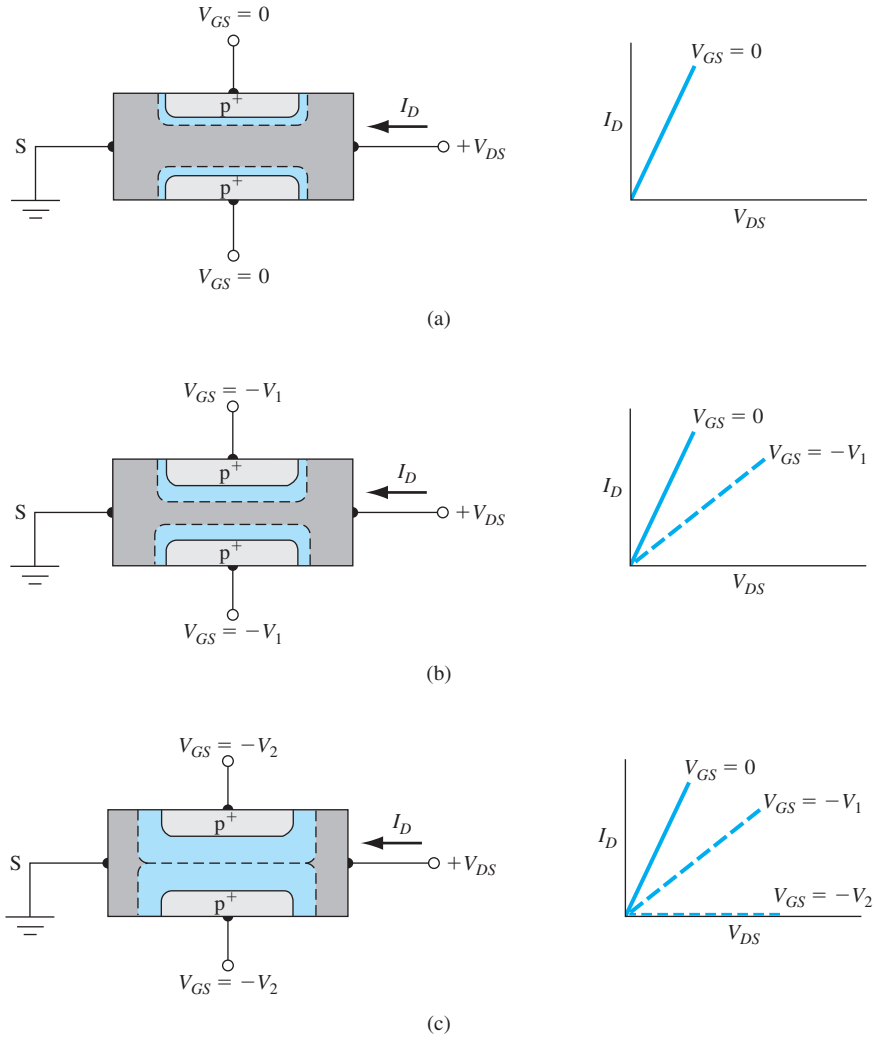

Figure 13.3 | Gate-to-channel space charge regions and *I–V* characteristics for small V_{DS} values and for (a) zero gate voltage, (b) small reverse-biased gate voltage, and (c) a gate voltage to achieve pinchoff.

If the drain voltage increases further, the condition shown in Figure 13.4c can result. The channel has been pinched off at the drain terminal. Any further increase in drain voltage will not cause an increase in drain current. The *I–V* characteristic for this condition is also shown in this figure. The drain voltage at pinchoff is referred to as $V_{DS}(\text{sat})$. For $V_{DS} > V_{DS}(\text{sat})$, the transistor is said to be in the saturation region and the drain current, for this ideal case, is independent of V_{DS}. At first glance, we might expect the drain current to go to zero when the channel becomes pinched off at the drain terminal, but we will show why this does not happen.

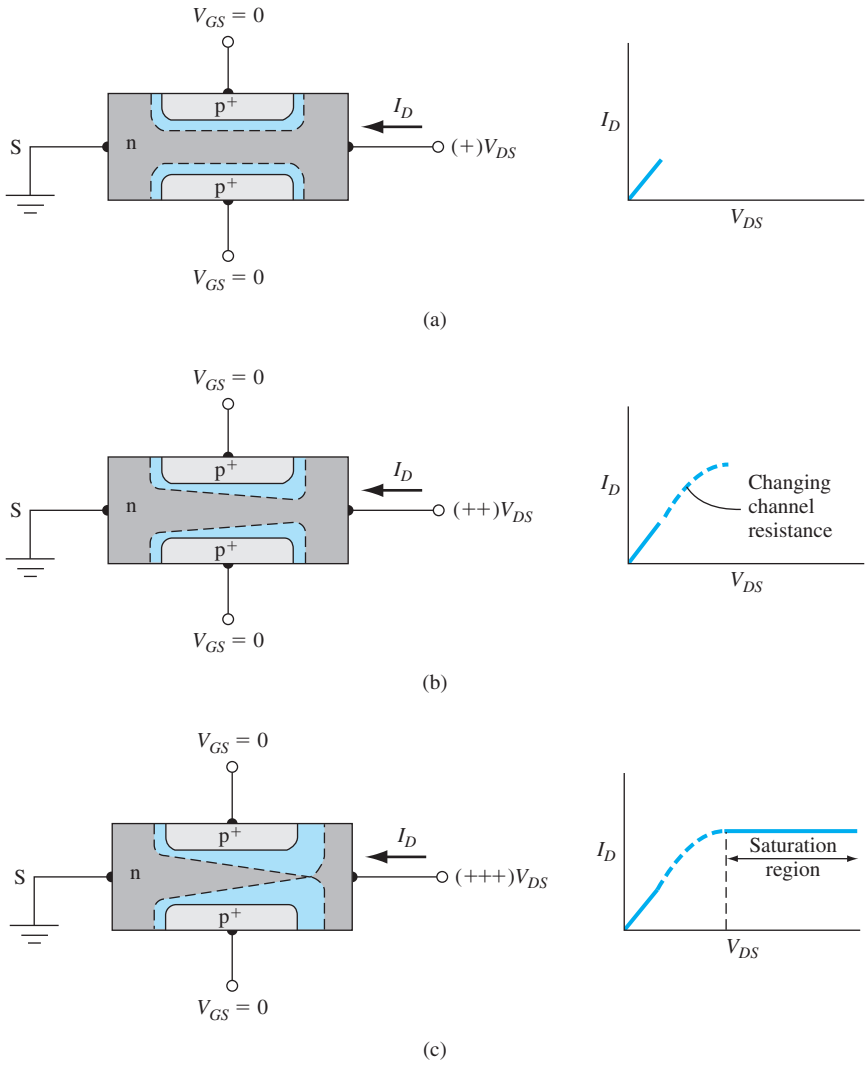

Figure 13.4 | Gate-to-channel space charge regions and *I–V* characteristics for zero gate voltage and for (a) a small drain voltage, (b) a larger drain voltage, and (c) a drain voltage to achieve pinchoff at the drain terminal.

Figure 13.5 shows an expanded view of the pinchoff region in the channel. The n channel and drain terminal are now separated by a space charge region which has a length ΔL. The electrons move through the n channel from the source and are injected into the space charge region where, subjected to the E-field force, they are swept through into the drain contact area. If we assume that $\Delta L \ll L$, then the electric field in the n-channel region remains unchanged from the V_{DS}(sat) case; the drain current will remain constant as V_{DS} changes. Once the carriers are in the drain region,

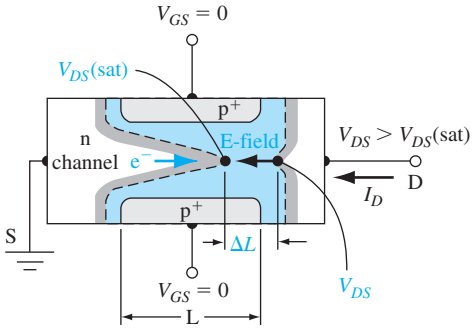

Figure 13.5 | Expanded view of the space charge region in the channel for $V_{DS} > V_{DS}$(sat).

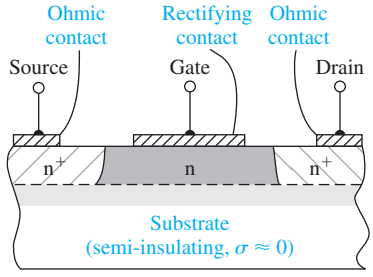

Figure 13.6 | Cross section of an n-channel MESFET with a semi-insulating substrate.

the drain current will be independent of V_{DS}; thus, the device looks like a constant current source.

13.1.2 Basic MESFET Operation

The second type of junction field-effect transistor is the MESFET. The gate junction in the pn junction FET is replaced by a Schottky barrier rectifying contact. Although MESFETs can be fabricated in silicon, they are usually associated with gallium arsenide or other compound semiconductor materials. A simplified cross section of a GaAs MESFET is shown in Figure 13.6. A thin epitaxial layer of GaAs is used for the active region; the substrate is a very high resistivity GaAs material referred to as a semi-insulating substrate. GaAs is intentionally doped with chromium, which behaves as a single acceptor close to the center of the energy bandgap, to make it semi-insulating with a resistivity as high as 10^9 Ω-cm. The advantages of these devices include higher electron mobility, hence smaller transit time and faster response; and decreased parasitic capacitance and a simplified fabrication process, resulting from the semi-insulating GaAs substrate.

In the MESFET shown in Figure 13.6, a reverse-biased gate-to-source voltage induces a space charge region under the metal gate that modulates the channel conductance as in the case of the pn JFET. The space charge region will eventually reach the substrate if the applied negative gate voltage is sufficiently large. This condition, again, is known as pinchoff. The device shown in this figure is also a depletion mode device, since a gate voltage must be applied to pinch off the channel.

If we treat the semi-insulating substrate as an intrinsic material, then the energy-band diagram of the substrate–channel–metal structure is as shown in Figure 13.7 for the case of zero bias applied to the gate. Because there is a potential barrier between the channel and substrate and between the channel and metal, the majority carrier electrons are confined to the channel region.

Consider, now, another type of MESFET in which the channel is pinched off even at $V_{GS} = 0$. Figure 13.8a shows this condition, in which the channel thickness is smaller than the zero-biased space charge width. To open a channel, the depletion region must be reduced: A forward-bias voltage must be applied to the gate–semiconductor

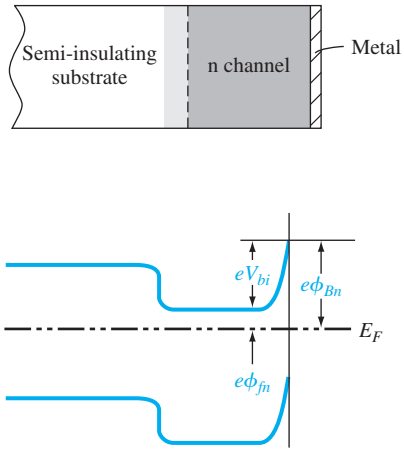

Figure 13.7 | Idealized energy-band diagram of the substrate–channel–metal in the n-channel MESFET.

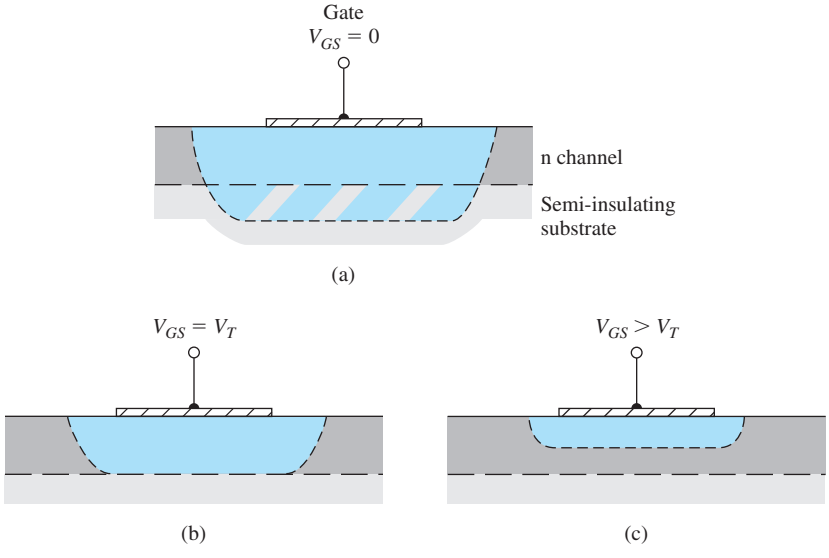

Figure 13.8 | Channel space charge region of an enhancement mode MESFET for (a) $V_{GS} = 0$, (b) $V_{GS} = V_T$, and (c) $V_{GS} > V_T$.

junction. When a slightly forward-bias voltage is applied, the depletion region just extends through the channel—a condition known as *threshold,* shown in Figure 13.8b. The threshold voltage is the gate-to-source voltage that must be applied to create the pinchoff condition. The threshold voltage for this n-channel MESFET is positive, in contrast to the negative voltage for the n-channel depletion mode device. If a larger forward bias is applied, the channel region opens as shown in Figure 13.8c. The

applied forward-bias gate voltage is limited to a few tenths of a volt before there is significant gate current. This device is known as an n-channel enhancement mode MESFET. Enhancement mode p-channel MESFETs and enhancement mode pn junction FETs have also been fabricated. The advantage of enhancement mode MESFETs is that circuits can be designed in which the voltage polarity on the gate and drain is the same. However, the output voltage swing will be quite small with these devices.

13.2 | THE DEVICE CHARACTERISTICS

To describe the basic electrical characteristics of the JFET, we initially consider a uniformly doped depletion mode pn JFET and then later discuss the enhancement mode device. The pinchoff voltage and drain-to-source saturation voltage are defined and expressions for these parameters derived in terms of geometry and electrical properties. The ideal current–voltage relationship is developed, and then the transconductance, or transistor gain is determined.

Figure 13.9a shows a symmetrical, two-sided pn JFET and Figure 13.9b shows a MESFET with the semi-insulating substrate. One can derive the ideal DC current–voltage relationship for both devices by simply considering the two-sided device to be two JFETs in parallel. We derive the *I–V* characteristics in terms of I_{D1} so that the drain current in the two-sided device becomes $I_{D2} = 2I_{D1}$. We ignore any depletion region at the substrate of the one-sided device in the ideal case.

13.2.1 Internal Pinchoff Voltage, Pinchoff Voltage, and Drain-to-Source Saturation Voltage

n-channel pn JFET Figure 13.10a shows a simplified one-sided n-channel pn JFET. The metallurgical channel thickness between the p^+ gate region and the substrate is a, and the induced depletion region width for the one-sided p^+n junction is h. Assume the drain-to-source voltage is zero. If we assume the abrupt depletion approximation, then the space charge width is given by

$$h = \left[\frac{2\epsilon_s(V_{bi} - V_{GS})}{eN_d}\right]^{1/2} \tag{13.1}$$

where V_{GS} is the gate-to-source voltage and V_{bi} is the built-in potential barrier. For a reverse-biased p^+n junction, V_{GS} must be a negative voltage.

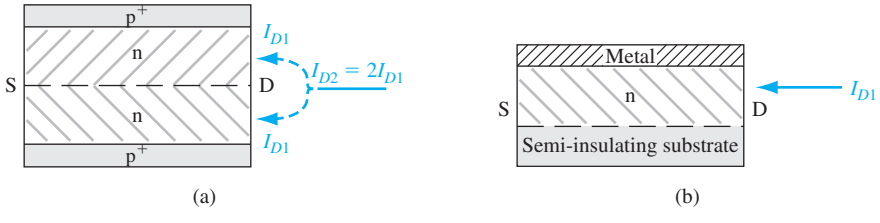

Figure 13.9 | Drain currents of (a) a symmetrical, two-sided pn JFET, and (b) a one-sided MESFET.

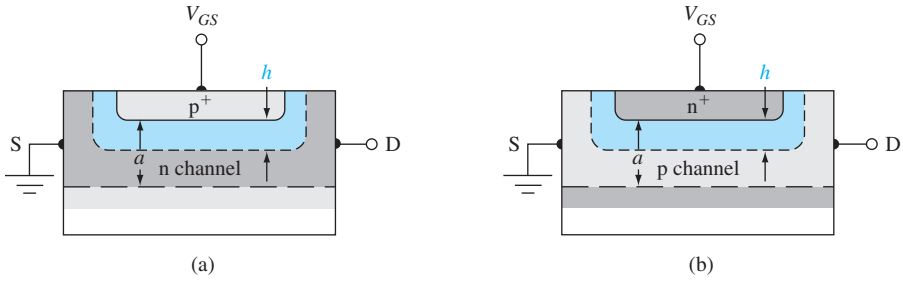

Figure 13.10 | Geometries of simplified (a) n-channel and (b) p-channel pn JFETs.

At pinchoff, $h = a$ and the total potential across the p^+n junction is called the *internal pinchoff voltage,* denoted by V_{p0}. We now have

$$a = \left[\frac{2\epsilon_s V_{p0}}{eN_d}\right]^{1/2} \tag{13.2}$$

or

$$\boxed{V_{p0} = \frac{ea^2 N_d}{2\epsilon_s}} \tag{13.3}$$

Note that the internal pinchoff voltage is defined as a positive quantity.

The internal pinchoff voltage V_{p0} is not the gate-to-source voltage to achieve pinchoff. The gate-to-source voltage that must be applied to achieve pinchoff is described as the *pinchoff voltage* and is also variously called the *turn-off voltage* or *threshold voltage*. The pinchoff voltage is denoted by V_p and is defined from Equations (13.1) and (13.2) as

$$V_{bi} - V_p = V_{p0} \qquad \text{or} \qquad \boxed{V_p = V_{bi} - V_{p0}} \tag{13.4}$$

The gate-to-source voltage to achieve pinchoff in an n-channel depletion mode JFET is negative; thus, $V_{p0} > V_{bi}$.

EXAMPLE 13.1

Objective: Calculate the internal pinchoff voltage and pinchoff voltage of an n-channel JFET.

Assume that the p^+n junction of a uniformly doped silicon n-channel JFET at $T = 300$ K has doping concentrations of $N_a = 10^{18}$ cm^{-3} and $N_d = 10^{16}$ cm^{-3}. Assume that the metallurgical channel thickness, a, is 0.75 μm $= 0.75 \times 10^{-4}$ cm.

■ Solution

The internal pinchoff voltage is given by Equation (13.3), so we have

$$V_{p0} = \frac{ea^2 N_d}{2\epsilon_s} = \frac{(1.6 \times 10^{-19})(0.75 \times 10^{-4})^2(10^{16})}{2(11.7)(8.85 \times 10^{-14})} = 4.35 \text{ V}$$

The built-in potential barrier is

$$V_{bi} = V_t \ln\left(\frac{N_a N_d}{n_i^2}\right) = (0.0259)\ln\left[\frac{(10^{18})(10^{16})}{(1.5\times 10^{10})^2}\right] = 0.814 \text{ V}$$

The pinchoff voltage, from Equation (13.4), is then found as

$$V_p = V_{bi} - V_{p0} = 0.814 - 4.35 = -3.54 \text{ V}$$

■ Comment

The pinchoff voltage, or gate-to-source voltage to achieve pinchoff, for the n-channel depletion mode device is a negative quantity as we have said.

■ EXERCISE PROBLEM

Ex 13.1 A silicon n-channel JFET at $T = 300$ K has a gate doping concentration of $N_a = 10^{18}$ cm^{-3} and a channel doping concentration of $N_d = 2 \times 10^{16}$ cm^{-3}. Determine the metallurgical channel thickness, a, such that the pinchoff voltage is $V_p = -2.50$ V.

(Ans. $a = 0.464\ \mu$m)

The pinchoff voltage is the gate-to-source voltage that must be applied to turn the JFET off and so must be within the voltage range of the circuit design. The magnitude of the pinchoff voltage must also be less than the breakdown voltage of the junction.

p-channel pn JFET Figure 13.10b shows a p-channel JFET with the same basic geometry as the n-channel JFET we considered. The induced depletion region for the one-sided n^+p junction is again denoted by h and is given by

$$h = \left[\frac{2\epsilon_s(V_{bi} + V_{GS})}{eN_a}\right]^{1/2} \tag{13.5}$$

For a reverse-biased n^+p junction, V_{GS} must be positive. The internal pinchoff voltage is again defined to be the total pn junction voltage to achieve pinchoff, so that when $h = a$ we have

$$a = \left[\frac{2\epsilon_s V_{p0}}{eN_a}\right]^{1/2} \tag{13.6}$$

or

$$\boxed{V_{p0} = \frac{ea^2 N_q}{2\epsilon_s}} \tag{13.7}$$

The internal pinchoff voltage for the p-channel device is also defined to be a positive quantity.

The pinchoff voltage is again defined as the gate-to-source voltage to achieve the pinchoff condition. For the p-channel depletion mode device, we have, from Equation (13.5), at pinchoff

$$V_{bi} + V_p = V_{p0} \qquad \text{or} \qquad \boxed{V_p = V_{p0} - V_{bi}} \tag{13.8}$$

The pinchoff voltage for a p-channel depletion mode JFET is a positive quantity.

DESIGN EXAMPLE 13.2

Objective: Design the channel doping concentration and metallurgical channel thickness to achieve a given pinchoff voltage.

Consider a silicon p-channel pn JFET at $T = 300$ K. Assume that the gate doping concentration is $N_d = 10^{18}$ cm^{-3}. Determine the channel doping concentration and channel thickness so that the pinchoff voltage is $V_p = 2.25$ V.

■ Solution

There is not a unique solution to this design problem. We will pick a channel doping concentration of $N_a = 2 \times 10^{16}$ cm^{-3} and determine the channel thickness. The built-in potential barrier is

$$V_{bi} = V_t \ln\left(\frac{N_a N_d}{n_i^2}\right) = (0.0259) \ln\left[\frac{(2 \times 10^{16})(10^{18})}{(1.5 \times 10^{10})^2}\right] = 0.832 \text{ V}$$

From Equation (13.8), the internal pinchoff voltage must be

$$V_{p0} = V_{bi} + V_p = 0.832 + 2.25 = 3.08 \text{ V}$$

and from Equation (13.6), the channel thickness can be determined as

$$a = \left[\frac{2\epsilon_s V_{p0}}{eN_a}\right]^{1/2} = \left[\frac{2(11.7)(8.85 \times 10^{-14})(3.08)}{(1.6 \times 10^{-19})(2 \times 10^{16})}\right]^{1/2} = 0.446 \ \mu\text{m}$$

■ Comment

If the channel doping concentration chosen were larger, the required channel thickness would decrease; a very small value of channel thickness would be difficult to fabricate within reasonable tolerance limits.

■ EXERCISE PROBLEM

Ex 13.2 The n$^+$p junction of a uniformly doped silicon p-channel JFET at $T = 300$ K has doping concentrations of $N_d = 10^{18}$ cm^{-3} and $N_a = 10^{16}$ cm^{-3}. The metallurgical channel thickness is $a = 0.40$ μm. Determine the internal pinchoff voltage and the pinchoff voltage of the JFET.

(Ans. $V_{od} = 1.236$ V, $V_p = 0.422$ V)

Also, we will see later that if the channel doping concentration were smaller the current capability of the device would decrease. There are definite tradeoffs to be considered in any design problem.

We have determined the pinchoff voltage for both n-channel and p-channel JFETs when the drain-to-source voltage is zero. Now consider the case when both gate and drain voltages are applied. The depletion region width will vary with distance through the channel. Figure 13.11 shows the simplified geometry for an n-channel device. The depletion width h_1 at the source end is a function of V_{bi} and V_{GS} but is not a function of drain voltage. The depletion width at the drain terminal is given by

$$h_2 = \left[\frac{2\epsilon_s(V_{bi} + V_{DS} - V_{GS})}{eN_d}\right]^{1/2} \tag{13.9}$$

Again, we must keep in mind that V_{GS} is a negative quantity for the n-channel device.

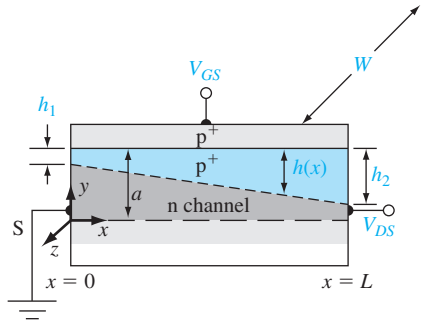

Figure 13.11 | Simplified geometry of an n-channel pn JFET.

Pinchoff at the drain terminal occurs when $h_2 = a$. At this point we reach what is known as the saturation condition; thus, we can write that $V_{DS} = V_{DS}(\text{sat})$. Then

$$a = \left[\frac{2\epsilon_s(V_{bi} + V_{DS}(\text{sat}) - V_{GS})}{eN_d}\right]^{1/2} \tag{13.10}$$

This can be rewritten as

$$V_{bi} + V_{DS}(\text{sat}) - V_{GS} = \frac{ea^2N_d}{2\epsilon_s} = V_{p0} \tag{13.11}$$

or

$$\boxed{V_{DS}(\text{sat}) = V_{p0} - (V_{bi} - V_{GS})} \tag{13.12}$$

Equation (13.12) gives the drain-to-source voltage to cause pinchoff at the drain terminal. The drain-to-source saturation voltage decreases with increasing reverse-biased gate-to-source voltage. We may note that Equation (13.12) has no meaning if $|V_{GS}| > |V_p|$.

In a p-channel JFET, the voltage polarities are the reverse of those in the n-channel device. We can show that, in the p-channel JFET at saturation,

$$\boxed{V_{SD}(\text{sat}) = V_{p0} - (V_{bi} + V_{GS})} \tag{13.13}$$

where now the source is positive with respect to the drain.

13.2.2 Ideal DC Current–Voltage Relationship—Depletion Mode JFET

The derivation of the ideal current–voltage relation of the JFET is somewhat tedious, and the resulting equations are cumbersome in hand calculations. Before we go through this derivation, consider the following expression, which is a good approximation

to the *I–V* characteristics when the JFET is biased in the saturation region. This equation is used extensively in JFET applications and is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{13.14}$$

where I_{DSS} is the saturation current when $V_{GS} = 0$. At the end of this section, we compare the approximation given by Equation (13.14) and the ideal current–voltage equation that we have derived.

***I–V* Derivation** The ideal current–voltage relationship of the JFET is derived by starting with Ohm's law. Consider an n-channel JFET with the geometry shown in Figure 13.11. We are considering half of the two-sided symmetrical geometry. The differential resistance of the channel at a point x in the channel is

$$dR = \frac{\rho dx}{A(x)} \tag{13.15}$$

where ρ is the resistivity and $A(x)$ is the cross-sectional area. If we neglect the minority carrier holes in the n channel, the channel resistivity is

$$\rho = \frac{1}{e\mu_n N_d} \tag{13.16}$$

The cross-sectional area is given by

$$A(x) = [a - h(x)]\,W \tag{13.17}$$

where W is the channel width. Equation (13.15) can now be written as

$$dR = \frac{dx}{e\mu_n N_d[a - h(x)]\,W} \tag{13.18}$$

The differential voltage across a differential length dx can be written as

$$dV(x) = I_{D1}\,dR(x) \tag{13.19}$$

where the drain current I_{D1} is constant through the channel. Substituting Equation (13.18) into Equation (13.19), we have

$$dV(x) = \frac{I_{D1}\,dx}{e\mu_n N_d W[a - h(x)]} \tag{13.20a}$$

or

$$I_{D1}\,dx = e\mu_n N_d\,W[a - h(x)]\,dV(x) \tag{13.20b}$$

The depletion width $h(x)$ is given by

$$h(x) = \left\{\frac{2\epsilon_s[V(x) + V_{bi} - V_{GS}]}{eN_d}\right\}^{1/2} \tag{13.21}$$

where $V(x)$ is the potential in the channel due to the drain-to-source voltage. Solving for $V(x)$ in Equation (13.21) and taking the differential, we have

$$dV(x) = \frac{eN_d h(x)\,dh(x)}{\epsilon_s} \tag{13.22}$$

Then Equation (13.20b) becomes

$$I_{D1}\,dx = \frac{\mu_n (eN_d)^2 W}{\epsilon_s}\,[ah(x)\,dh(x) - h(x)^2\,dh(x)] \tag{13.23}$$

The drain current I_{D1} is found by integrating Equation (13.23) along the channel length. Assuming the current and mobility are constant through the channel, we obtain

$$I_{D1} = \frac{\mu_n (eN_d)^2 W}{\epsilon_s L}\left[\int_{h_1}^{h_2} ah\,dh - \int_{h_1}^{h_2} h^2\,dh\right] \tag{13.24}$$

or

$$I_{D1} = \frac{\mu_n (eN_d)^2 W}{\epsilon_s L}\left[\frac{a}{2}(h_2^2 - h_1^2) - \frac{1}{3}(h_2^3 - h_1^3)\right] \tag{13.25}$$

Noting that

$$h_2^2 = \frac{2\epsilon_s (V_{DS} + V_{bi} - V_{GS})}{eN_d} \tag{13.26a}$$

$$h_1^2 = \frac{2\epsilon_s (V_{bi} - V_{GS})}{eN_d} \tag{13.26b}$$

and

$$V_{p0} = \frac{ea^2 N_d}{2\epsilon_s} \tag{13.26c}$$

Equation (13.25) can be written as

$$I_{D1} = \frac{\mu_n (eN_d)^2 W a^3}{2\epsilon_s L}\left[\frac{V_{DS}}{V_{p0}} - \frac{2}{3}\left(\frac{V_{DS} + V_{bi} - V_{GS}}{V_{p0}}\right)^{3/2} + \frac{2}{3}\left(\frac{V_{bi} - V_{GS}}{V_{p0}}\right)^{3/2}\right] \tag{13.27}$$

We may define

$$\boxed{I_{P1} \equiv \frac{\mu_n (eN_d)^2 W a^3}{6\epsilon_s L}} \tag{13.28}$$

where I_{P1} is called the pinchoff current. Equation (13.27) becomes

$$\boxed{I_{D1} = I_{P1}\left[3\left(\frac{V_{DS}}{V_{p0}}\right) - 2\left(\frac{V_{DS} + V_{bi} - V_{GS}}{V_{p0}}\right)^{3/2} + 2\left(\frac{V_{bi} - V_{GS}}{V_{p0}}\right)^{3/2}\right]} \tag{13.29}$$

Equation (13.29) is valid for $0 \le |V_{GS}| \le |V_p|$ and $0 \le V_{DS} \le V_{DS}(\text{sat})$. The pinchoff current I_{P1} would be the maximum drain current in the JFET if the zero-biased depletion regions could be ignored or if V_{GS} and V_{bi} were both zero.

Equation (13.29) is the current–voltage relationship for the one-sided n-channel JFET in the nonsaturation region. For the two-sided symmetrical JFET shown in Figure 13.9a, the total drain current would be $I_{D2} = 2I_{D1}$.

Equation (13.27) can also be written as

$$I_{D1} = G_{01}\left\{V_{DS} - \frac{2}{3}\sqrt{\frac{1}{V_{p0}}}\left[(V_{DS} + V_{bi} - V_{GS})^{3/2} - (V_{bi} - V_{GS})^{3/2}\right]\right\} \tag{13.30}$$

where

$$G_{01} = \frac{\mu_n (eN_d)^2\, Wa^3}{2\epsilon_s L V_{p0}} = \frac{e\mu_n N_d Wa}{L} = \frac{3I_{P1}}{V_{p0}} \tag{13.31}$$

The channel conductance is defined as

$$g_d = \left.\frac{\partial I_{D1}}{\partial V_{DS}}\right|_{V_{DS}\to 0} \tag{13.32}$$

Taking the derivative of Equation (13.30) with respect to V_{DS}, we obtain

$$g_d = \left.\frac{\partial I_{D1}}{\partial V_{DS}}\right|_{V_{DS}\to 0} = G_{01}\left[1 - \left(\frac{V_{bi} - V_{GS}}{V_{p0}}\right)^{1/2}\right] \tag{13.33}$$

We may note from Equation (13.33) that G_{01} would be the conductance of the channel if both V_{bi} and V_{GS} were zero. This condition would exist if no space charge regions existed in the channel. We may also note, from Equation (13.33), that the channel conductance is modulated or controlled by the gate voltage. This channel conductance modulation is the basis of the field-effect phenomenon.

We have shown that the drain becomes pinched off, for the n-channel JFET, when

$$V_{DS} = V_{DS}(\text{sat}) = V_{p0} - (V_{bi} - V_{GS}) \tag{13.34}$$

In the saturation region, the saturation drain current is determined by setting $V_{DS} = V_{DS}(\text{sat})$ in Equation (13.29) so that

$$\boxed{I_{D1} = I_{D1}(\text{sat}) = I_{P1}\left\{1 - 3\left(\frac{V_{bi} - V_{GS}}{V_{p0}}\right)\left[1 - \frac{2}{3}\sqrt{\frac{V_{bi} - V_{GS}}{V_{p0}}}\right]\right\}} \tag{13.35}$$

The ideal saturation drain current is independent of the drain-to-source voltage. Figure 13.12 shows the ideal current–voltage characteristics of a silicon n-channel JFET.

EXAMPLE 13.3

Objective: Calculate the maximum current in an n-channel JFET.

Consider a silicon n-channel JFET at $T = 300$ K with the following parameters: $N_a = 10^{18}$ cm^{-3}, $N_d = 10^{16}$ cm^{-3}, $a = 0.75$ μm, $L = 10$ μm, $W = 30$ μm, and $\mu_n = 1000$ cm^2/V-s.

■ Solution

The pinchoff current from Equation (13.28) becomes

$$I_{P1} = \frac{(1000)[(1.6 \times 10^{-19})(10^{16})]^2\,(30 \times 10^{-4})(0.75 \times 10^{-4})^3}{6(11.7)(8.85 \times 10^{-14})(10 \times 10^{-4})} = 0.522 \text{ mA}$$

We also have from Example 13.1 that $V_{bi} = 0.814$ V and $V_{p0} = 4.35$ V. The maximum current occurs when $V_{GS} = 0$, so from Equation (13.35)

$$I_{D1}(\text{max}) = I_{P1}\left\{1 - 3\left(\frac{V_{bi}}{V_{p0}}\right)\left[1 - \frac{2}{3}\sqrt{\frac{V_{bi}}{V_{p0}}}\right]\right\} \tag{13.36}$$

or

$$I_{D1}(\text{max}) = (0.522)\left\{1 - 3\left(\frac{0.814}{4.35}\right)\left[1 - \frac{2}{3}\sqrt{\frac{0.814}{4.35}}\right]\right\} = 0.313 \text{ mA}$$

Comment

The maximum current through the JFET is less than the pinchoff current I_{P1}.

EXERCISE PROBLEM

Ex 13.3 Consider an n-channel silicon pn JFET with parameters $N_a = 10^{18}$ cm^{-3}, $N_d = 10^{16}$ cm^{-3}, $a = 0.40$ μm, $L = 5$ μm, $W = 50$ μm, and $\mu_n = 900$ cm^2/V-s. Calculate the pinchoff current I_{P1} and the maximum drain current I_{D1}(sat) for $V_{GS} = 0$.

[Ans. $I_{P1} = 0.237$ mA, I_{D1}(sat) $= 22.13$ μA]

The maximum saturation current calculated in this example is considerably less than that shown in Figure 13.12 because of the big difference in the width-to-length ratios. Once the pinchoff voltage of JFET has been designed, the channel width W is the primary design variable for determining the current capability of a device.

Summary Equations (13.29) and (13.35) are rather cumbersome to use in any hand calculations. We may show that, in the saturation region, the drain current is given to a good approximation by Equation (13.14), stated at the beginning of this section as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

The current I_{DSS} is the maximum drain current and is the same as I_{D1}(max) in Equation (13.36). The parameter V_{GS} is the gate-to-source voltage and V_p is the pinchoff

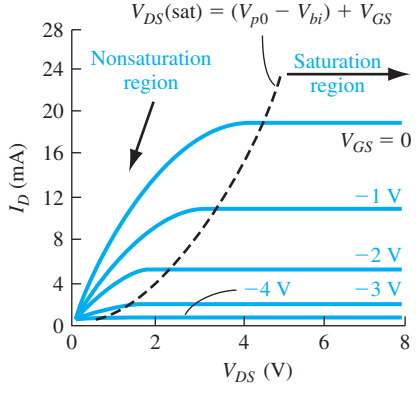

Figure 13.12 | Ideal current–voltage characteristics of a silicon n-channel JFET with $a = 1.5$ μm, $W/L = 170$, and $N_d = 2.5 \times 10^{15}$ cm^{-3}.
(From Yang [22].)

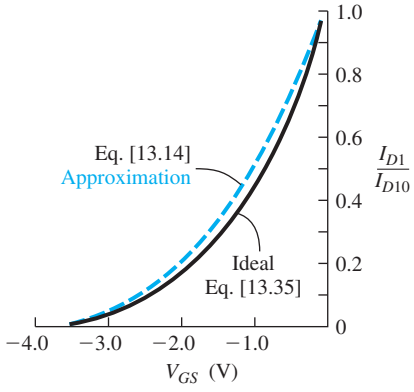

Figure 13.13 | Comparison of Equations (13.14) and (13.35) for the I_D versus V_{GS} characteristics of a JFET biased in the saturation region.

voltage. We may note that, for n-channel depletion mode JFET, both V_{GS} and V_p are negative and, for the p-channel depletion mode device, both are positive. Figure 13.13 shows the comparison between Equations (13.14) and (13.35).

13.2.3 Transconductance

The transconductance is the transistor gain of the JFET; it indicates the amount of control the gate voltage has on the drain current. The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{13.37}$$

Using the expressions for the ideal drain current derived in the last section, we can write the expressions for the transconductance.

The drain current for an n-channel depletion mode device in the nonsaturation region is given by Equation (13.29). We can then determine the transconductance of the transistor in the same region as

$$g_{mL} = \frac{\partial I_{D1}}{\partial V_{GS}} = \frac{3I_{P1}}{V_{p0}}\sqrt{\frac{V_{bi} - V_{GS}}{V_{p0}}}\left[\sqrt{\left(\frac{V_{DS}}{V_{bi} - V_{GS}}\right) + 1} - 1\right] \tag{13.38}$$

Taking the limit as V_{DS} becomes small, the transconductance becomes

$$g_{mL} \approx \frac{3I_{P1}}{2V_{p0}} \cdot \frac{V_{DS}}{\sqrt{V_{p0}(V_{bi} - V_{GS})}} \tag{13.39}$$

We can also write Equation (13.39) in terms of the conductance parameter G_{01} as

$$g_{mL} = \frac{G_{01}}{2} \cdot \frac{V_{DS}}{\sqrt{V_{p0}(V_{bi} - V_{GS})}} \tag{13.40}$$

The ideal drain current in the saturation region for the JFET is given by Equation (13.35). The transconductance in the saturation region is then found to be

$$g_{ms} = \frac{\partial I_{D1}(\text{sat})}{\partial V_{GS}} = \frac{3I_{P1}}{V_{p0}}\left(1 - \sqrt{\frac{V_{bi} - V_{GS}}{V_{p0}}}\right) = G_{01}\left(1 - \sqrt{\frac{V_{bi} - V_{GS}}{V_{p0}}}\right) \tag{13.41a}$$

Using the current–voltage approximation given by Equation (13.14), we can also write the transconductance as

$$g_{ms} = \frac{-2I_{DSS}}{V_p}\left(1 - \frac{V_{GS}}{V_p}\right) \tag{13.41b}$$

Since V_p is negative for the n-channel JFET, g_{ms} is positive.

EXAMPLE 13.4

Objective: Determine the maximum transconductance of an n-channel depletion mode JFET biased in the saturation region.

Consider the silicon JFET described in Example 13.3. We had calculated $I_{P1} = 0.522$ mA, $V_{bi} = 0.814$ V, and $V_{p0} = 4.35$ V.

■ Solution

The maximum transconductance occurs when $V_{GS} = 0$. Then Equation (13.41a) can be written as

$$g_{ms}(\text{max}) = \frac{3I_{P1}}{V_{p0}}\left(1 - \sqrt{\frac{V_{bi}}{V_{p0}}}\right) = \frac{3(0.522)}{4.35}\left(1 - \sqrt{\frac{0.814}{4.35}}\right) = 0.204 \text{ mA/V}$$

■ Comment

The saturation transconductance is a function of V_{GS} and becomes zero when $V_{GS} = V_P$.

■ EXERCISE PROBLEM

Ex 13.4 Determine the maximum transconductance of the n-channel JFET described in Exercise Problem Ex 13.3.

[Ans. $g_{ms}(\text{max}) = 0.109$ mA/V]

The experimental transconductance may deviate from this ideal expression due to a source series resistance. This effect will be considered later in the discussion of the small signal model of the JFET.

13.2.4 The MESFET

So far in our discussion, we have explicitly considered the pn JFET. The MESFET is the same basic device except that the pn junction is replaced by a Schottky barrier rectifying junction. The simplified MESFET geometry is shown in Figure 13.9b. MESFETs are usually fabricated in gallium arsenide. We will neglect any depletion region that may exist between the n channel and the substrate. We have also limited our discussion to depletion mode devices, wherein a gate-to-source voltage is applied to turn the transistor off. Enhancement mode GaAs MESFETs can be fabricated—their basic operation is discussed in Section 13.1.2. We can also consider enhancement mode GaAs pn JFETs.

Since the electron mobility in GaAs is much larger than the hole mobility, we will concentrate our discussion on n-channel GaAs MESFETs or JFETs. The definition of internal pinchoff voltage, given by Equation (13.3), also applies to these devices. In considering the enhancement mode JFET, the term threshold voltage is commonly used in place of pinchoff voltage. For this reason, we shall use the term threshold voltage in our discussion of MESFETs.

For the n-channel MESFET, the threshold voltage is defined from Equation (13.4) as

$$V_{bi} - V_T = V_{p0} \quad \text{or} \quad \boxed{V_T = V_{bi} - V_{p0}} \tag{13.42}$$

For an n-channel depletion mode JFET, $V_T < 0$, and for the enhancement mode device, $V_T > 0$. We can see from Equation (13.42) that $V_{bi} > V_{p0}$ for an enhancement mode n-channel JFET.

DESIGN EXAMPLE 13.5

Objective: Determine the channel thickness of a GaAs MESFET to achieve a specified threshold voltage.

Consider an n-channel GaAs MESFET at $T = 300$ K with a gold Schottky barrier contact. Assume the barrier height is $\phi_{Bn} = 0.89$ V. The n-channel doping is $N_d = 2 \times 10^{15}$ cm^{-3}. Design the channel thickness such that $V_T = +0.25$ V.

■ Solution

We find that

$$\phi_n = V_t \ln\left(\frac{N_c}{N_d}\right) = (0.0259) \ln\left(\frac{4.7 \times 10^{17}}{2 \times 10^{15}}\right) = 0.141 \text{ V}$$

The built-in potential barrier is then

$$V_{bi} = \phi_{Bn} - \phi_n = 0.89 - 0.141 = 0.749 \text{ V}$$

The threshold voltage, from Equation (13.42), is

$$V_T = V_{bi} - V_{p0}$$

or

$$V_{p0} = V_{bi} - V_T = 0.749 - 0.25 = 0.499 \text{ V}$$

Now

$$V_{p0} = \frac{eа^2 N_d}{2\epsilon_s}$$

or

$$0.499 = \frac{a^2 (1.6 \times 10^{-19}) (2 \times 10^{15})}{2(13.1) (8.85 \times 10^{-14})}$$

The channel thickness is then

$$a = 0.601 \ \mu\text{m}$$

Comment

For this enhancement mode n-channel MESFET, the internal pinchoff voltage is less than the built-in potential barrier. A smaller channel thickness would result in a larger threshold voltage.

EXERCISE PROBLEM

Ex 13.5 Consider an n-channel GaAs MESFET with a gate barrier height of $\phi_{Bn} = 0.85$ V. The channel doping concentration is $N_d = 5 \times 10^{15}$ cm^{-3} and the channel thickness is $a = 0.40$ μm. Calculate the internal pinchoff voltage and the threshold voltage.

(Ans. $V_{po} = 0.5520$ V, $V_T = 0.1180$ V)

The design of enhancement mode JFETs implies the use of narrow channel thicknesses and low channel doping concentrations to achieve this condition. The precise control of the channel thickness and doping concentration necessary to achieve internal pinchoff voltages of a few tenths of a volt makes the fabrication of enhancement mode MESFETs difficult.

EXAMPLE 13.6

Objective: Calculate the forward-bias gate voltage required in an n-channel GaAs enhancement mode pn JFET to open up a channel.

Consider a GaAs n-channel pn JFET at $T = 300$ K with $N_a = 10^{18}$ cm^{-3}, $N_d = 3 \times 10^{15}$ cm^{-3}, and $a = 0.70$ μm. Determine the forward-bias gate voltage required to open a channel region that is 0.10 μm thick with zero drain voltage.

Solution

The built-in potential barrier is

$$V_{bi} = V_t \ln\left(\frac{N_a N_d}{n_i^2}\right) = (0.0259)\ln\left[\frac{(10^{18})(3 \times 10^{15})}{(1.8 \times 10^6)^2}\right] = 1.25 \text{ V}$$

The internal pinchoff voltage is

$$V_{p0} = \frac{ea^2 N_d}{2\epsilon_s} = \frac{(1.6 \times 10^{-19})(0.7 \times 10^{-4})^2(3 \times 10^{15})}{2(13.1)(8.85 \times 10^{-14})} = 1.01 \text{ V}$$

which gives a threshold voltage of

$$V_T = V_{bi} - V_{p0} = 0.24 \text{ V}$$

The channel depletion width is given by Equation (13.1). Setting $h = 0.60$ μm will yield an undepleted channel thickness of 0.1 μm. Solving for V_{GS}, we obtain

$$V_{GS} = V_{bi} - \frac{eh^2 N_d}{2\epsilon_s} = 1.25 - \frac{(1.6 \times 10^{-19})(0.6 \times 10^{-4})^2(3 \times 10^{15})}{2(13.1)(8.85 \times 10^{-14})}$$

$$= 1.25 - 0.745 = 0.50 \text{ V}$$

Comment

An applied gate voltage of 0.50 V is greater than the threshold voltage, so the induced depletion region will be smaller than the metallurgical channel thickness. An n-channel region is