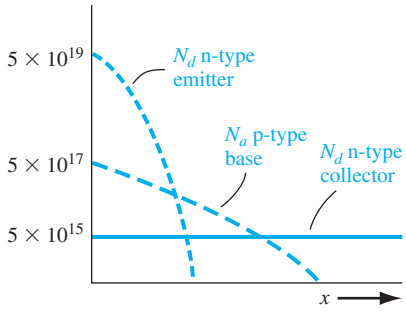

Figure 12.31 | Impurity concentration profiles of a double-diffused npn bipolar transistor.

Electrons are injected from the n-type emitter into the base, and the minority carrier base electrons begin diffusing toward the collector region. The induced electric field in the base, because of the nonuniform doping, produces a force on the electrons in the direction toward the collector. The induced electric field, then, aids the flow of minority carriers across the base region. This electric field is called an *accelerating field.*

The accelerating field will produce a drift component of current that is in addition to the existing diffusion current. Since the minority carrier electron concentration varies across the base, the drift current density will not be constant. The total current across the base, however, is nearly constant. The induced electric field in the base due to nonuniform base doping will alter the minority carrier distribution through the base so that the sum of drift current and diffusion current will be a constant. Calculations have shown that the uniformly doped base theory is very useful for estimating the base characteristics.

12.4.6 Breakdown Voltage

There are two breakdown mechanisms to consider in a bipolar transistor. The first is called punch-through. As the reverse-biased B–C voltage increases, the B–C space charge region widens and extends farther into the neutral base. It is possible for the B–C depletion region to penetrate completely through the base and reach the B–E space charge region, the effect called *punch-through*. Figure 12.32a shows the energy-band diagram of an npn bipolar transistor in thermal equilibrium, and Figure 12.32b shows the energy-band diagram for two values of reverse-biased B–C junction voltage. When a small C–B voltage, V_{R1}, is applied, the B–E potential barrier is not affected; thus, the transistor current is still essentially zero. When a large reverse-biased voltage, V_{R2}, is applied, the depletion region extends through the base region and the B–E potential barrier is lowered because of the C–B voltage. The lowering of the potential barrier at the B–E junction produces a large increase in current with a very small increase in C–B voltage. This effect is the punch-through breakdown phenomenon.

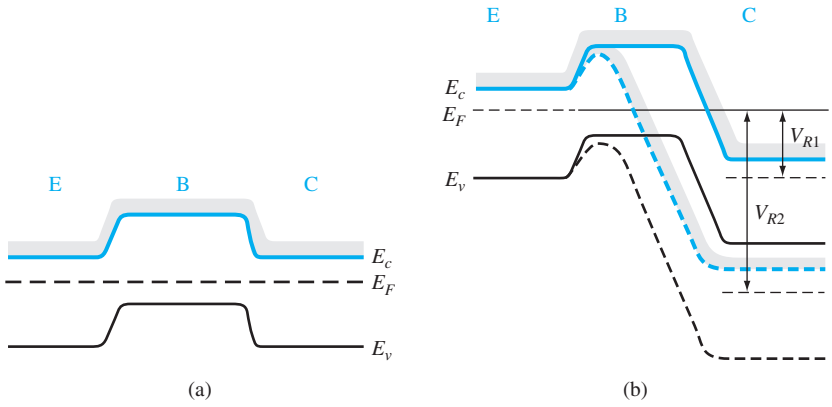

Figure 12.32 | Energy-band diagram of an npn bipolar transistor (a) in thermal equilibrium, and (b) with a reverse-biased B–C voltage before punch-through, V_{R1}, and after punch-through, V_{R2}.

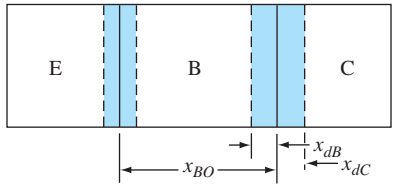

Figure 12.33 | Geometry of a bipolar transistor to calculate the punch-through voltage.

Figure 12.33 shows the geometry for calculating the punch-through voltage. Assume that N_B and N_C are the uniform impurity doping concentrations in the base and collector, respectively. Let x_{BO} be the metallurgical width of the base and let x_{dB} be the space charge width extending into the base from the B–C junction. If we neglect the narrow space charge width of a zero-biased or forward-biased B–E junction, then punch-through, assuming the abrupt junction approximation, occurs when $x_{dB} = x_{BO}$. We can write that

$$x_{dB} = x_{BO} = \left\{\frac{2\epsilon_s(V_{bi} + V_{pt})}{e} \cdot \frac{N_C}{N_B} \cdot \frac{1}{N_C + N_B}\right\}^{1/2} \tag{12.53}$$

where V_{pt} is the reverse-biased B–C voltage at punch-through. Neglecting V_{bi} compared to V_{pt}, we can solve for V_{pt} as

$$\boxed{V_{pt} = \frac{ex_{BO}^2}{2\epsilon_s} \cdot \frac{N_B(N_C + N_B)}{N_C}} \tag{12.54}$$

DESIGN EXAMPLE 12.10

Objective: Design the collector doping concentration and collector width to meet a punch-through voltage specification.

Consider a uniformly doped silicon bipolar transistor with a metallurgical base width of 0.5 μm and a base doping of $N_B = 10^{16}$ cm^{-3}. The punch-through voltage is to be $V_{pt} = 25$ V.

■ Solution

The maximum collector doping concentration can be determined from Equation (12.54) as

$$25 = \frac{(1.6 \times 10^{-19})(0.5 \times 10^{-4})^2(10^{16})(N_C + 10^{16})}{2(11.7)(8.85 \times 10^{-14})N_C}$$

or

$$12.94 = 1 + \frac{10^{16}}{N_C}$$

which yields

$$N_C = 8.38 \times 10^{14} \text{ cm}^{-3}$$

Using this n-type doping concentration for the collector, we can determine the minimum width of the collector region such that the depletion region extending into the collector will not reach the substrate and cause breakdown in the collector region. We have, using the results of Chapter 7,

$$x_{dC} = x_C = 5.97 \ \mu\text{m}$$

■ Comment

From Figure 7.15, the expected avalanche breakdown voltage for this junction is greater than 300 V. Obviously punch-through will occur before the normal breakdown voltage in this case. For a larger punch-through voltage, a larger metallurgical base width will be required, since a lower collector doping concentration is becoming impractical. A larger punch-through voltage will also require a larger collector width in order to avoid premature breakdown in this region.

■ EXERCISE PROBLEM

Ex 12.10 The metallurgical base width of a silicon npn bipolar transistor is $x_{B0} = 0.80$ μm. The base and collector doping concentrations are $N_B = 5 \times 10^{16}$ cm^{-3} and $N_C = 2 \times 10^{15}$ cm^{-3}, respectively. (*a*) Determine the punch-through voltage. (*b*) What is the expected avalanche breakdown voltage?

[Ans. (*a*) $V_{pt} = 643$ V; (*b*) $BV = 180$ V]

The second breakdown mechanism to consider is avalanche breakdown, but taking into account the gain of the transistor.[2] Figure 12.34a is an npn transistor with a reverse-biased voltage applied to the B–C junction and with the emitter left open. The current I_{CBO} is the reverse-biased junction current. Figure 12.34b shows the transistor with an applied C–E voltage and with the base terminal left open. This bias

[2]The doping concentrations in the base and collector of the transistor are small enough that Zener breakdown is not a factor to be considered.

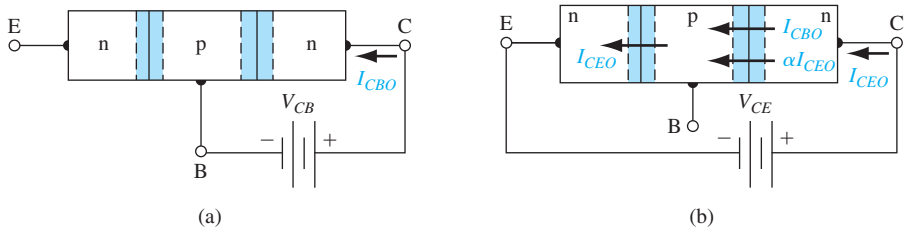

Figure 12.34 | (a) Open-emitter configuration with saturation current I_{CBO}: (b) Open-base configuration with saturation current I_{CEO}.

condition also makes the B–C junction reverse biased. The current in the transistor for this bias configuration is denoted as I_{CEO}.

The current I_{CBO} shown in Figure 12.34b is the normal reverse-biased B–C junction current. Part of this current is due to the flow of minority carrier holes from the collector across the B–C space charge region into the base. The flow of holes into the base makes the base positive with respect to the emitter, and the B–E junction becomes forward biased. The forward-biased B–E junction produces the current I_{CEO}, due primarily to the injection of electrons from the emitter into the base. The injected electrons diffuse across the base toward the B–C junction. These electrons are subject to all of the recombination processes in the bipolar transistor. When the electrons reach the B–C junction, this current component is αI_{CEO} where α is the common-base current gain. We therefore have

$$I_{CEO} = \alpha I_{CEO} + I_{CBO} \tag{12.55a}$$

or

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha} \approx \beta I_{CBO} \tag{12.55b}$$

where β is the common-emitter current gain. The reverse-biased junction current I_{CBO} is multiplied by the current gain β when the transistor is biased in the open-base configuration.

When the transistor is biased in the open-emitter configuration as in Figure 12.34a, the current I_{CBO} at breakdown becomes $I_{CBO} \rightarrow MI_{CBO}$, where M is the multiplication factor. An empirical approximation for the multiplication factor is usually written as

$$M = \frac{1}{1 - (V_{CB}/BV_{CBO})^n} \tag{12.56}$$

where n is an empirical constant, usually between 3 and 6, and BV_{CBO} is the B–C breakdown voltage with the emitter left open.

When the transistor is biased with the base open circuited as shown in Figure 12.34b, the currents in the B–C junction at breakdown are multiplied, so that

$$I_{CEO} = M(\alpha I_{CEO} + I_{CBO}) \tag{12.57}$$

Solving for I_{CEO}, we obtain

$$I_{CEO} = \frac{MI_{CBO}}{1 - \alpha M} \tag{12.58}$$

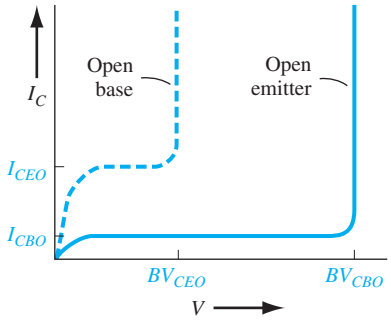

Figure 12.35 | Relative breakdown voltages and saturation currents of the open-base and open-emitter configurations.

The condition for breakdown corresponds to

$$\alpha M = 1 \tag{12.59}$$

Using Equation (12.56) and assuming that $V_{CB} \approx V_{CE}$, Equation (12.59) becomes

$$\frac{\alpha}{1 - (BV_{CEO}/BV_{CBO})^n} = 1 \tag{12.60}$$

where BV_{CEO} is the C–E voltage at breakdown in the open-base configuration. Solving for BV_{CEO}, we find

$$BV_{CEO} = BV_{CBO}\sqrt[n]{1 - \alpha} \tag{12.61}$$

where, again, α is the common-base current gain. The common-emitter and common-base current gains are related by

$$\beta = \frac{\alpha}{1 - \alpha} \tag{12.62a}$$

Normally $\alpha \approx 1$, so that

$$1 - \alpha \approx \frac{1}{\beta} \tag{12.62b}$$

Then Equation (12.61) can be written as

$$\boxed{BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}}} \tag{12.63}$$

The breakdown voltage in the open-base configuration is smaller, by the factor $\sqrt[n]{\beta}$, than the actual avalanche junction breakdown voltage. This characteristic is shown in Figure 12.35.

DESIGN EXAMPLE 12.11

Objective: Design a bipolar transistor to meet a breakdown voltage specification.

Consider a silicon bipolar transistor with a common-emitter current gain of $\beta = 100$ and a base doping concentration of $N_B = 10^{17}$ cm^{-3}. The minimum open-base breakdown voltage is to be 15 V.

■ Solution

From Equation (12.63), the minimum open-emitter junction breakdown voltage must be

$$BV_{CBO} = \sqrt[n]{\beta} BV_{CEO}$$

Assuming the empirical constant n is 3, we find

$$BV_{CBO} = \sqrt[3]{100}(15) = 69.6 \text{ V}$$

From Figure 7.15, the maximum collector doping concentration should be approximately 7×10^{15} cm^{-3} to achieve this breakdown voltage.

■ Comment

In a transistor circuit, the transistor must be designed to operate under a worst-case situation. In this example, the transistor must be able to operate in an open-base configuration without going into breakdown. As we have determined previously, an increase in breakdown voltage can be achieved by decreasing the collector doping concentration.

■ EXERCISE PROBLEM

Ex 12.11 A uniformly doped silicon bipolar transistor has base and collector doping concentrations of $N_B = 7 \times 10^{16}$ cm^{-3} and $N_C = 3 \times 10^{15}$ cm^{-3}, respectively. The common-emitter current gain is $\beta = 125$. Assuming an empirical constant of $n = 3$, determine (*a*) BV_{CBO} and (*b*) BV_{CEO}.

[Ans. (*a*) $BV_{CBO} \cong 125$ V; (*b*) $BV_{CEO} = 25$ V]

TEST YOUR UNDERSTANDING

TYU 12.8 A particular transistor has an output resistance of 200 kΩ and an Early voltage of $V_A = 125$ V. Determine the change in collector current when V_{CE} increases from 2 V to 8 V. (Ans. $\Delta I_C = 30\ \mu$A)

TYU 12.9 (*a*) If, because of fabrication tolerances, the neutral base width for a set of transistors varies over the range of $0.800 \le x_B \le 1.00\ \mu$m, determine the variation in the base transport factor α_T. Assume $L_B = 1.414 \times 10^{-3}$ cm. (*b*) Using the results of part (*a*) and assuming $\gamma = \delta = 0.9967$, what is the variation in common-emitter current gain? [Ans. (*a*) $0.9975 \le \alpha_T \le 0.9984$; (*b*) $109 \le \beta \le 121$]

TYU 12.10 The base impurity doping concentration is $N_B = 3 \times 10^{16}$ cm^{-3} and the metallurgical base width is $x_B = 0.70\ \mu$m. The minimum required punch-through breakdown voltage is specified to be $V_{pt} = 70$ V. What is the maximum allowed collector doping concentration? (Ans. $N_C = 5.81 \times 10^{15}$ cm^{-3})

12.5 | EQUIVALENT CIRCUIT MODELS

In order to analyze a transistor circuit either by hand calculations or using computer codes, one needs a mathematical model, or equivalent circuit, of the transistor. There are several possible models, each one having certain advantages and disadvantages.

A detailed study of all possible models is beyond the scope of this chapter. However, we will consider three equivalent circuit models. Each of these follows directly from the work we have done on the pn junction diode and on the bipolar transistor. Computer analysis of electronic circuits is more commonly used than hand calculations, but it is instructive to consider the types of transistor model used in computer codes.

It is useful to divide bipolar transistors into two categories—switching and amplification—defined by their use in electronic circuits. Switching usually involves turning a transistor from its "off" state, or cutoff, to its "on" state, either forward-active or saturation, and then back to its "off" state. Amplification usually involves superimposing sinusoidal signals on dc values so that bias voltages and currents are only perturbed. The *Ebers–Moll model* is used in switching applications; the *hybrid-pi* model is used in amplification applications.

*12.5.1 Ebers–Moll Model

The Ebers–Moll model, or equivalent circuit, is one of the classic models of the bipolar transistor. This particular model is based on the interacting diode junctions and is applicable in any of the transistor operating modes. Figure 12.36 shows the current directions and voltage polarities used in the Ebers–Moll model. The currents are defined as all entering the terminals so that

$$I_E + I_B + I_C = 0 \tag{12.64}$$

The direction of the emitter current is opposite to what we have considered up to this point, but as long as we are consistent in the analysis, the defined direction does not matter.

The collector current can be written in general as

$$I_C = \alpha_F I_F - I_R \tag{12.65a}$$

where α_F is the common-base current gain in the forward-active mode. In this mode, Equation (12.65a) becomes

$$I_C = \alpha_F I_F + I_{CS} \tag{12.65b}$$

where the current I_{CS} is the reverse-biased B–C junction current. The current I_F is given by

$$I_F = I_{ES}\left[\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right] \tag{12.66}$$

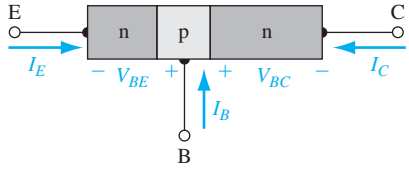

Figure 12.36 | Current direction and voltage polarity definitions for the Ebers–Moll model.

If the B–C junction becomes forward biased, such as in saturation, then we can write the current I_R as

$$I_R = I_{CS}\left[\exp\left(\frac{eV_{BC}}{kT}\right) - 1\right] \tag{12.67}$$

Using Equations (12.66) and (12.67), the collector current from Equation (12.65a) can be written as

$$I_C = \alpha_F I_{ES}\left[\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right] - I_{CS}\left[\exp\left(\frac{eV_{BC}}{kT}\right) - 1\right] \tag{12.68}$$

We can also write the emitter current as

$$I_E = \alpha_R I_R - I_F \tag{12.69}$$

or

$$I_E = \alpha_R I_{CS}\left[\exp\left(\frac{eV_{BC}}{kT}\right) - 1\right] - I_{ES}\left[\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right] \tag{12.70}$$

The current I_{ES} is the reverse-biased B–E junction current and α_R is the common-base current gain for the inverse-active mode. Equations (12.68) and (12.70) are the classic Ebers–Moll equations.

Figure 12.37 shows the equivalent circuit corresponding to Equations (12.68) and (12.70). The current sources in the equivalent circuit represent current components that depend on voltages across other junctions. The Ebers–Moll model has four parameters: α_F, α_R, I_{ES}, and I_{CS}. However, only three parameters are independent. The reciprocity relationship states that

$$\alpha_F I_{ES} = \alpha_R I_{CS} \tag{12.71}$$

Since the Ebers–Moll model is valid in each of the four operating modes, we can, for example, use the model for the transistor in saturation. In the saturation mode, both B–E and B–C junctions are forward biased, so that $V_{BE} > 0$ and $V_{BC} > 0$. The B–E voltage will be a known parameter since we will apply a voltage across this junction. The forward-biased B–C voltage is a result of driving the transistor into saturation and is the unknown to be determined from the Ebers–Moll equations.

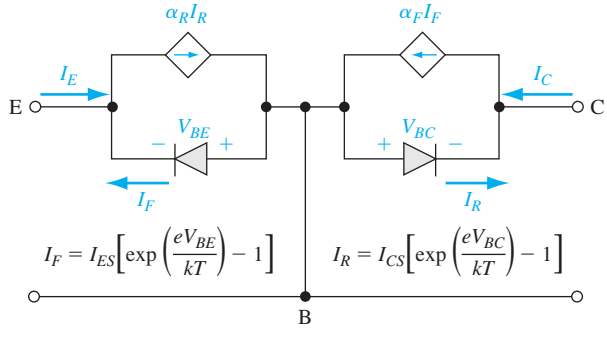

Figure 12.37 | Basic Ebers–Moll equivalent circuit.

Normally in electronic circuit applications, the collector–emitter voltage at saturation is of interest. We can define the C–E saturation voltage as

$$V_{CE}(\text{sat}) = V_{BE} - V_{BC} \tag{12.72}$$

We find an expression for $V_{CE}(\text{sat})$ by combining the Ebers–Moll equations. In the following example, we see how the Ebers–Moll equations can be used in a hand calculation, and we may also see how a computer analysis would make the calculations easier.

Combining Equations (12.64) and (12.70), we have

$$-(I_B + I_C) = \alpha_R I_{CS}\left[\exp\left(\frac{eV_{BC}}{kT}\right) - 1\right] - I_{ES}\left[\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right] \tag{12.73}$$

If we solve for $[\exp(eV_{BC}/kT) - 1]$ from Equation (12.73), and substitute the resulting expression into Equation (12.68), we can then find V_{BE} as

$$V_{BE} = V_t \ln\left[\frac{I_C(1-\alpha_R) + I_B + I_{ES}(1-\alpha_F\alpha_R)}{I_{ES}(1-\alpha_F\alpha_R)}\right] \tag{12.74}$$

where V_t is the thermal voltage. Similarly, if we solve for $[\exp(eV_{BE}/kT) - 1]$ from Equation (12.68), and substitute this expression into Equation (12.73), we can find V_{BC} as

$$V_{BC} = V_t \ln\left[\frac{\alpha_F I_B - (1-\alpha_F)I_C + I_{CS}(1-\alpha_F\alpha_R)}{I_{CS}(1-\alpha_F\alpha_R)}\right] \tag{12.75}$$

We may neglect the I_{ES} and I_{CS} terms in the numerators of Equations (12.74) and (12.75). Solving for $V_{CE}(\text{sat})$, we have

$$V_{CE}(\text{sat}) = V_{BE} - V_{CB} = V_t \ln\left[\frac{I_C(1-\alpha_R) + I_B}{\alpha_F I_B - (1-\alpha_F)I_C} \cdot \frac{I_{CS}}{I_{ES}}\right] \tag{12.76}$$

The ratio of I_{CS} to I_{ES} can be written in terms of α_F and α_R from Equation (12.71). We can finally write

$$V_{CE}(\text{sat}) = V_t \ln\left[\frac{I_C(1-\alpha_R) + I_B}{\alpha_F I_B - (1-\alpha_F)I_C} \cdot \frac{\alpha_F}{\alpha_R}\right] \tag{12.77}$$

EXAMPLE 12.12

Objective: Calculate the collector–emitter saturation voltage of a bipolar transistor at $T = 300$ K.

Assume that $\alpha_F = 0.99$, $\alpha_R = 0.20$, $I_C = 1$ mA, and $I_B = 50\ \mu$A.

■ Solution

Substituting the parameters into Equation (12.77), we have

$$V_{CE}(\text{sat}) = (0.0259)\ln\left[\frac{(1)(1-0.2) + (0.05)}{(0.99)(0.05) - (1-0.99)(1)}\left(\frac{0.99}{0.20}\right)\right] = 0.121 \text{ V}$$

■ Comment

This $V_{CE}(\text{sat})$ value is typical of collector–emitter saturation voltages. Because of the log function, $V_{CE}(\text{sat})$ is not a strong function of I_C or I_B.

EXERCISE PROBLEM

Ex 12.12 Repeat Example 12.12 for transistor parameters of $\alpha_F = 0.992$, $\alpha_R = 0.05$, $I_C = 0.5$ mA, and $I_B = 50\ \mu$A. (Ans. $V_{CE} = 0.141$ V)

12.5.2 Gummel–Poon Model

The Gummel–Poon model of the BJT considers more physics of the transistor than the Ebers–Moll model. This model can be used if, for example, there is a nonuniform doping concentration in the base.

The electron current density in the base of an npn transistor can be written as

$$J_n = e\mu_n n(x)\mathrm{E} + eD_n\frac{dn(x)}{dx} \tag{12.78}$$

An electric field will occur in the base if nonuniform doping exists in the base. This is discussed in Section 12.4.5. The electric field, from Equation (12.52), can be written in the form

$$\mathrm{E} = \frac{kT}{e}\cdot\frac{1}{p(x)}\cdot\frac{dp(x)}{dx} \tag{12.79}$$

where $p(x)$ is the majority carrier hole concentration in the base. Under low injection, the hole concentration is just the acceptor impurity concentration. With the doping profile shown in Figure 12.31, the electric field is negative (from the collector to the emitter). The direction of this electric field aids the flow of electrons across the base.

Substituting Equation (12.79) into Equation (12.78), we obtain

$$J_n = e\mu_n n(x)\cdot\frac{kT}{e}\cdot\frac{1}{p(x)}\cdot\frac{dp(x)}{dx} + eD_n\frac{dn(x)}{dx} \tag{12.80}$$

Using Einstein's relation, we can write Equation (12.80) in the form

$$J_n = \frac{eD_n}{p(x)}\left[n(x)\frac{dp(x)}{dx} + p(x)\frac{dn(x)}{dx}\right] = \frac{eD_n}{p(x)}\cdot\frac{d(pn)}{dx} \tag{12.81}$$

Equation (12.81) can be written in the form

$$\frac{J_n p(x)}{eD_n} = \frac{d(pn)}{dx} \tag{12.82}$$

Integrating Equation (12.82) through the base region while assuming that the electron current density is essentially a constant and the diffusion coefficient is a constant, we find

$$\frac{J_n}{eD_n}\int_0^{x_B} p(x)\,dx = \int_0^{x_B}\frac{dp(x)}{dx}\,dx = p(x_B)n(x_B) - p(0)n(0) \tag{12.83}$$

Assuming that the B–E junction is forward biased and the B–C junction is reverse biased, we have $n(0) = n_{B0}\exp(V_{BE}/V_t)$ and $n(x_B) = 0$. We may note that $n_{B0}p = n_i^2$ so that Equation (12.83) can be written as

$$J_n = \frac{-eD_n n_i^2\exp(V_{BE}/V_t)}{\displaystyle\int_0^{x_B} p(x)\,dx} \tag{12.84}$$

The integral in the denominator is the total majority carrier charge in the base and is known as the *base Gummel number,* defined as Q_B.

If we perform the same analysis in the emitter, we find that the hole current density in the emitter of an npn transistor can be expressed as

$$J_p = \frac{-eD_p n_i^2 \exp(V_{BE}/V_t)}{\displaystyle\int_0^{x_E} n(x')\,dx'} \tag{12.85}$$

The integral in the denominator is the total majority carrier charge in the emitter and is known as the emitter Gummel number, defined as Q_E.

Since the currents in the Gummel–Poon model are functions of the total integrated charges in the base and emitter, these currents can easily be determined for nonuniformly doped transistors.

The Gummel–Poon model can also take into account nonideal effects, such as the Early effect and high-level injection. As the B–C voltage changes, the neutral base width changes so that the base Gummel number Q_B changes. The change in Q_B with B–C voltage then makes the electron current density given by Equation (12.84) a function of the B–C voltage. This is the base width modulation effect or Early effect as discussed previously in Section 12.4.1.

If the B–E voltage becomes too large, low injection no longer applies, which leads to high-level injection. In this case, the total hole concentration in the base increases because of the increased excess hole concentration. This means that the base Gummel number will increase. The change in base Gummel number implies, from Equation (12.84), that the electron current density will also change. High-level injection has also been previously discussed in Section 12.4.2.

The Gummel–Poon model can then be used to describe the basic operation of the transistor as well as to describe nonideal effects.

12.5.3 Hybrid-Pi Model

Bipolar transistors are commonly used in circuits that amplify time-varying or sinusoidal signals. In these linear amplifier circuits, the transistor is biased in the forward-active region and small sinusoidal voltages and currents are superimposed on dc voltages and currents. In these applications, the sinusoidal parameters are of interest, so it is convenient to develop a small-signal equivalent circuit of the bipolar transistor using the small-signal admittance parameters of the pn junction developed in Chapter 8.

Figure 12.38a shows an npn bipolar transistor in a common-emitter configuration with the small-signal terminal voltages and currents. Figure 12.38b shows the cross section of the npn transistor. The C, B, and E terminals are the external connections to the transistor, while the C′, B′, and E′ points are the idealized internal collector, base, and emitter regions.

We can begin constructing the equivalent circuit of the transistor by considering the various terminals individually. Figure 12.39a shows the equivalent circuit between the external input base terminal and the external emitter terminal. The resistance r_b is the series resistance in the base between the external base terminal B and the internal base region B′. The B′−E′ junction is forward biased, so C_π is

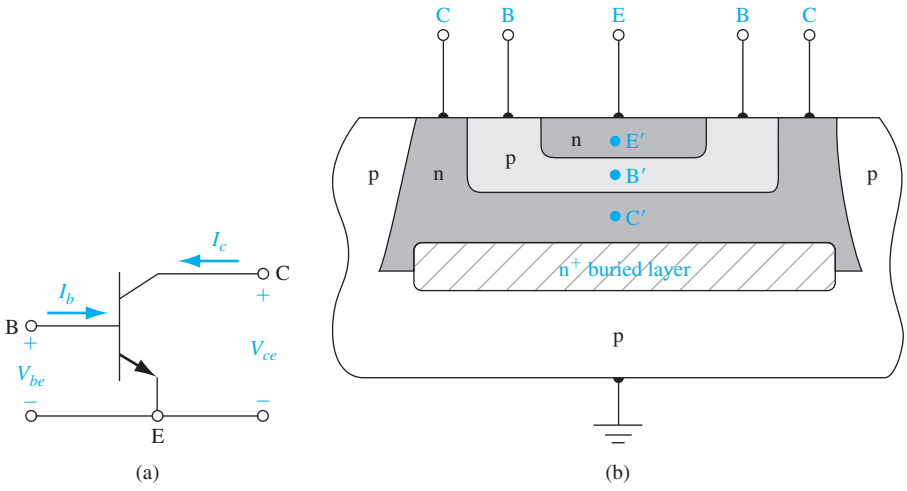

Figure 12.38 | (a) Common-emitter npn bipolar transistor with small-signal current and voltages. (b) Cross section of an npn bipolar transistor for the hybrid-pi model.

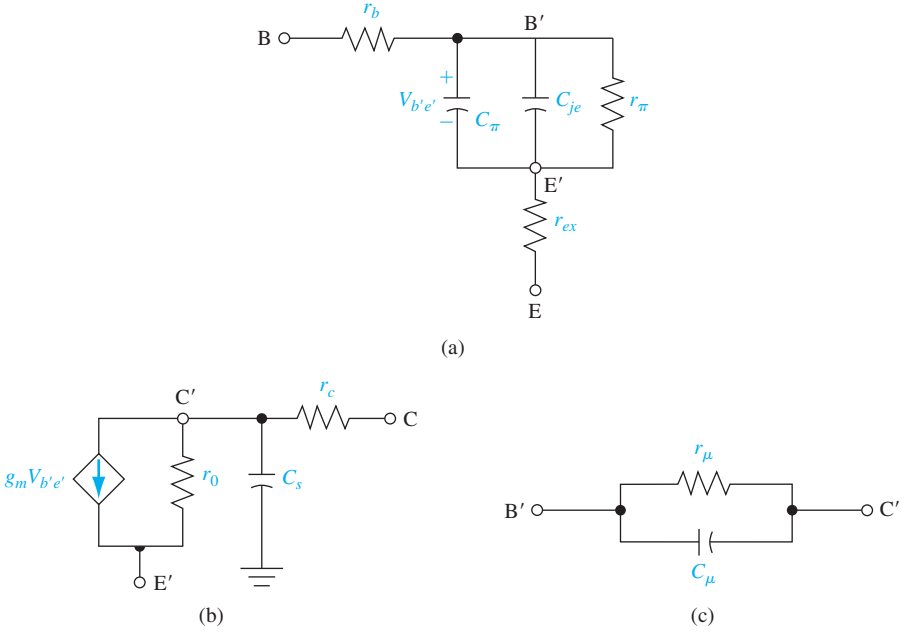

Figure 12.39 | Components of the hybrid-pi equivalent circuit between (a) the base and emitter, (b) the collector and emitter, and (c) the base and collector.

the junction diffusion capacitance and r_π is the junction diffusion resistance. The diffusion capacitance C_π is the same as the diffusion capacitance C_d given by Equation (8.105), and the diffusion resistance r_π is the same as the diffusion resistance r_d given by Equation (8.68). The values of both parameters are functions of the junction

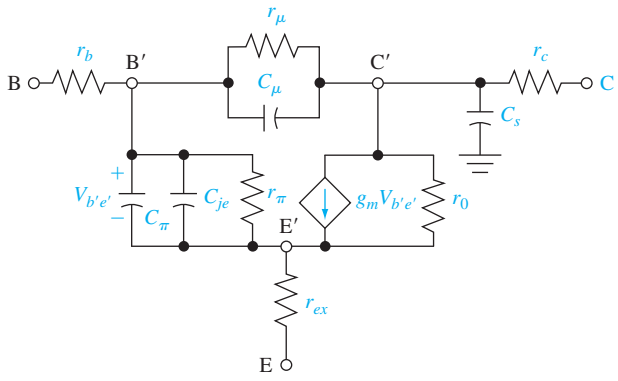

Figure 12.40 | Hybrid-pi equivalent circuit.

current. These two elements are in parallel with the junction capacitance, which is C_{je}. Finally, r_{ex} is the series resistance between the external emitter terminal and the internal emitter region. This resistance is usually very small and may be on the order of 1 to 2 Ω.

Figure 12.39b shows the equivalent circuit looking into the collector terminal. The r_c resistance is the series resistance between the external and internal collector connections and the capacitance C_s is the junction capacitance of the reverse-biased collector-substrate junction. The dependent current source, $g_m V_{b'e'}$, is the collector current in the transistor, which is controlled by the internal base–emitter voltage. The resistance r_0 is the inverse of the output conductance g_0 and is primarily due to the Early effect.

Finally, Figure 12.39c shows the equivalent circuit of the reverse-biased B′−C′ junction. The C_μ parameter is the reverse-biased junction capacitance and r_μ is the reverse-biased diffusion resistance. Normally, r_μ is on the order of megohms and can be neglected. The value of C_μ is usually much smaller than C_π but, because of the feedback effect that leads to the Miller effect and Miller capacitance, C_μ cannot be ignored in most cases. The Miller capacitance is the equivalent capacitance between B′ and E′ due to C_μ and the feedback effect, which includes the gain of the transistor. The Miller effect also reflects C_μ between the C′ and E′ terminals at the output. However, the effect on the output characteristics can usually be ignored.

Figure 12.40 shows the complete hybrid-pi equivalent circuit. A computer simulation is usually required for this complete model because of the large number of elements. However, some simplifications can be made in order to gain an appreciation for the frequency effects of the bipolar transistor. The capacitances lead to frequency effects in the transistor, which means that the gain, for example, is a function of the input signal frequency.

EXAMPLE 12.13

Objective: Determine, to a first approximation, the frequency at which the small-signal current gain decreases to $1/\sqrt{2}$ of its low-frequency value.

Consider the simplified hybrid-pi circuit shown in Figure 12.41. We are ignoring C_μ, C_s, r_μ, C_{je}, r_0, and the series resistances. We must emphasize that this is a first-order calculation and that C_μ normally cannot be neglected.

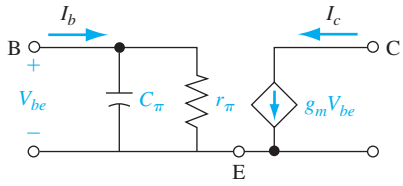

Figure 12.41 | Simplified hybrid-pi equivalent circuit.

■ Solution

At very low frequency, we may neglect C_π so that

$$V_{be} = I_b\, r_\pi \qquad \text{and} \qquad I_c = g_m V_{be} = g_m\, r_\pi\, I_b$$

We can then write

$$h_{fe0} = \frac{I_c}{I_b} = g_m r_\pi$$

where h_{fe0} is the low-frequency, small-signal common-emitter current gain.

Taking into account C_π, we have

$$V_{be} = I_b \left(\frac{r_\pi}{1 + j\omega r_\pi C_\pi} \right)$$

Then

$$I_c = g_m V_{be} = I_b \left(\frac{h_{fe0}}{1 + j\omega r_\pi C_\pi} \right)$$

or the small-signal current gain can be written as

$$A_i = \frac{I_c}{I_b} = \left(\frac{h_{fe0}}{1 + j\omega r_\pi C_\pi} \right)$$

The magnitude of the current gain is then

$$|A_i| = \left| \frac{I_c}{I_b} \right| = \frac{h_{fe0}}{\sqrt{1 + (\omega r_\pi\, C_\pi)^2}} = \frac{h_{fe0}}{\sqrt{1 + (2\pi f r_\pi C_\pi)^2}}$$

The magnitude of the current gain drops to $1/\sqrt{2}$ of its low-frequency value at $f = 1/2\pi r_\pi C_\pi$.

If, for example, $r_\pi = 2.6\ \text{k}\Omega$ and $C_\pi = 4$ pF, then

$$f = 15.3\ \text{MHz}$$

■ Comment

High-frequency transistors must have small-diffusion capacitances, implying the use of small devices.

■ EXERCISE PROBLEM

Ex 12.13 Using the results of Example 12.13, determine the maximum value of C_π such that the frequency at which $|A_i| = h_{fe0}/\sqrt{2}$ is $f = 35$ MHz.

(Ans. $C_\pi = 1.75$ pF)

12.6 | FREQUENCY LIMITATIONS

The hybrid-pi equivalent circuit, developed in the last section, introduces frequency effects through the capacitor–resistor circuits. We now discuss the various physical factors in the bipolar transistor affecting the frequency limitations of the device and then define the transistor cutoff frequency, which is a figure of merit for a transistor.

12.6.1 Time-Delay Factors

The bipolar transistor is a transit-time device. When the voltage across the B–E junction increases, for example, additional carriers from the emitter are injected into the base, diffuse across the base, and are collected in the collector region. As the frequency increases, this transit time can become comparable to the period of the input signal. At this point, the output response will no longer be in phase with the input and the magnitude of the current gain will decrease.

The total emitter-to-collector time constant or delay time is composed of four separate time constants. We can write

$$\tau_{ec} = \tau_e + \tau_b + \tau_d + \tau_c \tag{12.86}$$

where

τ_{ec} = emitter-to-collector time delay
τ_e = emitter–base junction capacitance charging time
τ_b = base transit time
τ_d = collector depletion region transit time
τ_c = collector capacitance charging time

The equivalent circuit of the forward-biased B–E junction is given in Figure 12.39a. The capacitance C_{je} is the junction capacitance. If we ignore the series resistance, then the emitter–base junction capacitance charging time is

$$\boxed{\tau_e = r'_e\,(C_{je} + C_p)} \tag{12.87}$$

where r'_e is the emitter junction or diffusion resistance. The capacitance C_p includes any parasitic capacitance between the base and emitter. The resistance r'_e is found as the inverse of the slope of the I_E versus V_{BE} curve. We obtain

$$r'_e = \frac{kT}{e} \cdot \frac{1}{I_E} \tag{12.88}$$

where I_E is the dc emitter current.

The second term, τ_b, is the base transit time, the time required for the minority carriers to diffuse across the neutral base region. The base transit time is related to the diffusion capacitance C_π of the B–E junction. For the npn transistor, the electron current density in the base can be written as

$$J_n = -en_B(x)v(x) \tag{12.89}$$

where $v(x)$ is an average velocity. We can write

$$v(x) = dx/dt \quad \text{or} \quad dt = dx/v(x) \tag{12.90}$$

The transit time can then be found by integrating, or

$$\tau_b = \int_0^{x_B} dt = \int_0^{x_B} \frac{dx}{v(x)} = \int_0^{x_B} \frac{en_B(x)\,dx}{(-J_n)} \tag{12.91}$$

The electron concentration in the base is approximately linear (see Equation (12.15b)) so we can write

$$n_B(x) \cong n_{B0}\left[\exp\left(\frac{eV_{BE}}{kT}\right)\right]\left(1 - \frac{x}{x_B}\right) \tag{12.92}$$

and the electron current density is given by

$$J_n = eD_n \frac{dn_B(x)}{dx} \tag{12.93}$$

The base transit time is then found by combining Equations (12.92) and (12.93) with Equation (12.91). We find that

$$\boxed{\tau_b = \frac{x_B^2}{2D_n}} \tag{12.94}$$

The third time-delay factor is τ_d, the collector depletion region transit time. Assuming that the electrons in the npn device travel across the B–C space charge region at their saturation velocity, we have

$$\boxed{\tau_d = \frac{x_{dc}}{v_s}} \tag{12.95}$$

where x_{dc} is the B–C space charge width and v_s is the electron saturation velocity.

The fourth time-delay factor, τ_c, is the collector capacitance charging time. The B–C is reverse biased so that the diffusion resistance in parallel with the junction capacitance is very large. The charging time constant is then a function of the collector series resistance r_c. We can write

$$\boxed{\tau_c = r_c(C_\mu + C_s)} \tag{12.96}$$

where C_μ is the B–C junction capacitance and C_s is the collector-to-substrate capacitance. The series resistance in small epitaxial transistors is usually small; thus, the time delay τ_c may be neglected in some cases.

Example calculations of the various time-delay factors are given in the next section as part of the cutoff frequency discussion.

12.6.2 Transistor Cutoff Frequency

The current gain as a function of frequency is developed in Example 12.13 so that we can also write the common-base current gain as

$$\alpha = \frac{\alpha_0}{1 + j\dfrac{f}{f_\alpha}} \tag{12.97}$$

where α_0 is the low-frequency common-base current gain and f_α is defined as the *alpha cutoff frequency*. The frequency f_α is related to the emitter-to-collector time delay τ_{ec} as

$$f_\alpha = \frac{1}{2\pi\tau_{ec}} \tag{12.98}$$

When the frequency is equal to the alpha cutoff frequency, the magnitude of the common-base current gain is $1/\sqrt{2}$ of its low-frequency value.

We can relate the alpha cutoff frequency to the common-emitter current gain by considering

$$\beta = \frac{\alpha}{1-\alpha} \tag{12.99}$$

We may replace α in Equation (12.99) with the expression given by Equation (12.97). When the frequency f is of the same order of magnitude as f_α, then

$$|\beta| = \left|\frac{\alpha}{1-\alpha}\right| \approx \frac{f_\alpha}{f} \tag{12.100}$$

where we have assumed that $\alpha_0 \approx 1$. When the signal frequency is equal to the alpha cutoff frequency, the magnitude of the common-emitter current gain is equal to unity. The usual notation is to define this *cutoff frequency* as f_T, so we have

$$\boxed{f_T = \frac{1}{2\pi\tau_{ec}}} \tag{12.101}$$

From the analysis in Example 12.13, we may also write the common-emitter current gain as

$$\beta = \frac{\beta_0}{1 + j(f/f_\beta)} \tag{12.102}$$

where f_β is called the *beta cutoff frequency* and is the frequency at which the magnitude of the common-emitter current gain β drops to $1/\sqrt{2}$ of its low-frequency value.

Combining Equations (12.99) and (12.97), we can write

$$\beta = \frac{\alpha}{1-\alpha} = \frac{\dfrac{\alpha_0}{1 + j(f/f_T)}}{1 - \dfrac{\alpha_0}{1 + j(f/f_T)}} = \frac{\alpha_0}{1 - \alpha_0 + j(f/f_T)} \tag{12.103}$$

or

$$\beta = \frac{\alpha_0}{(1-\alpha_0)\left[1 + j\dfrac{f}{(1-\alpha_0)f_T}\right]} \approx \frac{\beta_0}{1 + j\dfrac{\beta_0 f}{f_T}} \tag{12.104}$$

where

$$\beta_0 = \frac{\alpha_0}{1-\alpha_0} \approx \frac{1}{1-\alpha_0}$$

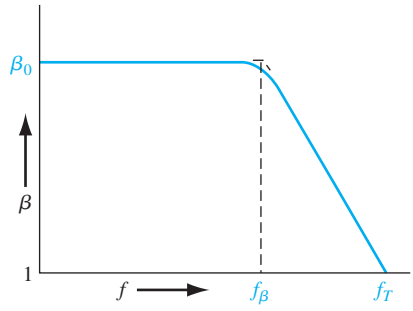

Figure 12.42 | Bode plot of common-emitter current gain versus frequency.

Comparing Equations (12.104) and (12.102), the beta cutoff frequency is related to the cutoff frequency by

$$f_\beta \cong \frac{f_T}{\beta_0} \tag{12.105}$$

Figure 12.42 shows a Bode plot of the common-emitter current gain as a function of frequency and shows the relative values of the beta and cutoff frequencies. Keep in mind that the frequency is plotted on a log scale, so f_β and f_T usually have significantly different values.

EXAMPLE 12.14

Objective: Calculate the emitter-to-collector transit time and the cutoff frequency of a bipolar transistor, with the following parameters.

Consider a silicon npn transistor at $T = 300$ K. Assume the following parameters:

$$\begin{aligned} I_E &= 1 \text{ mA} & C_{je} &= 1 \text{ pF} \\ x_B &= 0.5\ \mu\text{m} & D_n &= 25 \text{ cm}^2/\text{s} \\ x_{dc} &= 2.4\ \mu\text{m} & r_c &= 20\ \Omega \\ C_\mu &= 0.1 \text{ pF} & C_s &= 0.1 \text{ pF} \end{aligned}$$

■ Solution

We will initially calculate the various time-delay factors. If we neglect the parasitic capacitance, the emitter–base junction charging time is

$$\tau_e = r'_e C_{je}$$

where

$$r'_e = \frac{kT}{e} \cdot \frac{1}{I_E} = \frac{0.0259}{1 \times 10^{-3}} = 25.9\ \Omega$$

Then

$$\tau_e = (25.9)(10^{-12}) = 25.9 \text{ ps}$$

The base transit time is

$$\tau_b = \frac{x_B^2}{2D_n} = \frac{(0.5 \times 10^{-4})^2}{2(25)} = 50 \text{ ps}$$

The collector depletion region transit time is

$$\tau_d = \frac{x_{dc}}{v_s} = \frac{2.4 \times 10^{-4}}{10^7} = 24 \text{ ps}$$

The collector capacitance charging time is

$$\tau_c = r_c\,(C_\mu + C_s) = (20)(0.2 \times 10^{-12}) = 4 \text{ ps}$$

The total emitter-to-collector time delay is then

$$\tau_{ec} = 25.9 + 50 + 24 + 4 = 103.9 \text{ ps}$$

so that the cutoff frequency is calculated as

$$f_T = \frac{1}{2\pi\,\tau_{ec}} = \frac{1}{2\pi\,(103.9 \times 10^{-12})} = 1.53 \text{ GHz}$$

If we assume a low-frequency common-emitter current gain of $\beta = 100$, then the beta cutoff frequency is

$$f_\beta = \frac{f_T}{\beta_0} = \frac{1.53 \times 10^9}{100} = 15.3 \text{ MHz}$$

■ Comment

The design of high-frequency transistors requires small device geometries in order to reduce capacitances, and narrow base widths in order to reduce the base transit time.

■ EXERCISE PROBLEM

Ex 12.14 Consider a bipolar transistor with the same parameters as described in Example 12.14 except that $I_E = 50\ \mu$A, $C_{je} = 0.40$ pF, and $C_\mu = 0.05$ pF. Determine the emitter-to-collector transit time, the cutoff frequency, and the beta cutoff frequency.

(Ans. $\tau_{ec} = 282.2$ ps, $f_T = 564$ MHz, $f_\beta = 5.64$ MHz)

12.7 | LARGE-SIGNAL SWITCHING

Switching a transistor from one state to another is strongly related to the frequency characteristics just discussed. However, switching is considered to be a large-signal change, whereas the frequency effects assumed only small changes in the magnitude of the signal.

12.7.1 Switching Characteristics

Consider an npn transistor in the circuit shown in Figure 12.43a switching from cutoff to saturation, and then switching back from saturation to cutoff. We describe the physical processes taking place in the transistor during the switching cycle.

Consider, initially, the case of switching from cutoff to saturation. Assume that in cutoff $V_{BE} \approx V_{BB} < 0$, thus the B–E junction is reverse biased. At $t = 0$, assume that V_{BB} switches to a value of V_{BB0} as shown in Figure 12.43b. We assume that V_{BB0} is sufficiently positive to eventually drive the transistor into saturation. For $0 \le t \le t_1$, the base current supplies charge to bring the B–E junction from reverse bias to a slight forward bias. The space charge width of the B–E junction is narrowing, and ionized donors and acceptors are being neutralized. A small amount of charge is also

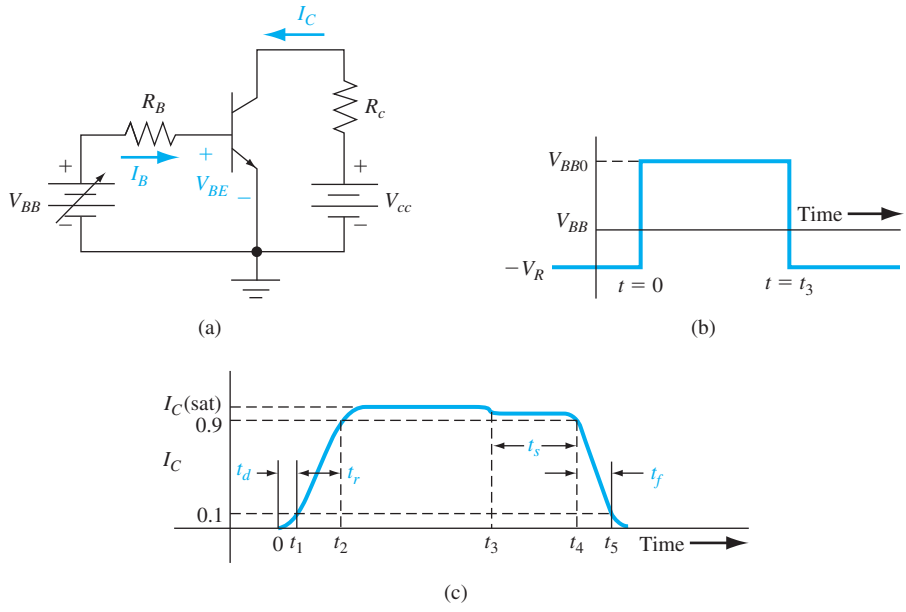

Figure 12.43 | (a) Circuit used for transistor switching. (b) Input base drive for transistor switching. (c) Collector current versus time during transistor switching.

injected into the base during this time. The collector current increases from zero to 10 percent of its final value during this time period, referred to as the delay time.

During the next time period, $t_1 \leq t \leq t_2$, the base current is supplying charge, which increases the B–E junction voltage from near cutoff to near saturation. During this time, additional carriers are being injected into the base so that the gradient of the minority carrier electron concentration in the base increases, causing the collector current to increase. We refer to this time period as the rise time, during which the collector current increases from 10 to 90 percent of the final value. For $t > t_2$, the base drive continues to supply base current, driving the transistor into saturation and establishing the final minority carrier distribution in the device.

The switching of the transistor from saturation to cutoff involves removing all of the excess minority carriers stored in the emitter, base, and collector regions. Figure 12.44 shows the charge storage in the base and collector when the transistor is in saturation. The charge Q_B is the excess charge stored in a forward-active transistor, and Q_{BX} and Q_C are the extra charges stored when the transistor is biased in saturation. At $t = t_3$, the base voltage V_{BB} switches to a negative value of $(-V_R)$. The base current in the transistor reverses direction as was the case in switching a pn junction diode from forward to reverse bias. The reverse base current pulls the excess stored carriers from the emitter and base regions. Initially, the collector current does not change significantly, since the gradient of the minority carrier concentration in the base does not