

### **Datasheet**

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#### 1. Introduction

ILI9325C is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes RAM for graphic data of 240RGBx320 dots, and power supply circuit.

ILI9325C has five kinds of system interfaces which are i80-system MPU interface (8-/9-/16-/18-bit bus width), VSYNC interface (system interface + VSYNC, internal clock, DB[17:0]), serial data transfer interface (SPI), RGB 6-/16-/18-bit interface (DOTCLK, VSYNC, HSYNC, ENABLE, DB[17:0]).

In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write function and widow address function enables to display a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to transfer display the refresh data only to minimize data transfers and power consumption.

ILI9325C can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9325C also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9325C an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, PDA and PMP where long battery life is a major concern.

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#### 2. Features

- Single chip solution for a liquid crystal QVGA TFT LCD display
- 240RGBx320-dot resolution capable with real 262,144 display color
- Support MVA (Multi-domain Vertical Alignment) wide view display
- Incorporate 720-channel source driver and 320-channel gate driver
- Internal 172,800 bytes graphic RAM
- CABC (Content Adaptive Brightness Control)
- System interfaces
  - > i80 system interface with 8-/ 9-/16-/18-bit bus width
  - Serial Peripheral Interface (SPI)
  - > RGB interface with 6-/16-/18-bit bus width (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
  - VSYNC interface (System interface + VSYNC)
- Internal oscillator and hardware reset
- Reversible source/gate driver shift direction
- Window address function to specify a rectangular area for internal GRAM access
- Bit operation function for facilitating graphics data processing
  - Bit-unit write data mask function
  - Pixel-unit logical/conditional write function
- Abundant functions for color display control
  - γ-correction function enabling display in 262,144 colors
  - Line-unit vertical scrolling function
- Partial drive function, enabling partially driving an LCD panel at positions specified by user
- Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- Power saving functions
  - > 8-color mode
  - > standby mode
  - > sleep mode
- Low -power consumption architecture
  - Low operating power supplies:
    - IOVcc = 1.65V ~ 3.3 V (interface I/O)
    - VCI = 2.5V ~ 3.3 V (analog)
- LCD Voltage drive:
  - Source/VCOM power supply voltage
    - DDVDH GND = 4.5V ~ 6.0
    - VCL GND = -2.0V ~ -3.0V
    - $VCI VCL \le 6.0V$
  - Gate driver output voltage
    - VGH GND = 10V ~ 20V
    - VGL GND = -5V ~ -15V





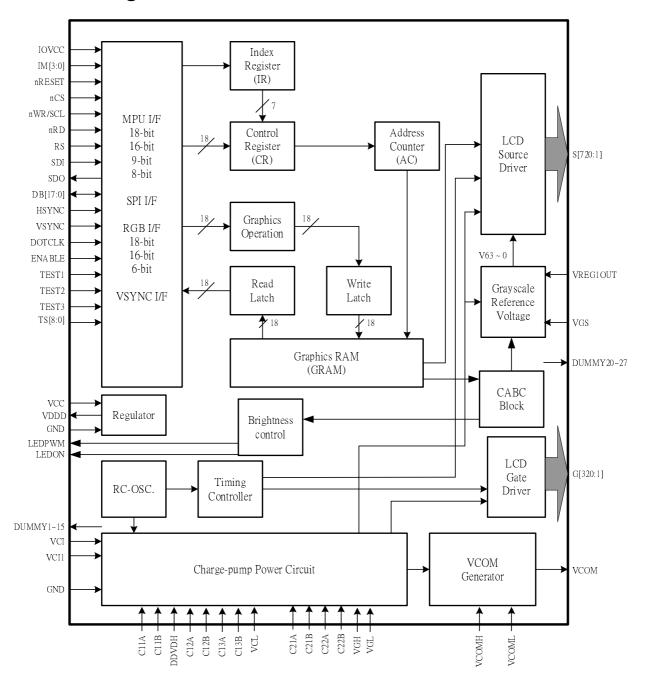
- VGH VGL ≤ 30V
- > VCOM driver output voltage
  - VCOMH = (VCI+0.2)V ~ (DDVDH-0.2)V
  - VCOML = (VCL+0.2)V ~ 0V
  - VCOMH-VCOML  $\leq 6.0$ V
- a-TFT LCD storage capacitor: Cst only

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#### 3. Block Diagram



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### 4. Pin Descriptions

Name	Descriptions Input Interface												
IM3   M2   M1   M0   MPU-Interface Mode   DB Pin in use   0 0 0 0   Setting invalid   0 0 0 1   Setting invalid   0 0 1 1 1   Setting invalid   0 0 1 1 1   Setting invalid   1 0 0 0   Setting invalid   1 0 0 1   Setting invalid   2 Nent the serial peripheral interface   DB[17:0]   3 Nent the serial peripheral interface   DB[17:0]   1 1 1 * Setting invalid   3 Setting invalid   4 Chip select signal.   3 Low: the ILI9325C is selected and accessible   4 High: the ILI9325C is not selected and not accessible   5 Fix to the GND level when not in use.   5 A register select a control register   6 Fix to either IOVcc or GND level when not in use.   5 A write strobe signal and enables an operation to write data whe signal is low.   6 Fix to either IOVcc or GND level when not in use.													
IM3, IM2, IM0/ID													
IM3, IM2, IM0/ID	se												
IM3, IM2, IM1, IM0/ID  I IOVcc IM1, IM0/ID  I I I I I I I I I I I I I I I I I I													
IM3, IM2, IM1, IM0/ID  I IOVcc  I I I IOVcc  I I I I I I I I I I I I I I I I I I													
IM3, IM2, IM1, IM0/ID  I IOVcc  I I I I I IOVcc  I I I I I I I I I I I I I I I I I I	8:1]												
IM3, IM2, IM1, IM0/ID  I IOVcc    0													
IM2, IM1, IM0/ID  I IOVcc  O 1 1 0 0 9-bit 3 wires Serial Peripheral Interface O 1 1 1 0 8-bit 4 wires Serial Peripheral Interface O 1 1 1 1 8-bit 4 wires Serial Peripheral Interface O 1 1 1 1 8-bit 4 wires Serial Peripheral Interface I O 0 0 0 Setting invalid O 0 1 Setting invalid O 1 0 1 Setting invalid O 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1													
IMO/ID    O													
nCS  I MPU IOVcc  I MPU IOVcc  I MPU IOVcc  A register select signal.  Low: the GND level when not in use.  A register select a control register Fix to either IOVcc or GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  MPU Fix to either IOVcc or GND level when not in use.	3, RS												
nCS  I  MPU IOVCC  IO													
nCS  I  MPU IOVCC High: the ILI9325C is selected and accessible Fix to the GND level when not in use.  A chips select a control register Fix to either IOVcc or GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  MPU IOVCC  MPU IO													
nCS  I  MPU IOVcc High: the GND level when not in use.  A register select a control register Fix to either IOVcc or GND level when not in use.  MPU IOVCC  MPU IOVCC High: strobe signal.  A register select and not accessible fix to the GND level when not in use.  A register select an index or status register High: select a control register Fix to either IOVcc or GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  Fix to either IOVcc or GND level when not in use.													
When the serial peripheral interface is selected, IM0 pin is for the device code ID setting.  A chip select signal.  Low: the ILI9325C is selected and accessible High: the ILI9325C is not selected and not accessible Fix to the GND level when not in use.  A register select signal.  Low: select an index or status register High: select a control register Fix to either IOVcc or GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  MPU  MPU  Fix to either IOVcc or GND level when not in use.  MPU  Fix to either IOVcc or GND level when not in use.													
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nCS  I MPU Low: the ILI9325C is selected and accessible High: the ILI9325C is not selected and not accessible Fix to the GND level when not in use.  A register select signal. Low: select an index or status register High: select a control register Fix to either IOVcc or GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  NPU Fix to either IOVcc or GND level when not in use.													
RS  I OVcc High: the ILI9325C is not selected and not accessible Fix to the GND level when not in use.  A register select signal. Low: select an index or status register High: select a control register Fix to either IOVcc or GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  MPU Fix to either IOVcc or GND level when not in use.													
RS  I  MPU IOVcc  High: select a control register Fix to either IOVcc or GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  MPU INVE/SCI  MPU Fix to the GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  Fix to either IOVcc or GND level when not in use.	High: the ILI9325C is not selected and not accessible												
RS  I MPU Low: select an index or status register High: select a control register Fix to either IOVcc or GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  MPU Fix to either IOVcc or GND level when not in use.													
High: select a control register Fix to either IOVcc or GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  MPU Fix to either IOVcc or GND level when not in use.	A register select signal.												
Fix to either IOVcc or GND level when not in use.  A write strobe signal and enables an operation to write data whe signal is low.  MPU Fix to either IOVcc or GND level when not in use.													
A write strobe signal and enables an operation to write data whe signal is low.  NPU Fix to either IOVcc or GND level when not in use.													
signal is low.  NPU Fix to either IOVcc or GND level when not in use.													
InWB/SCI III													
IOVcc SPI Mode:	SPI Mode:												
	SPI Mode: Synchronizing clock signal in SPI mode.												
MPU A read strobe signal and enables an operation to read out data	when												
nRD I NPO the signal is low.													
Fix to either IOVcc or GND level when not in use.													
nRESET I MPU Initializes the ILI9325B with a low input. Be sure to exec	ute a												
IOVcc   Initializes the ici93236 with a low input. Be sure to exect power-on reset after supplying power.	ui <del>c</del> a												
SPI interface input pin.													
The data is latched on the rising edge of the SCL signal.													
SDI / SDA I/O IOVcc In the 8/9-bit serial peripheral interface, this pin is used as													
bi-directional data pin.													
SPI interface output pin.													
SDO MPU The data is outputted on the falling edge of the SCL signal.													
IOVCC													
Let SDO as floating when not used.  MPU An 18-bit parallel bi-directional data bus for MPU system inte	rface												
DB[17:0] I/O NPO   An 18-bit parallel bi-directional data bus for MPO system inte	nace												

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Pin Name	I/O	Туре	Descriptions
Till Hallic	1/0	Турс	8-bit I/F: DB[17:10] is used.
			9-bit I/F: DB[17:9] is used.
			16-bit I/F: DB[17:10] and DB[8:1] is used.
			18-bit I/F: DB[17:0] is used.
			[ 1]
			18-bit parallel bi-directional data bus for RGB interface operation
			6-bit RGB I/F: DB[17:12] are used.
			16-bit RGB I/F: DB[17:13] and DB[11:1] are used.
			18-bit RGB I/F: DB[17:0] are used.
			Unused pins must be fixed to GND level.
			Data ENEABLE signal for RGB interface operation.
			Low: Select (access enabled)
ENABLE	l i	MPU	High: Not select (access inhibited)
		IOVcc	The EPL bit inverts the polarity of the ENABLE signal.
			Fix to either IOVac or CND level when not in use
			Fix to either IOVcc or GND level when not in use.  Dot clock signal for RGB interface operation.
		MPU	DPL = "0": Input data on the rising edge of DOTCLK
DOTCLK	I	IOVcc	DPL = 0 : Input data on the rising edge of DOTCLK  DPL = "1": Input data on the falling edge of DOTCLK
		10 400	Fix to the GND level when not in use
			Frame synchronizing signal for RGB interface operation.
		MPU	VSPL = "0": Active low.
VSYNC	I	IOVcc	VSPL = "1": Active high.
		10 700	Fix to the GND level when not in use.
			Line synchronizing signal for RGB interface operation.
		MPU	HSPL = "0": Active low.
HSYNC	I	IOVcc	HSPL = "1": Active high.
			Fix to the GND level when not in use
		MDII	Output a frame head pulse signal.
FMARK	0	MPU	The FMARK signal is used when writing RAM data in
		IOVcc	synchronization with frame. Leave the pin open when not in use.
LEDPWM/	0	VCI	PWM signal output to control LED driver for LED brightness
TESTO1	O	VOI	dimming.
			This pin is connected to external LED driver.
LEDON/		VOL	
TESTO2	0	VCI	It's a LED driver control pin which is used for turning ON/OFF of LED
			backlight.
	<u>L</u>	<u> </u>	LCD Driving signals
			Source output voltage signals applied to liquid crystal.
			To change the shift direction of signal outputs, use the SS bit.
0700 04		1.00	SS = "0", the data in the RAM address "h00000" is output from S1.
S720~S1	0	LCD	SS = "1", the data in the RAM address "h00000" is output from
			S720. S1, S4, S7, display red (R), S2, S5, S8, display green
			(G), and S3, S6, S9, display blue (B) (SS = 0).
			Gate line output signals.
G320~G1	0	LCD	VGH: the level selecting gate lines
			VGL: the level not selecting gate lines
		TFT	A supply voltage to the common electrode of TFT panel.
VCOM	0	common	VCOM is AC voltage alternating signal between the VCOMH and
		electrode	VCOML levels.
VCOMH	0	Stabilizing	The high level of VCOM AC voltage.
	_	capacitor	ŭ ŭ
VCOML	0	Stabilizing	The low level of VCOM AC voltage. Adjust the VCOML level with
		capacitor	the VDV bits.
VGS	l	GND or	Reference level for the grayscale voltage generating circuit. The

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Pin Name	I/O	Туре	Descriptions
riii Naine	1/0	external	VGS level can be changed by connecting to an external resistor.
		resistor	vao lever can be changed by connecting to an external resistor.
			arge-pump and Regulator Circuit
Mai		Power	A supply voltage to the analog circuit. Connect to an external
Vci	l	supply	power supply of 2.5 ~ 3.3V.
GND	I	Power supply	GND for the analog side: GND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
Vci1	0		An internal reference voltage for the step-up circuit1.  The amplitude between Vci and GND is determined by the VC[2:0] bits.  Make sure to set the Vci1 voltage so that the DDVDH, VGH and VGL voltages are set within the respective specification.
DDVDH	0	Stabilizing capacitor	Power supply for the source driver and Vcom drive.
VGH	0	Stabilizing capacitor	Power supply for the gate driver.
VGL	0	Stabilizing capacitor	Power supply for the gate driver.
VCL	0	Stabilizing capacitor	VcomL driver power supply.  VCL = 0.5 ~ -VCI . Place a stabilizing capacitor between GND
C11+, C11-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.
C13+, C13- C21+, C21- C22+, C22-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.
VREG1OUT	I/O	Stabilizing capacitor	Output voltage generated from the reference voltage.  The voltage level is set with the VRH bits.  VREG1OUT is (1) a source driver grayscale reference voltage, (2)  VcomH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH – 0.2)V.
			Power Pads
IOVcc	I	Power supply	A supply voltage to the interface pins: IM[3:0], nRESET, nCS, nWR, nRD, RS, DB[17:0], VSYNC, HSYNC, DOTCLK, ENABLE, SCL, SDI, SDO. IOVcc = 1.65 ~ 3.3V and Vcc ≧ IOVcc. In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent noise.
VDDD	0	Power	Digital circuit power pad. Connect these pins with the 1uF capacitor.
GND	I	Power supply	GND = 0V.
			Test Pads
DUMMY3~ 15 DUMMY20 ~ 27	-	-	Dummy pad. Leave these pins as open.
IOGNDDUM	0	GND	GND pin.
TESTO1~16	0	Open	Test pins. Leave them open.
TEST1, 2, 3	I	IOGND	Test pins (internal pull low).  Connect to GND or leave these pins as open.
TS0~8	I	OPEN	Test pins (internal pull low). Leave them open.
TSO	0	OPEN	Test output pin. Let it open
TEST_EN	I	OPEN	Test pins Enable (internal pull low). Leave them open.





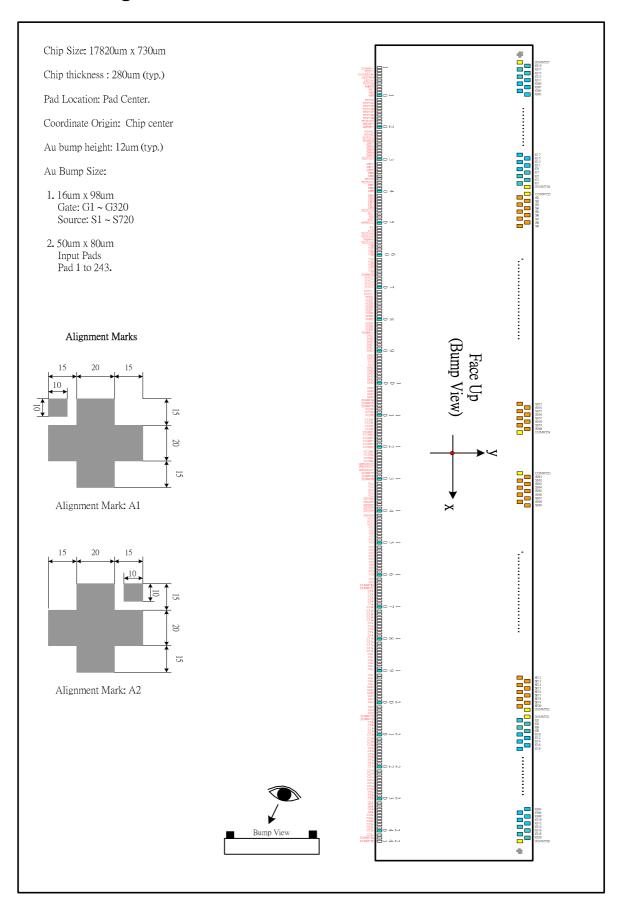
#### Liquid crystal power supply specifications Table 1

No.	Item	l	Description								
1	TFT Source Driver		720 pins (240 x RGB)								
2	TFT Gate Driver		320 pins								
3	TFT Display's Capacitor Structu	ire	Cst structure only (Common VCOM)								
		S1 ~ S720	V0 ~ V63 grayscales								
4	Liquid Crystal Drive Output	G1 ~ G320	VGH - VGL								
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes								
5	Inner A Vallage	IOVcc	1.65 ~ 3.30V								
5	Input Voltage	VCI	2.50 ~ 3.30V								
		DDVDH	4.5V ~ 6.0V								
		VGH	10V ~ 20V								
^	Lieurid Courtel Drive Veltages	VGL	-5V ~ -15V								
6	Liquid Crystal Drive Voltages	VCL	-1.9V ~ -3.0V								
		VGH - VGL	Max. 30V								
		VCI - VCL	Max. 6.0V								
		DDVDH	VCI1 x2								
7	Internal Step on Givenite	VGH	VCI1 x4, x5, x6								
1	Internal Step-up Circuits	VGL	VCI1 x-3, x-4, x-5								
		VCL	VCI1 x-1								





### 5. Pad Arrangement and Coordination





# **ILI9325C**

No.	Name	Х	Υ	No.	Name	Х	Υ	No.	Name	Х	Υ	No.	Name	Χ	Υ	No.	Name	Х	Υ
1	TEST_EN	-8610	-252	61	TS4	-4130	-252	121	VCOML	70	-252	181	C11+	4270	-252	241	C22+	8470	-252
2	TEST1	-8540	-252	62	TS3	-4060	-252	122	VCOML	140	-252	182	C11+	4340	-252	242	DUMMY14	8540	-252
3	IOGNDDUM	-8470	-252	63	TS2	-3990	-252	123	VCOML	210	-252	183	C11+	4410	-252	243	DUMMY15	8610	-252
4	LEDPWM / TESTO1	-8400	-252	64	TS1	-3920	-252	124	VCOML	280	-252	184	C11+	4480	-252	244	DUMMY20	8659	148
5	LEDON / TESTO2	-8330	-252	65	TS0	-3850	-252	125	VREG10UT	350	-252	185	VGL	4550	-252	245	G320	8643	265
6	TESTO3	-8260	-252	66	TSO	-3780	-252	126	VREG10UT	420	-252	186	VGL	4620	-252	246	G318	8627	148
7	IM0/ID	-8190	-252	67	IOVCC	-3710	-252	127	VREG10UT	490	-252	187	VGL	4690	-252	247	G316	8611	265
8	IM1	-8120	-252	68	IOVCC	-3640	-252	128	DUMMY7	560	-252	188	VGL	4760	-252	248	G314	8595	148
9	IM2	-8050	-252	69	IOVCC	-3570	-252	129	DUMMY8	630	-252	189	VGL	4830	-252	249	G312	8579	265
10	IM3	-7980	-252	70	IOVCC	-3500	-252	130	DUMMY9	700	-252	190	VGL	4900	-252	250	G310	8563	148
11	TEST2	-7910	-252	71	IOVCC	-3430	-252	131	VCL	770	-252	191	VGL	4970	-252	251	G308	8547	265
12	TESTO4	-7840	-252	72	IOVCC	-3360	-252	132	VCL	840	-252	192	VGL	5040	-252	252	G306	8531	148
13	TESTO5	-7770	-252	73	VDDD	-3290	-252	133	VCL	910	-252	193	VGL	5110	-252	253	G304	8515	265
14	TESTO6	-7700	-252	74	VDDD	-3220	-252	134	VCL	980	-252	194	VGL	5180	-252	254	G302	8499	148
15	TESTO7	-7630	-252	75	VDDD	-3150	-252	135	VCL	1050	-252	195	GND	5250	-252	255	G300	8483	265
16	TESTO8	-7560	-252	76	VDDD	-3080	-252	136	DDVDH	1120	-252	196	GND	5320	-252	256	G298	8467	148
17	TESTO9	-7490	-252	77	VDDD	-3010	-252	137	DDVDH	1190	-252	197	GND	5390	-252	257	G296	8451	265
18	TESTO10	-7420	-252	78	VDDD	-2940	-252	138	DDVDH	1260	-252	198	VGH	5460	-252	258	G294	8435	148
19	nRESET	-7350	-252	79	VDDD	-2870	-252	139	DDVDH	1330	-252	199	VGH	5530	-252	259	G292	8419	265
20	nRESET	-7280	-252	80	VDDD	-2800	-252	140		1400	-252	200	VGH	5600	-252	260	G290	8403	148
21	VSYNC	-7210	-252	81	VDDD	-2730	-252	141	DDVDH	1470	-252	201	VGH	5670	-252	261	G288	8387	265
22	HSYNC	-7140	-252	82	VDDD	-2660	-252	142		1540	-252	202	VGH	5740	-252	262	G286	8371	148
23	DOTCLK	-7070	-252	83	VDDD	-2590	-252	143	VCI1	1610	-252	203	VGH	5810	-252	263	G284	8355	265
24	ENABLE	-7000	-252	84	DUMMY3	-2520	-252	144	VCI1	1680	-252	204	DUMMY12	5880	-252	264	G282	8339	148
25	DB17	-6905	-252	85	GND	-2450	-252	145	VCI	1750	-252	205	DUMMY13	5950	-252	265	G280	8323	265
26	DB16	-6825	-252	86	GND	-2380	-252	146		1820	-252	206	C13-	6020	-252	266	G278	8307	148
27	DB15	-6745	-252	87	GND	-2310	-252	147		1890	-252	207	C13-	6090	-252	267	G276	8291	265
28	DB14	-6665	-252	88	GND	-2240	-252	148		1960	-252	208	C13-	6160	-252	268	G274	8275	148
29	DB13	-6585	-252	89	GND	-2170	-252	149		2030	-252	209	C13-	6230	-252	269	G272	8259	265
30	TESTO11	-6495	-252	90	GND	-2100	-252	150		2100	-252	210	C13+	6300	-252	270	G270	8243	148
31	DB12	-6405	-252	91	GND	-2030	-252	151	VCI	2170	-252	211	C13+	6370	-252	271	G268	8227	265
32	DB11	-6325	-252	92	GND	-1960	-252	152		2240	-252	212	C13+	6440	-252	272	G266	8211	148
33	DB10	-6245	-252	93	VGS	-1890	-252	153		2310	-252	213	C13+	6510	-252	273	G264	8195	265
34	DB9	-6165	-252	94	VGS	-1820	-252	154		2380	-252	214	C21-	6580	-252	274	G262	8179	148
35	DB8	-6085	-252	95	GND	-1750	-252	155		2450	-252 -252	215	C21-	6650	-252	275	G260	8163	265
36 37	TEST3 TESTO12	-5990 -5920	-252 -252	96 97	GND GND	-1680 -1610	-252 -252	156 157	VCI	2520 2590	-252	216 217	C21-	6720 6790	-252 -252	276 277	G258 G256	8147 8131	148 265
38	DB7	-5825	-252	98	GND	-1540	-252	158		2660	-252	218	C21-	6860	-252	278	G254	8115	148
39	DB6	-5745	-252	99	GND	-1470	-252	159		2730	-252	219	C21-	6930	-252	279	G252	8099	265
40	DB5	-5665	-252	100	GND	-1400	-252	160		2800	-252	220	C21-	7000	-252	280	G250	8083	148
41	DB4	-5585	-252	101	GND	-1330	-252	161		2870	-252	221	C21+	7070		281	G248	8067	265
42	DB3	-5505	-252	102	GND	-1260	-252	162		2940	-252	222	C21+	7140	-252	282	G246	8051	148
43	DB2	-5425	-252	103	GND	-1190	-252		DUMMY10	3010	-252	223	C21+	7210		283	G244	8035	265
44	DB1	-5345	-252	104	GND	-1120	-252	164		3080	-252	224	C21+	7280	-252	284	G242	8019	148
45	DB0	-5265	-252	105	DUMMY4	-1050	-252	165		3150	-252	225	C21+	7350	-252	285	G240	8003	265
46	TESTO13	-5180	-252	106	DUMMY5	-980	-252	166		3220	-252	226	C21+	7420	-252	286	G238	7987	148
47	SDO	-5110	-252	107	DUMMY6	-910	-252	167		3290	-252	227	C21+	7490	-252	287	G236	7971	265
48	SDI	-5040	-252	108	VCOM	-840	-252	168		3360	-252	228	C22-	7560	-252	288	G234	7955	148
49	nRD	-4970	-252	109	VCOM	-770	-252	169		3430	-252	229	C22-	7630	-252	289	G232	7939	265
50	nWR/SCL	-4900	-252	110	VCOM	-700	-252	170	C12+	3500	-252	230	C22-	7700	-252	290	G230	7923	148
51	RS	-4830	-252	111	VCOM	-630	-252	171	C12+	3570	-252	231	C22-	7770	-252	291	G228	7907	265
52	nCS	-4760	-252	112	VCOM	-560	-252	172	C12+	3640	-252	232	C22-	7840	-252	292	G226	7891	148
53	TESTO14	-4690	-252	113	VCOM	-490	-252	173	C12+	3710	-252	233	C22-	7910	-252	293	G224	7875	265
54	TESTO15	-4620	-252	114	VCOM	-420	-252	174	C12+	3780	-252	234	C22-	7980	-252	294	G222	7859	148
55	FMARK	-4550	-252	115	VCOMH	-350	-252	175	C11-	3850	-252	235	C22+	8050	-252	295	G220	7843	265
56	TESTO16	-4480	-252	116	VCOMH	-280	-252	176	C11-	3920	-252	236	C22+	8120	-252	296	G218	7827	148
57	TS8	-4410	-252	117	VCOMH	-210	-252	177	C11-	3990	-252	237	C22+	8190	-252	297	G216	7811	265
58	TS7	-4340	-252	118	VCOMH	-140	-252	178	C11-	4060	-252	238	C22+	8260	-252	298	G214	7795	148
59	TS6	-4270	-252	119	VCOMH	-70	-252	179	C11-	4130	-252	239	C22+	8330	-252	299	G212	7779	265
60	TS5	-4200	-252	120	VCOMH	0	-252	180	C11+	4200	-252	240	C22+	8400	-252	300	G210	7763	148





No.	Name	х	Υ	No.	Name	х	Υ	No.	Name	х	Υ	No.	Name	х	Υ	No.	Name	х	Υ
301	G208	7747	265	361	G88	6787	265	421	S706	5807	148	481	S646	4847	148	541	S586	3887	148
302	G206	7731	148	362	G86	6771	148	422	S705	5791	265	482	S645	4831	265	542	S585	3871	265
303	G204	7715	265	363	G84	6755	265	423	S704	5775	148	483	S644	4815	148	543	S584	3855	148
304	G202	7699	148	364	G82	6739	148	424	S703	5759	265	484	S643	4799	265	544	S583	3839	265
305	G200	7683	265	365	G80	6723	265	425	S702	5743	148	485	S642	4783	148	545	S582	3823	148
306	G198	7667	148	366	G78	6707	148	426	S701	5727	265	486	S641	4767	265	546	S581	3807	265
307	G196	7651	265	367	G76	6691	265	427	S700	5711	148	487	S640	4751	148	547	S580	3791	148
308	G194	7635	148	368	G74	6675	148	428	S699	5695	265	488	S639	4735	265	548	S579	3775	265
309	G192	7619	265	369	G72	6659	265	429	S698	5679	148	489	S638	4719	148	549	S578	3759	148
310	G190	7603	148	370	G70	6643	148	430	S697	5663	265	490	S637	4703	265	550	S577	3743	265
311	G188	7587	265	371	G68	6627	265	431	S696	5647	148	491	S636	4687	148	551	S576	3727	148
312	G186	7571	148	372	G66	6611	148	432	S695	5631	265	492	S635	4671	265	552	S575	3711	265
313	G184	7555	265	373	G64	6595	265	433	S694	5615	148	493	S634	4655	148	553	S574	3695	148
314	G182	7539	148	374	G62	6579	148	434	S693	5599	265	494	S633	4639	265	554	S573	3679	265
315	G180	7523	265	375	G60	6563	265	435	S692	5583	148	495	S632	4623	148	555	S572	3663	148
316	G178	7507	148	376	G58	6547	148	436	S691	5567	265	496	S631	4607	265	556	S571	3647	265
317	G176	7491	265	377	G56	6531	265	437	S690	5551	148	497	S630	4591	148	557	S570	3631	148
318	G174	7475	148	378	G54	6515	148	438	S689	5535	265	498	S629	4575	265	558	S569	3615	265
319	G172	7459	265	379	G52	6499	265	439	S688	5519	148	499	S628	4559	148	559	S568	3599	148
320	G170	7443	148	380	G50	6483	148	440	S687	5503	265	500	S627	4543	265	560	S567	3583	265
321	G168	7427	265	381	G48	6467	265	441	S686	5487	148	501	S626	4527	148	561	S566	3567	148
322	G166 G164	7411 7395	148 265	382	G46 G44	6451 6435	148 265	442	S685 S684	5471	265 148	502	S625 S624	4511 4495	265 148	562 563	S565 S564	3551 3535	265 148
324	G162	7379	148	384	G42	6419	148	444	S683	5455 5439	265	504	S623	4495	265	564	S563	3519	265
325	G160	7363	265	385	G42	6403	265	445	S682	5423	148	505	S622	4463	148	565	S562	3503	148
326	G158	7347	148	386	G38	6387	148	446	S681	5407	265	506	S621	4447	265	566	S561	3487	265
327	G156	7331	265	387	G36	6371	265	447	S680	5391	148	507	S620	4431	148	567	S560	3471	148
328	G154	7315	148	388	G34	6355	148	448	S679	5375	265	508	S619	4415	265	568	S559	3455	265
329	G152	7299	265	389	G32	6339	265	449	S678	5359	148	509	S618	4399	148	569	S558	3439	148
330	G150	7283	148	390	G30	6323	148	450	S677	5343	265	510	S617	4383	265	570	S557	3423	265
331	G148	7267	265	391	G28	6307	265	451	S676	5327	148	511	S616	4367	148	571	S556	3407	148
332	G146	7251	148	392	G26	6291	148	452	S675	5311	265	512	S615	4351	265	572	S555	3391	265
333	G144	7235	265	393	G24	6275	265	453	S674	5295	148	513	S614	4335	148	573	S554	3375	148
334	G142	7219	148	394	G22	6259	148	454	S673	5279	265	514	S613	4319	265	574	S553	3359	265
335	G140	7203	265	395	G20	6243	265	455	S672	5263	148	515	S612	4303	148	575	S552	3343	148
336	G138	7187	148	396	G18	6227	148	456	S671	5247	265	516	S611	4287	265	576	S551	3327	265
337	G136	7171	265	397	G16	6211	265	457	S670	5231	148	517	S610	4271	148	577	S550	3311	148
338	G134	7155	148	398	G14	6195	148	458	S669	5215	265	518	S609	4255	265	578	S549	3295	265
339	G132	7139	265	399	G12	6179	265	459	S668	5199	148	519	S608	4239	148	579	S548	3279	148
340	G130	7123	148	400	G10	6163	148	460	S667	5183	265	520	S607	4223	265	580	S547	3263	265
341	G128	7107	265	401	G8	6147	265	461	S666	5167	148	521	S606	4207	148	581	S546	3247	148
342	G126 G124	7091 7075	148 265	402	G6 G4	6131	148 265	462	S665 S664	5151 5135	265 148	522 523	S605 S604	4191 4175	265 148	582 583	S545 S544	3231 3215	265 148
343	G122	7075	148	404	G2	6099	148	464	S663	5119	265	523	S603	4175	265	584	S544 S543	3199	265
345	G120	7043	265	405	DUMMY21	6083	265	465	S662	5103	148	525	S602	4143	148	585	S542	3183	148
346	G118	7027	148	406	DUMMY22	6047	265	466	S661	5087	265	526	S601	4127	265	586	S541	3167	265
347	G116	7011	265	407	S720	6031	148	467	S660	5071	148	527	S600	4111	148	587	S540	3151	148
348	G114	6995	148	408	S719	6015	265	468	S659	5055	265	528	S599	4095	265	588	S539	3135	265
349	G112	6979	265	409	S718	5999	148	469	S658	5039	148	529	S598	4079	148	589	S538	3119	148
350	G110	6963	148	410	S717	5983	265	470	S657	5023	265	530	S597	4063	265	590	S537	3103	265
351	G108	6947	265	411	S716	5967	148	471	S656	5007	148	531	S596	4047	148	591	S536	3087	148
352	G106	6931	148	412	S715	5951	265	472	S655	4991	265	532	S595	4031	265	592	S535	3071	265
353	G104	6915	265	413	S714	5935	148	473	S654	4975	148	533	S594	4015	148	593	S534	3055	148
354	G102	6899	148	414	S713	5919	265	474	S653	4959	265	534	S593	3999	265	594	S533	3039	265
355	G100	6883	265	415	S712	5903	148	475	S652	4943	148	535	S592	3983	148	595	S532	3023	148
356	G98	6867	148	416	S711	5887	265	476	S651	4927	265	536	S591	3967	265	596	S531	3007	265
357	G96	6851	265	417	S710	5871	148	477	S650	4911	148	537	S590	3951	148	597	S530	2991	148
358	G94	6835	148	418	S709	5855	265	478	S649	4895	265	538	S589	3935	265	598	S529	2975	265
359	G92	6819	265	419	S708	5839	148	479	S648	4879	148	539	S588	3919	148	599	S528	2959	148
360	G90	6803	148	420	S707	5823	265	480	S647	4863	265	540	S587	3903	265	600	S527	2943	265





	No.	Name	х	Υ	No.	Name	х	Υ	No.	Name	х	Υ	No.	Name	х	Υ	No.	Name	х	Υ
100   100																				
Mathematical																				
1968   1979																				
10   10   10   10   10   10   10   10																				
1																				
14   15   15   15   17   18   18   18   18   18   18   18	612	S515	2751	265	672	S455	1791	265	732	S395	831	265	792	S337	-655	148	852	S277	-1615	148
915                 512                 2203                 146                 1783                 1581                 2581                 2581                2581                 2581                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                2582                 2582                2582                 2582                2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582                 2582	613	S514	2735	148	673	S454	1775	148	733	S394	815	148	793	S336	-671	265	853	S276	-1631	265
Sept	614	S513	2719	265	674	S453	1759	265	734	S393	799	265	794	S335	-687	148	854	S275	-1647	148
	615	S512	2703	148	675	S452	1743	148	735	S392	783	148	795	S334	-703	265	855	S274	-1663	265
	616	S511	2687	265	676	S451	1727	265	736	S391	767	265	796	S333	-719	148	856	S273	-1679	148
19	617	S510	2671	148	677	S450	1711	148	737	S390	751	148	797	S332	-735	265	857	S272	-1695	265
Sept	618	S509	2655	265	678	S449	1695	265	738	S389	735	265	798	S331	-751	148	858	S271	-1711	148
Sept	619	S508	2639	148	679	S448	1679	148	739	S388	719	148	799	S330	-767	265	859	S270	-1727	265
Second   S	620	S507	2623	265	680	S447	1663	265	740	S387	703	265	800	S329	-783	148	860	S269	-1743	148
Sect	621	S506	2607	148	681	S446	1647	148	741	S386	687	148	801	S328	-799	265	861	S268	-1759	265
Sect	622	S505	2591	265	682	S445	1631	265	742	S385	671	265	802	S327	-815	148	862	S267	-1775	148
625         5502         2543         148         685         S442         1583         148         745         S382         623         148         805         S324         -863         265         566         S264         -1823         265           626         5501         2527         2505         686         5841         1551         148         697         140         1551         148         897         540         1551         148         897         540         1551         148         897         540         1551         148         897         540         1551         148         897         540         1505         265         688         8439         1535         265         748         8379         576         265         898         8247         148         898         831         1519         148         749         5378         559         148         900         832         -892         265         869         833         149         148         481         531         848         2447         148         861         843         482         1471         265         482         483         849         2431         486 <td< td=""><td>623</td><td>S504</td><td>2575</td><td>148</td><td>683</td><td>S444</td><td>1615</td><td>148</td><td>743</td><td>S384</td><td>655</td><td>148</td><td>803</td><td>S326</td><td>-831</td><td>265</td><td>863</td><td></td><td>-1791</td><td>265</td></td<>	623	S504	2575	148	683	S444	1615	148	743	S384	655	148	803	S326	-831	265	863		-1791	265
Sec	624	S503	2559	265	684	S443	1599	265	744	S383	639	265	804	S325	-847	148	864	S265	-1807	148
627         S500         2511         148         687         S440         1551         148         747         S380         591         148         807         S322         995         265         867         S262         1488         3379         675         265         868         584         1533         265         748         8379         659         148         809         5230         148         809         5230         8497         2463         265         690         5437         1503         265         750         8377         543         265         810         3319         943         148         870         3258         1903         148           631         5486         2447         148         691         8336         1487         148         751         3376         527         148         811         3317         943         148         873         258         1932         2463         148         752         28375         511         285         812         3317         949         265         696         8431         1407         265         756         3371         449         265         481         331         1007	625	S502	2543	148	685	S442	1583	148	745	S382	623	148	805		-863	265	865	S264	-1823	265
628         8499         2495         265         688         8439         1535         285         748         8379         576         265         808         8321         9911         148         868         S261         148         269         9488         2479         148         689         8431         1519         148         749         3378         559         148         80         3220         927         265         869         2630         1868         868         868         868         868         868         868         868         868         868         868         868         868         869         8260         180         232         265         690         8431         1480         751         8576         8577         151         265         814         9431         148         870         2295         690         8431         1455         148         755         8377         495         148         812         331         969         265         7195         148         872         859         148         8433         1439         265         893         4431         1407         265         8373         466         1487																				
629         S488         2479         148         689         S438         1519         148         749         S378         559         148         809         S320         927         265         860         S260         1887         265           530         5494         2447         148         691         S436         1809         1836         559         180         831         846         691         S436         1471         265         552         188         811         331         346         691         S436         1471         265         552         188         811         331         391         938         148         872         252         1935         148           633         5494         2415         148         693         S431         1455         148         753         3374         496         148         813         3316         991         265         873         3266         1967         148         869         5431         1407         265         558         3372         463         148         815         331         1007         148         872         255         1967         431         148         7																				
630         S497         2463         265         690         S377         1503         265         750         S377         643         265         810         S319         -943         148         870         S259         -1903         148           631         S496         24471         148         691         S436         1487         148         751         S376         527         148         811         S318         -959         265         871         S258         11919         265           633         S494         2415         148         693         S434         1455         148         753         S374         495         148         813         S316         -991         265         873         S256         -1961         1265           635         S492         2383         148         6695         S432         1423         148         755         S372         463         148         15         S314         -1002         265         675         5871         437         448         415         5814         -1007         448         376         S252         -1967         148         637         5430         1391         148 <td></td>																				
631 S496 2447 148 691 S436 1487 148 751 S376 S27 148 811 S318 -959 265 871 S258 -1919 265 632 S495 2431 265 692 S435 1471 265 752 S375 511 265 812 S317 -975 148 872 S257 -1935 148 633 S494 2415 148 693 S434 1455 148 753 S374 495 148 813 S316 -991 265 843 S434 1455 148 754 S373 479 265 814 S315 -1007 148 874 S255 1967 148 835 S492 2333 148 695 S432 1423 148 755 S372 463 148 815 S314 1023 265 875 S254 1983 265 836 S491 2367 265 896 S431 1407 265 756 S371 447 265 816 S314 1023 265 875 S254 1983 265 837 S490 2351 148 697 S430 1391 148 757 S370 431 148 876 S255 265 879 S252 2015 185 838 S488 2319 148 699 S428 1559 148 755 S368 399 148 819 S310 1087 265 879 S250 -2047 265 840 S485 2271 265 700 S427 1343 265 760 S367 383 265 842 S255 148 701 S426 1327 148 761 S366 367 148 821 S310 1087 265 879 S250 -2047 265 842 S485 2271 265 704 S423 1279 56 S368 331 148 821 S309 1101 148 824 S255 148 703 S424 1295 148 761 S364 335 148 821 S309 1101 148 822 S249 2033 148 843 S248 2239 265 704 S423 1279 56 S368 331 148 821 S300 1103 148 882 S247 2095 148 643 S484 2255 148 703 S424 1295 148 761 S366 367 148 821 S300 1109 1265 881 S248 2212 1263 148 765 S362 303 148 821 S300 1109 148 882 S247 2095 148 643 S484 2255 148 705 S422 1263 148 765 S362 303 148 821 S300 1109 148 882 S247 2095 148 643 S482 2223 148 705 S422 1263 148 765 S362 303 148 822 S300 1103 148 888 S244 2111 265 644 S483 2270 265 704 S423 1279 265 764 S363 319 265 826 S300 1103 148 888 S244 2111 265 648 S481 2207 265 704 S423 1279 265 764 S363 319 265 826 S300 1103 148 888 S244 2110 265 846 S481 2207 265 704 S423 1279 265 766 S361 267 S362 S300 1124 148 888 S241 2111 148 645 S482 2223 148 707 S420 1231 148 769 S360 287 265 828 S300 1124 148 888 S241 2111 148 888 S241 2121 148 869 S479 2175 265 766 S361 S477 2131 148 889 S240 2207 265 865 S477 2131 341 348 775 S383 319 265 828 S300 1124 245 865 889 S240 2207 265 865 S477 2131 344 765 S364 3369 399 148 830 S299 1313 148 890 S233 2239 2233 225 865 S477 2131 348 890 S233 2239 2255 348 S300 2297 2255 348 S300 2297 2255 348 S300																				
632         S495         2431         265         692         S435         1471         265         752         S375         511         265         812         S317         -975         148         872         S257         -1935         148           633         S494         2415         148         693         S433         1439         265         694         S433         1439         265         754         S373         479         265         814         S315         -1907         148         875         S255         -1961         148           635         S492         283         148         695         S432         1423         148         755         S372         463         148         5314         1023         265         696         S431         1407         265         756         S371         447         265         816         S313         -1039         148         867         S252         -1993         148         637         S490         2351         148         699         S428         1359         148         759         S368         399         148         817         S312         -1055         265         877         S252 <td></td>																				
633         S494         2415         148         693         S434         1455         148         753         S374         495         148         813         S316         -991         265         873         S256         -1951         265           634         S493         2393         265         696         S432         1423         148         755         S372         463         148         815         S314         -1023         265         675         S65         696         S431         1407         265         666         S371         447         265         816         S313         -1039         148         876         S254         -1983         265           638         S489         2335         265         698         S429         1375         265         758         S369         415         265         818         S311         -1071         148         876         S250         -2015         265           638         S489         2335         265         698         S429         1348         759         S368         399         148         819         S311         -1075         148         699         5428         1327 <td></td>																				
634         S493         2399         265         694         S433         1439         265         754         S373         479         265         814         S315         -1007         148         874         S255         -1967         148           635         S492         2383         148         695         S432         1423         148         755         S372         463         148         165         S314         -1023         265         875         S254         -1983         265           636         S491         2367         265         698         S430         1391         148         697         5490         1391         148         697         5490         1391         148         697         5490         1391         148         759         S368         399         148         819         S310         -1055         265         877         S252         -2015         265         638         5489         2333         265         698         5429         1343         265         758         S369         415         265         818         S311         -1055         265         877         S252         -2047         265      <																				
635         S492         2383         148         695         S432         1423         148         755         S372         463         148         815         S314         -1023         265         876         S254         -1983         265           636         S491         2367         265         696         S430         1391         148         877         S370         431         148         816         S313         -1039         148         876         S253         -1999         148           637         S489         2335         265         698         S429         1375         265         758         S369         415         265         818         S311         -1071         148         878         S250         -2017         265         640         S487         2303         265         700         S427         148         265         700         S427         148         265         700         S427         148         265         381         820         S309         -1103         148         80         S249         -2063         148           641         S485         22271         148         701         S426         1321 <td></td>																				
636         S491         2367         265         696         S431         1407         265         756         S371         447         265         816         S313         -1039         148         876         S253         -1999         148           637         S490         2351         148         697         S420         1391         148         757         S370         431         148         817         S252         -2015         265           638         S488         2335         265         698         S429         1375         265         758         S369         415         265         816         S310         -1071         148         878         5251         -2031         148           640         S487         2303         265         700         S427         148         761         S366         367         148         821         S308         -1103         148         880         5291         -1071         148         861         2287         148         761         S366         367         148         821         S308         -1119         265         881         S248         -2079         265           642																				
638         S489         2335         265         698         S429         1375         265         758         S369         415         265         818         S311         -1071         148         678         S251         -2031         148           639         S488         2319         148         699         S428         1359         148         759         S368         399         148         819         S310         -1087         265         879         S250         -2047         265           640         S487         2303         265         700         S427         1343         265         760         S367         383         265         820         S309         -1103         148         880         S249         -2063         148           641         S486         2287         148         701         S426         1327         148         761         S366         351         265         822         S307         -1135         148         882         S247         -2063         148         645         484         2255         148         763         S364         335         148         822         S305         -1167         148 <td>636</td> <td>S491</td> <td>2367</td> <td>265</td> <td>696</td> <td>S431</td> <td>1407</td> <td>265</td> <td>756</td> <td>S371</td> <td>447</td> <td>265</td> <td>816</td> <td>S313</td> <td>-1039</td> <td>148</td> <td>876</td> <td>S253</td> <td>-1999</td> <td>148</td>	636	S491	2367	265	696	S431	1407	265	756	S371	447	265	816	S313	-1039	148	876	S253	-1999	148
639         S488         2319         148         699         S428         1359         148         759         S368         399         148         819         S310         -1087         265         879         S250         -2047         265           640         S487         2303         265         700         S427         1343         265         760         S367         383         265         820         S309         -1103         148         880         S249         -2063         148           641         S486         22871         148         701         S426         1327         148         762         S365         351         265         822         S307         -1135         148         880         S247         -2095         265           642         S485         2271         265         704         S423         1279         265         762         S365         351         265         822         3307         -1113         265         881         S247         -2095         148           643         S484         2259         148         763         S363         319         265         822         3307         -1167 <td>637</td> <td>S490</td> <td>2351</td> <td>148</td> <td>697</td> <td>S430</td> <td>1391</td> <td>148</td> <td>757</td> <td>S370</td> <td>431</td> <td>148</td> <td>817</td> <td>S312</td> <td>-1055</td> <td>265</td> <td>877</td> <td>S252</td> <td>-2015</td> <td>265</td>	637	S490	2351	148	697	S430	1391	148	757	S370	431	148	817	S312	-1055	265	877	S252	-2015	265
640         S487         2303         265         700         S427         1343         265         760         S367         383         265         820         S309         -1103         148         880         S249         -2063         148           641         S486         2287         148         701         S426         1327         148         761         S366         367         148         821         S308         -1119         265         881         S248         -2079         265           642         S485         2271         265         702         S422         1311         265         762         S365         351         265         822         S307         -1135         148         882         S247         -2095         148           643         S484         2255         148         705         S422         1283         148         765         S362         333         148         823         S306         -1167         148         884         S245         -2127         148           645         S481         2207         265         766         S421         1247         265         366         3361         287	638	S489	2335	265	698	S429	1375	265	758	S369	415	265	818	S311	-1071	148	878	S251	-2031	148
641         S486         2287         148         701         S426         1327         148         761         S366         367         148         821         S308         -1119         265         881         S248         -2079         265           642         S485         2271         265         702         S425         1311         265         762         S365         351         265         822         S307         -1135         148         882         S247         -2095         148           643         S484         2255         148         704         S423         1279         265         764         S363         319         265         824         S305         -1167         148         884         S246         -2117         148           645         S482         2223         148         705         S422         1263         148         765         S362         303         148         825         S304         -1183         265         886         S244         -2177         148         825         S304         -1183         265         885         S244         -2177         148         645         8481         2207         265	639	S488	2319	148	699	S428	1359	148	759	S368	399	148	819	S310	-1087	265	879	S250	-2047	265
642         S485         2271         265         702         S425         1311         265         762         S365         351         265         822         S307         -1135         148         882         S247         -2095         148           643         S484         2255         148         703         S424         1295         148         763         S364         335         148         823         S306         -1151         265         883         S246         -2111         265           644         S483         2239         265         704         S423         1279         265         764         S363         319         265         824         S305         -1167         148         884         S245         -2127         148           645         S482         2223         148         705         S422         1265         766         S361         287         265         826         S303         -1199         148         886         S244         -2113         265           648         S479         2175         265         708         S419         1215         265         766         S361         287         265	640	S487	2303	265	700	S427	1343	265	760	S367	383	265	820	S309	-1103	148	880	S249	-2063	148
643         S484         2255         148         703         S424         1295         148         763         S364         335         148         823         S306         -1151         265         883         S246         -2111         265           644         S483         2239         265         704         S423         1279         265         764         S363         319         265         824         S305         -1167         148         884         S245         -2127         148           645         S482         2223         148         705         S422         1263         148         765         S362         303         148         825         S304         -1183         265         885         S244         -2143         265           646         S481         2207         265         706         S421         1247         265         766         S361         287         265         826         S303         -1183         265         887         S242         -2175         265           648         S479         2175         265         788         S419         1215         265         768         DUMMY24         -271<	641	S486	2287	148	701	S426	1327	148	761	S366	367	148	821	S308	-1119	265	881	S248	-2079	265
644         S483         2239         265         704         S423         1279         265         764         S363         319         265         824         S305         -1167         148         884         S245         -2127         148           645         S482         2223         148         705         S422         1263         148         765         S362         303         148         825         S304         -1183         265         885         S244         -2143         265           646         S481         2207         265         706         S421         1247         265         766         S361         287         265         826         S303         -1199         148         886         S243         -2159         148           647         S480         2191         148         707         S420         1231         148         767         DUMMY23         271         148         827         S302         -1215         265         887         S242         -2175         265           648         S479         2175         265         708         S419         1215         265         770         S350         -287<	642	S485	2271	265	702	S425	1311	265	762	S365	351	265	822	S307	-1135	148	882	S247	-2095	148
645         S482         2223         148         705         S422         1263         148         765         S362         303         148         825         S304         -1183         265         885         S244         -2143         265           646         S481         2207         265         766         S361         287         265         826         S303         -1199         148         886         S243         -2159         148           647         S480         2191         148         707         S420         1231         148         767         DUMMY23         271         148         827         S302         -1215         265         887         S242         -2175         265           648         S479         2175         265         708         S419         1215         265         768         DUMMY24         -271         148         829         S300         -1215         265         887         S242         -2175         265           650         S477         2143         265         741         1183         265         770         S359         -303         148         829         S300         -1247	643	S484	2255	148	703	S424	1295	148	763	S364	335	148	823	S306	-1151	265	883	S246	-2111	265
646         S481         2207         265         706         S421         1247         265         766         S361         287         265         826         S303         -1199         148         886         S243         -2159         148           647         S480         2191         148         707         S420         1231         148         767         DUMMY23         271         148         827         S302         -1215         265         887         S242         -2175         265           648         S479         2175         265         708         S419         1215         265         768         DUMMY24         -271         148         828         S301         -1231         148         888         S241         -2191         148           649         S478         2159         148         709         S418         1199         148         769         S360         -287         265         829         S300         -1247         265         889         S240         -2207         265           650         S476         2127         148         711         S416         1167         148         771         S359	644		2239	265		S423	1279	265	764	S363	319	265	824		-1167	148	884	S245	-2127	148
647 S480 2191 148 707 S420 1231 148 767 DUMMY23 271 148 828 S301 -1231 148 888 S241 -2191 148 849 S478 2159 148 709 S418 1199 148 769 S360 -287 265 829 S300 -1247 265 889 S240 -2207 265 865 S472 2163 247 2111 265 712 S415 1151 265 772 S357 -335 148 832 S297 -1295 148 890 S239 -2223 148 713 S414 1135 148 773 S356 -351 265 8473 2079 265 744 S413 1119 265 744 S413 1119 265 745 S472 2063 148 715 S412 1103 148 775 S354 -383 265 S472 2063 148 715 S412 1103 148 775 S354 -383 265 S470 2031 148 717 S410 1071 148 777 S352 -415 265 848 1999 148 719 S408 1039 148 779 S350 -447 265 839 S290 -1407 265 899 S230 -2367 265 899 S230 -2365 265 848 1999 148 719 S408 1039 148 779 S350 -447 265 839 S290 -1407 265 899 S230 -2367																				
648         S479         2175         265         708         S419         1215         265         768         DUMMY24         -271         148         828         S301         -1231         148         888         S241         -2191         148           649         S478         2159         148         709         S418         1199         148         769         S360         -287         265         829         S300         -1247         265         889         S240         -2207         265           650         S477         2143         265         710         S417         1183         265         770         S359         -303         148         830         S299         -1263         148         890         S239         -2223         148           651         S476         2127         148         711         S416         1167         148         771         S358         -319         265         831         S298         -1279         265         891         S238         -2239         265           652         S475         2111         265         712         S415         1151         265         772         S357         -																				
649         S478         2159         148         709         S418         1199         148         769         S360         -287         265         829         S300         -1247         265         889         S240         -2207         265           650         S477         2143         265         710         S417         1183         265         770         S359         -303         148         830         S299         -1263         148         890         S239         -2223         148           651         S476         2127         148         711         S416         1167         148         771         S358         -319         265         831         S298         -1279         265         891         S238         -2239         265           652         S475         2111         265         712         S415         1151         265         772         S357         -335         148         832         S297         -1295         148         892         S237         -2255         148           653         S474         2095         148         713         S414         1135         148         773         S356         -351																				
650         S477         2143         265         710         S417         1183         265         770         S359         -303         148         830         S299         -1263         148         890         S239         -2223         148           651         S476         2127         148         711         S416         1167         148         771         S358         -319         265         831         S298         -1279         265         891         S238         -2239         265           652         S475         2111         265         712         S415         1151         265         772         S357         -335         148         832         S297         -1295         148         892         S237         -2255         148           653         S474         2095         148         713         S414         1135         148         773         S356         -351         265         833         S296         -1311         265         893         S236         -2271         265           654         S472         2063         148         715         S412         1103         148         775         S354         -383																				
651         S476         2127         148         711         S416         1167         148         771         S358         -319         265         831         S298         -1279         265         891         S238         -2239         265           652         S475         2111         265         712         S415         1151         265         772         S357         -335         148         832         S297         -1295         148         892         S237         -2255         148           653         S474         2095         148         713         S414         1135         148         773         S356         -351         265         833         S296         -1311         265         893         S236         -2271         265           654         S473         2079         265         714         S413         1119         265         774         S355         -367         148         834         S295         -1327         148         894         S235         -2287         148           655         S472         2063         148         715         S412         1103         148         775         S354         -383																				
652         S475         2111         265         712         S415         1151         265         772         S357         -335         148         832         S297         -1295         148         892         S237         -2255         148           653         S474         2095         148         713         S414         1135         148         773         S356         -351         265         833         S296         -1311         265         893         S236         -2271         265           654         S473         2079         265         714         S413         1119         265         774         S355         -367         148         834         S295         -1327         148         894         S235         -2287         148           655         S472         2063         148         715         S412         1103         148         775         S354         -383         265         835         S294         -1343         265         895         S234         -2303         265           656         S471         2047         265         716         S411         1087         265         776         S353         -399																				
653         S474         2095         148         713         S414         1135         148         773         S356         -351         265         833         S296         -1311         265         893         S236         -2271         265           654         S473         2079         265         714         S413         1119         265         774         S355         -367         148         834         S295         -1327         148         894         S235         -2287         148           655         S472         2063         148         715         S412         1103         148         775         S354         -383         265         835         S294         -1343         265         895         S234         -2303         265           656         S471         2047         265         716         S411         1087         265         776         S353         -399         148         836         S293         -1359         148         896         S233         -2319         148           657         S470         2031         148         717         S410         1071         148         777         S352         -415																				
654         S473         2079         265         714         S413         1119         265         774         S355         -367         148         834         S295         -1327         148         894         S235         -2287         148           655         S472         2063         148         715         S412         1103         148         775         S354         -383         265         835         S294         -1343         265         895         S234         -2303         265           656         S471         2047         265         716         S411         1087         265         776         S353         -399         148         836         S293         -1359         148         896         S233         -2319         148           657         S470         2031         148         717         S410         1071         148         777         S352         -415         265         837         S292         -1375         265         897         S232         -2335         265           658         S469         2015         265         718         S409         1055         265         778         S351         -431																				
655         S472         2063         148         715         S412         1103         148         775         S354         -383         265         835         S294         -1343         265         896         S234         -2303         265           656         S471         2047         265         716         S411         1087         265         776         S353         -399         148         836         S293         -1359         148         896         S233         -2319         148           657         S470         2031         148         717         S410         1071         148         777         S352         -415         265         837         S292         -1375         265         897         S232         -2335         265           658         S469         2015         265         718         S409         1055         265         778         S351         -431         148         838         S291         -1391         148         898         S231         -2351         148           659         S468         1999         148         719         S408         1039         148         779         S350         -447																				
656     S471     2047     265     716     S411     1087     265     776     S353     -399     148     836     S293     -1359     148     896     S233     -2319     148       657     S470     2031     148     717     S410     1071     148     777     S352     -415     265     837     S292     -1375     265     897     S232     -2335     265       658     S468     1999     148     719     S408     1039     148     779     S350     -447     265     839     S290     -1407     265     899     S230     -2367     265       659     S468     1999     148     719     S408     1039     148     779     S350     -447     265     839     S290     -1407     265     899     S230     -2367     265																				
657         S470         2031         148         717         S410         1071         148         777         S352         -415         265         837         S292         -1375         265         897         S232         -2335         265           658         S469         2015         265         718         S409         1055         265         778         S351         -431         148         838         S291         -1391         148         898         S231         -2351         148           659         S468         1999         148         719         S408         1039         148         779         S350         -447         265         839         S290         -1407         265         899         S230         -2367         265																				
658     S469     2015     265     718     S409     1055     265     778     S351     -431     148     838     S291     -1391     148     898     S231     -2351     148       659     S468     1999     148     719     S408     1039     148     779     S350     -447     265     839     S290     -1407     265     899     S230     -2367     265																				
660 S467 1983 265 720 S407 1023 265 780 S349 -463 148 840 S289 -1423 148 900 S229 -2383 148	659	S468	1999	148	719	S408	1039	148	779	S350	-447	265	839	S290	-1407	265	899	S230	-2367	265
	660	S467	1983	265	720	S407	1023	265	780	S349	-463	148	840	S289	-1423	148	900	S229	-2383	148





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No.	Name	Х	Υ	No.	Name	Х	Υ	No.	Name	Х	Υ	No.	Name	Х	Υ	No.	Name	Х	Υ
901	S228	-2399	265	961	S168	-3359	265	1021	S108	-4319	265	1081	S48	-5279	265	1141	G21	-6259	148
902	S227	-2415	148	962	S167	-3375	148	1022	S107	-4335	148	1082	S47	-5295	148	1142	G23	-6275	265
903	S226	-2431	265	963	S166	-3391	265	1023	S106	-4351	265	1083	S46	-5311	265	1143	G25	-6291	148
904	S225	-2447	148	964	S165	-3407	148	1024	S105	-4367	148	1084	S45	-5327	148	1144	G27	-6307	265
905	S224	-2463	265	965	S164	-3423	265	1025	S104	-4383	265	1085	S44	-5343	265	1145	G29	-6323	148
906	S223	-2479	148	966	S163	-3439	148	1026	S103	-4399	148	1086	S43	-5359	148	1146	G31	-6339	265
907	S222	-2495	265	967	S162	-3455	265	1027	S102	-4415	265	1087	S42	-5375	265	1147	G33	-6355	148
908	S221	-2511	148	968	S161	-3471	148	1028	S101	-4431	148	1088	S41	-5391	148	1148	G35	-6371	265
909	S220	-2527	265	969	S160	-3487	265	1029	S100	-4447	265	1089	S40	-5407	265	1149	G37	-6387	148
910	S219	-2543	148	970	S159	-3503	148	1030	S99	-4463	148	1090	S39	-5423	148	1150	G39	-6403	265
911	S218	-2559	265	971	S158	-3519	265	1031	S98	-4479	265	1091	S38	-5439	265	1151	G41	-6419	148
912	S217	-2575	148	972	S157	-3535	148	1032	S97	-4495	148	1092	S37	-5455	148	1152	G43	-6435	265
913	S216	-2591	265	973	S156	-3551	265	1033	S96	-4511	265	1093	S36	-5471	265	1153	G45	-6451	148
914	S215	-2607	148	974	S155	-3567	148	1034	S95	-4527	148	1094	S35	-5487	148	1154	G47	-6467	265
915	S214	-2623	265	975	S154	-3583	265	1035	S94	-4543	265	1095	S34	-5503	265	1155	G49	-6483	148
916	S213	-2639	148	976	S153	-3599	148	1036	S93	-4559	148	1096	S33	-5519	148	1156	G51	-6499	265
917	S212	-2655	265	977	S152	-3615	265	1037	S92	-4575	265	1097	S32	-5535	265	1157	G53	-6515	148
918	S211	-2671	148	978	S151	-3631	148	1038	S91	-4591	148	1098	S31	-5551	148	1158	G55	-6531	265
919	S210	-2687	265	979	S150	-3647	265	1039	S90	-4607	265	1099	S30	-5567	265	1159	G57	-6547	148
920	S209	-2703	148	980	S149	-3663	148	1040	S89	-4623	148	1100	S29	-5583	148	1160	G59	-6563	265
921	S208	-2719	265	981	S148	-3679	265	1041	S88	-4639	265	1101	S28	-5599	265	1161	G61	-6579	148
922	S207	-2735	148	982	S147	-3695	148	1042	S87	-4655	148	1102	S27	-5615	148	1162	G63	-6595	265
923	S206	-2751	265	983	S146	-3711	265	1043	S86	-4671	265	1103	S26	-5631	265	1163	G65	-6611	148
924	S205	-2767	148	984	S145	-3727	148	1044	S85	-4687	148	1104	S25	-5647	148	1164	G67	-6627	265
925	S204	-2783	265	985	S144	-3743	265	1045	S84	-4703	265	1105	S24	-5663	265	1165	G69	-6643	148
926	S203	-2799	148	986	S143	-3759	148	1046	S83	-4719	148	1106	S23	-5679	148	1166	G71	-6659	265
927	S202	-2815	265	987	S142	-3775	265	1047	S82	-4735	265	1107	S22	-5695	265	1167	G73	-6675	148
928	S201	-2831	148	988	S141	-3791	148	1048	S81	-4751	148	1108	S21	-5711	148	1168	G75	-6691	265
929	S200	-2847	265	989	S140	-3807	265	1049	S80	-4767	265	1109	S20	-5727	265	1169	G77	-6707	148
930	S199	-2863	148	990	S139	-3823	148	1050	S79	-4783	148	1110	S19	-5743	148	1170	G79	-6723	265
931	S198	-2879	265	991	S138	-3839	265	1051	S78	-4799	265	1111	S18	-5759	265	1171	G81	-6739	148
932	S197	-2895	148	992	S137	-3855	148	1052	S77	-4815	148	1112	S17	-5775	148	1172	G83	-6755	265
933	S196	-2911	265	993	S136	-3871	265	1053	S76	-4831	265	1113	S16	-5791	265	1173	G85	-6771	148
934	S195	-2927	148	994	S135	-3887	148	1054	S75	-4847	148	1114	S15	-5807	148	1174	G87	-6787	265
935	S194	-2943	265	995	S134	-3903	265	1055	S74	-4863	265	1115	S14	-5823	265	1175	G89	-6803	148
936	S193	-2959	148	996	S133	-3919	148	1056	S73	-4879	148	1116	S13	-5839	148	1176	G91	-6819	265
937	S192	-2975	265	997	S132	-3935	265	1057	S72	-4895	265	1117	S12	-5855	265	1177	G93	-6835	148
938	S191	-2991	148	998	S131	-3951	148	1058	S71	-4911	148	1118	S11	-5871	148	1178	G95	-6851	265
939	S190	-3007	265	999	S130	-3967	265	1059	S70	-4927	265	1119	S10	-5887	265	1179	G97	-6867	148
940	S189	-3023	148	1000	S129	-3983	148	1060	S69	-4943	148	1120	S9	-5903	148	1180	G99	-6883	265
941	S188	-3039	265	1001	S128	-3999	265	1061	S68	-4959	265	1121	S8	-5919	265	1181	G101	-6899	148
942	S187	-3055	148	1002	S127	-4015	148	1062	S67	-4975	148	1122	S7	-5935	148	1182	G103	-6915	265
943	S186	-3071	265	1003	S126	-4031	265	1063	S66	-4991	265	1123	S6	-5951	265	1183	G105	-6931	148
944	S185	-3087	148	1004	S125	-4047	148	1064	S65	-5007	148	1124	S5	-5967	148	1184	G107	-6947	265
945	S184	-3103	265	1005	S124	-4063	265	1065	S64	-5023	265	1125	S4	-5983	265	1185	G109	-6963	148
946	S183	-3119	148	1006	S123	-4079	148	1066	S63	-5039	148	1126	S3	-5999	148	1186	G111	-6979	265
947	S182	-3135	265	1007	S122	-4095	265	1067	S62	-5055	265	1127	S2	-6015	265	1187	G113	-6995	148
948	S181	-3151	148	1008	S121	-4111	148	1068	S61	-5071	148	1128	S1	-6031	148	1188	G115	-7011	265
949	S180	-3167	265	1009	S120	-4127	265	1069	S60	-5087	265	1129	DUMMY25	-6047	265	1189	G117	-7027	148
950	S179	-3183	148	1010	S119	-4143	148	1070	S59	-5103	148	1130	DUMMY26	-6083	265	1190	G119	-7043	265
951	S178	-3199	265	1011	S118	-4159	265	1071	S58	-5119	265	1131	G1	-6099	148	1191	G121	-7059	148
952	S177	-3215	148	1012	S117	-4175	148	1072	S57	-5135	148	1132	G3	-6115	265	1192	G123	-7075	265
953	S176	-3231	265	1013	S116	-4191	265	1073	S56	-5151	265	1133	G5	-6131	148	1193	G125	-7091	148
954	S175	-3247	148	1014	S115	-4207	148	1074	S55	-5167	148	1134	G7	-6147	265	1194	G127	-7107	265
955	S174	-3263	265	1015	S114	-4223	265	1075	S54	-5183	265	1135	G9	-6163	148	1195	G129	-7123	148
956	S173	-3279	148	1016	S113	-4239	148	1076	S53	-5199	148	1136	G11	-6179	265	1196	G131	-7139	265
957	S172	-3295	265	1017	S112	-4255	265	1077	S52	-5215	265	1137	G13	-6195	148	1197	G133	-7155	148
958	S171	-3311	148	1018	S111	-4271	148	1078	S51	-5231	148	1138	G15	-6211	265	1198	G135	-7171	265
959	S170	-3327	265	1019	S110	-4287	265	1079	S50	-5247	265	1139	G17	-6227	148	1199	G137	-7187	148
960	S169	-3343	148	1020	S109	-4303	148	1080	S49	-5263	148	1140	G19	-6243	265	1200	G139	-7203	265
000	0.00	0070							U-TU	0_00									



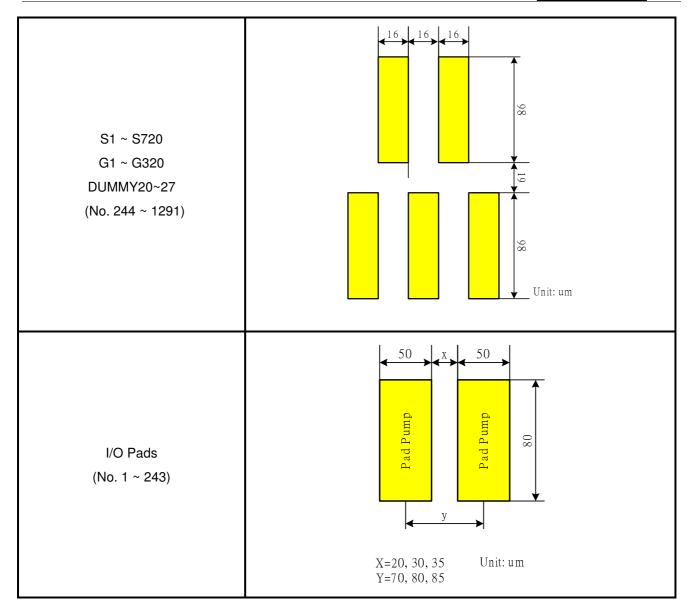
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No.	Name	Х	Υ	No.	Name	Х	Υ
1201	G141	-7219	148	1261	G261	-8179	148
1202	G143	-7235	265	1262	G263	-8195	265
1203	G145	-7251	148	1263	G265	-8211	148
1204	G147	-7267	265	1264	G267	-8227	265
1205	G149	-7283	148	1265	G269	-8243	148
1206	G151	-7299	265	1266	G271	-8259	265
1207	G153	-7315	148	1267	G273	-8275	148
1208	G155	-7331	265	1268	G275	-8291	265
1209	G157	-7347	148	1269	G277	-8307	148
1210	G159	-7363	265	1270	G279	-8323	265
1211	G161	-7379	148	1271	G281	-8339	148
1212	G163	-7395	265	1272	G283	-8355	265
1213	G165	-7411	148	1273	G285	-8371	148
1214	G167	-7427	265	1274	G287	-8387	265
1215	G169	-7443	148	1275	G289	-8403	148
1216	G171	-7459	265	1276	G291	-8419	265
1217	G173	-7475	148	1277	G293	-8435	148
1218	G175	-7491	265	1278	G295	-8451	265
1219	G177	-7507	148	1279	G297	-8467	148
1220	G179	-7523	265	1280	G299	-8483	265
1221	G181	-7539	148	1281	G301	-8499	148
1222	G183	-7555	265	1282	G303	-8515	265
1223	G185	-7571	148	1283	G305	-8531	148
1224	G187	-7587	265	1284	G307	-8547	265
1225	G189	-7603	148	1285	G309	-8563	148
1226	G191	-7619	265	1286	G311	-8579	265
1227	G193	-7635	148	1287	G313	-8595	148
1228	G195	-7651	265	1288	G315	-8611	265
1229	G197	-7667	148	1289	G317	-8627	148
1230	G199	-7683	265	1290	G319	-8643	265
1231	G201	-7699	148	1291	DUMMY27	-8659	148
1232	G203	-7715	265				
1233	G205	-7731	148				
1234	G207	-7747	265				
1235	G209	-7763	148				
1236	G211	-7779	265				
1237	G213	-7795	148				
1238	G215	-7811	265				
1239	G217	-7827	148				
1240	G219	-7843	265				
1241	G221	-7859	148				
1242	G223	-7875	265				
1243	G225	-7891	148				
1244	G227	-7907	265				
1245	G229	-7923	148				
1246	G231	-7939	265				
1247	G233	-7955	148				
1248	G235	-7971	265				
1249	G237	-7987	148				
1250	G239	-8003	265				
1251	G241	-8019	148				
1252	G243	-8035	265				
1253	G245	-8051	148				
1254	G247	-8067	265				
1255	G249	-8083	148				
1256	G251	-8099	265				
1257	G253	-8115	148				
1258	G255	-8131	265				
1259	G257	-8147	148				
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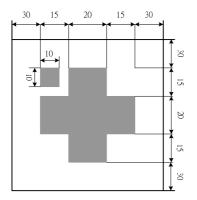


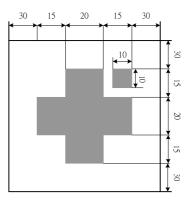






#### Alignment mark





Alignment Mark: 1

Alignment Mark: 2

Alignment mark	Х	Υ
1	-8751	214.5
2	8751	214.5





#### 6. Block Description

#### **MPU System Interface**

ILI9325C supports three system high-speed interfaces: i80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

ILI9325C has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9325C read the first data from the internal GRAM. Valid data are read out after the ILI9325C performs the second read operation.

Registers are written consecutively as the register execution time.

Registers selection by system interface (8-/9-/16-/18-bit bus width)		18	30
Function	RS	nWR	nRD
Write an index to IR register	0	0	1
Write to control registers or the internal GRAM by WDR register.	1	0	1
Read from the internal GRAM by RDR register.	1	1	0

Registers selection by the SPI system interface							
Function	R/W	RS					
Write an index to IR register	0	0					
Write to control registers or the internal GRAM by WDR register.	0	1					
Read from the internal GRAM by RDR register.	1	1					

#### **Parallel RGB Interface**

ILI9325C supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the "External Display Interface" section. The ILI9325C allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

V0.07





#### **Bit Operation**

The ILI9325C supports a write data mask function for selectively writing data to the internal RAM in units of bits and a logical/compare operation to write data to the GRAM only when a condition is met as a result of comparing the data and the compare register bits. For details, see "Graphics Operation Functions".

#### Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

#### **Graphics RAM (GRAM)**

GRAM is graphics RAM storing bit-pattern data of 172,800 (240 x 320x 18/8) bytes with 18 bits per pixel.

#### **Grayscale Voltage Generating Circuit**

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the  $\gamma$ -correction register to display in 262,144 colors. For details, see the " $\gamma$ -Correction Register" section.

#### **Timing Controller**

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

#### Oscillator (OSC)

ILI9325C generates RC oscillation with an internal oscillation resistor. The frame rate is adjusted by the register setting.

#### **LCD Driver Circuit**

The LCD driver circuit of ILI9325C consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). Display pattern data are latched when the 720<sup>th</sup> bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720 source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

#### **LCD Driver Power Supply Circuit**

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for





driving an LCD

#### 7. System Interface

#### 7.1. Interface Specifications

ILI9325C has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

ILI9325C also has the RGB interface and VSYNC interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB[17:0].

In VSYNC interface mode, the internal display timing is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface mode enables to display the moving picture display through the system interface. In this case, there are some constraints of speed and method to write data to the internal RAM.

ILI9325C operates in one of the following 4 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM[1:0])
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM[1:0] = 00)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 01)

Note 1) Registers are set only via the system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not available simultaneously.

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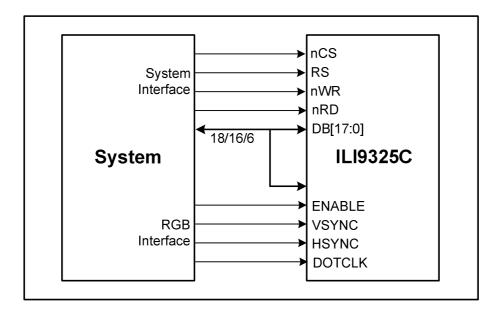


Figure1 System Interface and RGB Interface connection

#### **Input Interfaces** 7.2.

The following are the system interfaces available with the ILI9325C. The interface is selected by setting the IM[3:0] pins. The system interface is used for setting registers and GRAM access.

IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	0	Setting invalid	
0	0	0	1	Setting invalid	
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO (DB[1:0])
0	1	1	0	9-bit 3 wires Serial Peripheral Interface	SDA, SCL, nCS
0	1	1	1	8-bit 4 wires Serial Peripheral Interface	SDA, SCL, nCS, RS (D/CX)
1	0	0	0	Setting invalid	
1	0	0	1	Setting invalid	
1	0	1	0	i80-system18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]
1	1	*	*	Setting invalid	

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#### 7.2.1. i80/18-bit System Interface

The i80/18-bit system interface is selected by setting the IM[3:0] as "1010" levels.

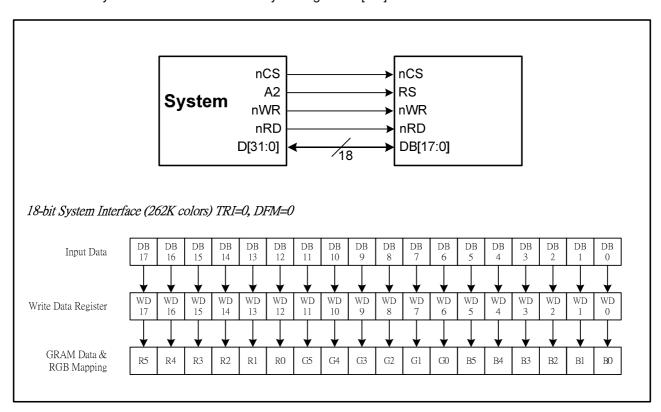


Figure 218-bit System Interface Data Format

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#### 7.2.2. i80/16-bit System Interface

The i80/16-bit system interface is selected by setting the IM[3:0] as "0010" levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1<sup>st</sup> transfer: 2 bits, 2<sup>nd</sup> transfer: 16 bits or 1<sup>st</sup> transfer: 16 bits, 2<sup>nd</sup> transfer: 2 bits) are necessary for the 16-bit CPU interface.

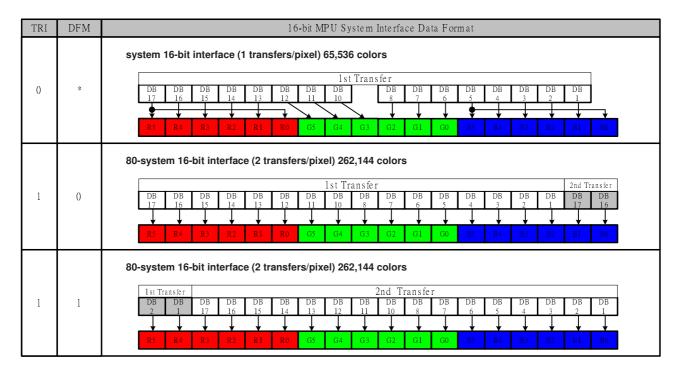


Figure 316-bit System Interface Data Format

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#### 7.2.3. i80/9-bit System Interface

The i80/9-bit system interface is selected by setting the IM[3:0] as "1011" and the DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to GND.

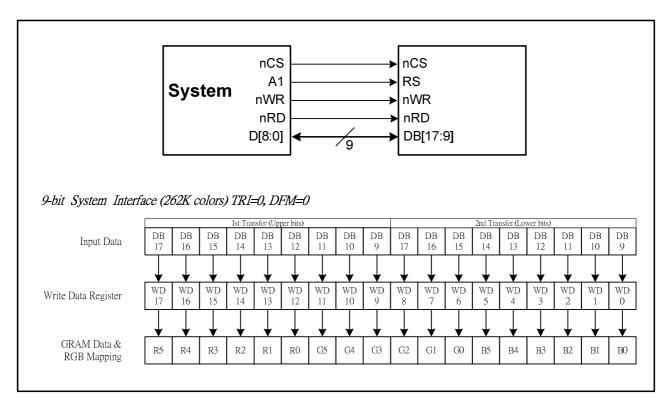


Figure 4 9-bit System Interface Data Format

#### 7.2.4. i80/8-bit System Interface

The i80/8-bit system interface is selected by setting the IM[3:0] as "0011" and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to GND.

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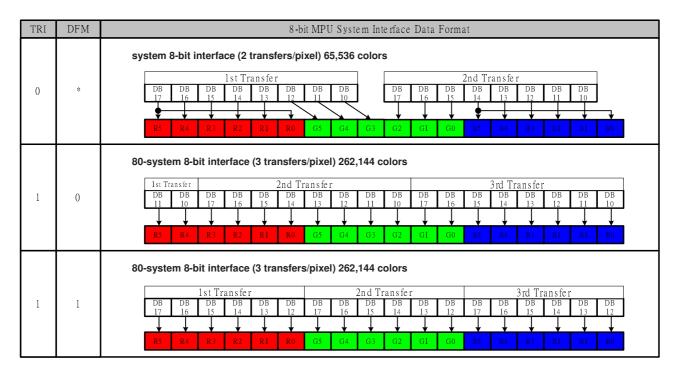


Figure 5 8-bit System Interface Data Format

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#### 7.3. Serial Peripheral Interface (SPI)

#### 7.3.1. 24-bit 4 wires Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as "010x" level. The chip select pin (nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ILI9325C.

The seventh bit of start byte is RS bit. When RS = "0", either index write operation or status read operation is executed. When RS = "1", either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is "0" and read back when the R/W bit is "1".

After receiving the start byte, ILI9325C starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ILI9325C are 16-bit format and receive the first and the second byte datat as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6<sup>th</sup> byte of read back data.

#### **Start Byte Format**

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Devid			evice ID code				R/W
		0	1	1	1	0	ID	1/0	1/0

Note: ID bit is selected by setting the IMO/ID pin.

#### RS and R/W Bit Function

RS	R/W	Function			
0	0 Set an index register				
0	1	Read a status			
1	0 Write a register or GRAM data				
1	1	Read a register or GRAM data			

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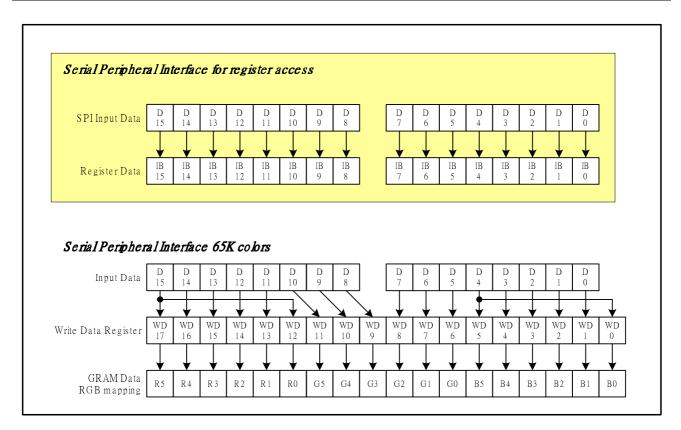


Figure 6 Data Format of SPI Interface

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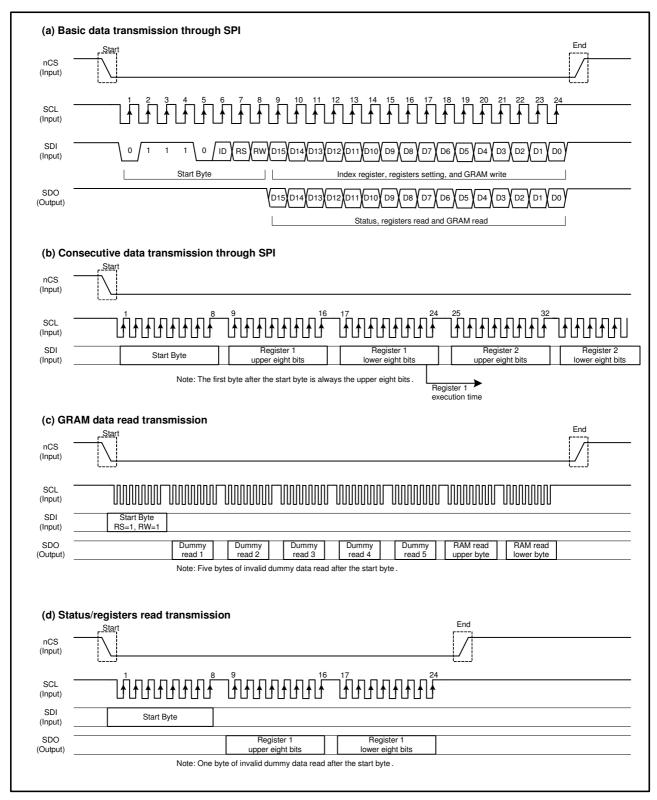


Figure 7 Data transmission through serial peripheral interface (SPI)

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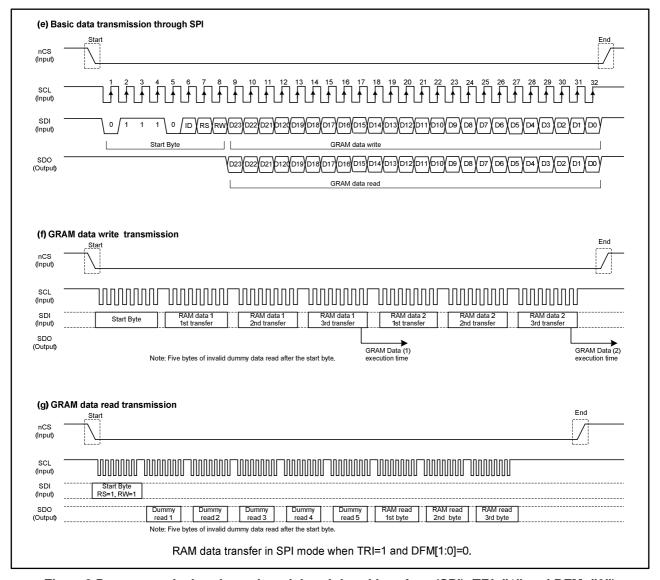


Figure8 Data transmission through serial peripheral interface (SPI), TRI="1" and DFM="0")



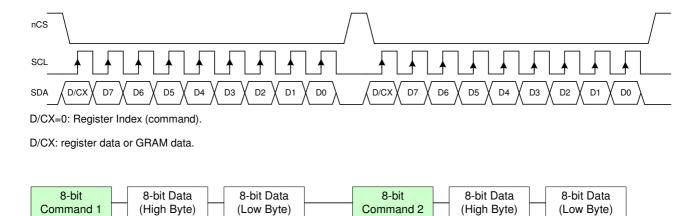


#### 7.3.2. 3-wire 9-bit Serial Interface

This SPI mode uses a 3-wire 9-bit serial interface. The chip-select **nCS** (active low) enables and disables the serial interface. **SCL** is the serial data clock and **SDA** is serial data.

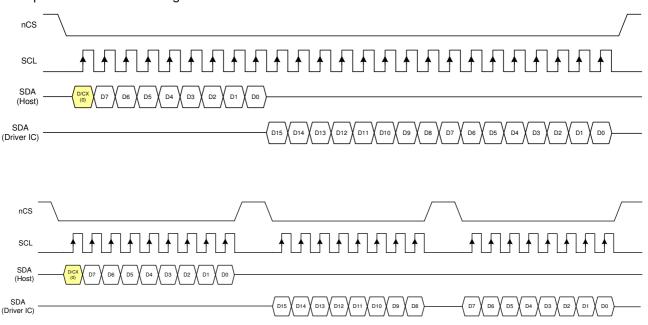
Serial data must be input to **SDA** in the sequence D/CX, D7 to D0. The ILI9325C reads the data at the rising edge of **SCL** signal. The first bit of serial data D/CX is data/command flag. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

#### **Register Write Mode:**



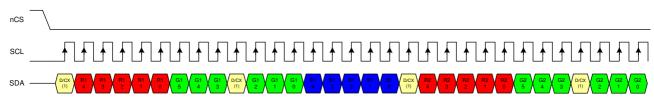
#### **Register Read Mode:**

When users need to read back the register or GRAM data, the register R66h must be set as "1" first, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.

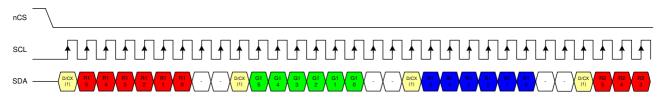




## Serial Data Transfer Interface (65K colors)



### Serial Data Transfer Interface (262K colors)



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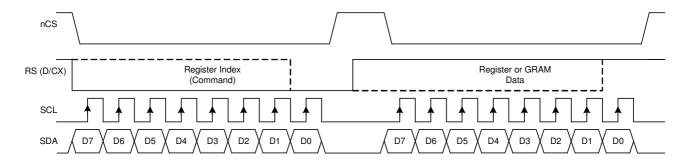


### 7.3.3. 4-wire 8-bit Serial Interface

This SPI mode uses a 4-wire 8-bit serial interface. The chip-select **nCS** (active low) enables and disables the serial interface. **D/CX** is the command or data select signal, **SCL** is the serial data clock and **SDA** is serial data.

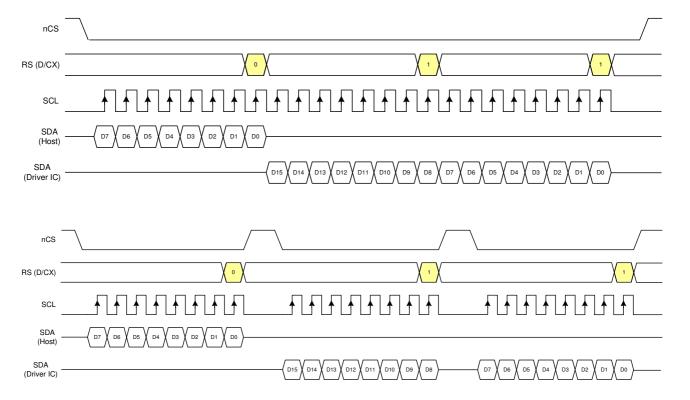
Serial data must be input to **SDA** in the sequence D7 to D0. The ILI9325C reads the data at the rising edge of **SCL** signal. The **D/CX** signal indicates data/command. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

## **Register Write Mode:**



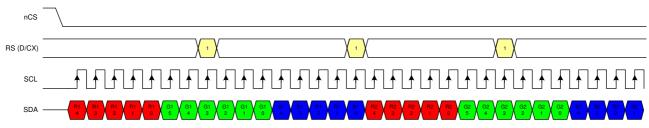
### **Register Read Mode:**

When users need to read back the register or GRAM data, the register R66h must be set as "1" first, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.

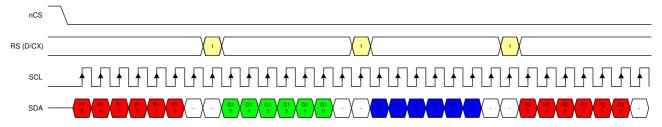




## Serial Data Transfer Interface (65K colors)



### Serial Data Transfer Interface (262K colors)





### 7.4. VSYNC Interface

ILI9325C supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the i80 system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".

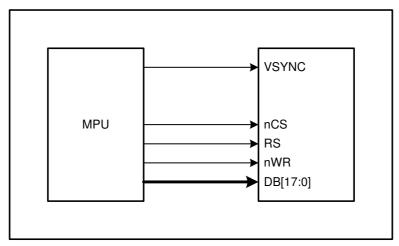


Figure 9 Data transmission through VSYNC interface)

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

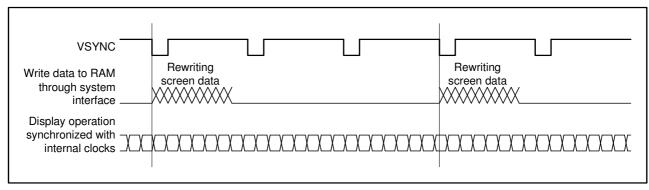


Figure 10 Moving picture data transmission through VSYNC interface

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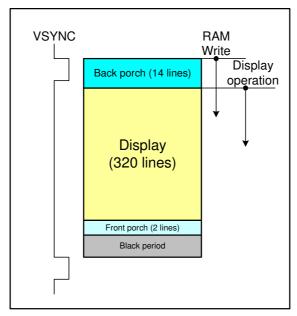


Figure 11 Operation through VSYNC Interface

The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (FP) + BackPorch (BP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

### [Example]

Display size: 240 RGB × 320 lines Lines: 320 lines (NL = 1000111) Back porch: 14 lines (BP = 1110) Front porch: 2 lines (FP = 0010)

Frame frequency: 60 Hz Frequency fluctuation: 10%

Internal oscillator clock (fosc.) [Hz] =  $60 \times [320+2+14] \times 16$  clocks  $\times (1.1/0.9) = 394$ KHz





When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz] > 240 x 320 x 394K / [ (14 + 320 - 2) lines x 16clocks] = 5.7 MHz

The above theoretical value is calculated based on the premise that the ILI9325C starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 5.7MHz or more will guarantee the completion of GRAM write operation before the ILI9325C starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

### Notes in using the VSYNC interface

- 1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
- 2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
- 3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
- 4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to "0" to transfer display data.



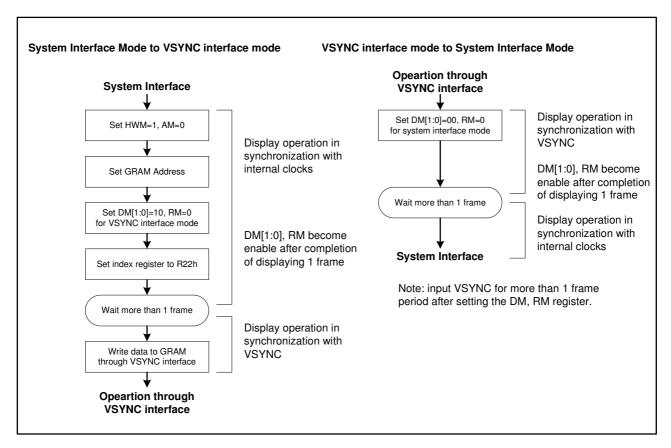


Figure 12 Transition flow between VSYNC and internal clock operation modes

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## 7.5. RGB Input Interface

The RGB Interface mode is available for ILI9325C and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

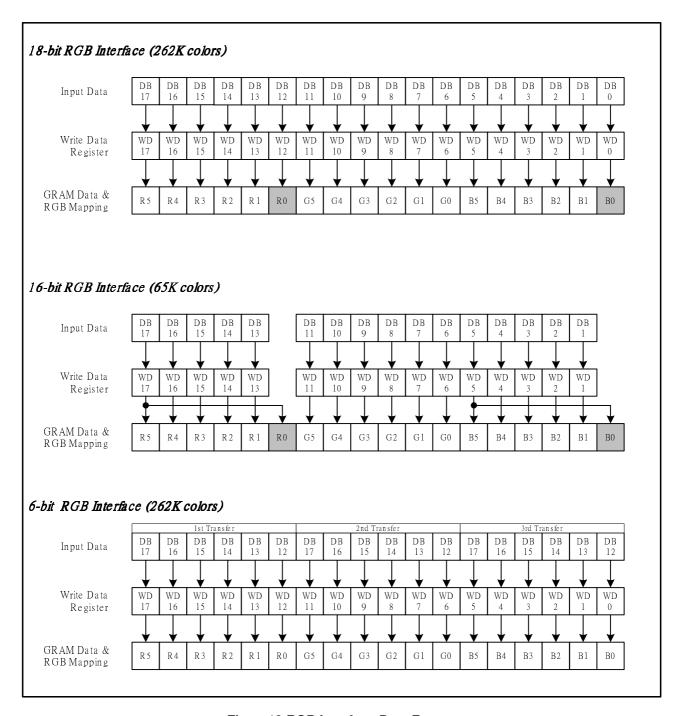


Figure 13 RGB Interface Data Format

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#### 7.5.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.

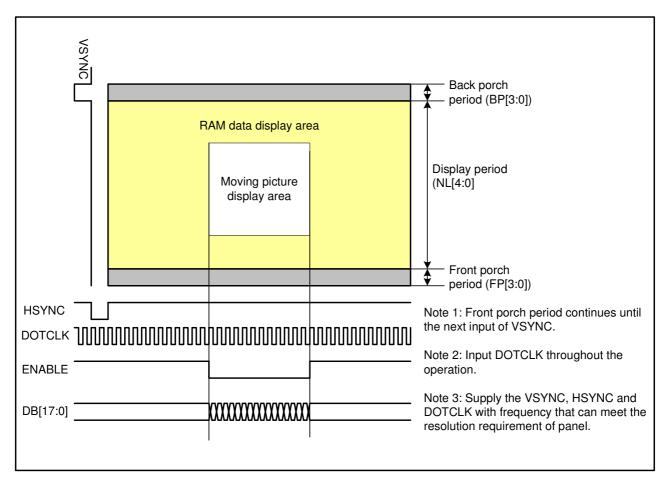


Figure 14 GRAM Access Area by RGB Interface

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### 7.5.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as follows.

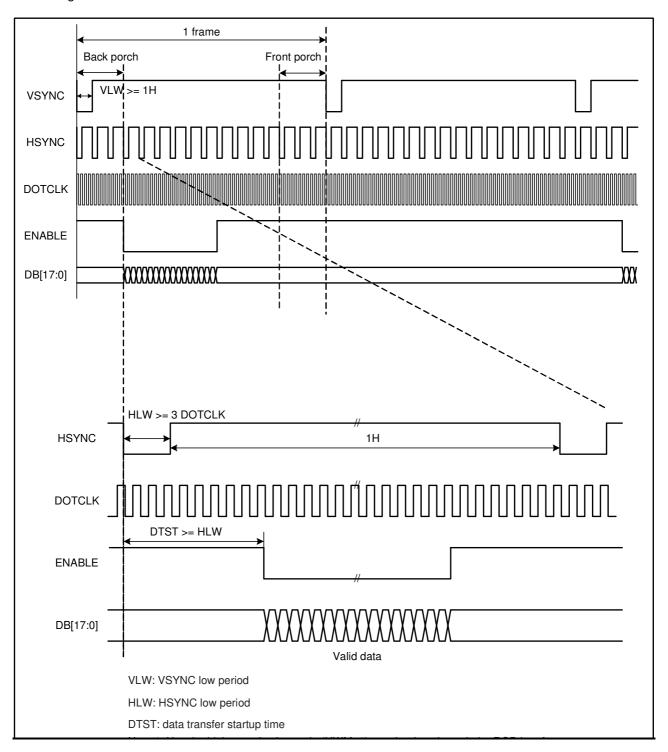


Figure 15 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

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The timing chart of 6-bit RGB interface mode is shown as follows.

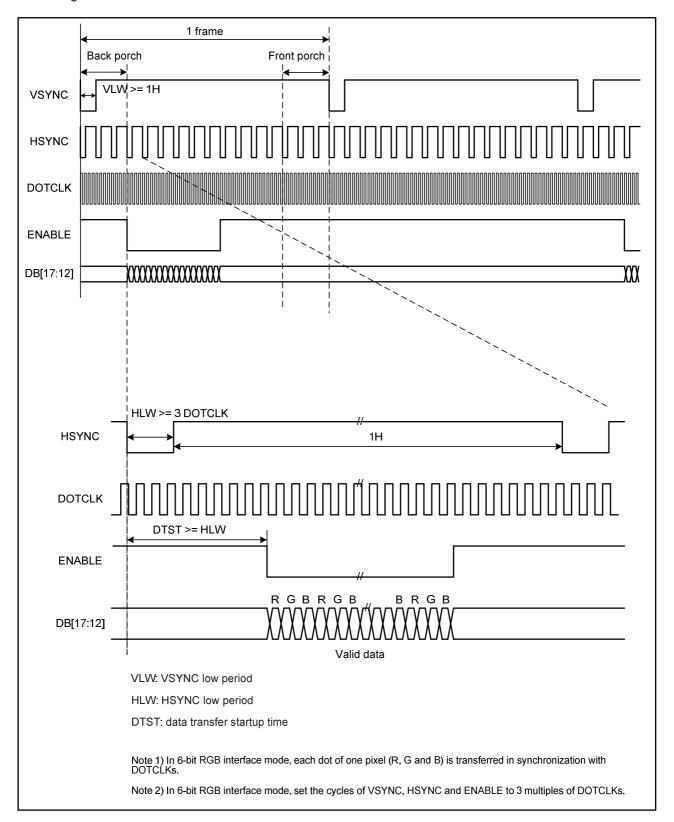


Figure16 Timing chart of signals in 6-bit RGB interface mode

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### 7.5.3. Moving Picture Mode

ILI9325C has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

### RAM access via a system interface in RGB-I/F mode

ILI9325C allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = "0") and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the ILI9325C when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

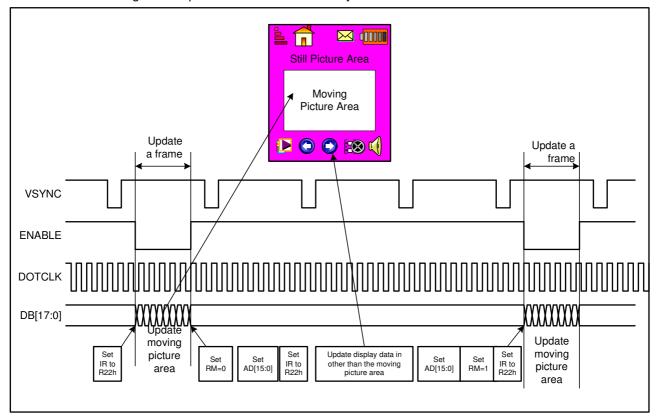


Figure 17 Example of update the still and moving picture

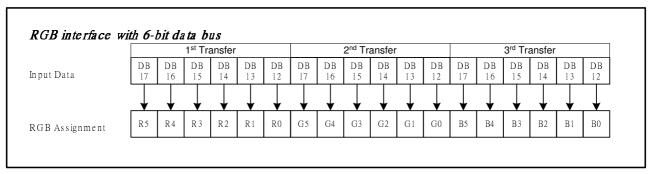
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#### 7.5.4. 6-bit RGB Interface

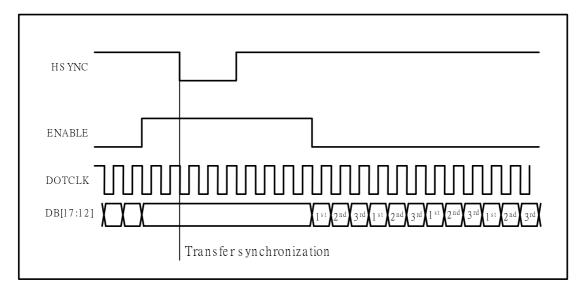
The 6-bit RGB interface is selected by setting the RIM[1:0] bits to "10". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at GND level. Registers can be set by the system interface (i80/SPI).



### Data transfer synchronization in 6-bit RGB interface mode

ILI9325C has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



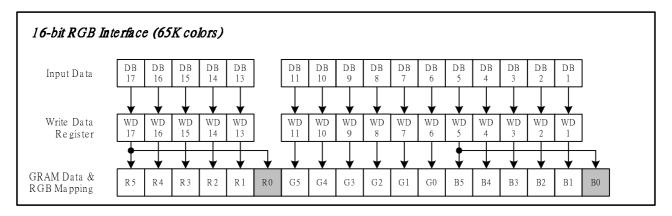
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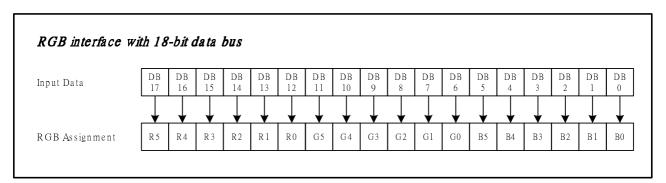
#### 7.5.5. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to "01". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.



### 7.5.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to "00". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.



#### Notes in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

Function	RGB interface	I80 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.

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3. The periods set with the NO[1:0] bits (gate output non-overlap period), STD[1:0] bits (source output delay period) and EQ[1:0] bits (equalization period) are not based on the internal clock but based on DOTCLK in The information contained herein is the exclusive property of ILI Technology Corp. and shall not be distributed,





RGB interface mode.

- 4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
- 5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
- 6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
- 7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
- 8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

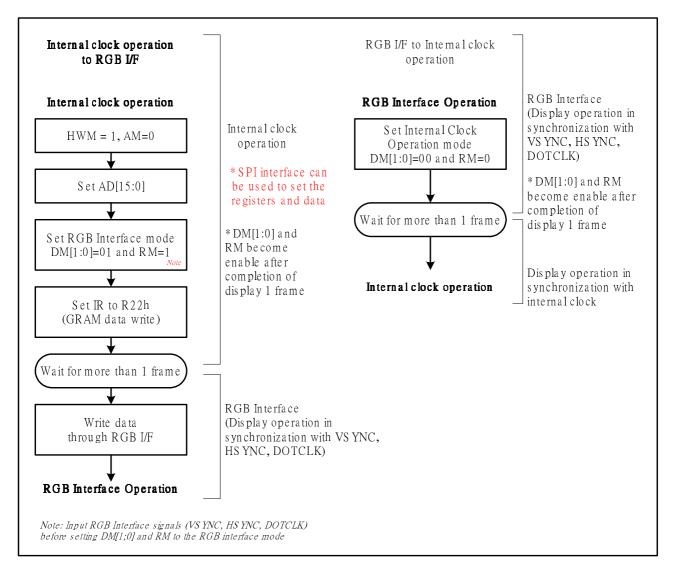


Figure 18 Internal clock operation/RGB interface mode switching



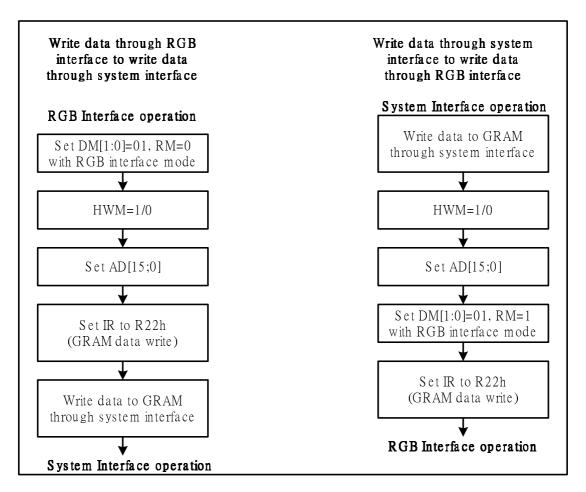


Figure19 GRAM access between system interface and RGB interface

### Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.



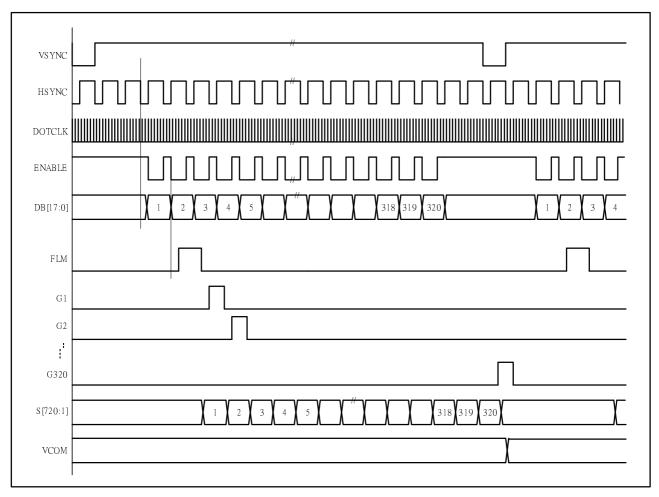


Figure 20 Relationship between RGB I/F signals and LCD Driving Signals for Panel



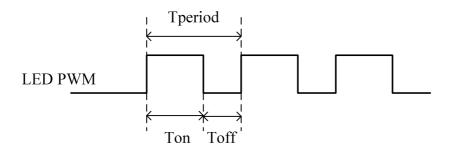


## 7.6. CABC (Content Adaptive Brightness Control)

ILI9325C provide a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce

the power consumption of the luminance source. ILI9325C will refer the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. Content adaptation means that the content of gray sale can be increased while simultaneously lowering brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and thus the power consumption reduction depend on the content of the image.

LIL9325C can calculate the backlight brightness level and send a PWM pulse to LED driver via LEDPWM pin for backlight brightness control purpose. The figure in the following is the basic timing diagram which is applied ILI9325C to control LED driver.



The period T<sub>period</sub> of PWM pulse can be changed by the PWM\_DIV[7:0] bits of the command "PWM\_DIV (F2h)".The LED-on time T<sub>on</sub> and the LED-off time T<sub>off</sub> are decided by the backlight brightness level which is calculated with CABC in ILI9325C. If CABC is off, then LEDPWM will forced to "H" level.

The PWM period value will be calculated via the equation as below.

$$f_{PWM\_OUT} = \frac{5.8MHz}{(PWM\_DIV[7:0]+1)\times255}$$





## 8. Register Descriptions

## 8.1. Registers Access

ILI9325C adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of ILI9325C starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of ILI9325C. The registers of the ILI9325C are categorized into the following groups.

- 1. Specify the index of register (IR)
- 2. Read a status
- 3. Display control
- 4. Power management Control
- 5. Graphics data processing
- Set internal GRAM address (AC)
- 7. Transfer data to/from the internal GRAM (R22)
- 8. Internal grayscale γ-correction (R30 ~ R39)

Normally, the display data (GRAM) is most often updated, and in order since the ILI9325C can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

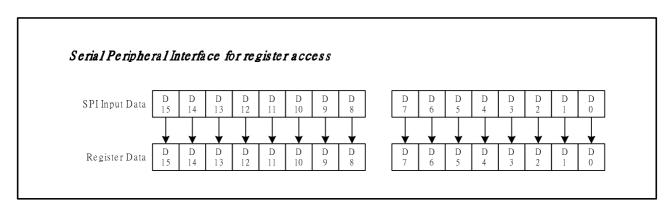


Figure21 Register Setting with Serial Peripheral Interface (SPI)

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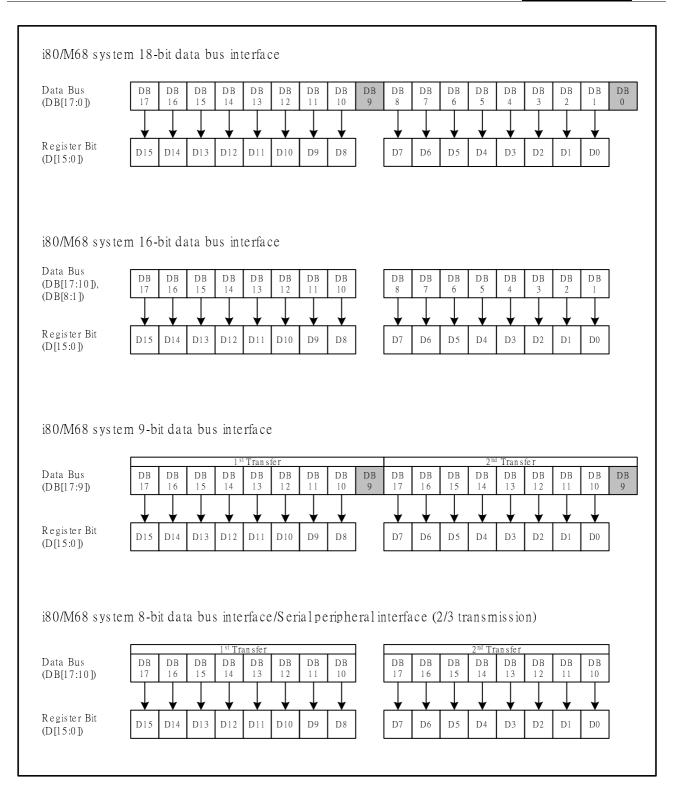


Figure 22 Register setting with i80 System Interface

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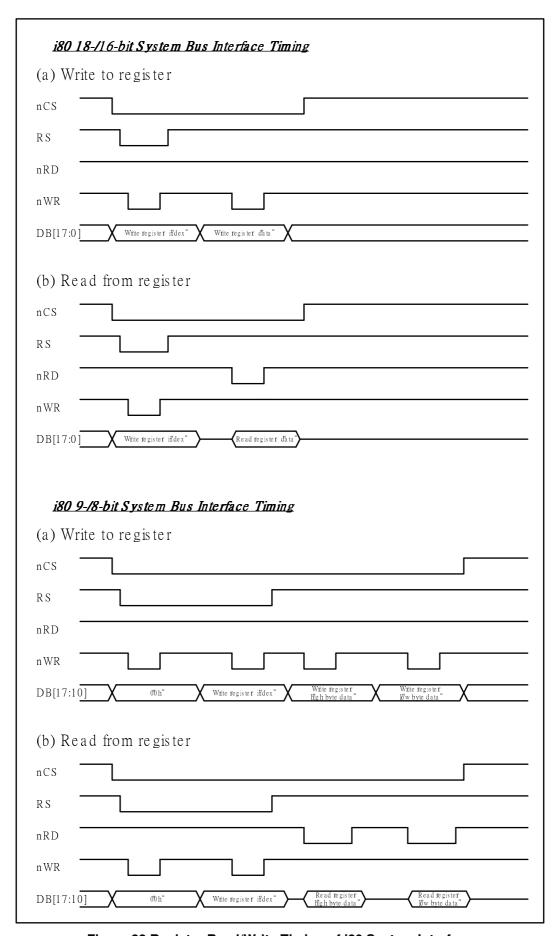


Figure 23 Register Read/Write Timing of i80 System Interface



# **ILI9325C**

## 8.2. Instruction Descriptions

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	RO	1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
05h	16 bits data format control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF1	EPF0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
10h	Power Control 1	W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM v	rite data (\	WD17-0) /	read data	(RD17-0) bi	ts are tran	sferred via	a different	data bus li	nes accor	ding to the	selected in	nterfaces.			
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS[3]	FRS[2]	FRS[1]	FRS[0]
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
3Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]





No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
66h	SPI Read/Write Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX (0)
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI00	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
A1h	OTP VCM Programming Control	W	1	0	0	0	0	OTP_ PGM_EN	0	0	0	0	0	VCM_ OTP5	VCM_ OTP4	VCM_ OTP3	VCM_ OTP2	VCM_ OTP1	VCM_ OTP0
A2h	OTP VCM Status and Enable	W	1	PGM_ CNT1	PGM_ CNT0	VCM_ D5	VCM_ D4	VCM_ D3	VCM_ D2	VCM_ D1	VCM_ D0	0	0	0	0	0	0	0	VCM_ EN
A5h	OTP Programming ID Key	W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
B1h	Write Display Brightness	W	1	Х	Х	Х	Х	Χ	Х	Х	Х	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
B2h	Read Display Brightness	R	1	Х	Х	Х	Χ	Х	Х	Χ	Х	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
B3h	Write CTRL Display value	W	1	Х	Х	Х	Χ	Х	Х	Х	Х	Х	Х	BCTRL	Х	DD	BL	Х	Х
B4h	Read CTRL Display value	R	1	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	BCTRL	Х	DD	BL	Х	Х
B5h	Write Content Adaptive Brightness Control value	W	1	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	C[	1:0]
B6h	Read Content Adaptive Brightness Control value	R	1	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	х	C[	1:0]
BEh	Write CABC Minimum Brightness	w	1	Х	Х	Х	Х	Х	Х	Х	Х	X CMB[7:0]							

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No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BFh	Read CABC Minimum	R	1	Х	Х	Х	Х	Х	Х	Х	Х				СМ	B[7:0]			
	Brightness																		
C8h	CABC Control 1	W	1	Х	Х	Χ	Χ	Χ	Χ	Χ	Х				PWM_	_DIV[7:0]			
C9h	CABC Control 2	W	1	X	Х	Χ	Х	Χ	Χ	Х	Х	THRES_MOV[3:0] THRES_STILL[3:0]							
CAh	CABC Control 3	W	1	Х	Х	Х	Х	Х	Х	Х	Х	0	0	0	0		THRES_	UI[3:0]	
CBh	CABC Control 4	W	1	X	Х	Х	Х	Χ	Х	Χ	X		DTH_N	MOV[3:0]			DTH_ST	ILL[3:0]	
CCh	CABC Control 5	W	1	Х	Х	Х	Х	Χ	Х	Χ	Х	0	0	0	0		DTH_L	II[3:0]	
CDh	CABC Control 6	W	1	Х	Х	Х	Х	Х	Х	Х	Х	DIM_OPT2[3:0] 0 DIM_OPT1[2:0]							
CEh	CABC Control 7	W	1	X	Х	Х	Х	Х	Х	Х		SCD_VLINE[8:0]					·		

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### 8.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the address of register (R00h ~ RFFh) or RAM which will be accessed.

## 8.2.2. ID code (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RO	1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1

The device code "9325C"h is read out when read this register.

## 8.2.3. Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Det	fault	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**SS:** Select the shift direction of outputs from the source driver.

When SS = 0, the shift direction of outputs is from S1 to S720

When SS = 1, the shift direction of outputs is from S720 to S1.

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

When changing SS or BGR bits, RAM data must be rewritten.

**SM:** Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module.



SM	GS	Scan Direction	Gate Output Sequence
0	0	G320 G319 G318 G317	G1, G2, G3, G4,,G316 G317, G318, G319, G320
0	1	G320 G319 G318 G317	G320, G319, G318,, G6, G5, G4, G3, G2, G1
1	0	G320  TFT Panel  G2  G319  Odd-number  G1 to G319  ILI9325C	G1, G3, G5, G7,,G311 G313, G315, G317, G319 G2, G4, G6, G8,,G312 G314, G316, G318, G320
1	1	Even-number  G320  TFT Panel  G2  G319  Odd-number  G1 to G319  ILI9325C	G320, G318, G316,, G10, G8, G6, G4, G2 G319, G317, G315,, G9, G78, G5, G3, G1





## 8.2.4. LCD Driving Wave Control (R02h)

R/W	RS	D1
W	1	0
Def	0	

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

.B/C 0: Frame/Field inversion

1: Line inversion

## 8.2.5. Entry Mode (R03h)

R/W	RS								
W	1								
Default									

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM Control the GRAM update direction.

When AM = "0", the address is updated in horizontal writing direction.

When AM = "1", the address is updated in vertical writing direction.

When a window area is set by registers R50h ~R53h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

I/D[1:0] Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.

	I/D[1:0] = 00 Horizontal: decrement Vertical: decrement	I/D[1:0] = 01 Horizontal: increment Vertical: decrement	I/D[1:0] = 10 Horizontal : decrement Vertical : increment	I/D[1:0] = 11 Horizontal : increment Vertical : increment
AM = 0 Horizontal	E	E E	B	B
AM = 1 Vertical				B

Figure 24 GRAM Access Direction Setting

**ORG** Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.

ORG = "0": The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.

ORG = "1": The original address "00000h" moves according to the I/D[1:0] setting.





Notes: 1. When ORG=1, only the origin address address"00000h" can be set in the RAM address set registers R20h, and R21h.

2. In RAM read operation, make sure to set ORG=0.

**BGR** Swap the R and B order of written data.

BGR="0": Follow the RGB order to write the pixel data.

BGR="1": Swap the RGB data to BGR in writing into GRAM.

**TRI** When TRI = "1", data are transferred to the internal RAM in 8-bit x 3 transfers mode via the 8-bit interface. It is also possible to send data via the 16-bit interface or SPI in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI = "0".

**DFM** Set the mode of transferring data to the internal RAM when TRI = "1". See the following figures for details.

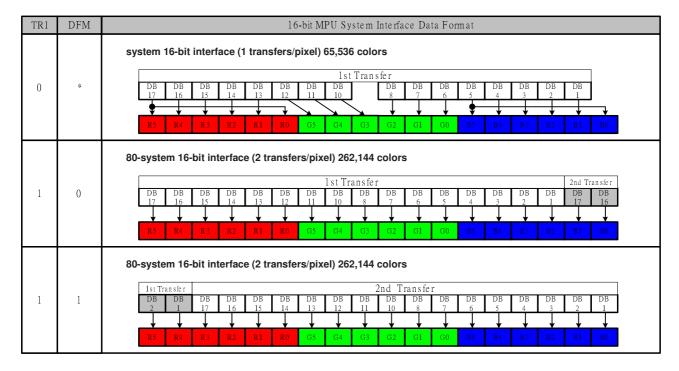


Figure 25 16-bit MPU System Interface Data Format

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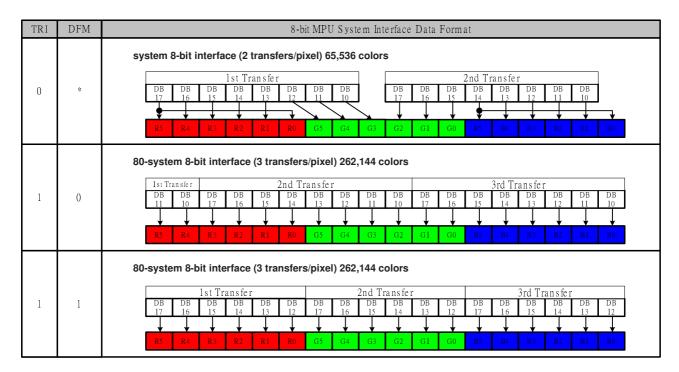


Figure 26 8-bit MPU System Interface Data Format

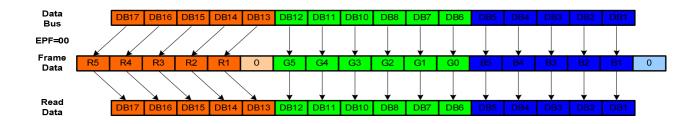
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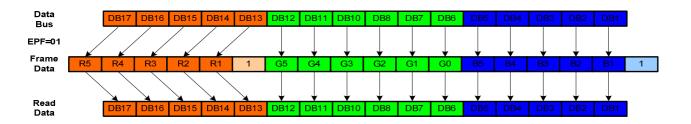


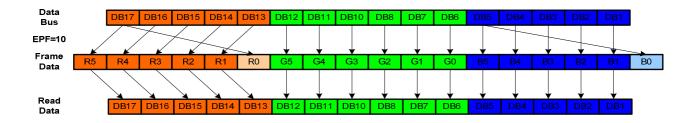


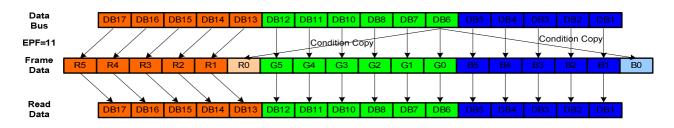
## 8.2.6. 16bits Data Format Selection (R05h)

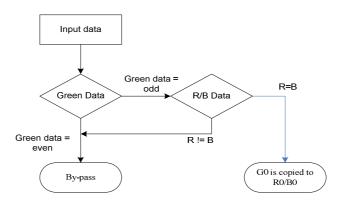
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FPF1	EPF0
Def	ault	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0















## 8.2.7. Display Control 1 (R07h)

R/W	RS
W	1
Defa	ault

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**D[1:0]** Set D[1:0]="11" to turn on the display panel, and D[1:0]="00" to turn off the display panel.

A graphics display is turned on the panel when writing D1 = "1", and is turned off when writing D1 = "0".

When writing D1 = "0", the graphics display data is retained in the internal GRAM and the ILI9325C displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D[1:0] = "01", the ILI9325C continues internal display operation. When the display is turned off by setting D[1:0] = "00", the ILI9325C internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF.

D1	D0	BASEE	Source, VCOM Output	ILI9325C internal operation
0	0	0	GND	Halt
0	1	1	GND	Operate
1	0	0	Non-lit display	Operate
1	1	0	Non-lit display	Operate
1	1	1	Base image display	Operate

Note: 1. data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

- 2. The D[1:0] setting is valid on both 1<sup>st</sup> and 2<sup>nd</sup> displays.
- 3. The non-lit display level from the source output pins is determined by instruction (PTS).

**CL** When CL = "1", the 8-color display mode is selected.

CL	Colors
0	262,144
1	8

GON and DTE Set the output level of gate driver G1 ~ G320 as follows

GON	DTE	G1 ~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal Display

#### **BASEE**

Base image display enable bit. When BASEE = "0", no base image is displayed. The ILI9325C drives liquid crystal at non-lit display level or displays only partial images. When BASEE = "1", the base image is displayed. The D[1:0] setting has higher priority over the BASEE setting.





### PTDE[1:0]

Partial image 2 and Partial image 1 enable bits

PTDE1/0 = 0: turns off partial image. Only base image is displayed.

PTDE1/0 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

## 8.2.8. Display Control 2 (R08h)

R/W	RS					
W	1					
Default						

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

### FP[3:0]/BP[3:0]

The FP[3:0] and BP[3:0] bits specify the line number of front and back porch periods respectively.

When setting the FP[3:0] and BP[3:0] value, the following conditions shall be met:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

## Set the BP[3:0] and FP[3:0] bits as below for each operation modes

Operation Mode	BP	FP	BP+FP
I80 System Interface Operation Mode	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
RGB interface Operation	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface Operation	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

FP[3:0]	Number of lines for Front Porch	
BP[3:0]	Number of lines for Back Porch	
0000	Setting Prohibited	
0001	Setting Prohibited	Back Porch
0010	2 lines	
0011	3 lines	
0100	4 lines	_
0101	5 lines	_ Display Area
0110	6 lines	_
0111	7 lines	
1000	8 lines	Front Porch
1001	9 lines	
1010	10 lines	_
1011	11 lines	
1100	12 lines	Note: The output timing to the LCD is delayed by 2
1101	13 lines	lines period from the input of synchronizing signal.
1110	14 lines	
1111	Setting Prohibited	





## 8.2.9. Display Control 3 (R09h)

R/W	RS
W	1
Defa	ault

D.	15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
(	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
(	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**ISC[3:0]:** Specify the scan cycle interval of gate driver in non-display area when PTG[1:0]="10" to select interval scan. Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f <sub>FLM</sub> =60 Hz
0	0	0	0	0 frame	=
0	0	0	1	0 frame	-
0	0	1	0	3 frame	50ms
0	0	1	1	5 frame	84ms
0	1	0	0	7 frame	117ms
0	1	0	1	9 frame	150ms
0	1	1	0	11 frame	184ms
0	1	1	1	13 frame	217ms
1	0	0	0	15 frame	251ms
1	0	0	1	17 frame	284ms
1	0	1	0	19 frame	317ms
1	0	1	1	21 frame	351ms
1	1	0	0	23 frame	384ms
1	1	0	1	25 frame	418ms
1	1	1	0	27 frame	451ms
1	1	1	1	29 frame	484ms

### PTG[1:0] Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	Vcom output
0	0	Normal scan	Set with the PTS[1:0] bits	VcomH/VcomL
0	1	Setting Prohibited	-	-
1	0	Interval scan	Set with the PTS[1:0] bits	VcomH/VcomL
1	1	Setting Prohibited	-	-

## PTS[1:0]

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

.

PTS[1:0]		SOURCE / VCOM output level in non-display area driver period		
00	frame with gate scan	white		
00	frame without gate scan	V63 / VCOML		
01	frame with gate scan	black		
01	frame without gate scan	V0 / VCOML		
10	frame with gate scan	white		
10	frame without gate scan	GND / GND		
11	frame with gate scan	white		
	frame without gate scan	Hi-Z / Hi-Z		



## 8.2.10. Display Control 4 (R0Ah)

R/W	RS				
W	1				
Default					

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**FMI[2:0]** Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

**FMARKOE** When FMARKOE=1, ILI9325C starts to output FMARK signal in the output interval set by FMI[2:0] bits.

FMI[2:0]	Output Interval
000	1 frame
001	2 frame
011	4 frame
101	6 frame
Others	Setting disabled

## 8.2.11. RGB Display Interface Control 1 (R0Ch)

R/W	RS				
W	1				
Default					

						-									-
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0] Select the RGB interface data width.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (1 transfer/pixel), DB[17:0]
0	1	16-bit RGB interface (1 transfer/pixel), DB[17:13] and DB[11:1]
1	0	6-bit RGB interface (3 transfers/pixel), DB[17:12]
1	1	Setting disabled

Note1: Registers are set only by the system interface.

Note2: Be sure that one pixel (3 dots) data transfer finished when interface switch.

### **DM[1:0]** Select the display operation mode.

DM1	DM0	Display Interface
0	0	Internal system clock
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM Select the interface to access the GRAM.

Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
----	--------------------------





0	System interface/VSYNC interface
1	RGB interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0]				
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)				
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)				
Rewrite still picture Displaying moving	e area while RGB interface pictures.	System interface (RM = 0)	RGB interface (DM[1:0] = 01)				
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)				

Note 1: Registers are set only via the system interface or SPI interface.

Note 2: Refer to the flowcharts of "RGB Input Interface" section for the mode switch.

### ENC[2:0] Set the GRAM write cycle through the RGB interface

ENC[2:0]	GRAM Write Cycle (Frame periods)
000	1 Frame
001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

## 8.2.12. Frame Marker Position (R0Dh)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
I	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Ī	Defa	ault	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**EMP[8:0]** Sets the output position of frame cycle (frame marker).

When FMP[8:0]=0, a high-active pulse FMARK is output at the start of back porch period for one display line period (1H).

Make sure the 9'h000  $\leq$  FMP  $\leq$  BP+NL+FP

FMP[8:0]	FMARK Output Position
9'h000	0 <sup>th</sup> line
9'h001	1 <sup>st</sup> line
9'h002	2 <sup>nd</sup> line
9'h003	3 <sup>rd</sup> line
_	
9'h175	373 <sup>rd</sup> line
9'h176	374 <sup>th</sup> line
9'h177	375 <sup>th</sup> line

## 8.2.13. RGB Display Interface Control 2 (R0Fh)

								_ `									
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0





Ī	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
	Defa	ult	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**DPL:** Sets the signal polarity of the DOTCLK pin.

DPL = "0" The data is input on the rising edge of DOTCLK

DPL = "1" The data is input on the falling edge of DOTCLK

**EPL:** Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB17-0 is written when ENABLE = "0". Disable data write operation when

ENABLE = "1".

EPL = "1" The data DB17-0 is written when ENABLE = "1". Disable data write operation when

ENABLE = "0".

**HSPL:** Sets the signal polarity of the HSYNC pin.

HSPL = "0" Low active

HSPL = "1" High active

**VSPL:** Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active

VSPL = "1" High active

### 8.2.14. Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
Def	ault	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**SLP:** When SLP = 1, ILI9325C enters the sleep mode and the display operation stops except the RC oscillator to reduce the power consumption. In the sleep mode, the GRAM data and instructions cannot be updated except the following instruction.

a. Exit sleep mode (SLP = "0")

**STB:** When STB = 1, ILI9325C enters the standby mode and the display operation stops except the GRAM power supply to reduce the power consumption. In the STB mode, the GRAM data and instructions cannot be updated except the following instruction.

a. Exit standby mode (STB = "0")

**AP[2:0]:** Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = "000" to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	Gamma driver amplifiers	Source driver amplifiers
000	Halt	Halt
001	1.00	1.00
010	1.00	0.75
011	1.00	0.50
100	0.75	1.00





101	0.75	0.75
110	0.75	0.50
111	0.50	0.50

SAP: Source Driver output control

SAP=0, Source driver is disabled.

SAP=1, Source driver is enabled.

When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

APE: Power supply enable bit.

Set APE = "1" to start the generation of power supply according to the power supply startup sequence.

BT[3:0]: Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	VCI1 x 2	- VCI1		- VCI1 x 5
3'h1	VOI4 :: 0	VCII x 6	- VCI1 x 4	
3'h2	VCI1 x 2	- VCI1		- VCI1 x 3
3'h3				- VCI1 x 5
3'h4	VCI1 x 2	- VCI1	VCI1 x 5	- VCI1 x 4
3'h5				- VCI1 x 3
3'h6	VCI1 x 2	VOI4	VOI1 1	- VCI1 x 4
3'h7	VCIT X 2	- VCI1	VCI1 x 4	- VCI1 x 3

Notes: 1. Connect capacitors to the capacitor connection pins when generating DDVDH, VGH, VGL and VCL levels.

2. Make sure DDVDH = 6.0V (max.),

### 8.2.15. Power Control 2 (R11h)

R/W	RS
W	1
Defa	ault

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0

#### **VC[2:0]** Sets the ratio factor of VCI to generate the reference voltages VCI1.

VC2	VC1	VC0	VCI1 voltage
0	0	0	0.95 x VCI
0	0	1	0.90 x VCI
0	1	0	0.85 x VCI
0	1	1	0.80 x VCI
1	0	0	0.75 x VCI
1	0	1	0.70 x VCI
1	1	0	Disabled
1	1	1	1.0 x VCI





**DC0[2:0]:** Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

**DC1[2:0]:** Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC02	DC01	DC00	Step-up circuit1 step-up frequency (f <sub>DCDC1</sub> )
0	0	0	Fosc
0	0	1	Fosc / 2
0	1	0	Fosc / 4
0	1	1	Fosc / 8
1	0	0	Fosc / 16
1	0	1	Fosc / 32
1	1	0	Fosc / 64
1	1	1	Halt step-up circuit 1

DC12	DC11	DC10	Step-up circuit2 step-up frequency (f <sub>DCDC2</sub> )
0	0	0	Fosc / 4
0	0	1	Fosc / 8
0	1	0	Fosc / 16
0	1	1	Fosc / 32
1	0	0	Fosc / 64
1	0	1	Fosc / 128
1	1	0	Fosc / 256
1	1	1	Halt step-up circuit 2

Note: Be sure f<sub>DCDC1</sub>≥f<sub>DCDC2</sub> when setting DC0[2:0] and DC1[2:0].

### 8.2.16. Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
Defa	ault	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**VRH[3:0]** Set the amplifying rate (1.6 ~ 1.9) of VCI applied to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VCIRE: Select the external reference voltage VCI or internal reference voltage VCIR.

VCIRE=0	External reference voltage VCI (default)
VCIRE =1	Internal reference voltage 2.5V

	VCIRE =0											
VRH3	VRH2	VRH1	VRH0	VREG10UT								
0	0	0	0	Halt								
0	0	0	1	VCI x 2.00								
0	0	1	0	VCI x 2.05								
0	0	1	1	VCI x 2.10								
0	1	0	0	VCI x 2.20								
0	1	0	1	VCI x 2.30								
0	1	1	0	VCI x 2.40								
0	1	1	1	VCI x 2.40								
1	0	0	0	VCI x 1.60								
1	0	0	1	VCI x 1.65								
1	0	1	0	VCI x 1.70								
1	0	1	1	VCI x 1.75								
1	1	0	0	VCI x 1.80								

		V	CIRE =1	
VRH3	VRH2	VRH1	VRH0	VREG10UT
0	0	0	0	Halt
0	0	0	1	2.5V x 2.00 = 5.000V
0	0	1	0	2.5V x 2.05 = 5.125V
0	0	1	1	2.5V x 2.10 = 5.250V
0	1	0	0	2.5V x 2.20 = 5.500V
0	1	0	1	2.5V x 2.30 = 5.750V
0	1	1	0	2.5V x 2.40 = 6.000V
0	1	1	1	2.5V x 2.40 = 6.000V
1	0	0	0	2.5V x 1.60 = 4.000V
1	0	0	1	2.5V x 1.65 = 4.125V
1	0	1	0	2.5V x 1.70 = 4.250V
1	0	1	1	2.5V x 1.75 = 4.375V
1	1	0	0	2.5V x 1.80 = 4.500V

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1	1	0	1	VCI x 1.85
1	1	1	0	VCI x 1.90
1	1	1	1	VCI x 1.95

1	1	0	1	2.5V x 1.85 = 4.625V
1	1	1	0	2.5V x 1.90 = 4.750V
1	1	1	1	2.5V x 1.95 = 4.875V

When VCI<2.5V, Internal reference voltage will be same as VCI.

Make sure that VC and VRH setting restriction:  $VREG1OUT \leq (DDVDH - 0.2)V$ .

## 8.2.17. Power Control 4 (R13h)

R/W	RS
W	1
Defa	ault

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**VDV[4:0]** Select the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.70 to 1.24 x VREG1OUT.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
1	0	0	0	0	VREG1OUT x 0.94
1	0	0	0	1	VREG1OUT x 0.96
1	0	0	1	0	VREG1OUT x 0.98
1	0	0	1	1	VREG1OUT x 1.00
1	0	1	0	0	VREG1OUT x 1.02
1	0	1	0	1	VREG1OUT x 1.04
1	0	1	1	0	VREG1OUT x 1.06
1	0	1	1	1	VREG1OUT x 1.08
1	1	0	0	0	VREG1OUT x 1.10
1	1	0	0	1	VREG1OUT x 1.12
1	1	0	1	0	VREG1OUT x 1.14
1	1	0	1	1	VREG1OUT x 1.16
1	1	1	0	0	VREG1OUT x 1.18
1	1	1	0	1	VREG1OUT x 1.20
1	1	1	1	0	VREG1OUT x 1.22
1	1	1	1	1	VREG1OUT x 1.24

Set VDV[4:0] to let Vcom amplitude less than 6V.

### 8.2.18. GRAM Horizontal/Vertical Address Set (R20h, R21h)

R/W	RS
W	1
W	1
Defa	ault

ĺ	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
I	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Ī	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
I	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**AD[16:0]** Set the initial value of address counter (AC).

The address counter (AC) is automatically updated in accordance to the setting of the AM, I/D bits as data is written to the internal GRAM. The address counter is not automatically updated when read data from the internal GRAM.

AD[16:0]	GRAM Data Map
17'h00000 ~ 17'h000EF	1 <sup>st</sup> line GRAM Data
17'h00100 ~ 17'h001EF	2 <sup>nd</sup> line GRAM Data
17'h00200 ~ 17'h002EF	3 <sup>rd</sup> line GRAM Data





17'h00300 ~ 17'h003EF	4 <sup>th</sup> line GRAM Data
17'h13D00 ~ 17' h13DEF	318 <sup>th</sup> line GRAM Data
17'h13E00 ~ 17' h13EEF	319 <sup>th</sup> line GRAM Data
17'h13F00 ~ 17'h13FEF	320 <sup>th</sup> line GRAM Data

Note1: When the RGB interface is selected (RM = "1"), the address AD[16:0] is set to the address counter every frame on the falling edge of VSYNC.

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### 8.2.19. Write Data to GRAM (R22h)

F	R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	W	1		RAM write data (WD[17:0], the DB[17:0] pin assignment differs for each interface.																

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

### 8.2.20. Read Data from GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1		RAM Read Data (RD[17:0], the DB[17:0] pin assignment differs for each interface.																

RD[17:0] Read 18-bit data from GRAM through the read data register (RDR).



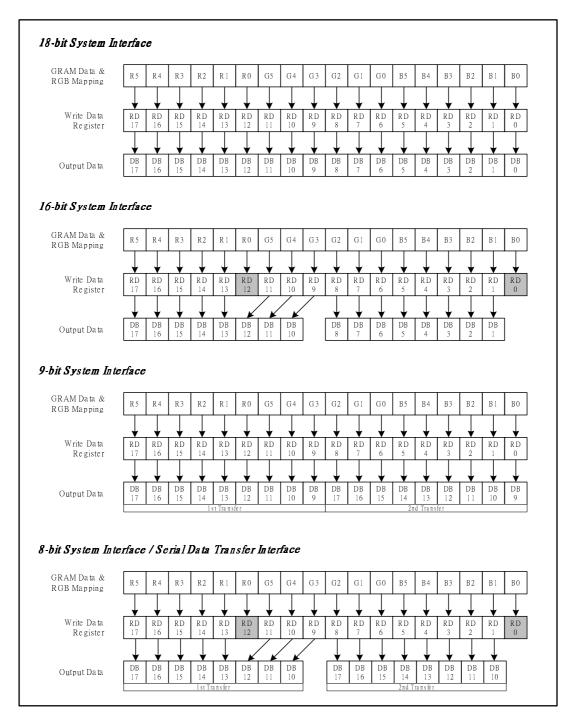


Figure 27 Data Read from GRAM through Read Data Register in 18-/16-/9-/8-bit Interface Mode

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V0.07

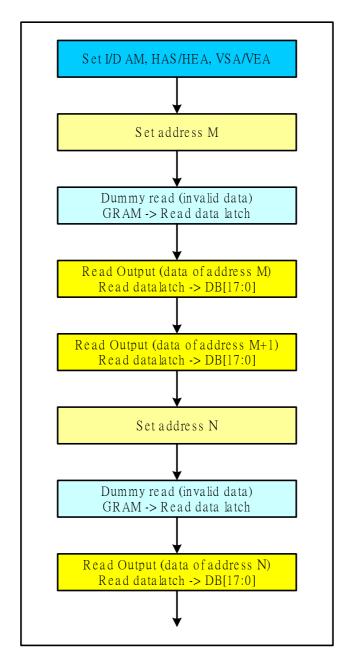


Figure 28 GRAM Data Read Back Flow Chart

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## 8.2.21. Power Control 7 (R29h)

R/	W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
٧	٧	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	Defa	ult	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM[5:0] Set the internal VcomH voltage.

	[0.0]	001 1.	.0	iiiai v		i voltage.
VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	VREG1OUT x 0.685
0	0	0	0	0	1	VREG1OUT x 0.690
0	0	0	0	1	0	VREG1OUT x 0.695
0	0	0	0	1	1	VREG1OUT x 0.700
0	0	0	1	0	0	VREG1OUT x 0.705
0	0	0	1	0	1	VREG1OUT x 0.710
0	0	0	1	1	0	VREG1OUT x 0.715
0	0	0	1	1	1	VREG1OUT x 0.720
0	0	1	0	0	0	VREG1OUT x 0.725
0	0	1	0	0	1	VREG1OUT x 0.730
0	0	1	0	1	0	VREG1OUT x 0.735
0	0	1	0	1	1	VREG1OUT x 0.740
0	0	1	1	0	0	VREG1OUT x 0.745
0	0	1	1	0	1	VREG1OUT x 0.750
0	0	1	1	1	0	VREG1OUT x 0.755
0	0	1	1	1	1	VREG1OUT x 0.760
0	1	0	0	0	0	VREG1OUT x 0.765
0	1	0	0	0	1	VREG1OUT x 0.770
0	1	0	0	1	0	VREG1OUT x 0.775
0	1	0	0	1	1	VREG1OUT x 0.780
0	1	0	1	0	0	VREG1OUT x 0.785
0	1	0	1	0	1	VREG1OUT x 0.790
0	1	0	1	1	0	VREG1OUT x 0.795
0	1	0	1	1	1	VREG1OUT x 0.800
0	1	1	0	0	0	VREG1OUT x 0.805
0	1	1	0	0	1	VREG1OUT x 0.810
0	1	1	0	1	0	VREG1OUT x 0.815
0	1	1	0	1	1	VREG1OUT x 0.820
0	1	1	1	0	0	VREG1OUT x 0.825
0	1	1	1	0	1	VREG1OUT x 0.830
0	1	1	1	1	0	VREG1OUT x 0.835
0	1	1	1	1	1	VREG1OUT x 0.840

VCM5         VCM4         VCM3         VCM2         VCM1         VCM0         VCOMH           1         0         0         0         0         VREG1OUT         x 0.845           1         0         0         0         1         VREG1OUT         x 0.850           1         0         0         0         1         0         VREG1OUT         x 0.865           1         0         0         1         0         0         VREG1OUT         x 0.866           1         0         0         1         0         0         VREG1OUT         x 0.865           1         0         0         1         0         VREG1OUT         x 0.870           1         0         0         1         0         VREG1OUT         x 0.875           1         0         0         1         1         VREG1OUT         x 0.880           1         0         1         0         0         VREG1OUT         x 0.885           1         0         1         0         1         VREG1OUT         x 0.895           1         0         1         0         1         VREG1OUT         x 0.905 <th></th> <th>1</th> <th>1</th> <th></th> <th></th> <th></th> <th></th>		1	1				
1         0         0         0         1         VREGIOUT x 0.850           1         0         0         0         1         0         VREGIOUT x 0.865           1         0         0         0         1         1         VREGIOUT x 0.860           1         0         0         1         0         VREGIOUT x 0.865           1         0         0         1         0         VREGIOUT x 0.870           1         0         0         1         0         VREGIOUT x 0.870           1         0         0         1         0         VREGIOUT x 0.875           1         0         0         1         1         VREGIOUT x 0.880           1         0         1         0         0         VREGIOUT x 0.880           1         0         1         0         0         VREGIOUT x 0.880           1         0         1         0         0         VREGIOUT x 0.885           1         0         1         0         0         VREGIOUT x 0.895           1         0         1         0         1         VREGIOUT x 0.990           1         0         1         1 <td>VCM5</td> <td>VCM4</td> <td>VCM3</td> <td>VCM2</td> <td>VCM1</td> <td>VCM0</td> <td>VCOMH</td>	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
1         0         0         0         1         0         VREG1OUT x 0.855           1         0         0         0         1         1         VREG1OUT x 0.866           1         0         0         1         0         VREG1OUT x 0.870           1         0         0         1         0         VREG1OUT x 0.870           1         0         0         1         0         VREG1OUT x 0.870           1         0         0         1         1         VREG1OUT x 0.887           1         0         1         0         0         VREG1OUT x 0.880           1         0         1         0         0         VREG1OUT x 0.885           1         0         1         0         0         VREG1OUT x 0.890           1         0         1         0         0         VREG1OUT x 0.885           1         0         1         0         0         VREG1OUT x 0.895           1         0         1         1         VREG1OUT x 0.990           1         0         1         1         VREG1OUT x 0.910           1         0         1         1         1         VREG	1	0	0	0	0	0	VREG1OUT x 0.845
1         0         0         1         1         VREG1OUT x 0.866           1         0         0         1         0         0         VREG1OUT x 0.875           1         0         0         1         1         VREG1OUT x 0.875           1         0         0         1         1         VREG1OUT x 0.885           1         0         1         0         0         VREG1OUT x 0.885           1         0         1         0         0         VREG1OUT x 0.890           1         0         1         0         1         VREG1OUT x 0.895           1         0         1         0         1         VREG1OUT x 0.990           1         0         1         0         1         VREG1OUT x 0.990           1         0         1         1         VREG1OUT x 0.990           1         0         1         1         VREG1OUT x 0.990           1         0         1         1         VREG1OUT x 0.991           1         0         1         1         1         VREG1OUT x 0.991           1         1         0         0         0         VREG1OUT x 0.995	1	0	0	0	0	1	VREG1OUT x 0.850
1         0         0         1         0         VREG1OUT x 0.865           1         0         0         1         VREG1OUT x 0.870           1         0         0         1         1         VREG1OUT x 0.875           1         0         0         1         1         VREG1OUT x 0.880           1         0         1         0         0         VREG1OUT x 0.885           1         0         1         0         0         VREG1OUT x 0.890           1         0         1         0         1         VREG1OUT x 0.895           1         0         1         0         1         VREG1OUT x 0.990           1         0         1         0         1         VREG1OUT x 0.990           1         0         1         1         VREG1OUT x 0.990           1         0         1         1         VREG1OUT x 0.991           1         0         1         1         VREG1OUT x 0.991           1         0         1         1         1         VREG1OUT x 0.991           1         1         0         0         0         VREG1OUT x 0.995           1         1	1	0	0	0	1	0	VREG1OUT x 0.855
1         0         0         1         VREG1OUT         x 0.870           1         0         0         1         1         0         VREG1OUT         x 0.875           1         0         0         1         1         1         VREG1OUT         x 0.880           1         0         1         0         0         0         VREG1OUT         x 0.885           1         0         1         0         1         0         VREG1OUT         x 0.895           1         0         1         0         1         0         VREG1OUT         x 0.895           1         0         1         0         1         0         VREG1OUT         x 0.990           1         0         1         0         1         1         VREG1OUT         x 0.905           1         0         1         1         0         0         VREG1OUT         x 0.905           1         0         1         1         0         1         VREG1OUT         x 0.915           1         0         1         1         1         1         1         VREG1OUT         x 0.925           1 <td< td=""><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>VREG1OUT x 0.860</td></td<>	1	0	0	0	1	1	VREG1OUT x 0.860
1         0         0         1         1         0         VREG1OUT x 0.875           1         0         0         1         1         1         VREG1OUT x 0.880           1         0         1         0         0         VREG1OUT x 0.885           1         0         1         0         1         VREG1OUT x 0.890           1         0         1         0         1         0         VREG1OUT x 0.990           1         0         1         0         1         1         VREG1OUT x 0.900           1         0         1         1         0         1         VREG1OUT x 0.900           1         0         1         1         0         0         VREG1OUT x 0.900           1         0         1         1         0         0         VREG1OUT x 0.910           1         0         1         1         1         0         VREG1OUT x 0.910           1         0         1         1         1         0         VREG1OUT x 0.915           1         1         0         1         1         VREG1OUT x 0.920           1         1         0         0	1	0	0	1	0	0	VREG1OUT x 0.865
1         0         0         1         1         1         VREG1OUT x 0.880           1         0         1         0         0         0         VREG1OUT x 0.885           1         0         1         0         1         VREG1OUT x 0.890           1         0         1         0         1         VREG1OUT x 0.895           1         0         1         0         1         VREG1OUT x 0.900           1         0         1         1         VREG1OUT x 0.905           1         0         1         1         VREG1OUT x 0.905           1         0         1         1         0         VREG1OUT x 0.905           1         0         1         1         0         VREG1OUT x 0.915           1         0         1         1         1         VREG1OUT x 0.915           1         1         0         0         0         VREG1OUT x 0.915           1         1         0         0         0         VREG1OUT x 0.920           1         1         0         0         0         VREG1OUT x 0.920           1         1         0         0         0         VREG	1	0	0	1	0	1	VREG1OUT x 0.870
1         0         1         0         0         VREG1OUT x 0.885           1         0         1         0         0         1         VREG1OUT x 0.890           1         0         1         0         1         0         VREG1OUT x 0.895           1         0         1         0         1         1         VREG1OUT x 0.900           1         0         1         1         0         0         VREG1OUT x 0.905           1         0         1         1         0         0         VREG1OUT x 0.910           1         0         1         1         0         1         VREG1OUT x 0.910           1         0         1         1         1         0         VREG1OUT x 0.910           1         0         1         1         1         0         VREG1OUT x 0.915           1         0         1         1         1         1         VREG1OUT x 0.920           1         1         0         0         0         VREG1OUT x 0.925           1         1         0         0         0         VREG1OUT x 0.935           1         1         0         1	1	0	0	1	1	0	VREG1OUT x 0.875
1         0         1         0         1         VREG1OUT x 0.890           1         0         1         0         1         0         VREG1OUT x 0.895           1         0         1         0         1         1         VREG1OUT x 0.900           1         0         1         1         0         VREG1OUT x 0.905           1         0         1         1         0         VREG1OUT x 0.910           1         0         1         1         0         VREG1OUT x 0.910           1         0         1         1         0         VREG1OUT x 0.910           1         0         1         1         0         VREG1OUT x 0.915           1         1         0         0         0         VREG1OUT x 0.920           1         1         0         0         0         VREG1OUT x 0.930           1         1         0         0 <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>VREG1OUT x 0.880</td>	1	0	0	1	1	1	VREG1OUT x 0.880
1         0         1         0         VREG1OUT         x 0.895           1         0         1         0         VREG1OUT         x 0.900           1         0         1         1         VREG1OUT         x 0.905           1         0         1         1         VREG1OUT         x 0.910           1         0         1         1         0         VREG1OUT         x 0.910           1         0         1         1         1         0         VREG1OUT         x 0.915           1         0         1         1         1         VREG1OUT         x 0.920           1         1         0         0         0         VREG1OUT         x 0.920           1         1         0         0         0         VREG1OUT         x 0.920           1         1         0         0         0         VREG1OUT         x 0.925           1         1         0         0         0         VREG1OUT         x 0.935           1         1         0         0         1         VREG1OUT         x 0.940           1         1         0         1         0         VREG1	1	0	1	0	0	0	VREG1OUT x 0.885
1         0         1         0         1         1         VREG1OUT x 0.900           1         0         1         1         VREG1OUT x 0.905           1         0         1         1         VREG1OUT x 0.910           1         0         1         1         VREG1OUT x 0.915           1         0         1         1         VREG1OUT x 0.920           1         1         0         0         0         VREG1OUT x 0.932           1         1         0         0         1         VREG1OUT x 0.935           1         1         0         1         1         VREG1OUT x 0.940           1         1         0         1         1         VREG1OUT x 0.945           1	1	0	1	0	0	1	VREG1OUT x 0.890
1         0         1         1         0         0         VREG1OUT x 0.905           1         0         1         1         0         1         VREG1OUT x 0.910           1         0         1         1         1         0.915           1         0         1         1         1         VREG1OUT x 0.915           1         1         0         0         0         VREG1OUT x 0.920           1         1         0         0         0         VREG1OUT x 0.922           1         1         0         0         0         VREG1OUT x 0.925           1         1         0         0         1         VREG1OUT x 0.930           1         1         0         0         1         VREG1OUT x 0.935           1         1         0         0         1         VREG1OUT x 0.940           1         1         0         1         1         VREG1OUT x 0.935           1         1         0         1         0         VREG1OUT x 0.945           1         1         0         1         1         VREG1OUT x 0.955           1         1         0         1	1	0	1	0	1	0	VREG1OUT x 0.895
1         0         1         1         VREG1OUT x 0.910           1         0         1         1         0         VREG1OUT x 0.915           1         0         1         1         1         VREG1OUT x 0.920           1         1         0         0         0         VREG1OUT x 0.925           1         1         0         0         1         VREG1OUT x 0.930           1         1         0         0         1         VREG1OUT x 0.930           1         1         0         0         1         VREG1OUT x 0.935           1         1         0         0         1         VREG1OUT x 0.940           1         1         0         0         1         VREG1OUT x 0.940           1         1         0         1         0         VREG1OUT x 0.940           1         1         0         1         0         VREG1OUT x 0.940           1         1         0         1         0         VREG1OUT x 0.945           1         1         0         1         0         VREG1OUT x 0.950           1         1         0         1         1         0         VREG	1	0	1	0	1	1	VREG1OUT x 0.900
1         0         1         1         1         0         VREG1OUT x 0.915           1         0         1         1         1         VREG1OUT x 0.920           1         1         0         0         0         VREG1OUT x 0.925           1         1         0         0         1         VREG1OUT x 0.930           1         1         0         0         1         VREG1OUT x 0.930           1         1         0         0         1         VREG1OUT x 0.935           1         1         0         0         1         VREG1OUT x 0.940           1         1         0         1         0         VREG1OUT x 0.945           1         1         0         1         0         VREG1OUT x 0.950           1         1         0         1         1         VREG1OUT x 0.960           1         1         1         0         0 <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>VREG1OUT x 0.905</td>	1	0	1	1	0	0	VREG1OUT x 0.905
1         0         1         1         1         VREG1OUT x 0.920           1         1         0         0         0         VREG1OUT x 0.920           1         1         0         0         0         VREG1OUT x 0.930           1         1         0         0         1         VREG1OUT x 0.930           1         1         0         0         1         VREG1OUT x 0.935           1         1         0         0         1         VREG1OUT x 0.940           1         1         0         1         0         VREG1OUT x 0.950           1         1         0         1         1         VREG1OUT x 0.960           1         1         1         0         0         VREG1OUT x 0.970           1         1         1         0         1         VREG	1	0	1	1	0	1	VREG1OUT x 0.910
1         1         0         0         0         VREG1OUT x 0.925           1         1         0         0         1         VREG1OUT x 0.930           1         1         0         0         1         VREG1OUT x 0.935           1         1         0         0         1         VREG1OUT x 0.940           1         1         0         1         0         VREG1OUT x 0.945           1         1         0         1         0         VREG1OUT x 0.955           1         1         0         1         1         VREG1OUT x 0.960           1         1         0         1         1         VREG1OUT x 0.965           1         1         1         0         0         VREG1OUT x 0.970           1         1         1         0         1         VREG1OUT x 0.975           1         1         1         0         1         VREG1OUT x 0.980           1         1         1         0         0         VREG1OUT x 0.985           1         1         1         0         0         VREG1OUT x 0.990           1         1         1         1         0         0 <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>VREG1OUT x 0.915</td>	1	0	1	1	1	0	VREG1OUT x 0.915
1         1         0         0         0         1         VREG1OUT x 0.930           1         1         0         0         1         0         VREG1OUT x 0.935           1         1         0         0         1         1         VREG1OUT x 0.940           1         1         0         1         0         VREG1OUT x 0.945           1         1         0         1         0         VREG1OUT x 0.950           1         1         0         1         1         0         VREG1OUT x 0.955           1         1         0         1         1         VREG1OUT x 0.960           1         1         1         0         0         VREG1OUT x 0.965           1         1         1         0         0         VREG1OUT x 0.970           1         1         1         0         1         VREG1OUT x 0.975           1         1         1         0         1         VREG1OUT x 0.980           1         1         1         0         1         VREG1OUT x 0.990           1         1         1         1         0         1         VREG1OUT x 0.995	1	0	1	1	1	1	VREG1OUT x 0.920
1         1         0         0         1         0         VREG1OUT x 0.935           1         1         0         0         1         1         VREG1OUT x 0.940           1         1         0         1         0         VREG1OUT x 0.945           1         1         0         1         VREG1OUT x 0.950           1         1         0         1         1         VREG1OUT x 0.955           1         1         0         1         1         VREG1OUT x 0.960           1         1         1         0         0         VREG1OUT x 0.965           1         1         1         0         0         VREG1OUT x 0.970           1         1         1         0         1         VREG1OUT x 0.975           1         1         1         0         1         VREG1OUT x 0.980           1         1         1         1         0         VREG1OUT x 0.995           1         1         1         1         0         VREG1OUT x 0.990           1         1         1         1         0         VREG1OUT x 0.995	1	1	0	0	0	0	VREG1OUT x 0.925
1         1         0         0         1         1         VREG1OUT x 0.940           1         1         0         1         0         VREG1OUT x 0.945           1         1         0         1         0         VREG1OUT x 0.950           1         1         0         1         1         0.955           1         1         0         1         1         VREG1OUT x 0.955           1         1         1         0         0         VREG1OUT x 0.960           1         1         1         0         0         VREG1OUT x 0.965           1         1         1         0         0         1         VREG1OUT x 0.970           1         1         1         0         1         VREG1OUT x 0.975           1         1         1         0         1         VREG1OUT x 0.980           1         1         1         1         0         0         VREG1OUT x 0.995           1         1         1         1         0         1         VREG1OUT x 0.990           1         1         1         1         0         0         VREG1OUT x 0.995	1	1	0	0	0	1	VREG1OUT x 0.930
1         1         0         1         0         VREG1OUT x 0.945           1         1         0         1         VREG1OUT x 0.950           1         1         0         1         1         VREG1OUT x 0.955           1         1         0         1         1         VREG1OUT x 0.960           1         1         1         0         0         VREG1OUT x 0.965           1         1         1         0         0         1         VREG1OUT x 0.970           1         1         1         0         1         VREG1OUT x 0.975           1         1         1         0         1         VREG1OUT x 0.980           1         1         1         1         0         VREG1OUT x 0.985           1         1         1         1         0         VREG1OUT x 0.990           1         1         1         1         0         VREG1OUT x 0.995	1	1	0	0	1	0	VREG1OUT x 0.935
1         1         0         1         VREG1OUT x 0.950           1         1         0         1         1         0         VREG1OUT x 0.955           1         1         0         1         1         VREG1OUT x 0.960           1         1         1         0         0         VREG1OUT x 0.965           1         1         1         0         0         1         VREG1OUT x 0.970           1         1         1         0         1         0         VREG1OUT x 0.975           1         1         1         0         1         1         VREG1OUT x 0.980           1         1         1         1         0         0         VREG1OUT x 0.985           1         1         1         1         1         0         VREG1OUT x 0.990           1         1         1         1         1         0         VREG1OUT x 0.995	1	1	0	0	1	1	VREG1OUT x 0.940
1         1         0         1         1         0         VREG1OUT x 0.955           1         1         0         1         1         1         VREG1OUT x 0.960           1         1         1         0         0         VREG1OUT x 0.965           1         1         1         0         0         1         VREG1OUT x 0.970           1         1         1         0         1         0         VREG1OUT x 0.975           1         1         1         0         1         1         VREG1OUT x 0.980           1         1         1         1         0         0         VREG1OUT x 0.985           1         1         1         1         0         1         VREG1OUT x 0.990           1         1         1         1         1         0         VREG1OUT x 0.995	1	1	0	1	0	0	VREG1OUT x 0.945
1     1     0     1     1     1     VREG1OUT x 0.960       1     1     1     0     0     VREG1OUT x 0.965       1     1     1     0     0     1     VREG1OUT x 0.970       1     1     1     0     1     0     VREG1OUT x 0.975       1     1     1     0     1     1     VREG1OUT x 0.980       1     1     1     1     0     0     VREG1OUT x 0.985       1     1     1     1     0     1     VREG1OUT x 0.990       1     1     1     1     1     0     VREG1OUT x 0.995	1	1	0	1	0	1	VREG1OUT x 0.950
1         1         1         0         0         VREG1OUT x 0.965           1         1         1         0         0         1         VREG1OUT x 0.970           1         1         1         0         1         0         VREG1OUT x 0.975           1         1         1         0         1         1         VREG1OUT x 0.980           1         1         1         1         0         0         VREG1OUT x 0.985           1         1         1         1         0         1         VREG1OUT x 0.990           1         1         1         1         0         VREG1OUT x 0.995	1	1	0	1	1	0	VREG1OUT x 0.955
1         1         1         0         0         1         VREG1OUT x 0.970           1         1         1         0         1         0         VREG1OUT x 0.975           1         1         1         0         1         1         VREG1OUT x 0.980           1         1         1         1         0         0         VREG1OUT x 0.985           1         1         1         1         0         1         VREG1OUT x 0.990           1         1         1         1         0         VREG1OUT x 0.995	1	1	0	1	1	1	VREG1OUT x 0.960
1     1     1     0     1     0     VREG1OUT x 0.975       1     1     1     0     1     1     VREG1OUT x 0.980       1     1     1     1     0     0     VREG1OUT x 0.985       1     1     1     1     0     1     VREG1OUT x 0.990       1     1     1     1     1     0     VREG1OUT x 0.995	1	1	1	0	0	0	VREG1OUT x 0.965
1         1         1         0         1         1         VREG1OUT x 0.980           1         1         1         1         0         0         VREG1OUT x 0.985           1         1         1         1         0         1         VREG1OUT x 0.990           1         1         1         1         0         VREG1OUT x 0.995	1	1	1	0	0	1	VREG1OUT x 0.970
1         1         1         1         0         0         VREG1OUT x 0.985           1         1         1         1         0         1         VREG1OUT x 0.990           1         1         1         1         0         VREG1OUT x 0.995	1	1	1	0	1	0	VREG1OUT x 0.975
1 1 1 1 0 1 VREG1OUT x 0.990 1 1 1 1 1 0 VREG1OUT x 0.995	1	1	1	0	1	1	VREG1OUT x 0.980
1 1 1 1 0 VREG1OUT x 0.995	1	1	1	1	0	0	VREG1OUT x 0.985
	1	1	1	1	0	1	VREG1OUT x 0.990
1 1 1 1 1 VREGIOUT v 1 000	1	1	1	1	1	0	VREG1OUT x 0.995
I I I I I I I I I VILLATOOT X 1.000	1	1	1	1	1	1	VREG1OUT x 1.000

## 8.2.22. Frame Rate and Color Control (R2Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS3	FRS2	FRS1	FRS0
De	fault	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

FRS[4:0] Set the frame rate when the internal resistor is used for oscillator circuit.

FRS[3:0]	FRS[3:0]	Frame Rate
0000	4'h0	28
0001	4'h1	30
0010	4'h2	32
0011	4'h3	34
0100	4'h4	36
0101	4'h5	39
0110	4'h6	41
0111	4'h7	45
1000	4'h8	49
1001	4'h9	54
1010	4'hA	60
1011	4'hB	67
1100	4'hC	77
1101	4'hD	90
1110	4'hE	Setting Prohibited
1111	4'hF	Setting Prohibited





## 8.2.23. Gamma Control (R30h ~ R3Dh)

	R/W	RS
R30h	W	1
R31h	W	1
R32h	W	1
R35h	W	1
R36h	W	1
R37h	W	1
R38h	W	1
R39h	W	1
R3Ch	W	1
R3Dh	W	1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

KP5-0[2:0]:  $\gamma$  fine adjustment register for positive polarity

RP1-0[2:0]:  $\gamma$  gradient adjustment register for positive polarity

VRP1-0[4:0]:  $\gamma$  amplitude adjustment register for positive polarity

KN5-0[2:0]:  $\gamma$  fine adjustment register for negative polarity

RN1-0[2:0]:  $\gamma$  gradient adjustment register for negative polarity

VRN1-0[4:0]:  $\gamma$  amplitude adjustment register for negative polarity

For details " $\gamma$  -Correction Function" section.

## 8.2.24. Horizontal and Vertical RAM Address Position (R50h, R51h, R52h, R53h)

	R/W	RS
R50h	W	1
R51h	W	1
R52h	W	1
R53h	W	1
R50h		
R51h	Defa	sult
R52h	Dela	uii
R53h		

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

HSA[7:0]/HEA[7:0] HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure "00"h ≤ HSA[7:0] < "EF"h. and "01"h≤HEA-HAS.

VSA[8:0]/VEA[8:0] VSA[8:0] and VEA[8:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure "000"  $h \le VSA[8:0] < VEA[8:0] \le "13F$ " h.

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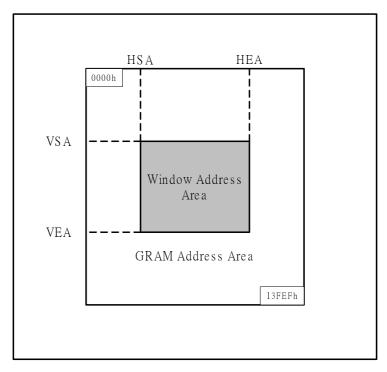


Figure 29 GRAM Access Range Configuration

"00"h ≤HSA[7:0] ≤HEA[7:0] ≤"EF"h "00"h ≤VSA[8:0] ≤VEA[8:0] ≤"13F"h

Note1. The window address range must be within the GRAM address space.

Note2. Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

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## 8.2.25. Gate Scan Control (R60h, R61h, R6Ah)

	R/W	RS
R60h	W	1
R61h	W	1
R6Ah	W	1
R60h		
R61h	Defa	ault
R6Ah		

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**SCN[5:0]** The ILI9325C allows to specify the gate line from which the gate driver starts to scan by setting the SCN[5:0] bits.

		Scanning S	tart Position	
SCN[5:0]	SM		SM	<b>1</b> =1
	GS=0	GS=1	GS=0	GS=1
00h	G1	G320	G1	G320
01h	G9	G312	G17	G304
02h	G17	G304	G33	G288
03h	G25	G296	G49	G272
04h	G33	G288	G65	G256
05h	G41	G280	G81	G240
06h	G49	G272	G97	G224
07h	G57	G264	G113	G208
08h	G65	G256	G129	G192
09h	G73	G248	G145	G176
0Ah	G81	G240	G161	G160
0Bh	G89	G232	G177	G144
0Ch	G97	G224	G193	G128
0Dh	G105	G216	G209	G112
0Eh	G113	G208	G2	G96
0Fh	G121	G200	G18	G80
10h	G129	G192	G34	G64
11h	G137	G184	G50	G48
12h	G145	G176	G66	G32
13h	G153	G168	G82	G16
14h	G161	G160	G98	G319
15h	G169	G152	G114	G303
16h	G177	G144	G130	G287
17h	G185	G136	G146	G271
18h	G193	G128	G162	G255
19h	G201	G120	G178	G239
1Ah	G209	G112	G194	G223
1Bh	G217	G104	G114	G207
1Ch	G225	G96	G130	G191
1Dh	G233	G88	G146	G175
1Eh	G241	G80	G162	G159
1Fh	G249	G72	G178	G143
20h	G257	G64	G194	G127
21h	G265	G56	G210	G111
22h	G273	G48	G226	G95
23h	G281	G40	G242	G79
24h	G289	G32	G258	G63
25h	G297	G24	G274	G47
26h	G305	G16	G290	G31
27h	G313	G8	G306	G15
28h ~ 3Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled

Note: When SM=1, it is a interlacing scanning. Please reference page 72!





**NL[5:0]:** Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00	8 lines
6'h01	16 lines
6'h02	24lines
6'h1D	240 lines
6'h1E	248 lines
6'h1F	256 lines
6'h20	264 lines
6'h21	272 lines
6'h22	280 lines
6'h23	288 lines
6'h24	296 lines
6'h25	304 lines
6'h26	312 line
6'h27	320 line
Others	Setting inhibited

NDL: Sets the source driver output level in the non-display area.

NDL	Non-Disp	olay Area
NDL	Positive Polarity	Negative Polarity
0	V63	V0
1	VO	V63

**GS:** Sets the direction of scan by the gate driver in the range determined by SCN[4:0] and NL[4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G320.

When GS = 1, the scan direction is from G320 to G1

**REV:** Enables the grayscale inversion of the image by setting REV=1.

REV	GRAM Data	Source Output in	Display Area
I IL V	CITANI Dala	Positive polarity	negative polarity
	18'h00000	V63	V0
	•	•	•
0			•
			•
	18'h3FFFF	V0	V63
	18'h00000	V0	V63
1	•		•
	18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the ILI9325C starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the





number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image Display
0	Fixed
1	Enable Scrolling

**VL[8:0]:** Sets the scrolling amount of base image. The base image is scrolled in vertical direction and displayed from the line determined by VL[8:0]. Make sure that VL[8:0]  $\leq 320$ .

### 8.2.26. SPI Read/Write Control (R66h, Write Only)

R/W	RS	_	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX

This register is used to control the read/write function of registers when the 8/9-bit serial interface is used. If users need to read back the register data by the 8/9-bit serial interface, the R/WX bit must be set as '1'.

R/WX	Description
0	Register write mode (default)
1	Register read mode

### 8.2.27. Partial Image 1 Display Position (R80h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	W	4	0	0	0	0	0	0	0	PTD								
	VV	ı	U	U	U	0	O	0	U	P0[8]	P0[7]	P0[6]	P0[5]	P0[4]	P0[3]	P0[2]	P0[1]	P0[0]
	Defa	ult	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
_																		

**PTDP0[8:0]:** Sets the display start position of partial image 1. The display areas of the partial images 1 and 2 must not overlap each another.

#### 8.2.28. Partial Image 1 RAM Start/End Address (R81h, R82h)

ı	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ŀ	Π/ V V	no	כום	D14	סוט	DIZ	ווט	סוט	Da									
ı	W	4	Λ	^	^	0	0	0	^	PTS								
l	VV	1	0	0	U	0	0	U	0	A0[8]	A0[7]	A0[6]	A0[5]	A0[4]	A0[3]	A0[2]	A0[1]	A0[0]
I	14/	4	0	0	0	0	0		•	PTE								
	W	'	U	U	U	U	U	U	0	A0[8]	A0[7]	A0[6]	A0[5]	A0[4]	A0[3]	A0[2]	A0[1]	A0[0]
I	Defa	v. 11+	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
L	Dela	tuit	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTSA0[8:0] PTEA0[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[8:0] ≤ PTEA0[8:0].

### 8.2.29. Partial Image 2 Display Position (R83h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	-1	0	0	0	0	0	0	0	PTD								
VV	1	U	0	U	0	U	U	U	P1[8]	P1[7]	P1[6]	P1[5]	P1[4]	P1[3]	P1[2]	P1[1]	P1[0]
Defa	ault	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0





D0 RTNI0

**PTDP1[8:0]:** Sets the display start position of partial image 2 The display areas of the partial images 1 and 2 must not overlap each another.

## 8.2.30. Partial Image 2 RAM Start/End Address (R84h, R85h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
w	1	0	0	0	0	0	0	0	PTS								
VV		U	U	0	U	0	U	U	A1[8]	A1[7]	A1[6]	A1[5]	A1[4]	A1[3]	A1[2]	A1[1]	A1[0]
w	1	_		0	0	0	0		PTE								
VV	'	U	U	U	U	U	U	0	A1[8]	A1[7]	A1[6]	A1[5]	A1[4]	A1[3]	A1[2]	A1[1]	A1[0]
Defa	l+	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Dela	auit	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**PTSA1[8:0] PTEA1[8:0]:** Sets the start line address and the end line address of the RAM area storing the data of partial image 2 Make sure PTSA1[8:0] ≤ PTEA1[8:0].

#### 8.2.31. Panel Interface Control 1 (R90h)

								,	,								
R/W	RS	3	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
W	1		0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1
Defa	ault		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

**RTNI[4:0]:** Sets 1H (line) clock number of internal clock operating mode. In this mode, ILI9325C display operation is synchronized with internal clock signal.

RTNI[4:0]	Clocks/Line
00000~01111	Setting Disabled
10000	16 clocks
10001	17 clocks
10010	18 clocks
10011	19 clocks
10100	20 clocks
10101	21 clocks
10110	22 clocks
10111	23 clocks

RTNI[4:0]	Clocks/Line
11000	24 clocks
11001	25 clocks
11010	26 clocks
11011	27 clocks
11100	28 clocks
11101	29 clocks
11110	30 clocks
11111	31 clocks

### **DIVI[1:0]:** Sets the division ratio of internal clock frequency.

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

### 8.2.32. Panel Interface Control 2 (R92h)

R/W	/ F	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W		1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0
De	efaul	lt	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

**NOWI[2:0]:** Sets the gate output non-overlap period when ILI9325C display operation is synchronized with internal clock signal.

NOWI[2:0]	Gate Non-overlap Period
000	Setting inhibited
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks





111	Setting inhibited

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

### 8.2.33. Panel Interface Control 4 (R95h)

R/W	RS						
W	1						
Defa	Default						

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

**DIVE[1:0]:** Sets the division ratio of DOTCLK when ILI9325C display operation is synchronized with RGB interface signals.

DIVE[1:0]	Division Ratio	18/16-bit RGB Interface	DOTCLK=5MHz	6-bit x 3 Transfers RGB Interface	DOTCLK=5MHz
00	Setting Prohibited	Setting Prohibited	-	Setting Prohibited	-
01	1/4	4 DOTCLKS	0.8 <i>μs</i>	12 DOTCLKS	0.8 <i>µs</i>
10	1/8	8 DOTCLKS	1.6 <i>μs</i>	24 DOTCLKS	1.6 <i>μs</i>
11	1/16	16 DOTCLKS	3.2 µs	48 DOTCLKS	3.2 µs

### 8.2.34. Panel Interface Control 5 (R97h)

R/W	RS
W	1
Defa	ault

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

**NOWE[3:0]:** Sets the gate output non-overlap period when the ILI9325C display operation is synchronized with RGB interface signals.

NOWE[3:0]	Gate Non-overlap Period
0000	Setting inhibited
0001	1 clocks
0010	2 clocks
0011	3 clocks
0100	4 clocks
0101	5 clocks
0110	6 clocks
0111	7 clocks

NOWE[3:0]	Gate Non-overlap Period
1000	8 clocks
1001	9 clocks
1010	10 clocks
1011	11 clocks
1100	12 clocks
1101	Setting inhibited
1110	Setting inhibited
1111	Setting inhibited

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

#### 8.2.35. OTP VCM Programming Control (RA1h)

R/W	RS
W	1
Defa	ault

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	OTP_ PGM_EN	0	0	0	0	0	VCM_ OTP5	VCM_ OTP4	VCM_ OTP3	VCM_ OTP2	VCM_ OTP1	VCM_ OTP0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**OTP\_PGM\_EN:** OTP programming enable. When program OTP, must set this bit. OTP data can be programmed 3 times.

**VCM\_OTP[5:0]:** OTP programming data for VCOMH voltage, the voltage refer to VCM[5:0] value.

## 8.2.36. OTP VCM Status and Enable (RA2h)

R/W	RS
W	1
Defa	ault

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PGM_ CNT1	PGM_ CNT0	VCM_ D5	VCM_ D4	VCM_ D3	VCM_	VCM_	VCM_ D0	0	0	0	0	0	0	0	VCM_ EN
OIVII	CIVIO	D3	D4	D3	D2	וט	D0								LIN
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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**PGM\_CNT[1:0]:** OTP programmed record. These bits are read only.

OTP_PGM_CNT[1:0]	Description
00	OTP clean
01	OTP programmed 1 time
10	OTP programmed 2 times
11	OTP programmed 3 times

**VCM\_D[5:0]:** OTP VCM data read value. These bits are read only.

VCM\_EN: OTP VCM data enable.

'1': Set this bit to enable OTP VCM data to replace R29h VCM value.

'0': Default value, use R29h VCM value.

#### 8.2.37. OTP Programming ID Key (RA5h)

R/W	RS	
W	1	K
Defa	ault	

Ī	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	KEY															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**KEY[15:0]:** OTP Programming ID key protection. Before writing OTP programming data RA1h, it must write RA5h with 0xAA55 value first to make OTP programming successfully. If RA5h is not written with 0xAA55, OTP programming will be fail. See OTP Programming flow.

## 8.2.38. Write Display Brightness Value (RB1h)

									•								
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Х	Χ	Х	Χ	Х	Х	Χ	Χ	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

#### **Description**

This command is used to adjust the brightness value of the display.

**DBV[7:0]**: 8 bit, for display brightness of manual brightness setting and CABC in ILI9325C. There is a PWM output signal, LEDPWM pin, to control the LED driver IC in order to control display brightness.

### 8.2.39. Read Display Brightness Value (RB2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

#### Description

This command is used to return the brightness value of the display.

DBV[7:0] is reset when display is in sleep-in mode.

DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (B3h)" command is '0'.

DBV[7:0] is manual set brightness specified with "Write CTRL Display (B3h)" command when BCTRL bit is '1'.

When bit BCTRL of "Write CTRL Display (B3h)" command is '1' and C1/C0 bit of "Write Content Adaptive

Brightness Control (B5h)" command are '0', DBV[7:0] output is the brightness value specified with "Write

Display Brightness (B1h)" command.





### 8.2.40. Write CTRL Display Value (RB3h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Χ	Χ	Χ	X	Χ	Χ	Χ	Χ	X	X	BCTRL	Χ	DD	BL	Χ	X

### **Description**

This command is used to control display brightness.

**BCTRL**: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

**DD**: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g.

BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected

X: don't care

### 8.2.41. Read CTRL Display Value (RB4h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	Χ	X	Χ	Χ	Χ	Х	Χ	Χ	Х	Χ	BCTRL	Χ	DD	BL	Х	Χ

#### **Description**

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

**DD**: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

**BL**: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

X = Don't care

## 8.2.42. Write Content Adaptive Brightness Control Value (RB5h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	C[1	:0]





#### Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C[1	1:0]	Description
0	0	CABC OFF
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

X = Don't care

## 8.2.43. Read Content Adaptive Brightness Control Value (RB6h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	Χ	Х	Χ	Χ	Χ	Х	Х	Χ	Χ	Х	Х	Χ	Χ	Χ	C[1	1:0]

#### **Description**

This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a

table below.

C[1	:0]	Description
0	0	CABC OFF
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

X = Don't care

#### 8.2.44. Write CABC Minimum Brightness (RBEh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ				CME	[7:0]			

#### **Description**

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

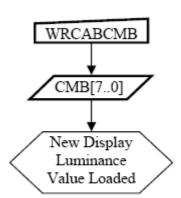
This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

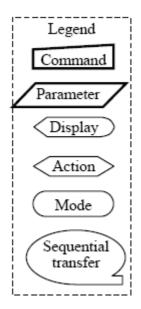
When display brightness is turned off (BCTRL=0 of "Write CTRL Display (B3h)"), CABC minimum brightness setting is ignored.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.













### 8.2.45. Read CABC Minimum Brightness (RBFh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ				CMB	[7:0]			

### **Description**

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of "Write CTRL Display (B3h)"), CABC minimum brightness setting is ignored.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

### 8.2.46. CABC Control 1 (RC7h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Χ	Χ	Х	Х	Х	Х	Х	Х	Χ	Х	Х	Х	Χ	LEDONR	LEDONPOL	LEDPWMPOL

LEDPWMPOL: The bit is used to define polarity of LEDPWM signal.

BL	LEDPWMPOL	LEDPWM pin
0	0	0
0	1	1
1	0	Original polarity of PWM signal
1	1	Inversed polarity of PWM signal

LEDONPOL: This bit is used to control LEDON pin.

В	L	LEDONPOL	LEDON pin
C	)	0	0
C	)	1	1
1		0	LEDONR
1		1	Inversed LEDONR





LEDONR: This bit is used to control LEDON pin.

LEDONR	Description
0	Low
1	High

## 8.2.47. CABC Control 1 (RC8h)

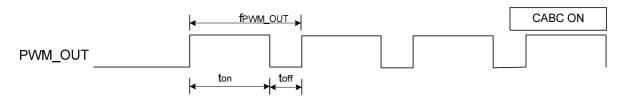
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Χ	Х	Χ	Χ	X	Χ	Χ	Х				_MW_I	DIV[7:0	]		

#### **Description**

**PWM\_DIV[7:0]**: PWM\_OUT output period control. This command is used to adjust the PWM waveform period of PWM\_OUT. The PWM period can be calculated using the equation in the following.

$$f_{PWM\_OUT} = \frac{5.8MHz}{(PWM\_DIV[7:0]+1) \times 255}$$

			`			L		,
		Р	WM_[	DIV[7:	0]			4
D7	D6	D5	D4	D3	D2	D1	D0	f <sub>PWM_OUT</sub>
0	0	0	0	0	0	0	0	22.74 KHz
0	0	0	0	0	0	0	1	11.37 KHz
0	0	0	0	0	0	1	0	7.58KHz
0	0	0	0	0	0	1	1	5.68 KHz
0	0	0	0	0	1	0	0	4.54 KHz
				:				:
								:
1	1	1	1	1	0	1	1	90.26 Hz
1	1	1	1	1	1	0	0	89.9Hz
1	1	1	1	1	1	0	1	89.53Hz
1	1	1	1	1	1	1	0	89.17 Hz
1	1	1	1	1	1	1	1	88.81 Hz



Note: The output frequency tolerance of internal frequency divider in CABC is  $\pm 10\%$ 





## 8.2.48. CABC Control 2 (RC9h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	THRE	ES_MC	V[3:0]		TH	IRES_S	STILL[3	3:0]

### **Description**

**THRES\_MOV[3:0]**: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in MOVING image mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

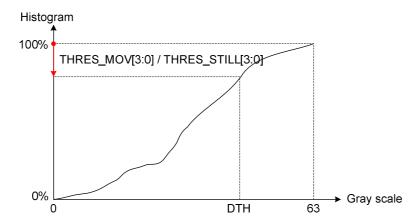
TH	RES_I	MOV[	3:0]	Description
D3	D2	D1	D0	Description
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

TH	RES_I	MOV[	3:0]	Description
D3	D2	D1	D0	Description
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %

**THRES\_STILL[3:0]**: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in STILL mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THE	RES_S	STILLI	[3:0]	Docariation
D3	D2	D1	D0	Description
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THE	RES_S	STILL[	3:0]	Description
D3	D2	D1	D0	Description
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %







## 8.2.49. CABC Control 3 (RCAh)

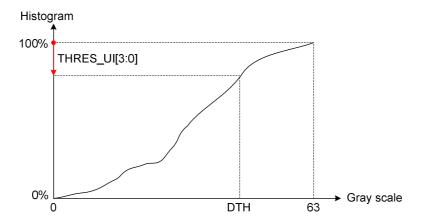
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Х	Χ	Χ	Χ	Χ	Χ	Χ	Χ	0	0	0	0	Т	HRES	_UI[3:0	)]

#### **Description**

THRES\_UI[3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in USER INTERFACE mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

TI	HRES	_UI[3:	0]	Docorintion
D3	D2	D1	D0	Description
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

			Dogoription
D2	D1	D0	Description
0	0	0	84 %
0	0	1	82 %
0	1	0	80 %
0	1	1	78 %
1	0	0	76 %
1	0	1	74 %
1	1	0	72 %
1	1	1	70 %
	0 0	0 0 0 0 0 1 0 1 1 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1



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## 8.2.50. CABC Control 4 (RCBh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Χ	Χ	X	Χ	Χ	Χ	Χ	Χ		M_HTC	OV[3:0	]		TH_S1	TILL[3:0	)]

#### **Description**

**DTH\_MOV[3:0]**: This parameter is used set the minimum limitation of grayscale threshold value in MOVING image mode.

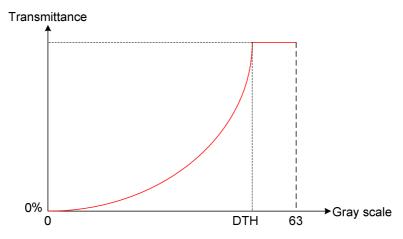
D	TH_M	OV[3:	0]	Docorintion			
D3	D2	D1	D0	Description			
0	0	0	0	224			
0	0	0	1	220			
0	0	1	0	216			
0	0	1	1	212			
0	1	0	0	208			
0	1	0	1	204			
0	1	1	0	200			
0	1	1	1	196			

Ď	TH_M	Description			
D3	D2	D1 D0		Description	
1	0	0	0	192	
1	0	0	1	188	
1	0	1	0	184	
1	0	1	1	180	
1	1	0	0	176	
1	1	0	1	172	
1	1	1	0	168	
1	1	1	1	164	

**DTH\_STILL[3:0]**: This parameter is used to set the minimum limitation of grayscale threshold value in STILL image mode.

DT	H_ST	TLLI[3	:0]	Description			
D3	D2	D1	D0	Description			
0	0	0	0	224			
0	0	0	1	220			
0	0	1	0	216			
0	0	1	1	212			
0	1	0	0	208			
0	1	0	1	204			
0	1	1	0	200			
0	1	1	1	196			

D <sup>-</sup>	TH_ST	:0]	Description				
D3	D2	D1	D0	Description			
1	0	0	0	192			
1	0	0	1	188			
1	0	1	0	184			
1	0	1	1	180			
1	1	0	0	176			
1	1	0	1	172			
1	1	1	0	168			
1	1	1	1	164			







## 8.2.51. CABC Control 5 (RCCh)

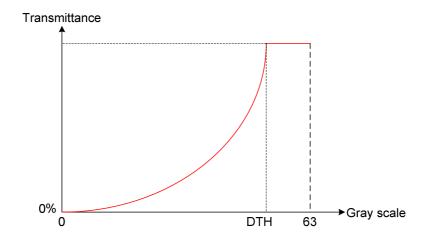
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	0	0	0	0		DTH_	UI[3:0]	

### **Description**

DTH\_UI[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in USER INTERFACE mode.

	DTH_		Description			
D3	D2	D1	D0	Description		
0	0	0	0	252		
0	0	0	1	248		
0	0	1	0	244		
0	0	1	1	240		
0	1	0	0	236		
0	1	0	1	232		
0	1	1	0	228		
0	1	1	1	224		

	DTH_I	]	Description	
D3	D2	D1	D0	Description
1	0	0	0	220
1	0	0	1	216
1	0	1	0	212
1	0	1	1	208
1	1	0	0	2-4
1	1	0	1	200
1	1	1	0	196
1	1	1	1	192



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## 8.2.52. CABC Control 6 (RCDh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ		O_MIC	PT2[3:0	)]	0	DIM	_OPT1	[2:0]

#### **Description**

**DIM\_OPT1[2:0]**: This parameter is used set the transition time of brightness level change to avoid the sharp brightness change on vision.

DII	M_OPT1[2	2:0]	Description				
D2	D1	D0	Description				
0	0	0	1 frame				
0	0	1	1 frame				
0	1	0	2 frames				
0	1	1	4 frames				
1	0	0	8 frames				
1	0	1	16 frames				
1	1	0	32 frames				
1	1	1	64 frames				

**DIM\_OPT2[3:0]**: This parameter is used to set the imitation of minimum brightness change. If this parameter is large than the difference between target brightness and current brightness, then the brightness will not change.

nd



D7



D0

SCD VLINE[8]

D5 D4 D3 D2 D1

SCD\_VLINE[7:0]

X X X X

### 8.2.53. CABC Control 7 (RCEh)

		<u> </u>			- (	<u> </u>				
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	
W	1	Х	Х	Х	Х	Х	Х	X	Х	
W	1	Х	Х	Х	Х	Х	Х	Х	Х	

**Description** 

SCD\_VLINE[8:0]: This parameter is used set the display line per frame while partial mode ON.

			SCD	_VLINE	[8:0]				Display line
D8	D7	D6	D5	D4	D3	D2	D1	D0	Display lifle
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	0	1	1	3 lines
0	0	0	0	0	0	1	0	0	4 lines
				:					:
				:					:
1	0	0	1	1	1	1	0	1	317 lines
1	0	0	1	1	1	1	1	0	318 lines
1	0	0	1	1	1	1	1	1	319lines
1	0	1	0	0	0	0	0	0	320 lines
		Setting prohibited							

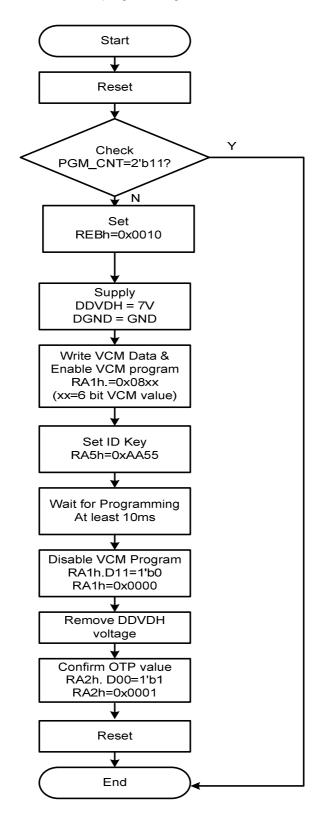
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## 9. OTP Programming Flow

VCOMH OTP programming Flow



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## 10. GRAM Address Map & Read/Write

ILI9325C has an internal graphics RAM (GRAM) of 172,800 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80 system, SPI and RGB interfaces.

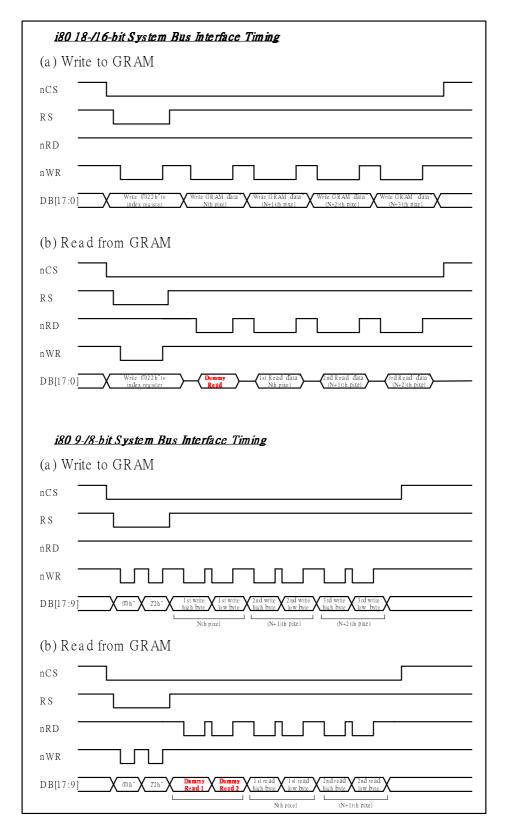


Figure 30 GRAM Read/Write Timing of i80-System Interface





#### GRAM address map table of SS=0, BGR=0

SS=0,	BGR=0	S1S3	S4S6	S7S9	S10S12	 S517S519	S520S522	S523S525	S526S720
GS=0	GS=1	DB170	DB170	DB170	DB170	 DB170	DB170	DB170	DB170
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	 "000ECh"	"000EDh"	"000EEh"	"000EFh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	 "001ECh"	"001EDh"	"001EEh"	"001EFh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	 "002ECh"	"002EDh"	"002EEh"	"002EFh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	 "003ECh"	"003EDh"	"003EEh"	"003EFh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	 "004ECh"	"004EDh"	"004EEh"	"004EFh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	 "005ECh"	"005EDh"	"005EEh"	"005EFh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	 "006ECh"	"006EDh"	"006EEh"	"006EFh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	 "007ECh"	"007EDh"	"007EEh"	"007EFh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	 "008ECh"	"008EDh"	"008EEh"	"008EFh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	 "009ECh"	"009EDh"	"009EEh"	"009EFh"
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	 "136ECh"	"136EDh"	"136EEh"	"136EFh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	 "137ECh"	"137EDh"	"137EEh"	"137EFh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	 "138ECh"	"138EDh"	"138EEh"	"138EFh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	 "139ECh"	"139EDh"	"139EEh"	"139EFh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	 "13AECh"	"13AEDh"	"13AEEh"	"13AEFh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	 "13BECh"	"13BEDh"	"13BEEh"	"13BEFh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	 "13CECh"	"13CEDh"	"13CEEh"	"13CEFh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	 "13DECh"	"13DEDh"	"13DEEh"	"13DEFh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	 "13EECh"	"13EEDh"	"13EEEh"	"13EEFh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	 "13FECh"	"13FEDh"	"13FEEh"	"13FEFh"



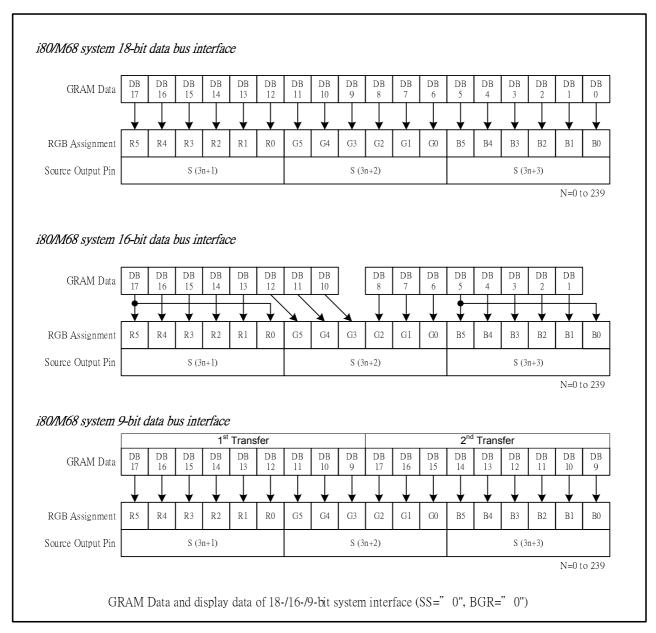


Figure31 i80-System Interface with 18-/16-/9-bit Data Bus (SS="0", BGR="0")



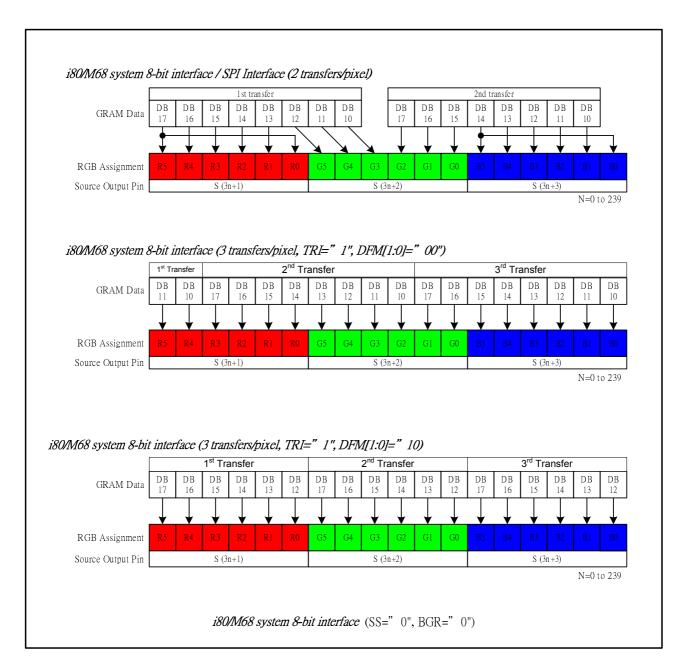


Figure 32 i80-System Interface with 8-bit Data Bus (SS="0", BGR="0")





#### GRAM address map table of SS=1, BGR=1

SS=1,	BGR=1	S720S718	S717S715	S714S712	S711S709	 S12S10	S9S7	S6S4	S3S1
GS=0	GS=1	DB170	DB170	DB170	DB170	 DB170	DB170	DB170	DB170
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	 "000ECh"	"000EDh"	"000EEh"	"000EFh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	 "001ECh"	"001EDh"	"001EEh"	"001EFh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	 "002ECh"	"002EDh"	"002EEh"	"002EFh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	 "003ECh"	"003EDh"	"003EEh"	"003EFh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	 "004ECh"	"004EDh"	"004EEh"	"004EFh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	 "005ECh"	"005EDh"	"005EEh"	"005EFh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	 "006ECh"	"006EDh"	"006EEh"	"006EFh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	 "007ECh"	"007EDh"	"007EEh"	"007EFh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	 "008ECh"	"008EDh"	"008EEh"	"008EFh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	 "009ECh"	"009EDh"	"009EEh"	"009EFh"
	-	•							
	-								
		•		•					
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	 "136ECh"	"136EDh"	"136EEh"	"136EFh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	 "137ECh"	"137EDh"	"137EEh"	"137EFh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	 "138ECh"	"138EDh"	"138EEh"	"138EFh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	 "139ECh"	"139EDh"	"139EEh"	"139EFh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	 "13AECh"	"13AEDh"	"13AEEh"	"13AEFh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	 "13BECh"	"13BEDh"	"13BEEh"	"13BEFh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	 "13CECh"	"13CEDh"	"13CEEh"	"13CEFh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	 "13DECh"	"13DEDh"	"13DEEh"	"13DEFh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	 "13EECh"	"13EEDh"	"13EEEh"	"13EEFh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	 "13FECh"	"13FEDh"	"13FEEh"	"13FEFh"

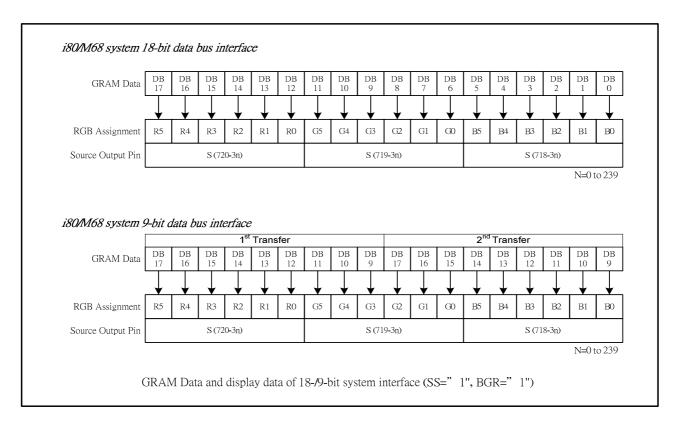


Figure 33 i80-System Interface with 18-/9-bit Data Bus (SS="1", BGR="1")





## 11. Window Address Function

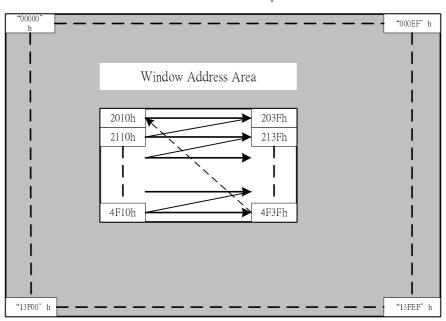
The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[8:0], end: VEA[8:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the ILI9325C to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the GRAM address bits (RAM address set register) must be an address within the window address area.

[Window address setting area]

(Horizontal direction) 00H ≤ HSA[7:0] ≤ HEA[7:0] ≤ "EF"H (Vertical direction) 00H ≤ VSA[8:0] ≤ VEA[8:0]≤ "13F"H [RAM address, AD (an address within a window address area)]]  $(RAM \ address) \ HSA[7:0] \le AD[7:0] \le HEA[7:0]$  $VSA[8:0] \le AD[15:8] \le VEA[8:0]$ 

GRAM Address Map



Window address setting area

HSA[7:0] = 10h, HEA[7:0] = 3Fh,I/D = 1 (increment) VSA[8:0] = 20h, VEA[8:0] = 4Fh,AM = 0 (horizontal writing)

Figure 34 GRAM Access Window Map

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## 12. Gamma Correction

ILI9325C incorporates the  $\gamma$ -correction function to display 262,144 colors for the LCD panel. The  $\gamma$ -correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9325C available with liquid crystal panels of various characteristics.

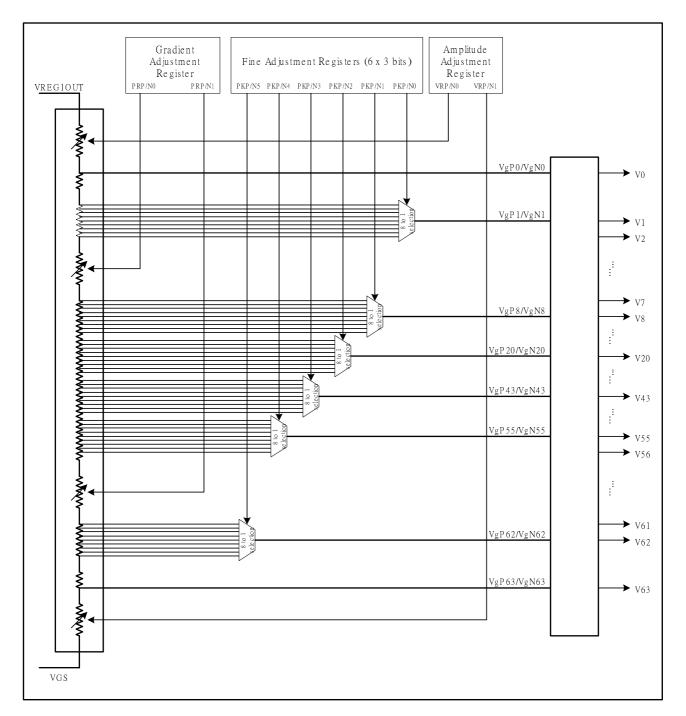


Figure 35 Grayscale Voltage Generation

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V0.07



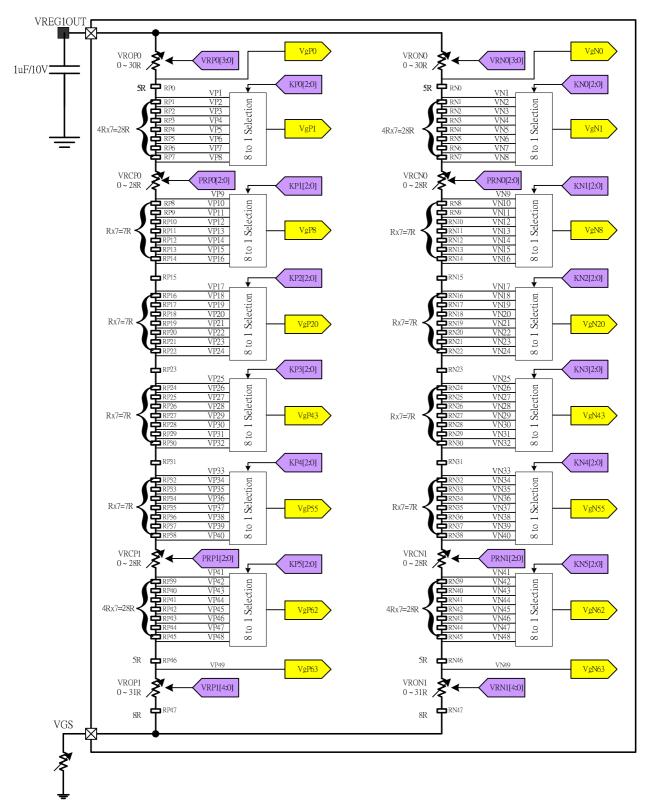


Figure 36 Grayscale Voltage Adjustment





#### 1. Gradient adjustment registers

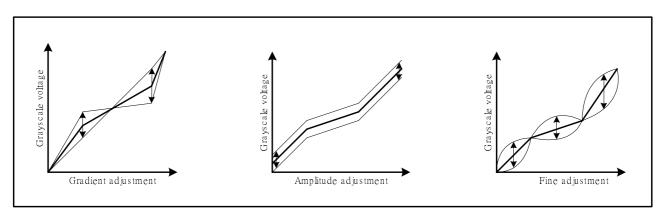
The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

#### 2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

#### 3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.



**Figure 37 Gamma Curve Adjustment** 

Register Groups	Positive Polarity	Negative Polarity	Description				
Gradient	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRCP0, VRCN0				
adjustment	PRP1 [2:0] PRN1 [2:0]		Variable resistor VRCP1, VRCN1				
Amplitude	VRP0 [3:0]	VRN0 [3:0]	Variable resistor VROP0, VRON0				
adjustment	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VROP1, VRON1				
	KP0 [2:0]	KN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)				
	KP1 [2:0]	KN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)				
Fine a division and	KP2 [2:0]	KN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)				
Fine adjustment	KP3 [2:0]	KN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)				
	KP4 [2:0]	KN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)				
	KP5 [2:0]	KN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)				





#### Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ-correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

#### Variable resistors

ILI9325C uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment					
PRP(N)0/1[2:0]	VRCP(N)0/1				
Register	Resistance				
000	0R				
001	4R				
010	8R				
011	12R				
100	16R				
101	20R				
110	24R				
111	28R				

Amplitude adjustment (1)							
VRP(N)0[3:0]	VROP(N)0						
Register	Resistance						
0000	0R						
0001	2R						
0010	4R						
:	:						
:	:						
1101	26R						
1111	28R						
1111	30R						

Amplitude adjustment (2)						
VRP(N)1[4:0]	VROP(N)1					
Register	Resistance					
00000	0R					
00001	1R					
00010	2R					
:	:					
:	:					
11101	29R					
11110	30R					
11111	31R					

#### 8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

		Fine adjustr	ment registers and s	elected voltage		
Register			Select	ed Voltage		
KP(N)[2:0]	VgP(N)1	VgP(N)8	VgP(N)20	VgP(N)43	VgP(N)55	VgP(N)62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48



		Fine adjust	ment registers and s	elected resistor					
Register		Selected Resistor							
KP(N)[2:0]	RMP(N)0	RMP(N)1	RMP(N)2	RMP(N)3	RMP(N)4	RMP(N)5			
000	0R	0R	0R	0R	0R	0R			
001	4R	1R	1R	1R	1R	4R			
010	8R	2R	2R	2R	2R	8R			
011	12R	3R	3R	3R	3R	12R			
100	16R	4R	4R	4R	4R	16R			
101	20R	5R	5R	5R	5R	20R			
110	24R	6R	6R	6R	6R	24R			
111	28R	7R	7R	7R	7R	28R			

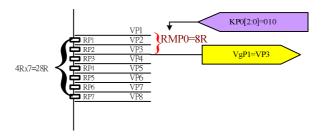


Figure 38 Example of RMP(N)0~5 definition





#### Gamma correction resister ratio

Data	Positive polarity output voltage			Negative polarity output voltage
00h	VP0	(VgP0)	VN0	(VgN0)
01h	VP1	(VgP1)	VN1	(VgN1)
02h	VP2	(VP8+(VP1-VP8)*(30/48))	VN2	(VN8+(VN1-VN8)*(30/48))
03h	VP3	(VP8+(VP1-VP8)*(23/48))	VN3	(VN8+(VN1-VN8)*(23/48))
04h	VP4	(VP8+(VP1-VP8)*(16/48))	VN4	(VN8+(VN1-VN8)*(16/48))
05h	VP5	(VP8+(VP1-VP8)*(12/48))	VN5	(VN8+(VN1-VN8)*(12/48))
06h	VP6	(VP8+(VP1-VP8)*(8/48))	VN6	(VN8+(VN1-VN8)*(8/48))
07h	VP7	(VP8+(VP1-VP8)*(4/48))	VN7	(VN8+(VN1-VN8)*(4/48))
08h	VP8	(VgP8)	VN8	(VgN8)
09h	VP9	VP20+(VP8-VP20)*(22/24)	VN9	VN20+(VN8-VN20)*(22/24)
0Ah	VP10	VP20+(VP8-VP20)*(20/24)	VN10	VN20+(VN8-VN20)*(20/24)
0Bh	VP11	VP20+(VP8-VP20)*(18/24)	VN11	VN20+(VN8-VN20)*(18/24)
0Ch	VP12	VP20+(VP8-VP20)*(16/24)	VN12	VN20+(VN8-VN20)*(16/24)
0Dh	VP13	VP20+(VP8-VP20)*(14/24)	VN13	VN20+(VN8-VN20)*(14/24)
0Eh	VP14	VP20+(VP8-VP20)*(12/24)	VN14	VN20+(VN8-VN20)*(12/24)
0Fh	VP15	VP20+(VP8-VP20)*(10/24)	VN15	VN20+(VN8-VN20)*(10/24)
10h	VP16	VP20+(VP8-VP20)*(8/24)	VN16	VN20+(VN8-VN20)*(8/24)
11h	VP17	VP20+(VP8-VP20)*(6/24)	VN17	VN20+(VN8-VN20)*(6/24)
12h	VP18	VP20+(VP8-VP20)*(4/24)	VN18	VN20+(VN8-VN20)*(4/24)
13h	VP19	VP20+(VP8-VP20)*(2/24)	VN19	VN20+(VN8-VN20)*(2/24)
14h	VP20	(VgP20)	VN20	(VgN20)
15h	VP21	(VP43+(VP20-VP43)*(22/23))	VN21	(VN43+(VN20-VN43)*(22/23))
16h	VP22	(VP43+(VP20-VP43)*(21/23))	VN22	(VN43+(VN20-VN43)*(21/23))
17h	VP23	(VP43+(VP20-VP43)*(20/23))	VN23	(VN43+(VN20-VN43)*(20/23))
18h	VP24	(VP43+(VP20-VP43)*(19/23))	VN24	(VN43+(VN20-VN43)*(19/23))
19h	VP25	(VP43+(VP20-VP43)*(18/23))	VN25	(VN43+(VN20-VN43)*(18/23))
1Ah	VP26	(VP43+(VP20-VP43)*(17/23))	VN26	(VN43+(VN20-VN43)*(17/23))
1Bh	VP27	(VP43+(VP20-VP43)*(16/23))	VN27	(VN43+(VN20-VN43)*(16/23))
1Ch	VP28	(VP43+(VP20-VP43)*(15/23))	VN28	(VN43+(VN20-VN43)*(15/23))
1Dh	VP29	(VP43+(VP20-VP43)*(14/23))	VN29	(VN43+(VN20-VN43)*(14/23))
1Eh	VP30	(VP43+(VP20-VP43)*(13/23))	VN30	(VN43+(VN20-VN43)*(13/23))
1Fh	VP31	(VP43+(VP20-VP43)*(12/23))	VN31	(VN43+(VN20-VN43)*(12/23))





Data		Positive polarity output voltage		Negative polarity output voltage
20h	VP32	(VP43+(VP20-VP43)*(11/23))	VN32	(VN43+(VN20-VN43)*(11/23))
21h	VP33	(VP43+(VP20-VP43)*(10/23))	VN33	(VN43+(VN20-VN43)*(10/23))
22h	VP34	(VP43+(VP20-VP43)*(9/23))	VN34	(VN43+(VN20-VN43)*(9/23))
23h	VP35	(VP43+(VP20-VP43)*(8/23))	VN35	(VN43+(VN20-VN43)*(8/23))
24h	VP36	(VP43+(VP20-VP43)*(7/23))	VN36	(VN43+(VN20-VN43)*(7/23))
25h	VP37	(VP43+(VP20-VP43)*(6/23))	VN37	(VN43+(VN20-VN43)*(6/23))
26h	VP38	(VP43+(VP20-VP43)*(5/23))	VN38	(VN43+(VN20-VN43)*(5/23))
27h	VP39	(VP43+(VP20-VP43)*(4/23))	VN39	(VN43+(VN20-VN43)*(4/23))
28h	VP40	(VP43+(VP20-VP43)*(3/23))	VN40	(VN43+(VN20-VN43)*(3/23))
29h	VP41	(VP43+(VP20-VP43)*(2/23))	VN41	(VN43+(VN20-VN43)*(2/23))
2Ah	VP42	(VP43+(VP20-VP43)*(1/23))	VN42	(VN43+(VN20-VN43)*(1/23))
2Bh	VP43	(VgP43)	VN43	(VgN43)
2Ch	VP44	(VP55+(VP43-VP55)*(22/24))	VN44	(VN55+(VN43-VN55)*(22/24))
2Dh	VP45	(VP55+(VP43-VP55)*(20/24))	VN45	(VN55+(VN43-VN55)*(20/24))
2Eh	VP46	(VP55+(VP43-VP55)*(18/24))	VN46	(VN55+(VN43-VN55)*(18/24))
2Fh	VP47	(VP55+(VP43-VP55)*(16/24))	VN47	(VN55+(VN43-VN55)*(16/24))
30h	VP48	(VP55+(VP43-VP55)*(14/24))	VN48	(VN55+(VN43-VN55)*(14/24))
31h	VP49	(VP55+(VP43-VP55)*(12/24))	VN49	(VN55+(VN43-VN55)*(12/24))
32h	VP50	(VP55+(VP43-VP55)*(10/24))	VN50	(VN55+(VN43-VN55)*(10/24))
33h	VP51	(VP55+(VP43-VP55)*(8/24))	VN51	(VN55+(VN43-VN55)*(8/24))
34h	VP52	(VP55+(VP43-VP55)*(6/24))	VN52	(VN55+(VN43-VN55)*(6/24))
35h	VP53	(VP55+(VP43-VP55)*(4/24))	VN53	(VN55+(VN43-VN55)*(4/24))
36h	VP54	(VP55+(VP43-VP55)*(2/24))	VN54	(VN55+(VN43-VN55)*(2/24))
37h	VP55	(VgP55)	VN55	(VgN55)
38h	VP56	(VP62+(VP55-VP62)*(44/48))	VN56	(VN62+(VN55-VN62)*(44/48))
39h	VP57	(VP62+(VP55-VP62)*(40/48))	VN57	(VN62+(VN55-VN62)*(40/48))
3Ah	VP58	(VP62+(VP55-VP62)*(36/48))	VN58	(VN62+(VN55-VN62)*(36/48))
3Bh	VP59	(VP62+(VP55-VP62)*(32/48))	VN59	(VN62+(VN55-VN62)*(32/48))
3Ch	VP60	(VP62+(VP55-VP62)*(25/48))	VN60	(VN62+(VN55-VN62)*(25/48))
3Dh	VP61	(VP62+(VP55-VP62)*(18/48))	VN61	(VN62+(VN55-VN62)*(18/48))
3Eh	VP62	(VgP62)	VN62	(VgN62)
3Fh	VP63	(VgP63)	VN63	(VgN63)



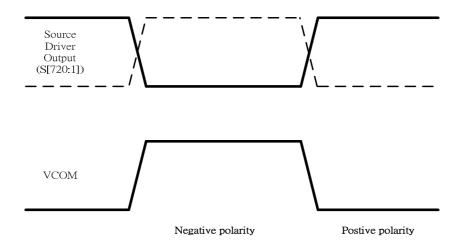


Figure 39 Relationship between Source Output and VCOM

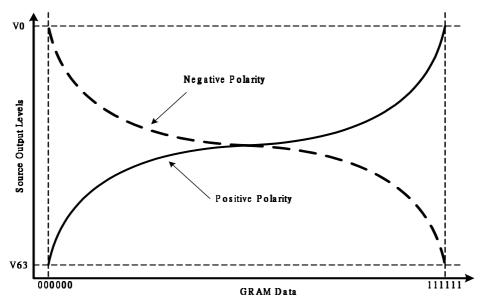


Figure 40 Relationship between GRAM Data and Output Level

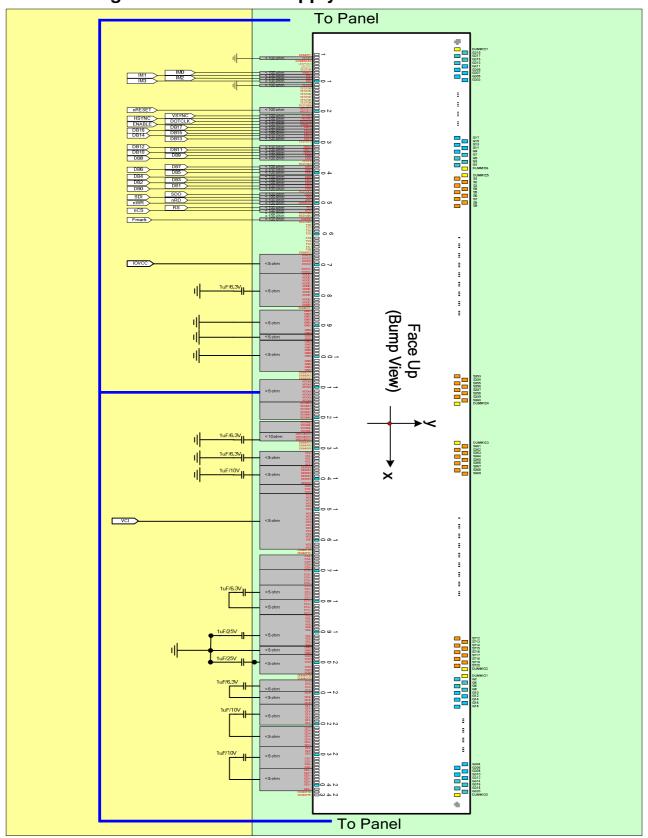
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## 13. Application

### 13.1. Configuration of Power Supply Circuit



**Figure 41 Power Supply Circuit Block** 

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The following table shows specifications of external elements connected to the ILI9325C's power supply circuit.

Items	Recommended Specification	Pin connection		
Capacity	6.3V	VDD, VCL, C11A/B, C13 A/B, VREG1OUT		
1 μF (B characteristics)	10V	DDVDH, C21 A/B, C22 A/B		
	25V	VGH, VGL		





### 13.2. Display ON/OFF Sequence

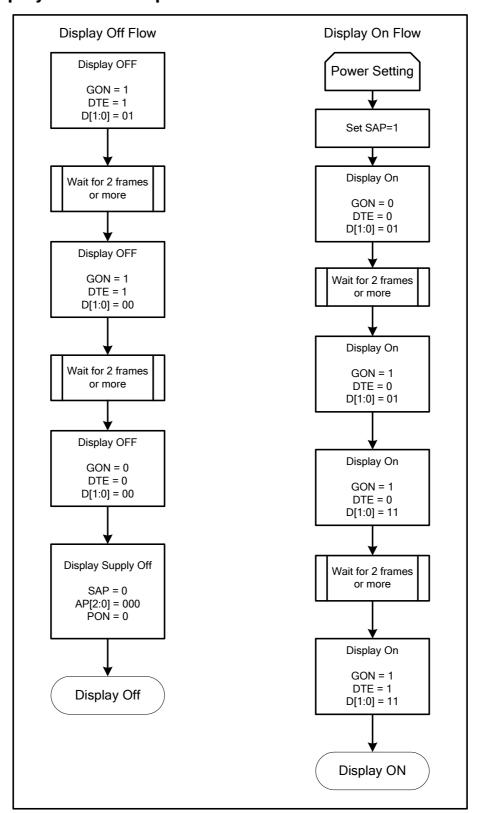


Figure 42 Display On/Off Register Setting Sequence

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### 13.3. Standby and Sleep Mode

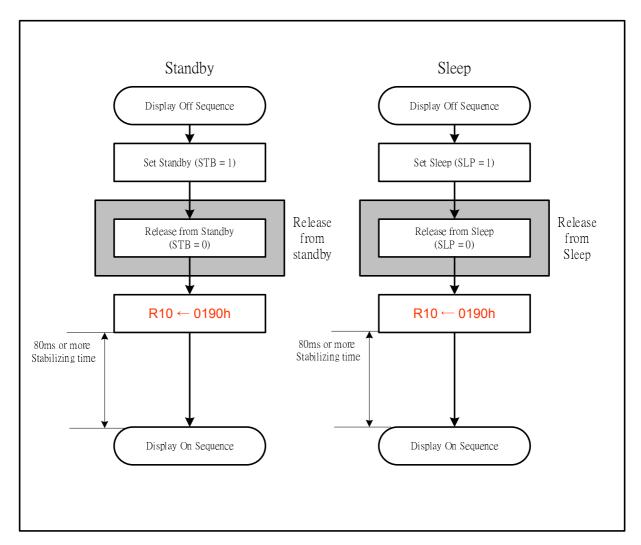


Figure 43 Standby/Sleep Mode Register Setting Sequence

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### 13.4. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for step-up circuits and operational amplifiers depends on external resistance and capacitance.

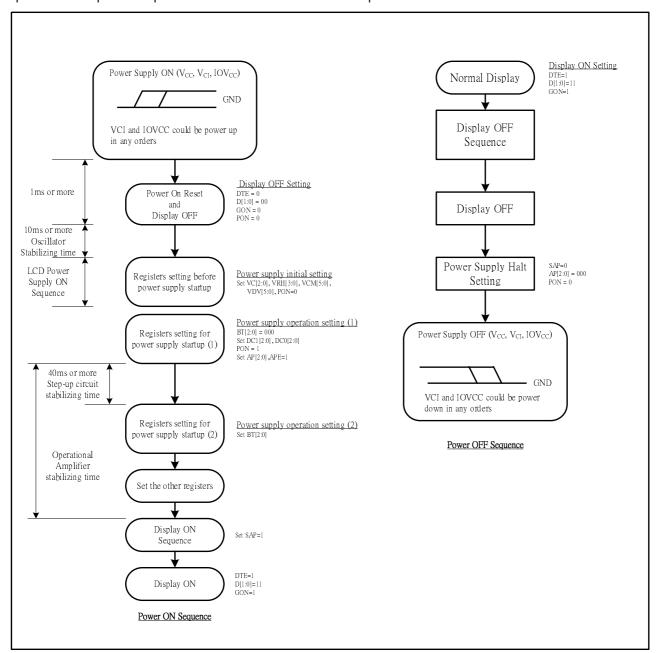


Figure 44 Power Supply ON/OFF Sequence

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### 13.5. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ILI9325C are as follows.

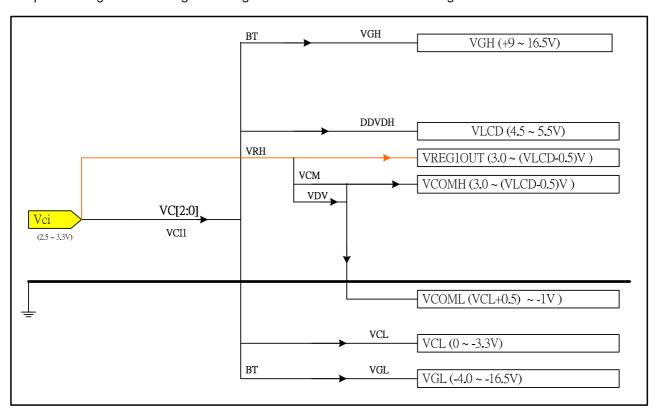


Figure 45 Voltage Configuration Diagram

Note: The DDVDH, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective outputs. The voltage levels in the following relationships (DDVDH - VREG1OUT ) > 0.2V and (VCOML - VCL) > 0.5V are the actual voltage levels. When the alternating cycles of VCOM are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.

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### 13.6. Applied Voltage to the TFT panel

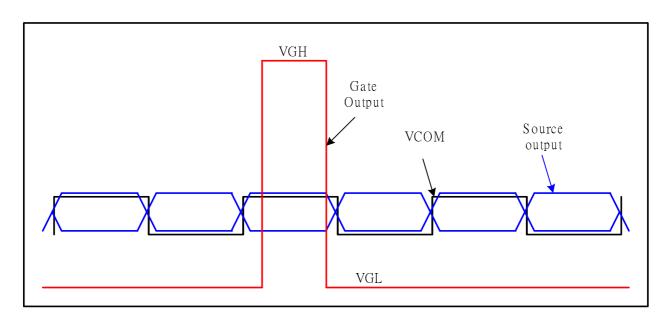


Figure 46 Voltage Output to TFT LCD Panel

### 13.7. Partial Display Function

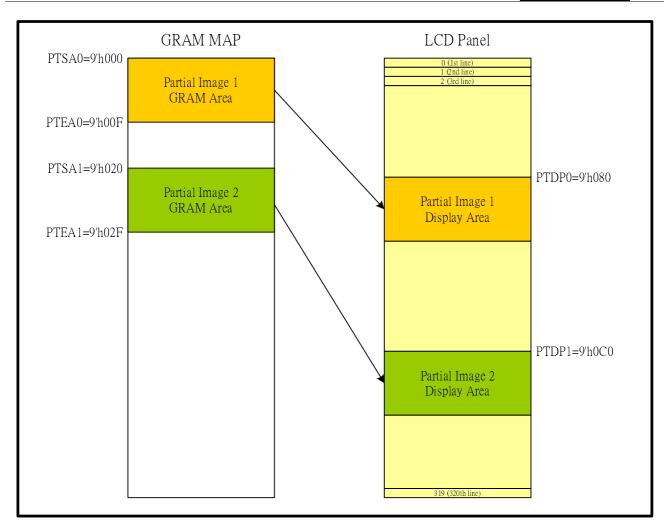
The ILI9325C allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers.

The following example shows the setting for partial display function:

	Base Image Display Setting					
BASEE	0					
NL[5:0]	6'h27					
	Partial Image 1 Display Setting					
PTDE0	1					
PTSA0[8:0]	9'h000					
PTEA0[8:0]	9'h00F					
PTDP0[8:0]	9'h080					
Partial Image 2 Display Setting						
PTDE1	1					
PTSA1[8:0]	9'h020					
PTEA1[8:0]	9'h02F					
PTDP1[8:0]	9'h0C0					

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**Figure 47 Partial Display Example** 

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### 14. Electrical Characteristics

### 14.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9325C is used out of the absolute maximum ratings, the ILI9325C may be permanently damaged. To use the ILI9325C within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9325C will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	IOVCC	OVCC V -0.3 ~ + 4.6		1, 2
Power supply voltage (1)	VCI – GND	V	-0.3 ~ + 4.6	1, 4
Power supply voltage (1)	DDVDH – GND	V -0.3 ~ + 6.0		1, 4
Power supply voltage (1)	GND -VCL	V -0.3 ~ + 4.6		1
Power supply voltage (1)	DDVDH – VCL	V -0.3 ~ + 9.0		1, 5
Power supply voltage (1)	VGH – VGL	V	0.3 ~ + 30	1, 5
Input voltage	Vt	V	-0.3 ~ VCC+ 0.3	1
Operating temperature	Topr	.€	-40 ~ + 85	8, 9
Storage temperature	Tstg	∞	-55 ~ + 110	8, 9

#### Notes:

- 1. GND must be maintained
- 2. (High)  $(VCC = VCC) \ge GND (Low)$ , (High)  $IOVCC \ge GND (Low)$ .
- 3. Make sure (High) VCI ≥ GND (Low).
- 4. Make sure (High) DDVDH ≥ GND (Low).
- 5. Make sure (High) DDVDH  $\geq$  VCL (Low).
- 6. Make sure (High) VGH ≥ GND (Low).
- 7. Make sure (High) GND ≥ VGL (Low).
- 8. For die and wafer products, specified up to 85 °C.
- 9. This temperature specifications apply to the TCP package

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### 14.2. DC Characteristics

(VCC = VCI=2.50  $\sim$  3.3V, IOVCC = 1.65  $\sim$  3.30V, Ta= -40  $\sim$  85  $^{\circ}$ C)

<b>\</b>	- ,		,				
Item	Symbol	Unit	Test Condition	Min.	Тур.	Max.	Note
Input high voltage	V <sub>IH</sub>	V	IOVCC= 1.65 ~ 3.3V	0.8*IOV CC	-	IOVCC	-
Input low voltage	$V_{IL}$	V	IOVCC= 1.65 ~ 3.3V	-0.3	-	0.2*IOVCC	-
Output high voltage(1) ( DB0-17 Pins)	V <sub>OH1</sub>	V	IOH = -0.1 mA	0.8*IOV CC	-	-	-
Output low voltage ( DB0-17 Pins)	V <sub>OL1</sub>	٧	IOVCC=1.65~3.3V	-	-	0.2*IOVCC	1
I/O leakage current	ILI	μΑ	Vin = 0 ~ VCC	-0.1	ı	0.1	ı
Standby Current consumption (VCC - GND)+ (VCI - GND)	I <sub>ST</sub>	μА	VCC=IOVCC=2.8V , Ta=25 ℃	-	40	120	-
Sleep Current consumption (VCC - GND)+ (VCI - GND)	I <sub>SLP</sub>	μА	VCC=IOVCC=2.8V , Ta=25 ℃	-	70	200	-
Current consumption during normal operation (VCC - GND)+ (VCI - GND)	ILCD	mA	VCI=2.8V , VREG1OUT =4.8V DDVDH=5.2V , Frame Rate: 70Hz, line-inversion, Ta=25 °C, GRAM data = 0000h,	-	5.5	-	1
LCD Driving Voltage ( DDVDH-GND )	DDVDH	V	-	4.5	-	6	-
Output deviation voltage	$V_{DEV}$	mV	-	-	-	50	-
Output offset voltage	V <sub>OFFSET</sub>	mV	Note1	-	-	50	-

Note1: The Max. value is between with measure point and Gamma setting value.

### 14.3. Reset Timing Characteristics

Reset Timing Characteristics (IOVCC = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Min.	Тур.	Max.
Reset low-level width	t <sub>RES_L</sub>	ms	1	-	-
Reset rise time	$t_{rRES}$	μs	-	-	10
Reset high-level width	t <sub>RES H</sub>	ms	50	-	-







### 14.4. AC Characteristics

### 14.4.1. i80-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V)

	Symbol	Unit	Min.	Тур.	Max.	Test Condition	
Bus cycle time	Write	t <sub>CYCW</sub>	ns	80	-		-
	Read	t <sub>cycr</sub>	ns	300	-	-	-
Write low-level pulse	$PW_{LW}$	ns	50	-	500	-	
Write high-level pulse	$PW_{HW}$	ns	15	-	-	-	
Read low-level pulse	$PW_{LR}$	ns	150	-	-	-	
Read high-level pulse	$PW_{HR}$	ns	150	-	-		
Write / Read rise / fall time		$t_{WRr}/t_{WRf}$	ns	-	-	25	
Setup time	Write ( RS to nCS, E/nWR )		ns	10	-	-	
	Read ( RS to nCS, RW/nRD )	t <sub>AS</sub>		5	-	-	
Address hold time	t <sub>AH</sub>	ns	5	-	-		
Write data set up time		t <sub>DSW</sub>	ns	10	-	-	
Write data hold time		t <sub>H</sub>	ns	15	-	-	
Read data delay time	t <sub>DDR</sub>	ns	-	-	100		
Read data hold time	t <sub>DHR</sub>	ns	5	-	-		

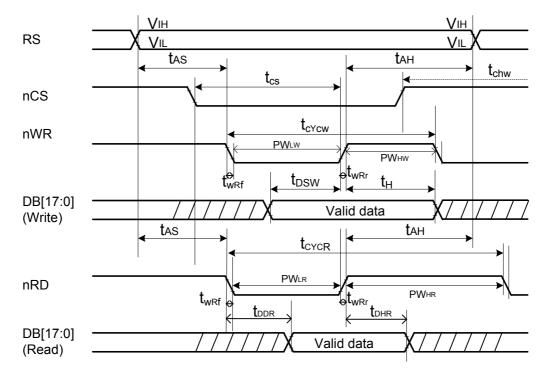


Figure 48 i80-System Bus Timing

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### 14.4.2. Serial Data Transfer Interface Timing Characteristics

(IOVCC= 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Тур.	Max.	Test Condition	
Ondal alask anda tha	Write ( received )	t <sub>scyc</sub>	Ns	100	-	ı	
Serial clock cycle time	Read (transmitted)	t <sub>scyc</sub>	ns	200	-	-	
Serial clock high – level	Write ( received )	t <sub>sch</sub>	ns	40	-	i	
pulse width	Read (transmitted)	t <sub>sch</sub>	ns	100	-	i	
Serial clock low – level pulse	Write ( received )	t <sub>SCL</sub>	ns	40	-	i	
width	Read (transmitted)	t <sub>SCL</sub>	ns	100	-	-	
Serial clock rise / fall time	t <sub>SCr</sub> , t <sub>SCf</sub>	ns	-	-	5		
Chip select set up time	t <sub>CSU</sub>	ns	10	-	-		
Chip select hold time	t <sub>CH</sub>	ns	50	-	i		
Serial input data set up time	t <sub>sisu</sub>	ns	20	-	i		
Serial input data hold time	t <sub>SIH</sub>	ns	20	-	ı		
Serial output data set up time	t <sub>SOD</sub>	ns	-	-	100		
Serial output data hold time	t <sub>soн</sub>	ns	5	-	-		

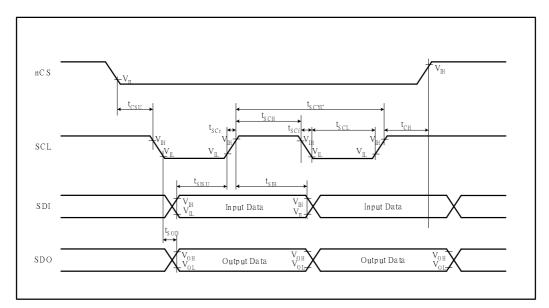


Figure 49 SPI System Bus Timing

### 14.4.3. RGB Interface Timing Characteristics

#### 18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Тур.	Max.	Test Condition
VSYNC/HSYNC setup time	t <sub>SYNCS</sub>	ns	0	-	-	-
ENABLE setup time	t <sub>ENS</sub>	ns	10	-	-	-
ENABLE hold time	t <sub>ENH</sub>	ns	10	-	i	-
PD Data setup time	t <sub>PDS</sub>	ns	10	1	i	-
PD Data hold time	$t_{PDH}$	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	ı	i	-
DOTCLK cycle time	t <sub>CYCD</sub>	ns	100	1	1	-
DOTCLK, VSYNC, HSYNC, rise/fall time	$t_{rghr,}t_{rghf}$	ns	-	-	25	=



#### 6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Тур.	Max.	Test Condition
VSYNC/HSYNC setup time	t <sub>SYNCS</sub>	ns	0	-	-	-
ENABLE setup time	t <sub>ENS</sub>	ns	10	-	1	-
ENABLE hold time	t <sub>ENH</sub>	ns	10	-	-	-
PD Data setup time	t <sub>PDS</sub>	ns	10	-	i	-
PD Data hold time	t <sub>PDH</sub>	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	1	-
DOTCLK low-level pulse width	PWDL	ns	30	-	ı	-
DOTCLK cycle time	t <sub>CYCD</sub>	ns	80	-	ı	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t <sub>rghr</sub> , t <sub>rghf</sub>	ns	-	-	25	-

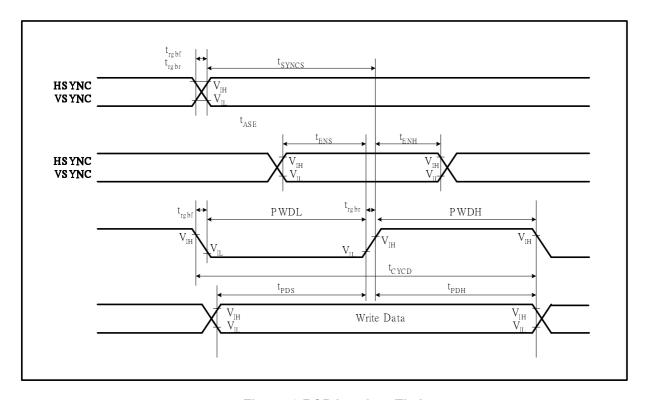


Figure 50 RGB Interface Timing





## 15. Revision History

Version No.	Date	Page	Description
V0.00	2008/11/14	all	new built
	2008/11/20	12	Modify TESTO2] description
V0.01	2008/12/18	35~37	ILI9225→ILI9325C
		37	4 wire 9 bits → 4 wire 8 bit
V0.02	2009/05/04	12, 13,115,	Modify external capacitors number 14→ 10
		116	
V0.03	2009/06/23	80	Modify frame rate
V0.04	2009/07/28	124 ~ 127	Update AC/DC characteristic
V0.05	2010/0107	114	Remove schottky diode item from table Add TSO and TEST_EN PIN Description
V0.06	2010/01/10	126	Modify SPI write cycle timing
V0.07	2010/2/24	118	Power Supply ON/OFF Sequence
V0.07	2010/2/24	110	Fower Supply ON/OFF Sequence
1			