



UTM
UNIVERSITI TEKNOLOGI MALAYSIA

RESEARCH UNIVERSITY

SCSR1013 DIGITAL LOGIC



Selamat Datang



(1995 – 2001)



(2001 - now)



(2012)

Learning Outcomes

SYNOPSIS

Digital electronics is the foundation of all microprocessor-based systems found in computers, robots, automobiles, and industrial control systems. This course introduces the students to digital electronics and provides a broad overview of many important concepts, components, and tools. The students will get the up-to-date coverage of digital fundamentals-from basic concepts to programmable logic devices. Laboratory experiments provide hands-on experience with the devices and circuits studied in the classroom.

Learning Outcomes

Course Learning Outcome (CLO)

CLO 1	Explain the fundamental of digital logic and be able to use the numbering systems.
CLO 2	Apply logic gates and Boolean algebra in combinational logic circuit designs.
CLO 3	Explain the fundamental of latches and flip-flops and be able to design and analyse sequential circuits.
CLO 4	Effectively design, troubleshoot and implement digital logic circuit based on practical problem.

Syllabus

Weekly Schedule

W 1	Module 1: Introductory Concepts Digital and Analogue Quantities, Binary Digits, Logic Levels and Digital Waveforms, Basic Logic Operations, Introduction to the System Concept, Fixed-Function Integrated Circuits
W 2	Module 2: Number Systems, Operations and Codes Decimal, Binary, Octal and Hexadecimal Numbers, Number Conversion between Bases, Digital Codes: BCD, GRAY, Parity, Data Representation: Integer, Signed Number and Character, Operations: Addition and Subtraction
W 3	Module 3: Logic Gates Inverter, AND, OR, NAND, NOR, EX-OR, and EX-NOR Gates Introduction to DEEDS
W 4	Module 4: Boolean Algebra and Logic Simplification Boolean Operation and Expression, Laws and Rules of Boolean Algebra
W 6	MID-SEMESTER BREAK

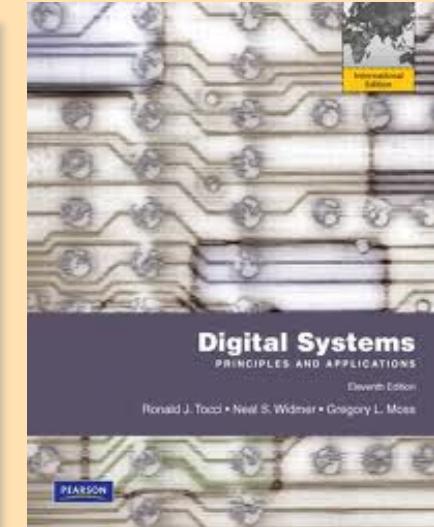
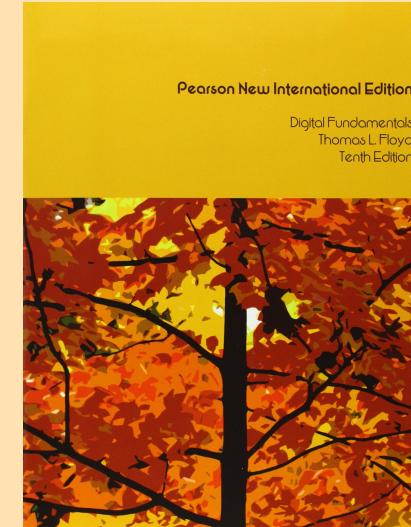
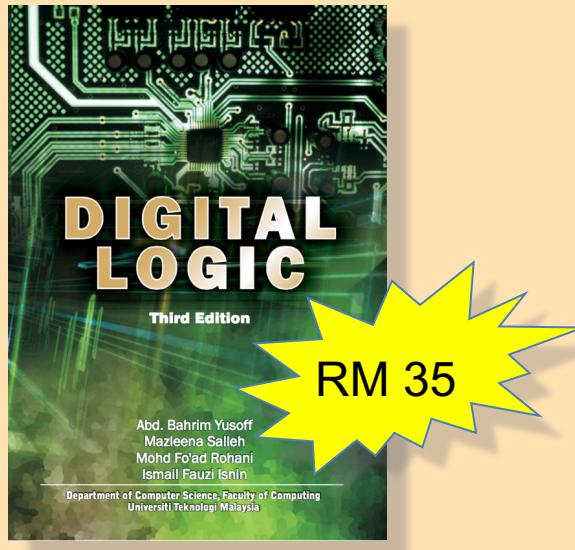
Syllabus ...

W 7	DeMorgan's Theorem, Combinational Logic Representation, Boolean Expressions, Truth Table, Karnaugh Map (K-Map)
W 8	
W 9	Module 5: Combinational Logic Circuit AND-OR, AND-OR-INVERT, XOR, XNOR, Universal Property of NAND and NOR
W 10	Module 6: Functions of Combinational Logic Decoders, Encoders, Multiplexer (Data Selector), Demultiplexer, Code Converter, Parity Generator/ Checker
W 11	Module 7: Latches, Flip-Flops and Timers

Syllabus ...

W 12	Module 8: Counters Operation, Design and Analysis of Asynchronous Counter, Operation, Design and Analysis of Synchronous Counter (Up/Down, Cascaded) Counter Applications
W 13	
W 14	
W 15	Module 9: Shift Register Shift Register, Bidirectional Shift Register, Shift Register Counter
W 16 - 18	REVISION WEEK AND FINAL EXAM

References



Main references:

- Digital Logic (2017), Edition 3, Department of Computer Science, Faculty of Computing.
- Floyd, T.L., (2014), “Digital Fundamentals”, 10th Edition, Prentice Hall, USA.

Additional references:

- Tocci, R.J., Widmer, N.S. and Moss, G.L, (2014), “Digital Systems”, 11th Edition, Prentice Hall, USA.
- Roth, C., (2014), “Fundamental of Logic Design”, 7th Edition, Thomson Brooks, USA.

Assessments

No	Continuous Assessment	Percentage	Important Dates:
1	Lab 1	3	W4 & W5
2	Lab 2	4	W8 & W9
3	Lab 3	4	W12 & W13
4	Test 1	15	6 October 2017
5	Test 2	25	24 November 2017
6	Project Report	9	W15
7	Project Demo	5	W15
	Final Assessment	PLO	
1	Final Exam	35	

Course Policies

Course Policy:

1. Attendance is compulsory and will be taken in every lecture session. Student with less than 80% of total attendance is not allowed to sit for final exam.
2. Students are required to behave and follow the University's dressing regulation and etiquette while in the class, lab, and exam hall.
3. Exercises and tutorial will be given in class and some may be taken for assessment. Students who do not do the exercise will lose the coursework marks for the exercise.
4. Assignments must be submitted on the due dates. Some points will be deducted for the late submission.
5. Assignments that are hand over after three days from the due dates will not be accepted.
6. Make up exam will not be given, except to students who are sick and submit medical certificate which is confirmed by UTM panel doctors. Make up exam can only be given within one week from the initial date of exam.