DATE

EXPT.NO.

Implement an odd/even parity generator and checker using only 2-input NAND gates.

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What is Parity Bit?

During data transmission on the basis of data bits Extra bit is transmitted and in the receiver side it is checked whether there is an error or not.

- There may be two types of parity generator -
  odd (generates parity bit keeping number of 1s odd)
  even (keeping number of 1s even)

- I will implement Three bit even parity generator.

3-bit data			
A	B	C	P(parity Bit<even>)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

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K-Map

C \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

We can see the check-board configuration

$\therefore \boxed{P = A \oplus B \oplus C}$

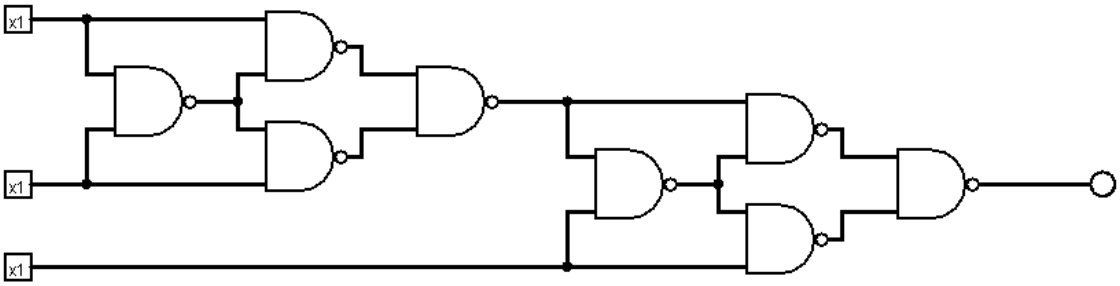
$P = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$

$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$

$= A \oplus B \oplus C$

Now, we will implement the even parity generator circuit using 2-input NAND gates.



EVEN PARITY GENERATOR

Parity checker :

It will check the data bits with parity bit and output will be high if there is error.

As we have generated even parity, so we will check even parity and generate error output.

A	B	C	P	Parity Error (C_P)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

K-Map:-

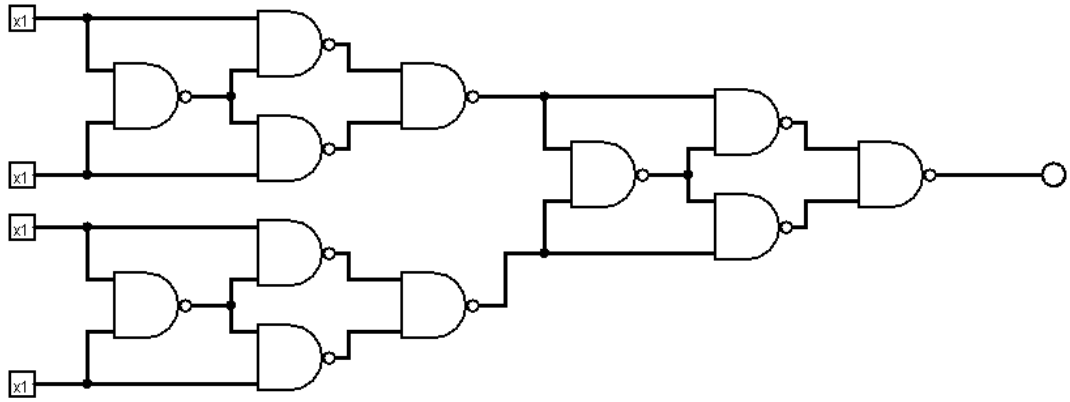
AB \ Cp	00	01	11	10
00	0	(1)	0	(1)
01	(1)	0	(1)	0
11	0	(1)	0	(1)
10	(1)	0	(1)	0

We can see here check-board configuration

So, Cp can be written as -

$$C_p = A \oplus B \oplus C \oplus P$$

Now, we will implement even parity checker circuit using 2-input NAND gates.



EVEN PARITY CHECKER