

DATE
EXPT.NO.

Assignment 4:

Implement a 4-to-1 multiplexer using two input NAND logic gates.

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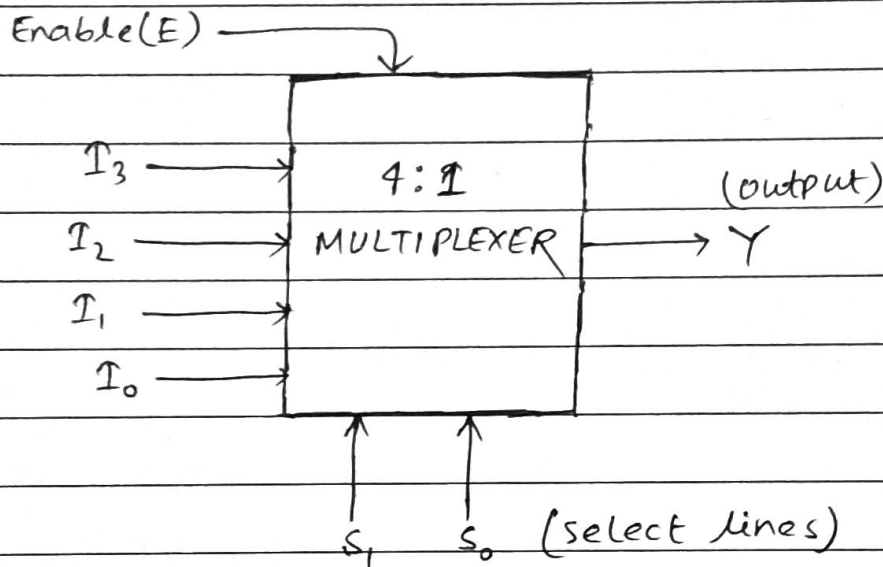
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Dept - CSE

4 to 1 Multiplexer :

This consists four data input lines I_0, I_1, I_2, I_3 , and two select lines S_0, S_1 and One output Y that will give one of the four Input lines. There will be an Enable (E) to actually enable the circuitry.



Truth Table :

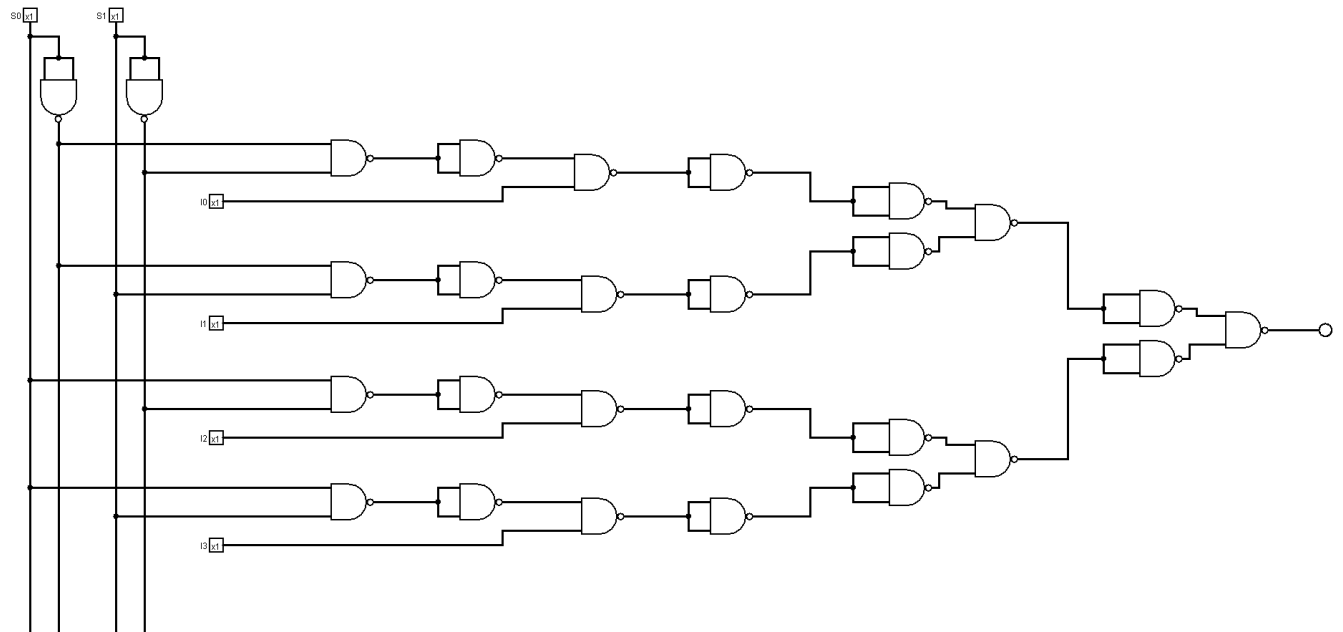
S_0	S_1	$Y (E=1)$	[Here the output line selects one of the inputs on the basis of select lines value]
0	0	I_0	
0	1	I_1	
1	0	I_2	
1	1	I_3	

Teacher's Signature

So, the expression for Y will be \rightarrow

$$Y = \bar{S}_0 \bar{S}_1 I_0 + \bar{S}_0 S_1 I_1 + S_0 \bar{S}_1 I_2 + S_0 S_1 I_3$$

Now we will implement the circuit using two input NAND gates.

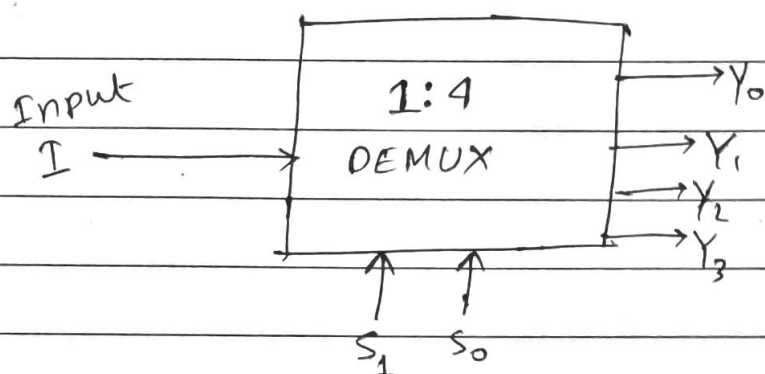


4 to 1 MULTIPLEXER

1 to 4 demultiplexer using two input NAND logic gates.

1-to-4 demultiplexer :

It consists of a single Input I two select lines S_0, S_1 , and four outputs Y_0, Y_1, Y_2, Y_3 . The input data goes to any of the four outputs for a particular combination of select lines.



Truth Table

S_0	S_1	Y_0	Y_1	Y_2	Y_3
0	0	I	0	0	0
0	1	0	I	0	0
1	0	0	0	I	0
1	1	0	0	0	I

[Here the input comes to any of four outputs]

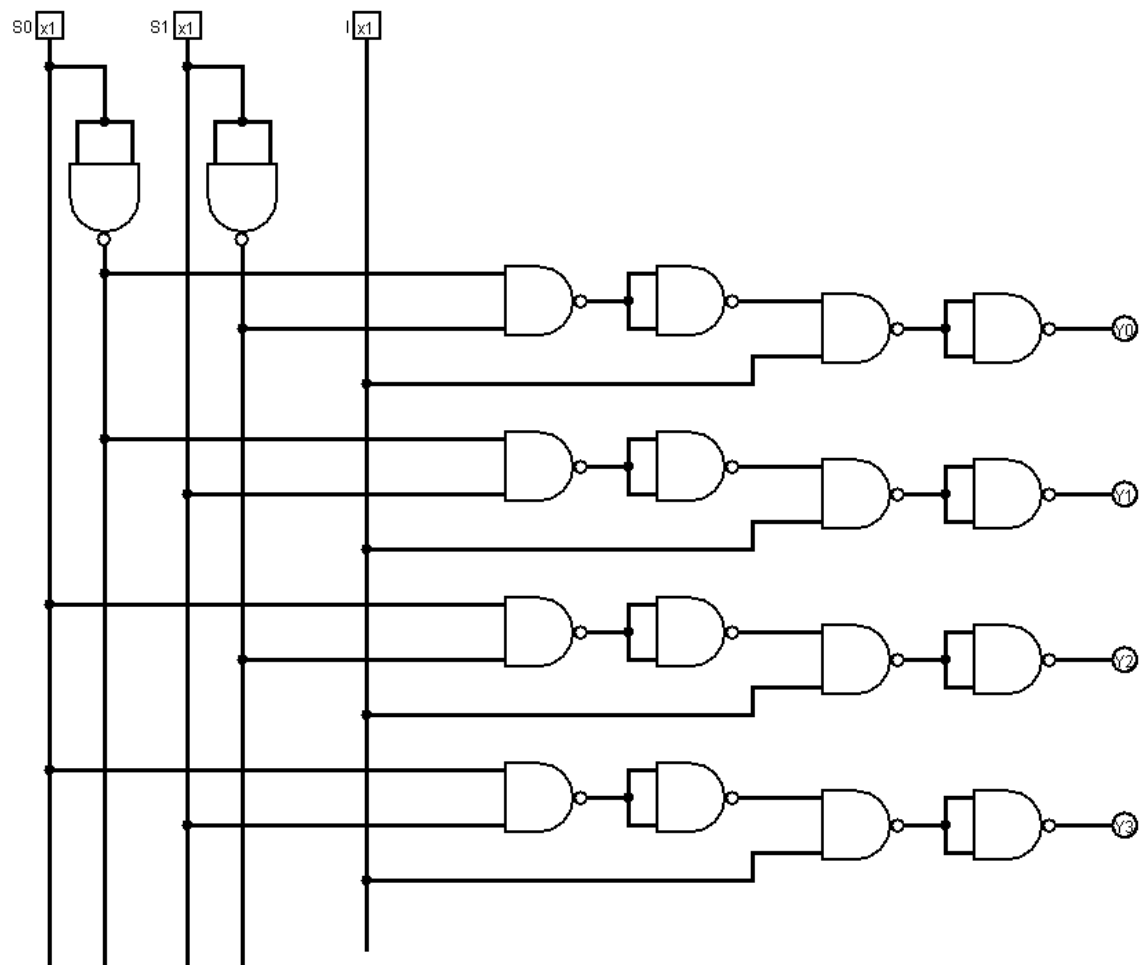
$$S_0, Y_0 = \bar{S}_0 \bar{S}_1 I$$

$$Y_1 = \bar{S}_0 S_1 I$$

$$Y_2 = S_0 \bar{S}_1 I$$

$$Y_3 = S_0 S_1 I$$

Now, we will implement the circuit using two-input NAND gates.



1 TO 4 DEMULTIPLEXER