DATE

EXPT.NO.

Implement a comparator circuit for two 3-bit numbers using only 2-input NAND gates.

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Dept: - CSE

What Is A comparator Circuit ?

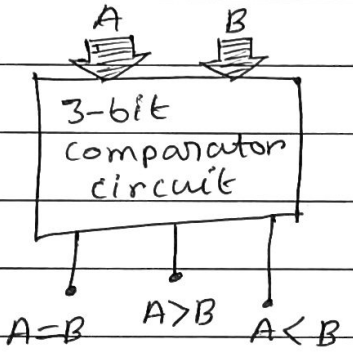
A comparator circuit is used ~~two~~ to compare magnitude of two n-bit binary numbers.

Here, we will implement a 3-bit comparator circuit

Let, the two 3-bit numbers are A and B

There will be three possibilities ⇒ 1) A=B, 2) A>B, 3) A<B

$A = A_2 A_1 A_0$ and $B = B_2 B_1 B_0$



For A=B

In this case, corresponding bits will be equal

$\therefore A_2 = B_2$ and $A_1 = B_1$ and $A_0 = B_0$

We can use XNOR to implement equality of bits

Here,

$$(\text{Output}) = (A_2 \odot B_2) \cdot (A_1 \odot B_1) \cdot (A_0 \odot B_0)$$

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Output = $(\overline{A_2}\,\overline{B_2} + A_2B_2) \cdot (\overline{A_1}\,\overline{B_1} + A_1B_1) \cdot (\overline{A_0}\,\overline{B_0} + A_0B_0)$

For A > B

Case I :→ If $A_2 > B_2$

$\Rightarrow A_2 = 1$ and $B_2 = 0$ $\Rightarrow$ Output = $A_2\overline{B_2}$

(other bit values doesn't matter)

Case II :→

If $A_2 = B_2$ and $A_1 > B_1$

$\Rightarrow (A_2 \odot B_2) = 1$ and $A_1 = 1$ and $B_1 = 0$

output $\Rightarrow$ $A_1\overline{B_1}(\overline{A_2}\,\overline{B_2} + A_2B_2)$

Case III :→

If $A_2 = B_2$ and $A_1 = B_1$ and $A_0 > B_0$

$\therefore$ output = $A_0\overline{B_0}(\overline{A_1}\,\overline{B_1} + A_1B_1)(\overline{A_2}\,\overline{B_2} + A_2B_2)$

So, Final Output for A > B

$= A_2\overline{B_2} + A_1\overline{B_1}(\overline{A_2}\,\overline{B_2} + A_2B_2) + A_0\overline{B_0}(\overline{A_1}\,\overline{B_1} + A_1B_1) \cdot (\overline{A_2}\,\overline{B_2} + A_2B_2)$

For A < B

Case I :→ If $A_2 < B_2$

$\therefore$ output = $\overline{A_2}\,B_2$

Case II :→

If $A_2 = B_2$ and $A_1 < B_1$

output = $\overline{A_1}\,B_1(\overline{A_2}\,\overline{B_2} + A_2B_2)$

Case III :→

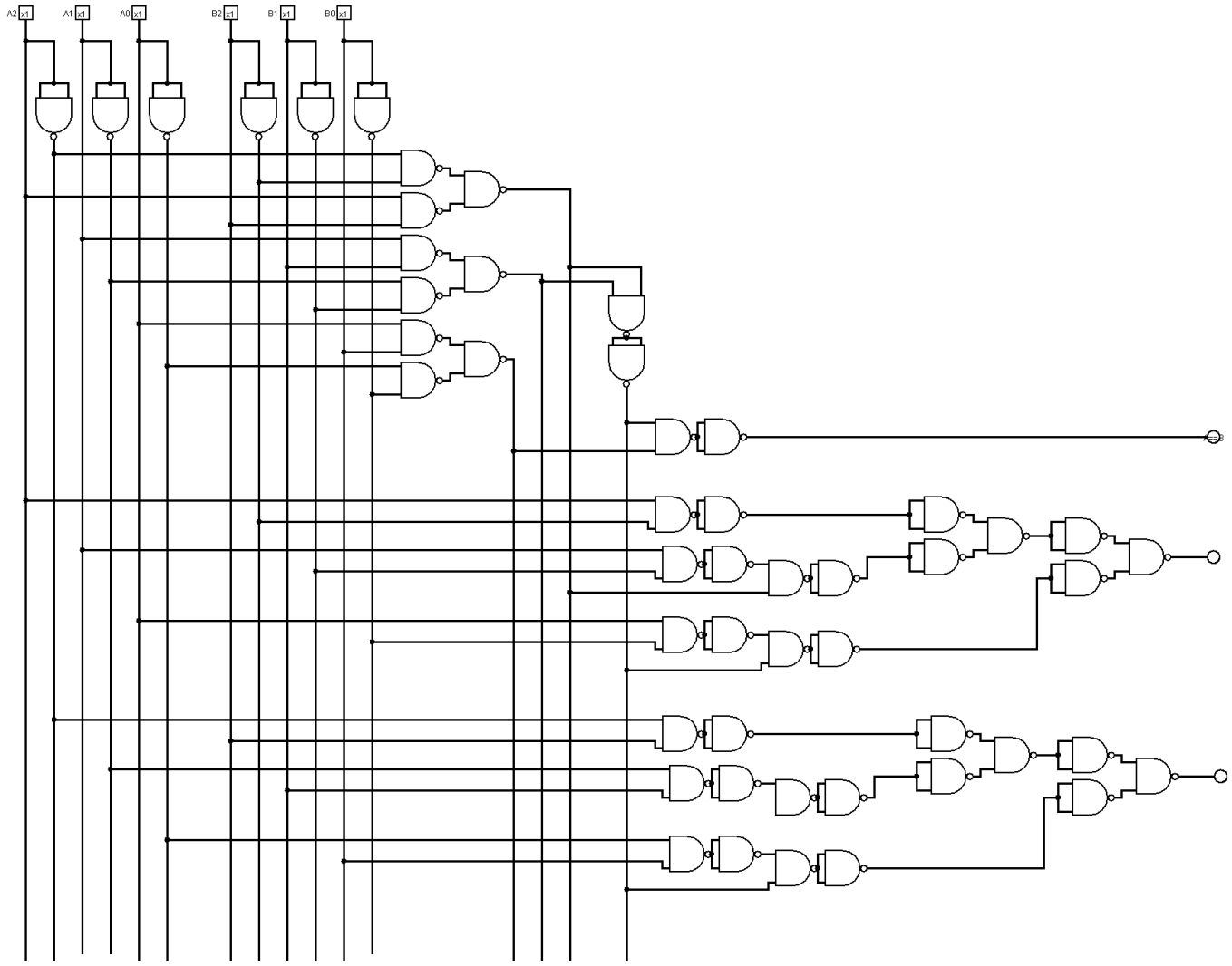
If $A_2 = B_2$ and $A_1 = B_1$ and $A_0 < B_0$

output = $\overline{A}_0 B_0 (\overline{A}_2 \overline{B}_2 + A_2 B_2)(\overline{A}_1 \overline{B}_1 + A_1 B_1)$

Final output for $(A < B)$

$= \overline{A}_2 B_2 + \overline{A}_1 B_1 (\overline{A}_2 \overline{B}_2 + A_2 B_2) + \overline{A}_0 B_0 (\overline{A}_2 \overline{B}_2 + A_2 B_2)(\overline{A}_1 \overline{B}_1 + A_1 B_1)$

Now, I will implement the circuit using only two input NAND gates.



FIRST OUTPUT: A=B | SECOND OUTPUT: A>B

THIRD OUTPUT: A<B

THREE BIT COMPARATOR CIRCUIT