

3. Clippers and Clampers

3.1. Clippers

A Clipper is a circuit which removes the peak of a waveform. There are two types of clippers:

- ✓ **Series clippers**, where the diode is in series with the output voltage.
- ✓ **Parallel clippers**, where the diode is in parallel with the output voltage.

Example: Half wave rectifier is a clipper.

Application 1 :

Positive Clipper Circuit (ideal diode)

This is a parallel clipper with positive bias E

With : $E < V_{ip}$

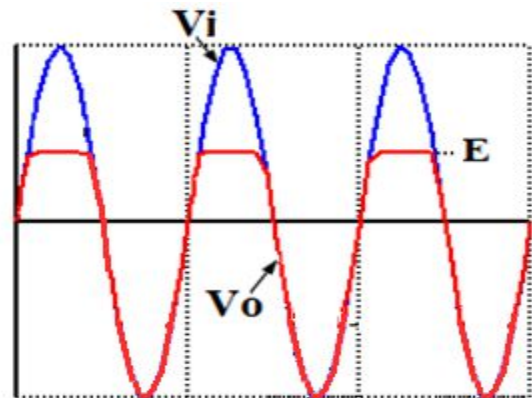
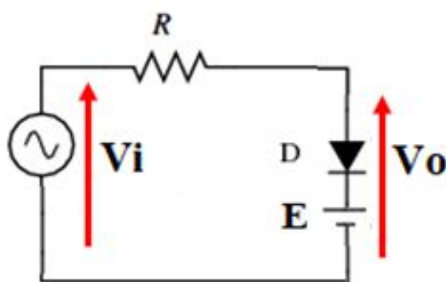


Fig.2.12.1. Positive Clipper Circuit

D is **ON** if $V_a - V_k > 0$

$V_i - E > 0 \Rightarrow V_i > E$

$V_o = E$

D is **OFF** if **$V_i < E$**

$V_o = V_i$

Application 2 :

Negative Clipper Circuit (ideal diode)

This is a parallel clipper with negative bias $-E$

With : $E < V_{ip}$

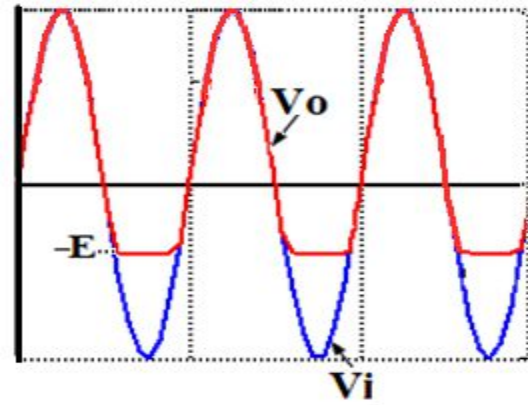
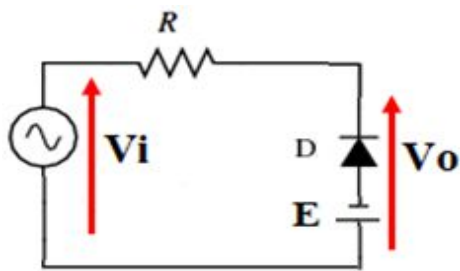


Fig.2.12.2. Negative Clipper Circuit

D is **ON** if $V_a - V_k > 0$

$$-E - V_i > 0 \Rightarrow V_i < -E$$

$$V_o = -E$$

D is **OFF** if $V_i > -E$

$$V_o = V_i$$

Application 3:

Positive and negative Clipper Circuit (ideal diodes)

E_1 and E_2 are both $< V_{ip}$

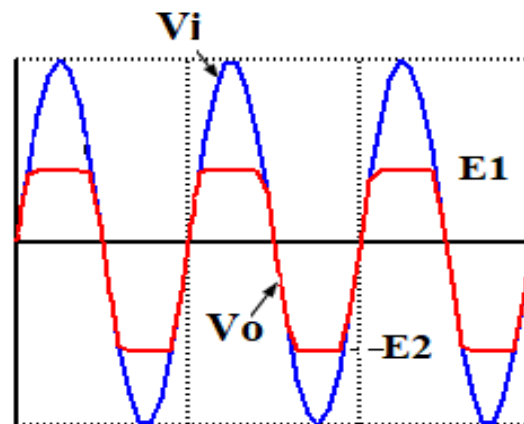
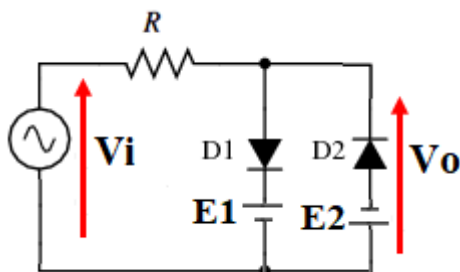


Fig.2.12.3. Positive and Negative Clipper Circuit

D1 is **ON** if $V_a - V_k > 0$

$$V_i - E_1 > 0 \Rightarrow V_i > E_1$$

$$V_o = E_1$$

D2 is **ON** if $V_a - V_k > 0$

$$-E_2 - V_i > 0 \Rightarrow V_i < -E_2$$

$$V_o = -E_2$$

D1 and D2 are **OFF** if $-E2 < V_i < E1$

$$V_o = V_i$$

Note:

There is also a **Zener diode clipper** circuit in the “Zener diode” section. A Zener diode replaces both the diode and the DC voltage source.

3.2. Clampers

A clamper is a network constructed of a diode, a resistor and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Application 1:

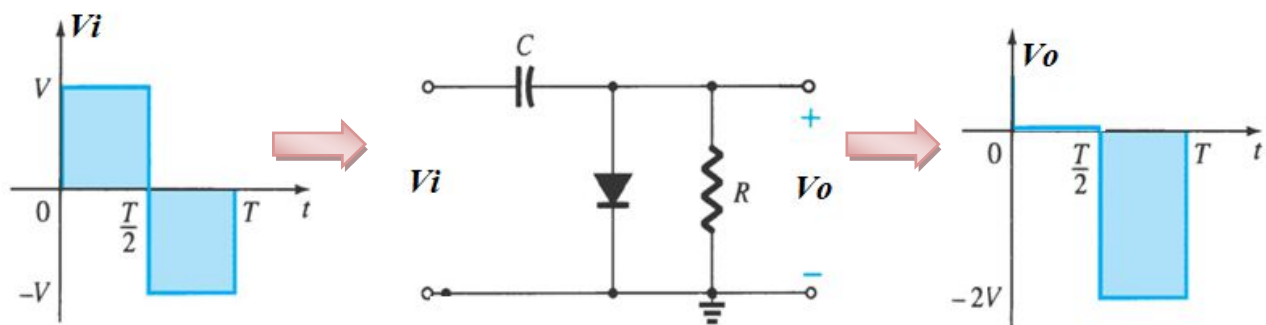


Fig.2.13.1. Clamper Circuit

Analysis (ideal diode)

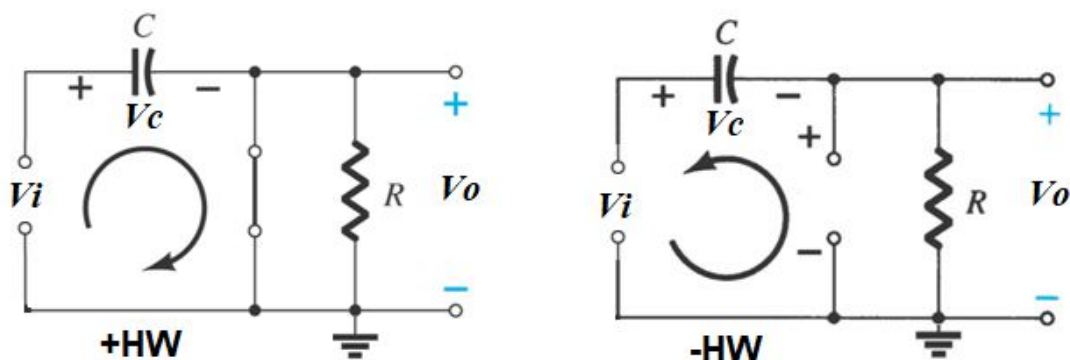
Operation at forward biased ($V_i > 0$), the diode is short circuited (ON). The voltage will be:

$$V_o = 0$$

Since the current is shorted through the diode and the capacitor is charged up to a voltage

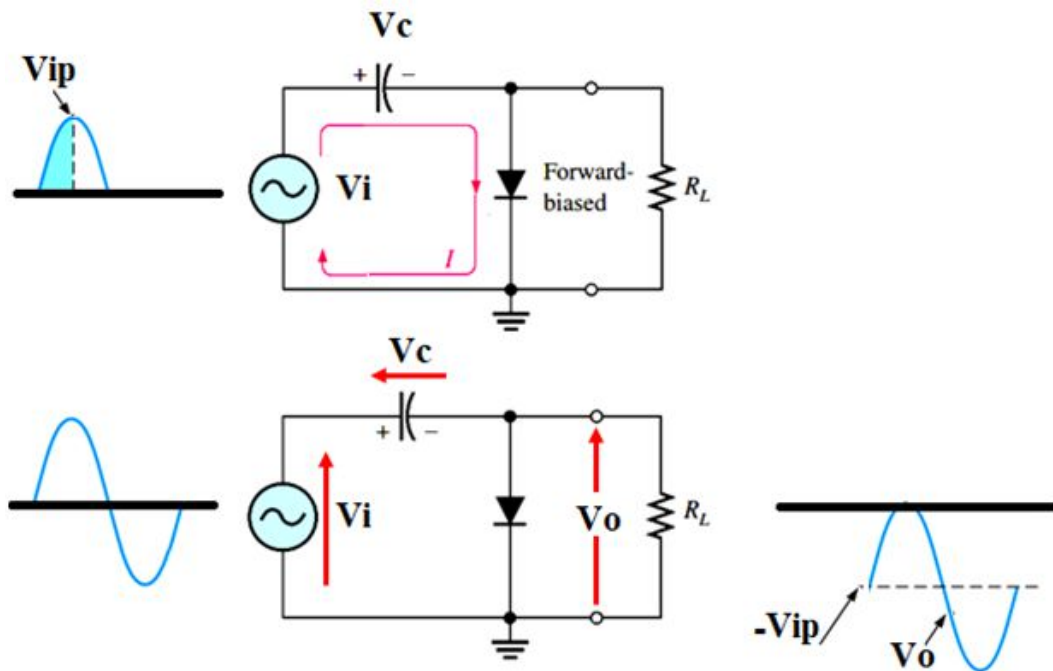
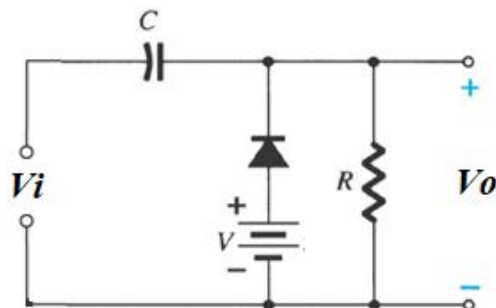
$$V_c = V_i(\text{peak}).$$

During reverse biased ($V_i < 0$), the diode is open circuited (OFF). The voltage across R will be: $V_o = V_i - V_c = V_i - V_i(\text{peak})$



Application 2: Clampers with sin signal.

When the input voltage initially goes positive, the diode is forward biased, allowing the capacitor to charge to near the peak of the input (V_{ip}). Just after the positive peak, the diode is reverse-biased. This is because the anode is held near ($-V_{ip}$) by the charge on the capacitor. The capacitor can only discharge through the resistance R_L . So, from the peak of one positive half-cycle to the next, the capacitor discharges very little.

*Application 3:*

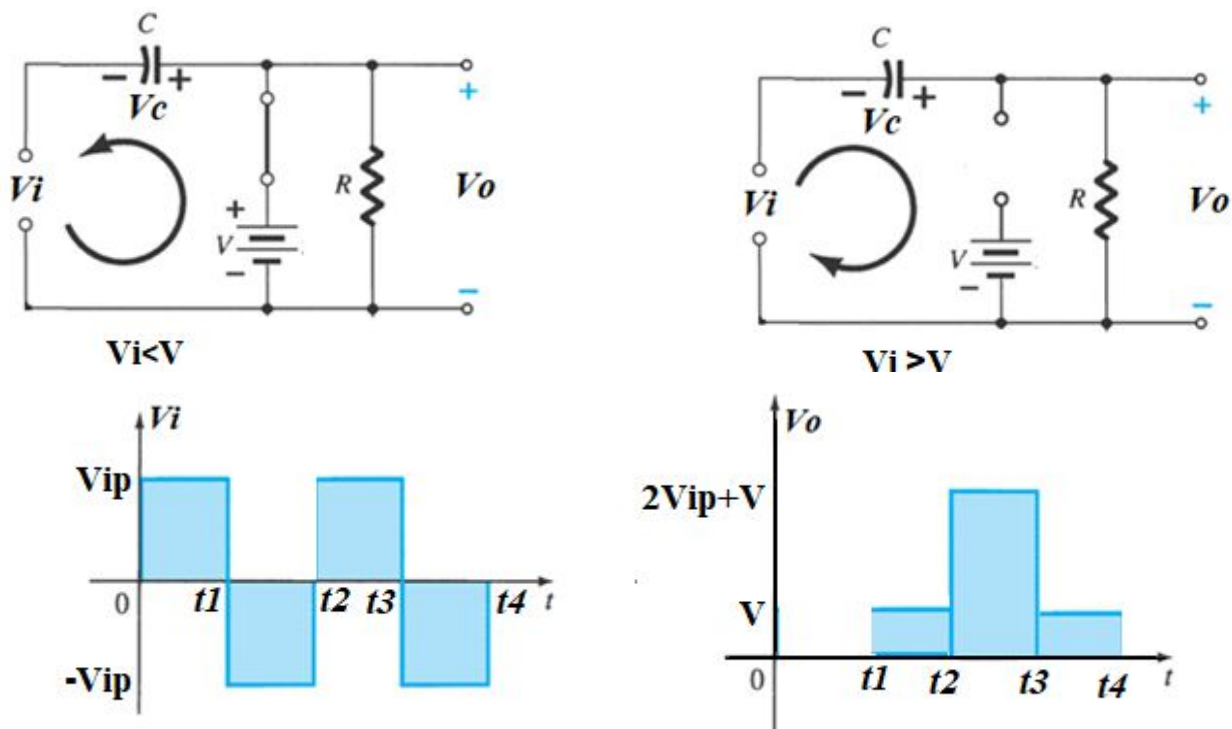
Operation at forward biased ($V_i < V$), the diode is short circuited (**ON**). The voltage will be:

$$V_o = V$$

The capacitor is charged up to a voltage:

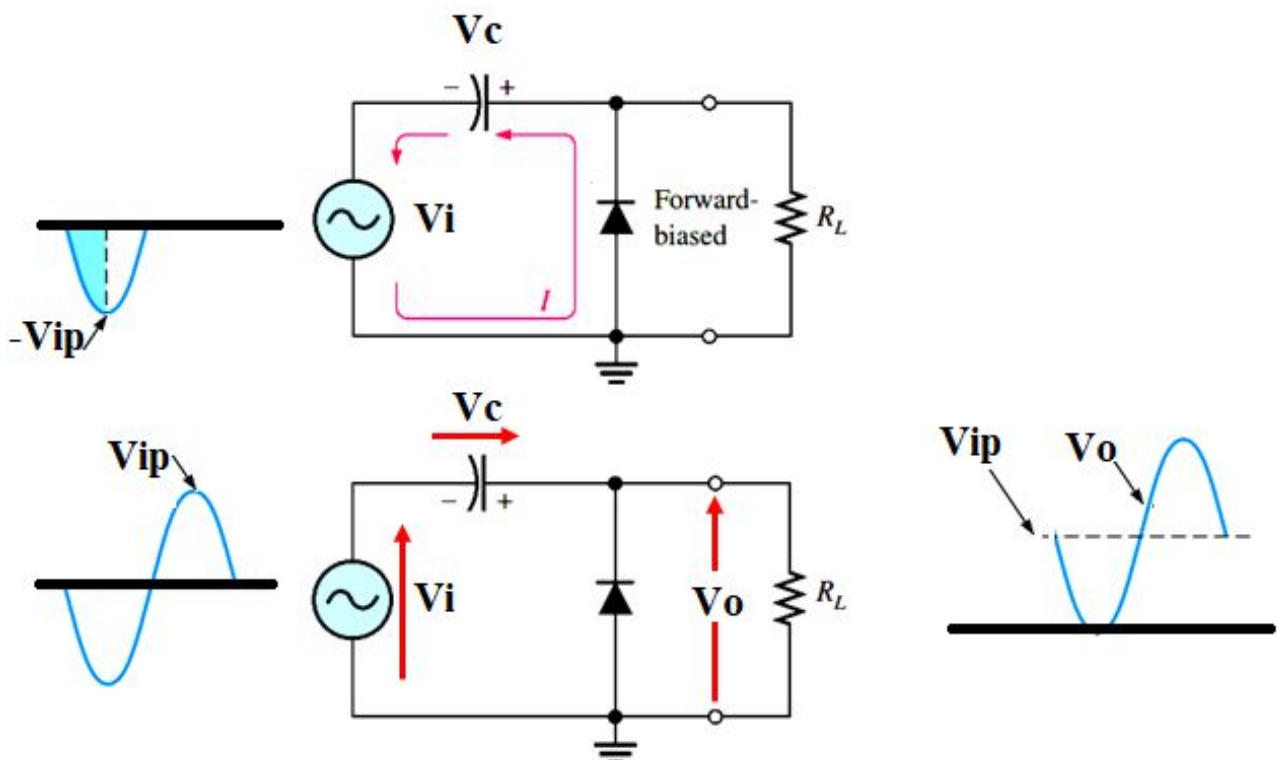
$$V_c = -V_i + V = V_i(\text{peak}) + V$$

During reverse biased ($V_i > V$), the diode is open circuited (**OFF**). The voltage across R will be: $V_o = V_i + V_c = V_i + V_i(\text{peak}) + V$



Application 4: Clampers with sin signal.

When the input voltage initially goes negative, the diode is forward biased, allowing the capacitor to charge to near the peak of the input (V_{ip}).



Just after the negative peak, the diode is reverse-biased. This is because the cathode is held near (V_{ip}) by the charge on the capacitor.

The capacitor can only discharge through the resistance RL . So, from the peak of one negative half-cycle to the next, the capacitor discharges very little. The amount that is discharged, of course, depends on the value of RL and C .

All clamper circuits:

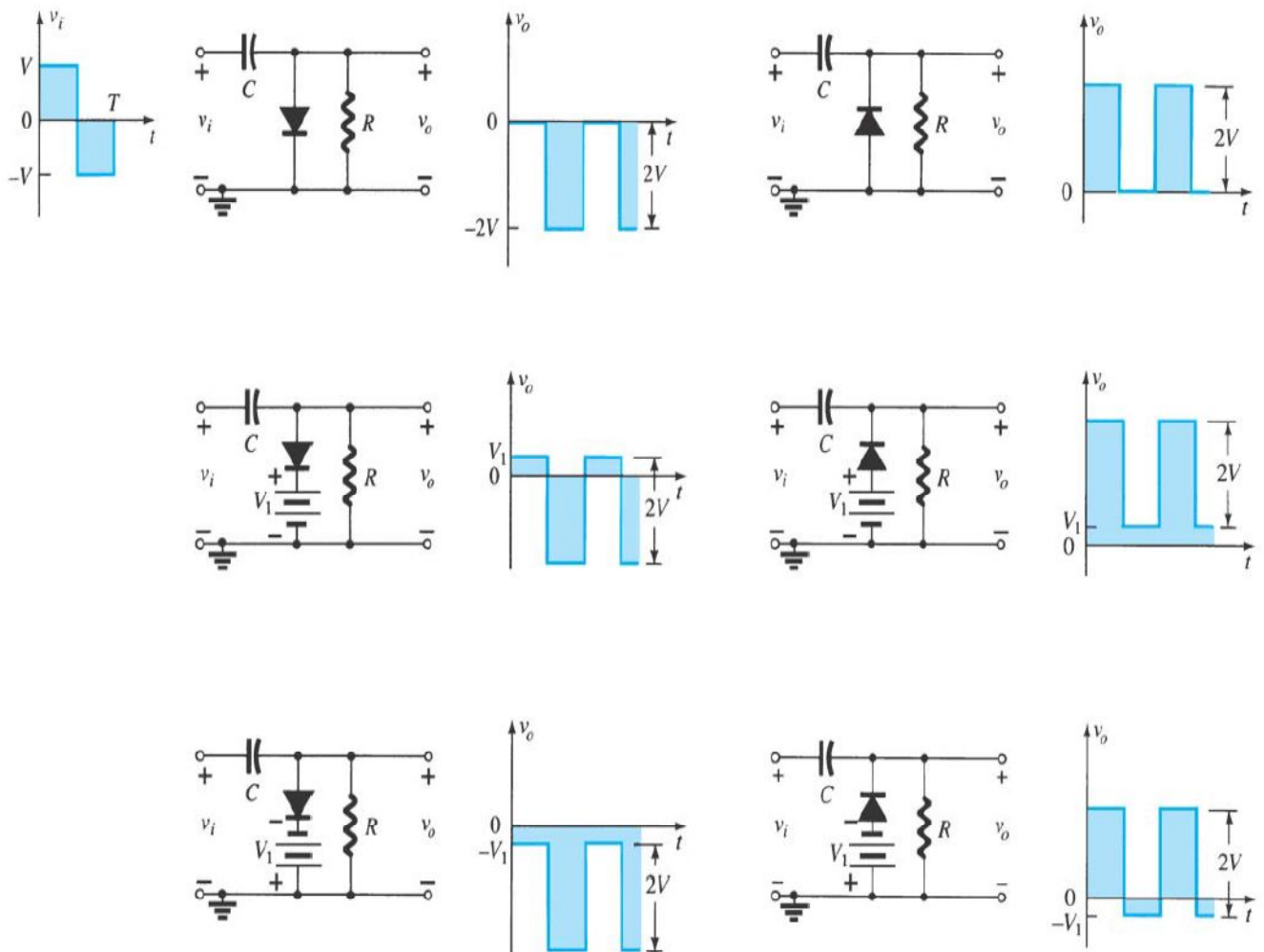


Fig.2.13.2. Clamper Circuits

4. Voltage multiplier circuits

A *voltage multiplier* is a specialized rectifier circuit producing an output which is theoretically an integer times the AC peak input, for example, 2, 3, or 4 times the AC peak input. Thus, it is possible to get 200V(DC) from a 100 Vpeak (AC) source using a doubler, 400V(DC) from a quadrupler. Any load in a practical circuit will lower these voltages.

4.1. Half-Wave Voltage Doubler

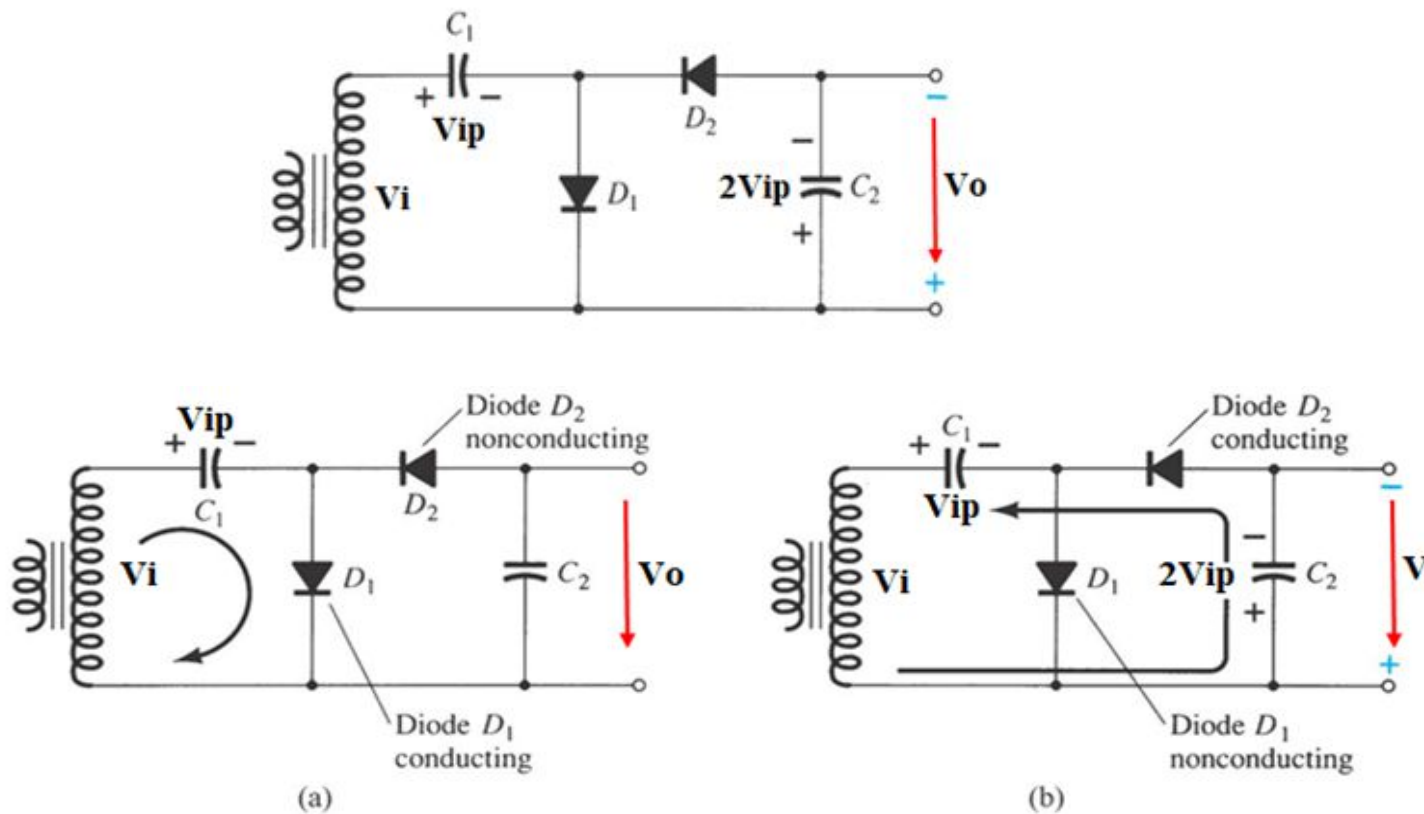
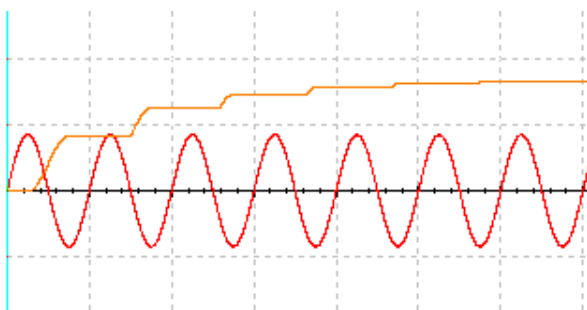
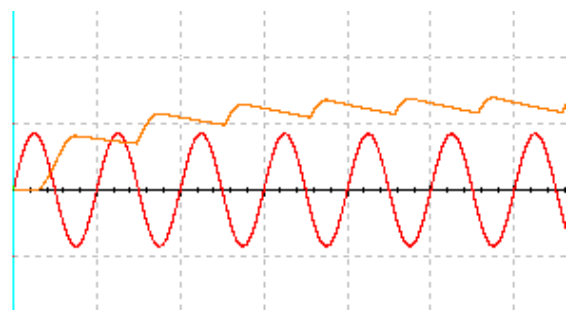


Fig.2.14.1. Half-Wave Voltage Doubler

- During the positive half-cycle across the transformer, the diode D_1 conducts and D_2 is cut off. The capacitor C_1 charge-up to peak rectified voltage V_{ip} .
- Second half cycle, D_2 conducts and D_1 is cut-off. Now the capacitor C_2 is charged up with $V_{ip} + V_C = V_{ip} + V_{ip} = 2V_{ip}$



Half wave doubler (V_o)



Half wave doubler (with load $R // V_o$)

4.2. Full-Wave Voltage Doubler

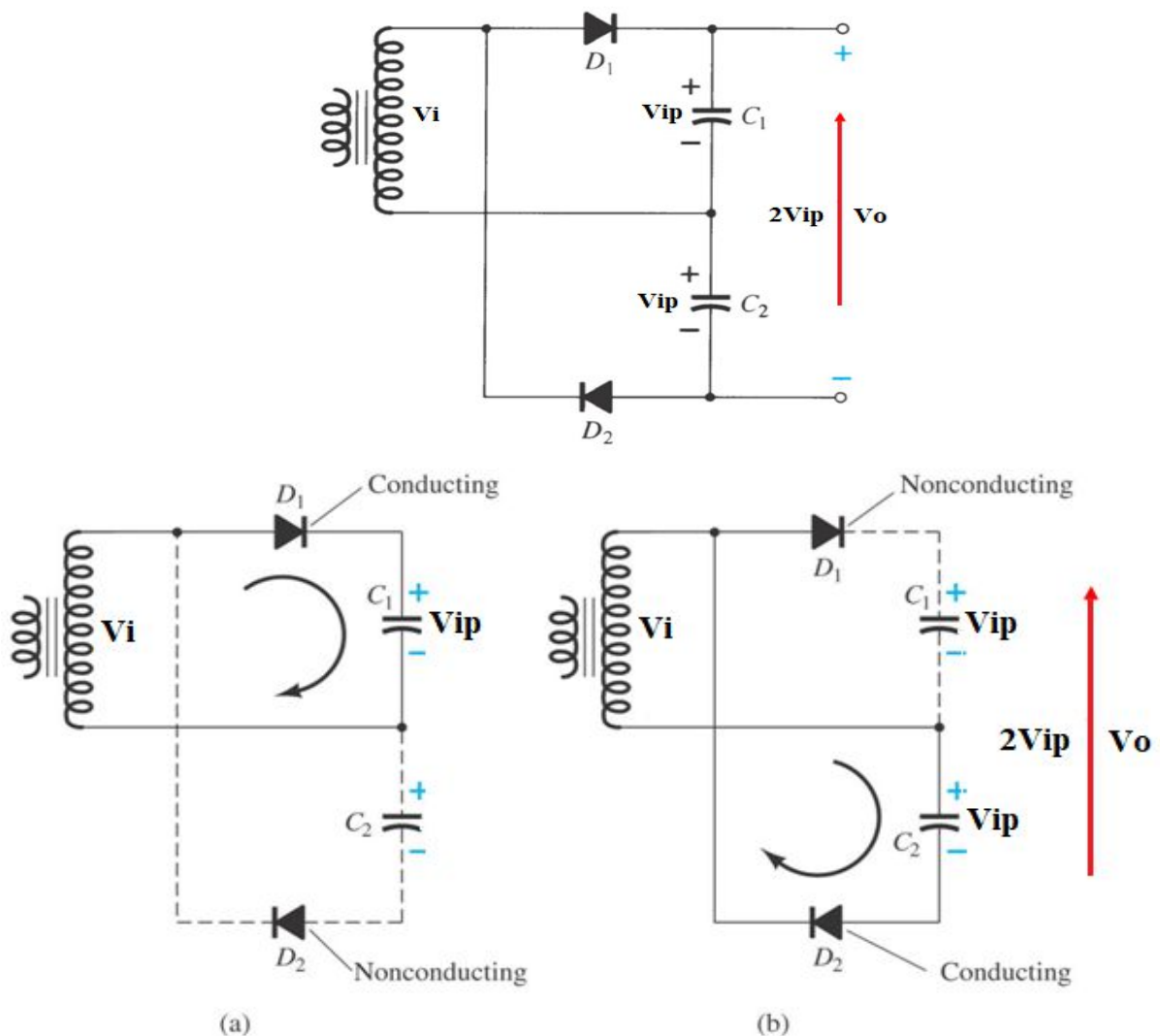
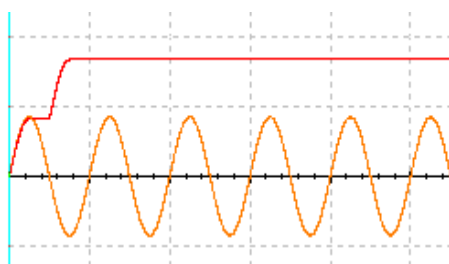
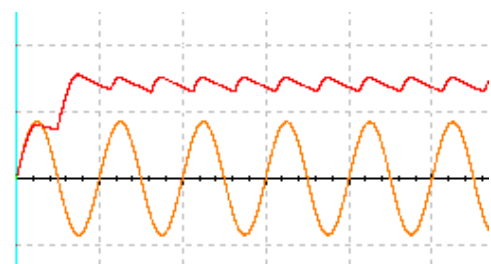


Fig.2.14.2. Full-Wave Voltage Doubler

- Positive cycle, D_1 is conducting, thus charging C_1 to V_{ip} . D_2 is not conducting \Rightarrow No charging of the capacitor C_2 .
- Negative cycle, D_2 is conducting, thus charging C_2 to V_{ip} . D_1 is not conducting \Rightarrow C_1 still maintain the charging voltage V_{ip} .



Full wave doubler (V_o)



Full wave doubler (with load $R // V_o$)

4.3. Half-Wave Doubler, Tripler and Quadrupler

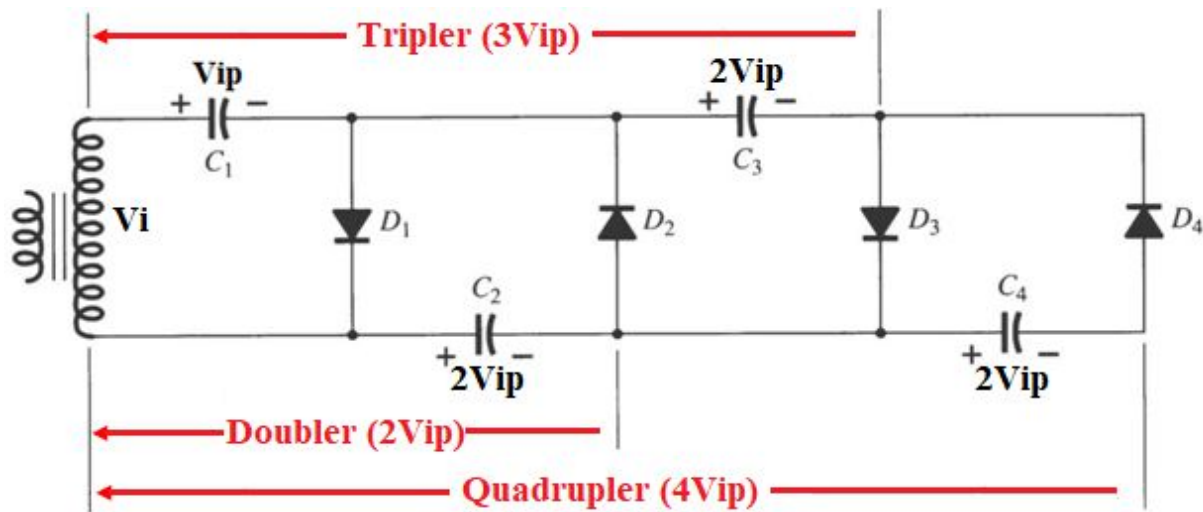


Fig.2.14.3. Voltage Multiplier circuit

By arranging alternately capacitor and diode, we are able to obtain voltage **doubler**, **tripler** and **quadrupler**.

C_1 plus transformer will charge C_2 . C_2 will charge C_3 and C_3 will charge C_4 .

5. Peak detector

A *peak detector* is a series connection of a diode and a capacitor outputting a DC voltage equal to the peak value of the applied AC signal (The circuit is shown in the following Figure).

An AC voltage source applied to the peak detector, charges the capacitor to the peak of the input. The diode conducts positive “half cycles,” charging the capacitor to the waveform peak. When the input waveform falls below the DC “peak” stored on the capacitor, the diode is reverse biased, blocking current flow from capacitor back to the source. Thus, the capacitor retains the peak value even as the waveform drops to zero.

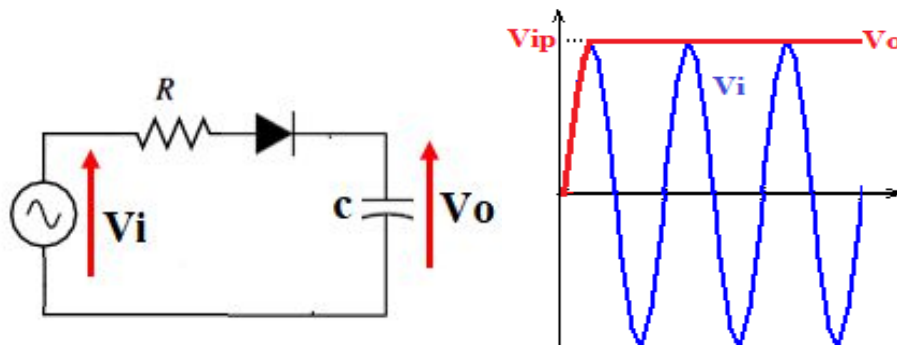


Fig.2.15. Peak detector circuit