BIPOLAR JUNCTION TRANSISTORS (BJT'S)

1. Introduction

The pn junction studied in Chapter II forms the basis of a large number of semiconductor devices. The semiconductor diode, a two-terminal device, is the most direct application of the pn junction. In this Chapter, we will introduce the physics of transistor devices as intuitively as possible, resorting to an analysis of their i -v characteristics to discover important properties and applications.

2. Definitions

a. Transistor : Transfer resistor

The term **Transistor** was adopted because it best describes the operation of the transistor which is the **transfer** of an input signal current from a **low-resistance** circuit to a **high-resistance** circuit.

The transistor is used to

- Amplify current, voltage and power signals.
- Switch electronic signals (such as logic gates) and electrical power (such as switched power supplies)

b. Bipolar junction transistor (BJT)

A BJT is formed by joining three sections of semiconductor material, each with a different doping concentration.

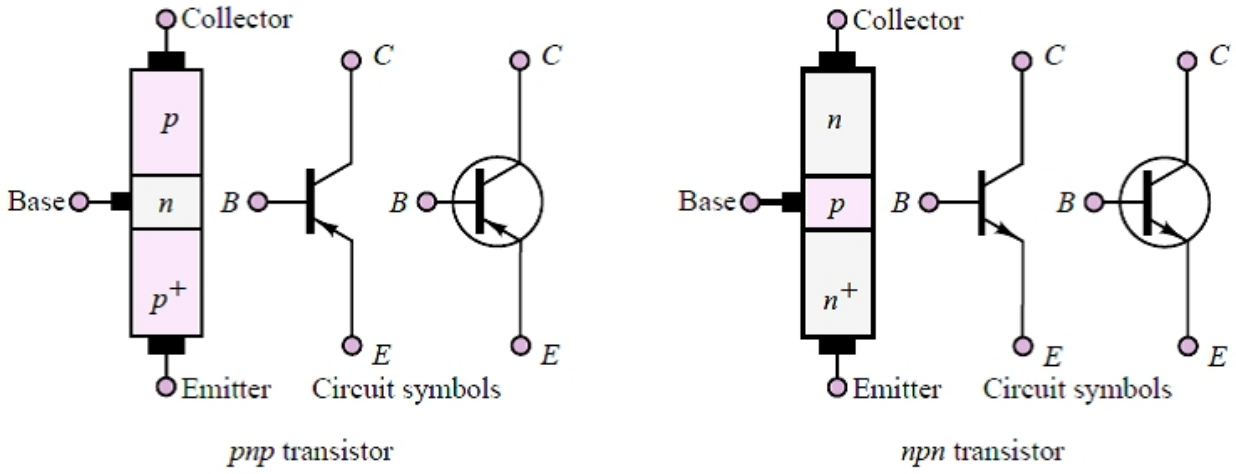


Fig.3.1: *npn* and *pnp* bipolar junction transistors (Structures and symbols)

The three sections can be either a thin n region sandwiched between p and p layers, or a p region between n and n layers, the resulting BJTs are called **pnp** and **npn** transistors, respectively. (See **Fig.3.1**)

The three layers of a BJT are:

- The emitter layer (E) is heavily doped semiconductor, it emits current carriers.
- The collector layer (C) lightly doped, it collects the current carriers.
- The base (B) is very thin lightly doped section which controls the flow of current carriers.

The most important property of the bipolar transistor is that the small bas current controls the amount of the much larger collector current.

3. BJT's description

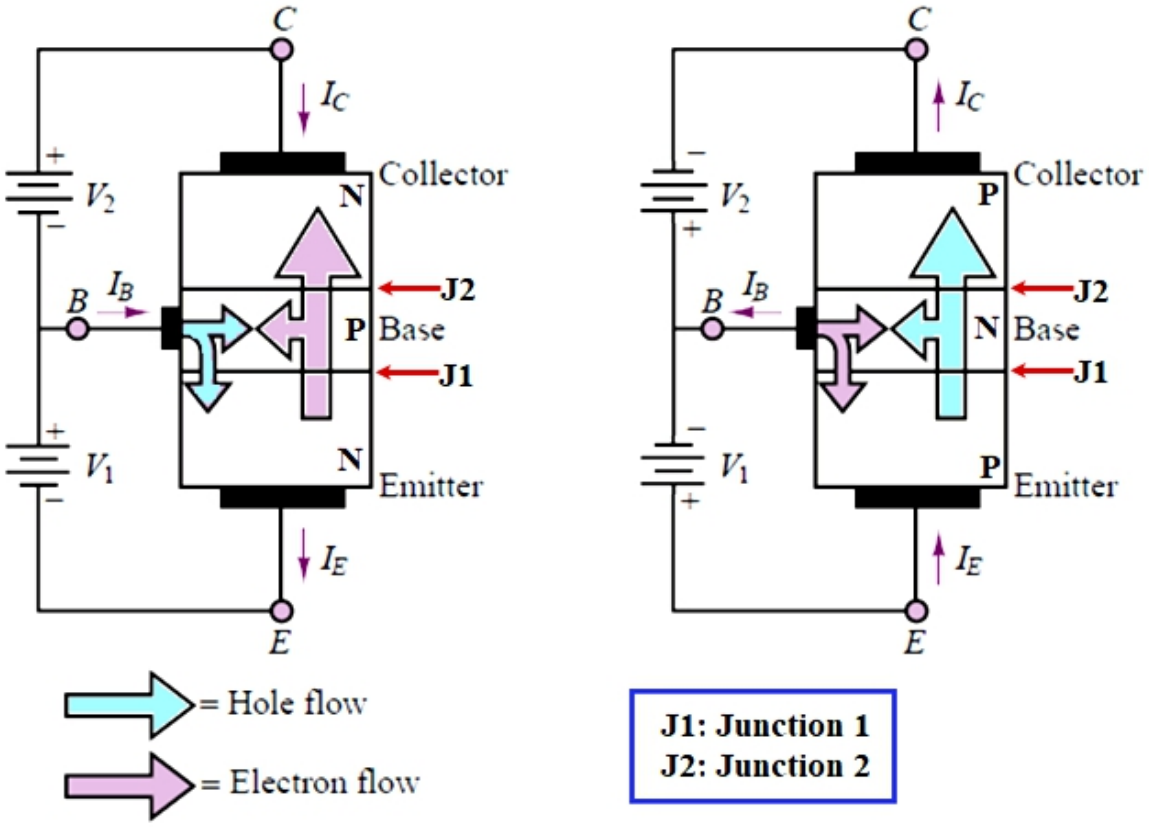


Fig.3.2: BJT's biasing

The operation of the *npn* BJT (***pnp* BJT**) may be explained by considering the transistor as consisting of two back-to-back ***pn*** junctions. The **base-emitter (*BE*) junction (J1) acts very much like a diode** when it is **forward-biased**; this bias allows the free electrons (**holes**) in emitter to go through the ***pn*** junction to arrive at the base, forming the emitter current ($\mathbf{I_E}$).

As the **p-type base** (**n-type base**) is thin and lightly doped, only a small number of the electrons (**holes**) from the emitter are combined with the holes (**electrons**) in base to form the base current (I_B).
The **base-collector (BC) junction (J2)** is **reverse-biased**, in this case, most of the electrons (**holes**) coming from the emitter, will diffuse and cross the reverse biased junction to arrive at the collector to create the collector current (I_C).

By applying KCL, we have:

$$I_E = I_B + I_C$$

4. BJT's configurations

Depending on which of the three terminals is used as common terminal, there can be three possible configurations for the two port network formed by transistor.

1) Common base configuration (CB)
2) Common emitter configuration (CE)
3) Common collector configuration (CC)

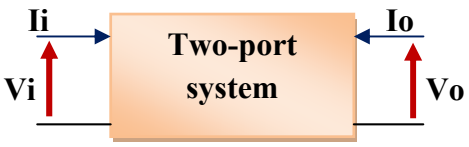


Fig.3.3: Two-port system

4.1. Common base configuration (CB)

In this configuration the input stage is the Emitter-Base stage, with: input current is I_E, input voltage is V_{EB} and The output stage is the collector –base stage, with: output current is I_C, output voltage is V_{CB}. (See **Fig.3.3.1**)

The total collector current:

$$I_C = \alpha I_E + I_{CBO}$$

Where : I_{CBO} is the minority carriers current of (BC) junction with $I_E=0$ (Saturation current).

I_{CBO} can be ignored, $I_C \approx \alpha I_E \Rightarrow$ The current gain: $I_C/I_E \approx \alpha<1$.

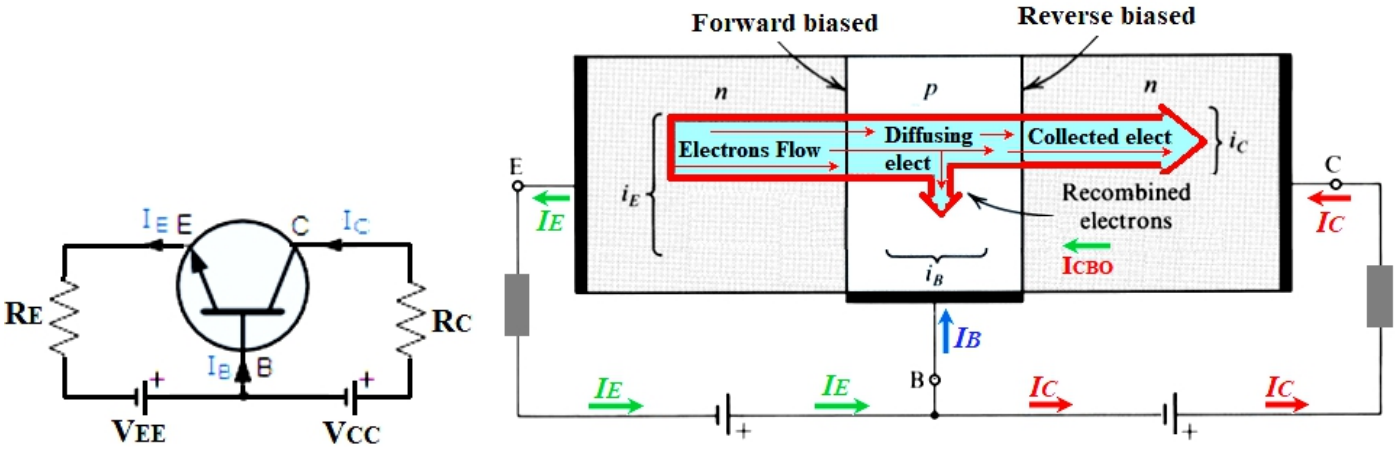


Fig.3.3.1: Common base configuration (CB)

The input ($I_E = f(V_{EB})$)and the output ($I_C = f(V_{CB})$) characteristics are given by the following figure:

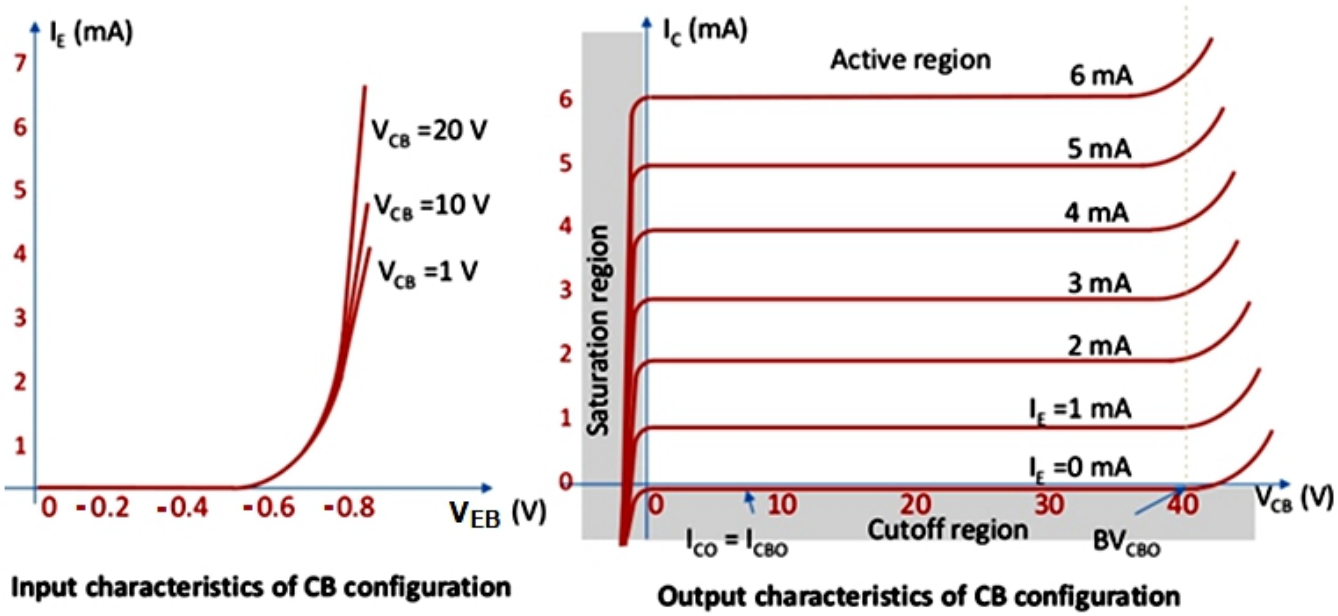


Fig.3.3.2: Common base Characteristics

4.2. Common Emitter configuration (CE)

In this configuration the input stage is the Base - Emitter stage , with: input current I_B, input voltage V_{BE} and The output stage is the collector –Emitter stage, with: output current I_C, output voltage V_{CE}.

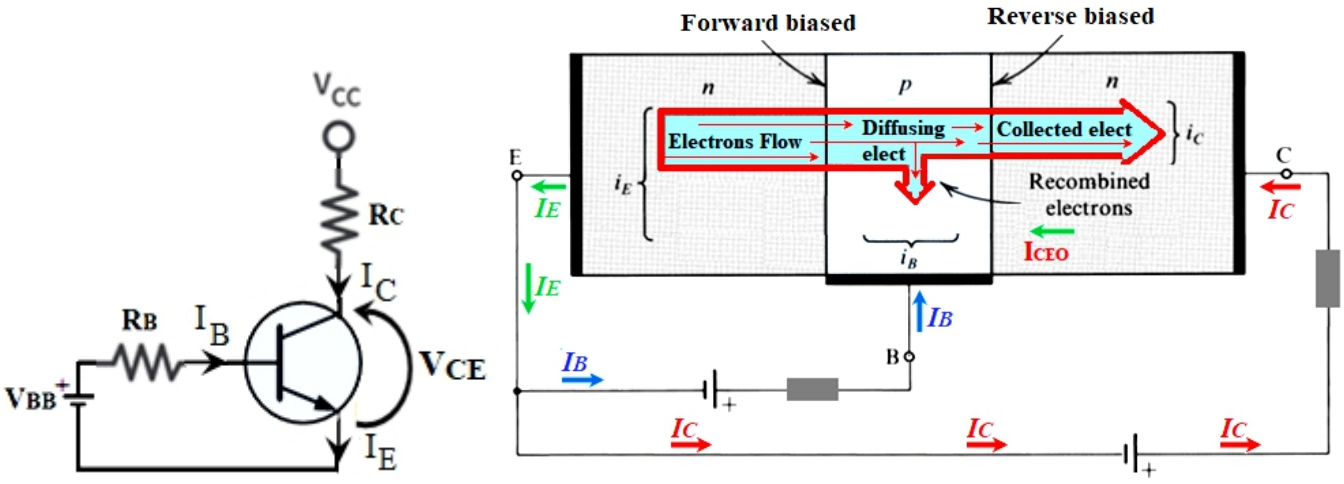


Fig.3.3.3: Common Emitter configuration (CE)

The total collector current: $I_C = \beta I_B + I_{CEO}$

Where : I_{CEO} is the (CE) minority carriers current , with $I_B=0 \Rightarrow$(Saturation current).

$I_{CEO} = (\beta+1)\, I_{CBO}$, Therefore, the total collector current can be written as:

$$\mathbf{I_C = \beta I_B + (\beta+1)\, I_{CBO}}$$

I_{CEO} can be ignored, $I_C \approx \beta I_B \Rightarrow$The current gain: $I_C/I_B \approx \beta$.

The input ($\mathbf{I_B = f(V_{BE})}$) and the output ($\mathbf{I_C = f(V_{CE})}$) characteristics are given by the following figure:

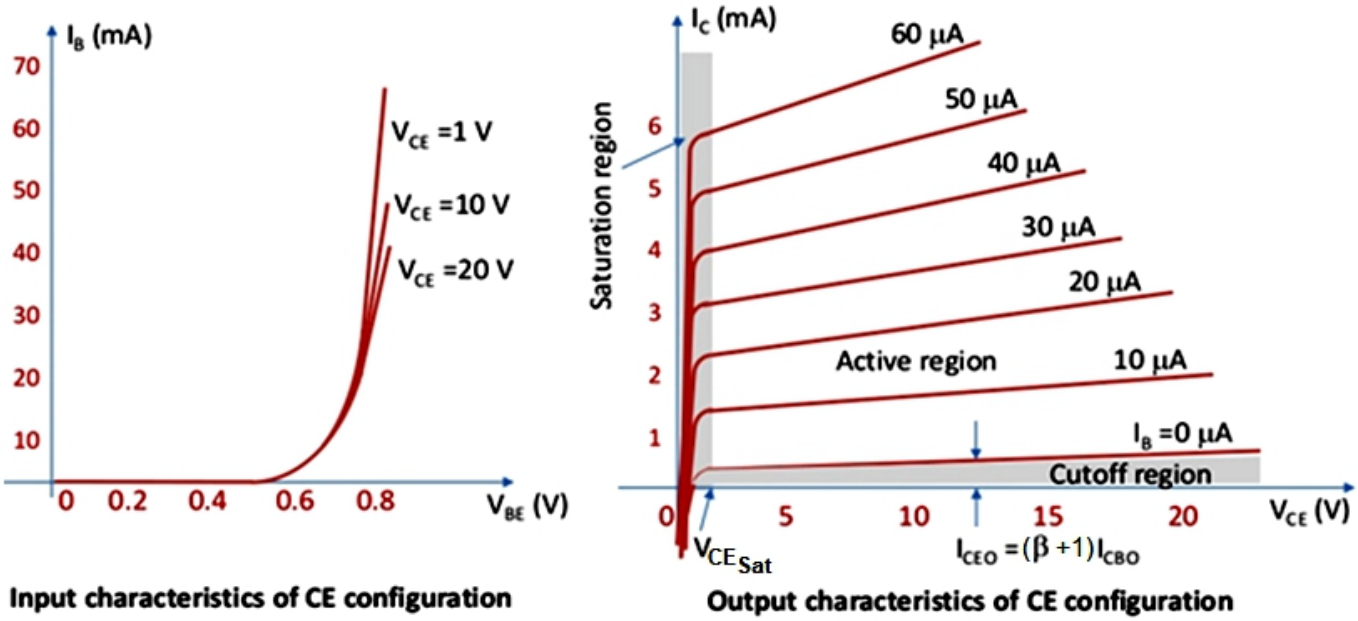


Fig.3.3.4: Common Emitter Characteristics

We identify three operating regions:

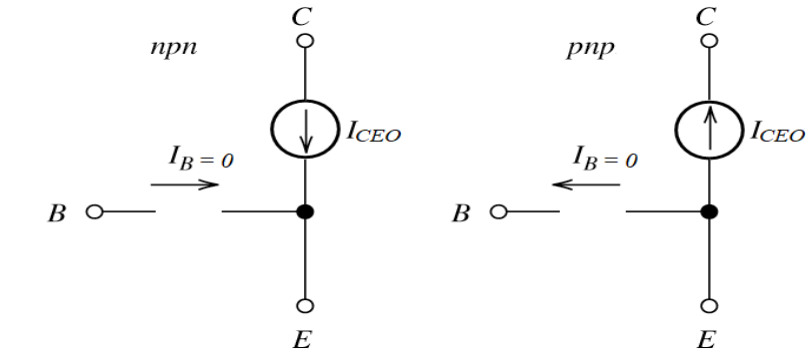
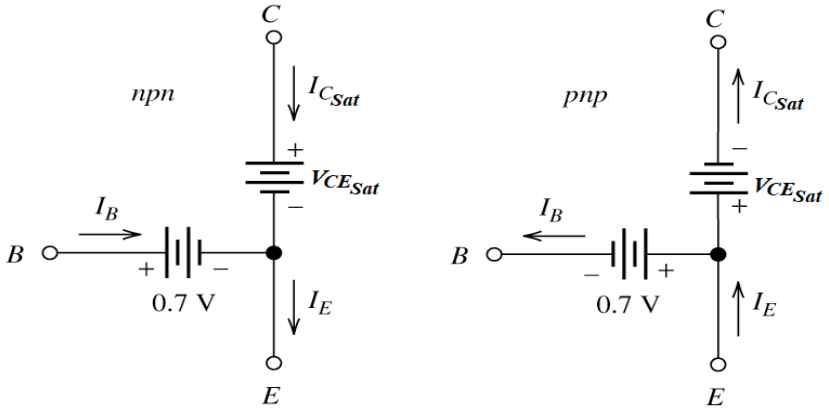
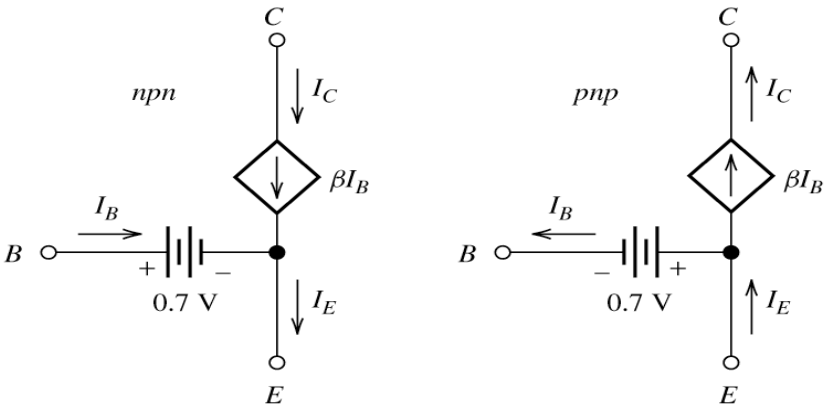
Operating region	Large signal equivalent circuit of the BJT
Cut-off region Both junctions are reverse biased; The base current ≈0, I_C≈0 ⇒ the transistor is OFF. V_{BE}<0.7V , I_C=I_{CEO}≈0	
Saturation region Both junctions are forward biased with: V_{BE}=0.7V and 0<V_{BC}<0.7V I_{Csat}<βI_B , V_{CE}= V_{CEsat} ***Note: For ideal analysis*** V_{CEsat} =0	
The active linear region Base-emitter junction is forward biased and Collector-base junction is reverse biased. V_{BE}=0.7V and V_{BC}<0V (or V_{CB}>0V) I_B>0 and I_C=βI_B V_{CE}=V_{CB}+V_{BE}⇒V_{CE}>0.7	

Table.3.1: The equivalent circuit of the BJT in the three Operating regions

- BJT can be used in switching mode or to amplify signals.

Switching mode ⇒ { **Cut-off region**, **Saturation region**

Amplification mode ⇒ {**The active linear region**

4.3. Common Collector configuration (CC)

In this configuration the input stage is the Collector-base stage, with: input current I_B, input voltage V_{BC}, and The output stage is the collector –Emitter stage, with: output current I_E, output voltage V_{EC}.

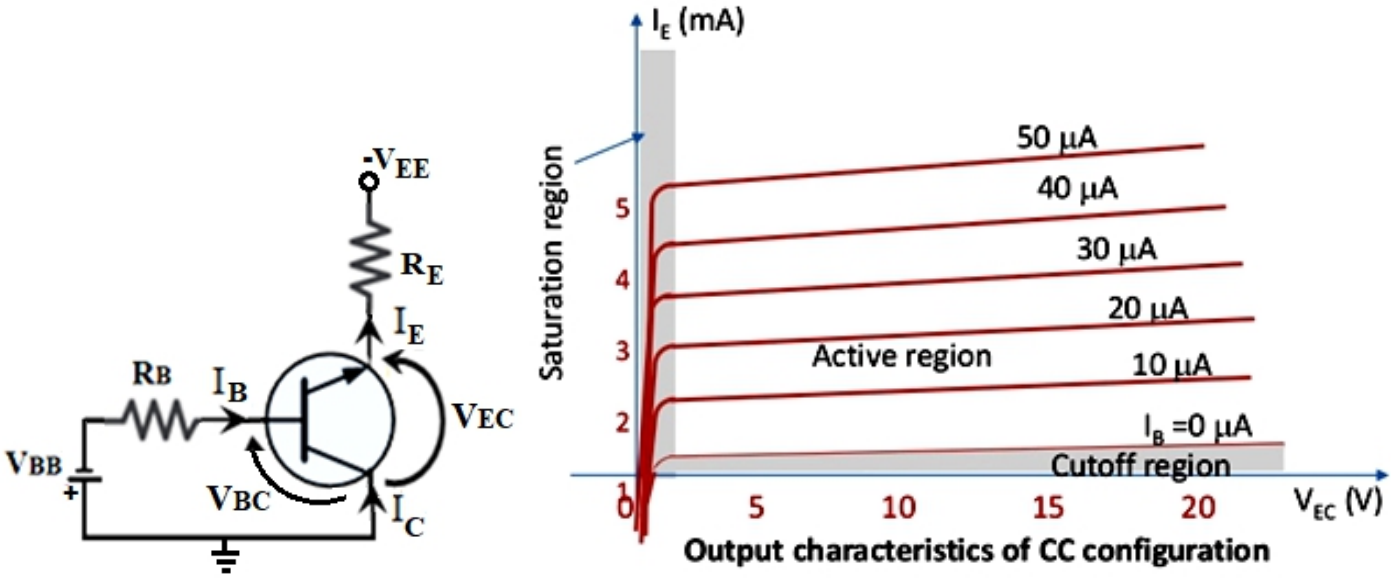


Fig.3.3.5: Common Collector Characteristics

Common collector configuration is Emitter-follower configuration used for impedance matching since it has high input impedance and low output impedance.

The output current $I_E = I_C + I_B \approx (\beta+1)I_B \Rightarrow$The current gain: $I_E/I_B \approx \beta+1$.

For $\beta >>$, $I_E/I_B \approx \beta$

5. Load line analysis

The load line is drawn on the collector curves between the cut-off and saturation points. Intersection between the DC load line and the (I_C, V_{CE}) curve gives the quiescent point (**Q(I_{CQ}, V_{CEQ})**) or the operating point.

This load line is determined by the collector circuit:

$Vcc - V_{CE} - RC\ I_C = 0$

The load line equation:

$$I_C = \frac{Vcc - V_{CE}}{RC}$$

If $I_C=0 \Rightarrow V_{CE}= Vcc$ (**Cut-off region**)
If $V_{CE}= 0 \Rightarrow I_C=Vcc/RC$ (**Saturation region**)

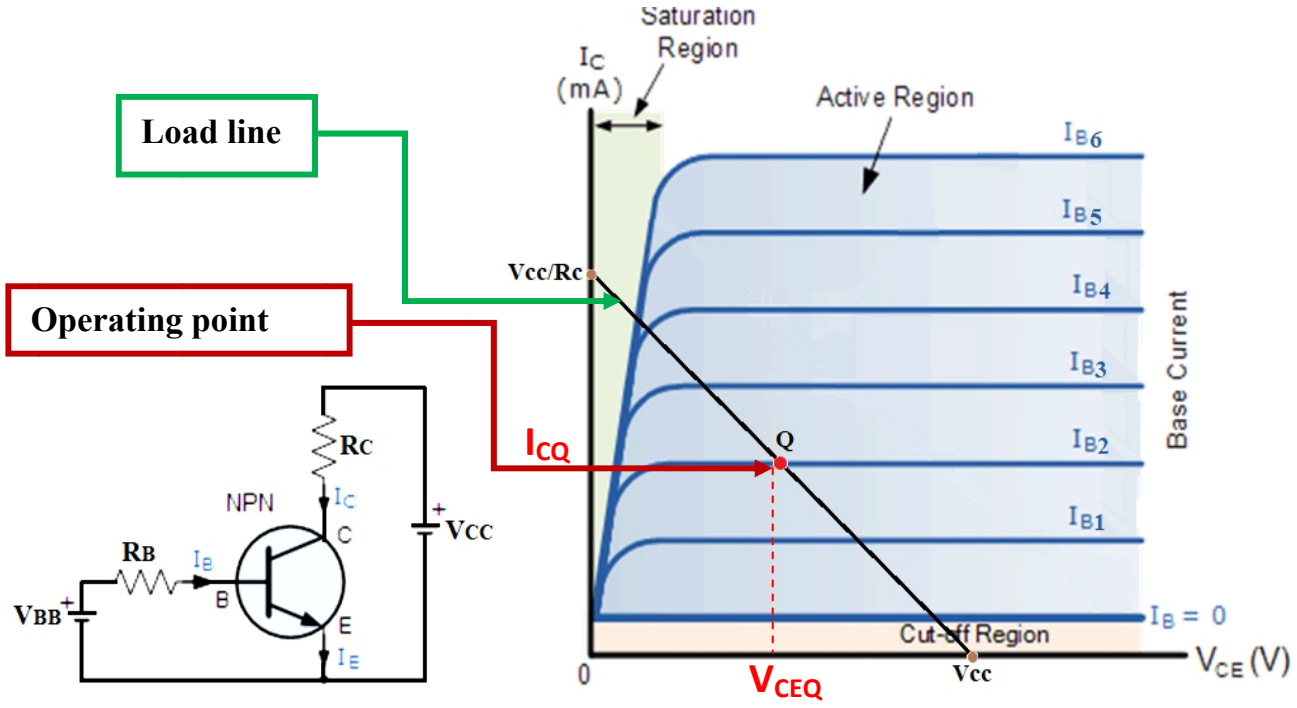
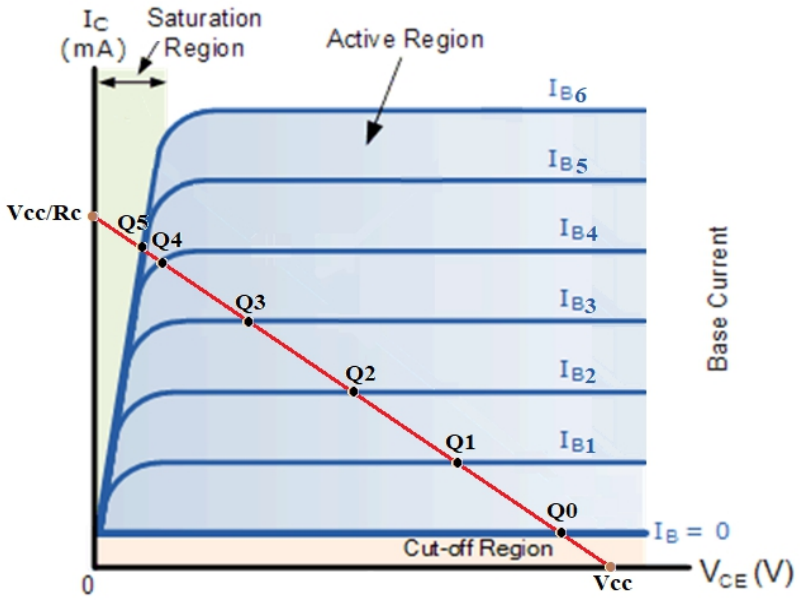


Fig.3.4: Load line analysis

In order to change the operating point from one position to another, we have three possibilities:

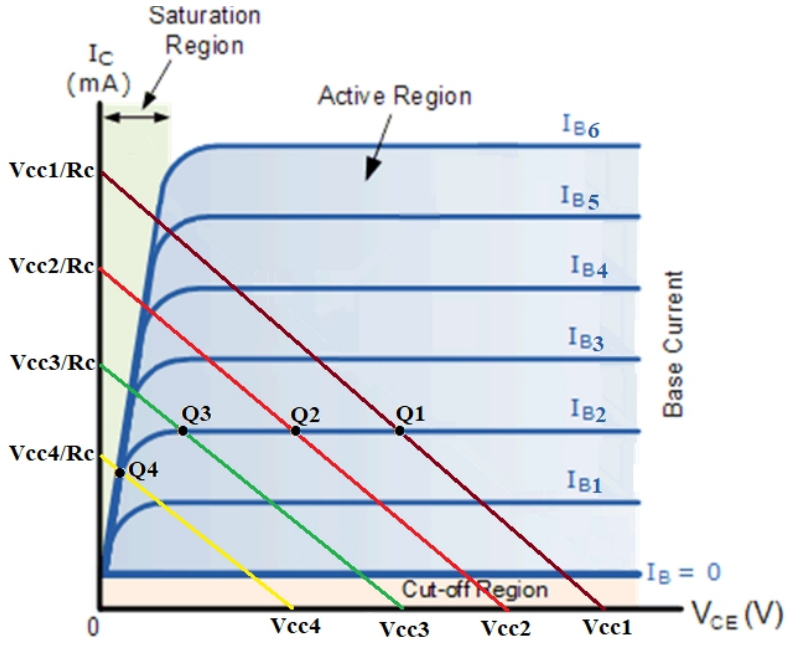
a. By changing the current I_B (changing the input stage)



$I_{B0}<I_{B1}< I_{B2}<I_{B3}<I_{B4}<I_{B5}$

$I_{BQ}\uparrow$, $V_{CEQ}\downarrow$, $I_{CQ}\uparrow$

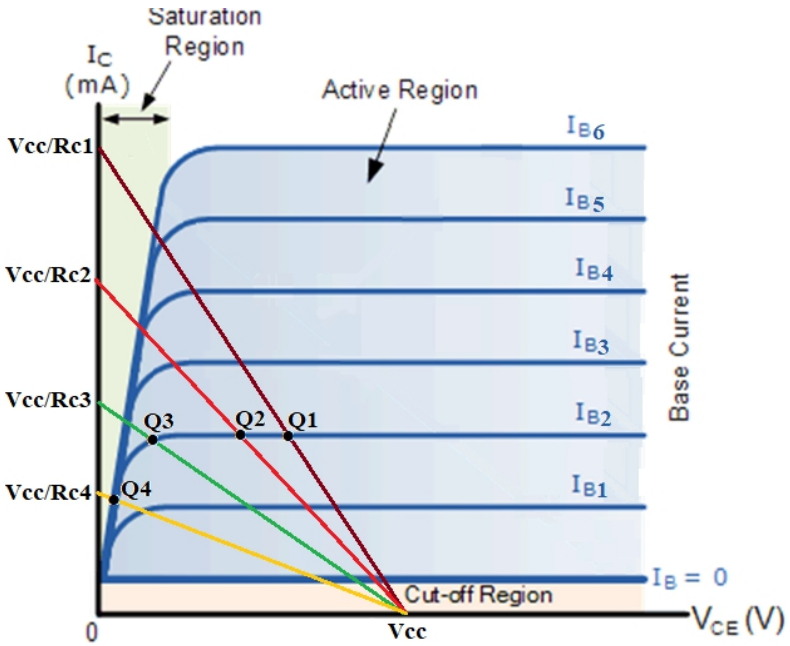
b. By changing the power supply Vcc (changing the output stage)



Vcc4<Vcc3< Vcc2<Vcc1

For $I_{BQ}\approx$ Const, Vcc$\uparrow$, $V_{CEQ}\uparrow$, $I_{CQ}\approx$ Const

c. By changing the resistor Rc (changing the output stage)



Rc1< Rc2< Rc3 < Rc4

For $I_{BQ} \approx$ Const, Rc↑, V_{CEQ}↓, $I_{CQ} \approx$ Const

6. Types of Biasing

The operation of steady-state, mainly dependents on collector current ($\mathbf{I_C}$), base current ($\mathbf{I_B}$) and collector to emitter voltage ($\mathbf{V_{CE}}$). If the transistor is supposed to operate properly as an amplifier, then these parameters must be chosen correctly which is known as biasing of transistor. The aim of the transistor biasing is to achieve a known quiescent operating point or Q-point for BJT to produce an undistorted output signal.

Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor.

For proper amplification purpose, BJT is biased through different techniques. Though there are many different techniques, but few most common techniques are discussed briefly.

6.1. Fixed Bias

Fixed Bias configuration is one of the most frequently used biasing circuits for a transistor circuits where a single power supply is used for both collector and base of the transistor using only two resistors.

Both V_{CC} and V_{BE} have a fixed value in the fixed bias type circuit. Meanwhile, R_B remains constant. As a result, I_B will also have a constant value, leading to a fixed operating point.

Applying KVL to the circuit of **Fig.3.5.a**:

$$\mathbf{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$$

Where V_{BE} = 0.7V for standard silicon transistors and using the current gain (β) relationship, Q (I_C, V_{CE}) can also be found out accordingly:

$I_C = \beta * I_B$.

$V_{CE} = V_{CC} - RC\ I_C$

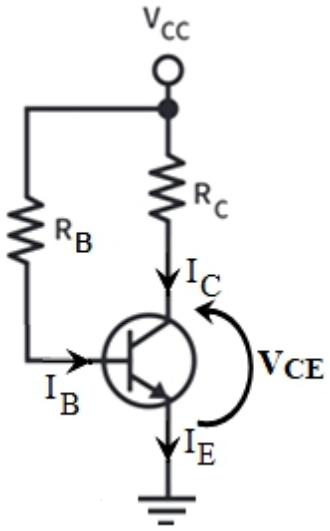


Fig.3.5.a: Fixed bias configuration

By merely changing the value of the resistor R_B, the base current can be adjusted to the desired value, as well as the operating point Q.

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

Problem of the fixed bias: it provides poor thermal stability.

6.2. *Fixed Bias with Emitter Resistance*

It is the modified form of fixed biased circuit to solve the problem of stability, where external resistance is connected to the emitter terminal (See **Fig.3.5.b**).

The equations of this circuit are given by:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$V_{CC} - V_{CE} - R_C I_C - R_E I_E = 0$

The problem with this configuration is that it reduces the gain of BJT amplifier. This problem can be overcome very easily by bypassing the emitter resistance (See **Fig.3.5.c**).

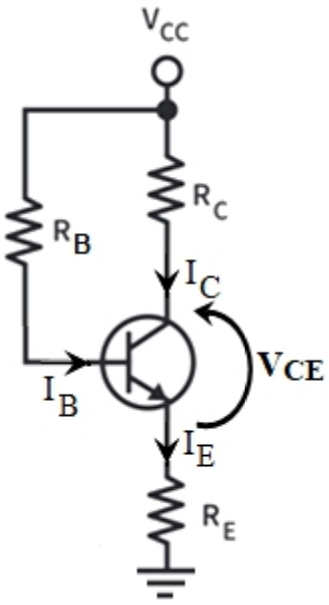


Fig.3.5.b: Fixed bias with Emitter Resistance

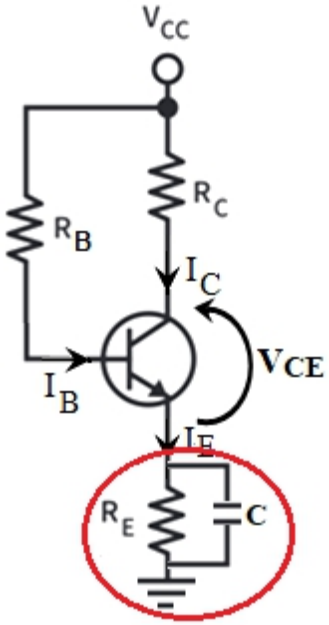


Fig.3.5.c: Bypassing the emitter resistance

6.3. Collector Feedback

This configuration is also called as collector to base bias circuit. This configuration is the improved version of the fixed bias configuration. The biasing resistor is connected between collector and base which provide feedback path. This configuration stabilizes the operating point.

The base current and the load line equations are:

$V_{CC}-V_{BE} - R_B I_B - (R_C + R_E) I_E = 0$

$$I_B = \frac{V_{CC}-V_{BE}}{R_B+(\beta+1)(R_C+R_E)}$$

$V_{CC} - V_{CE} - (R_C + R_E) I_E = 0$

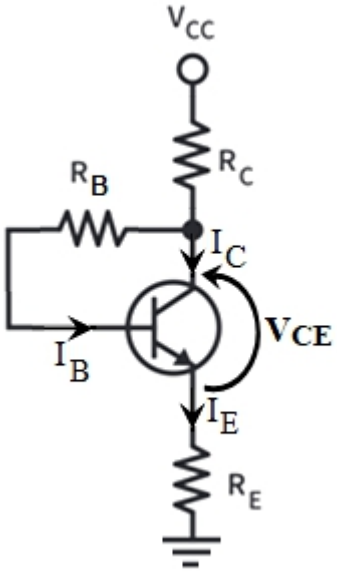


Fig.3.5.d: Collector Feedback

6.4. Voltage divider bias configuration

Voltage divider bias is the most popular and used method for biasing a transistor. Two external resistors R1 and R2 are used for this type. The voltage across R2 forward biases the emitter junction.

In this configuration, the equivalent **Thevenin** circuit is given by the **Fig.3.5.e** and the following equations: $R_B = R_1 \parallel R_2$ and $V_{BB} = V_{CC} * R_2/(R_1+R_2)$

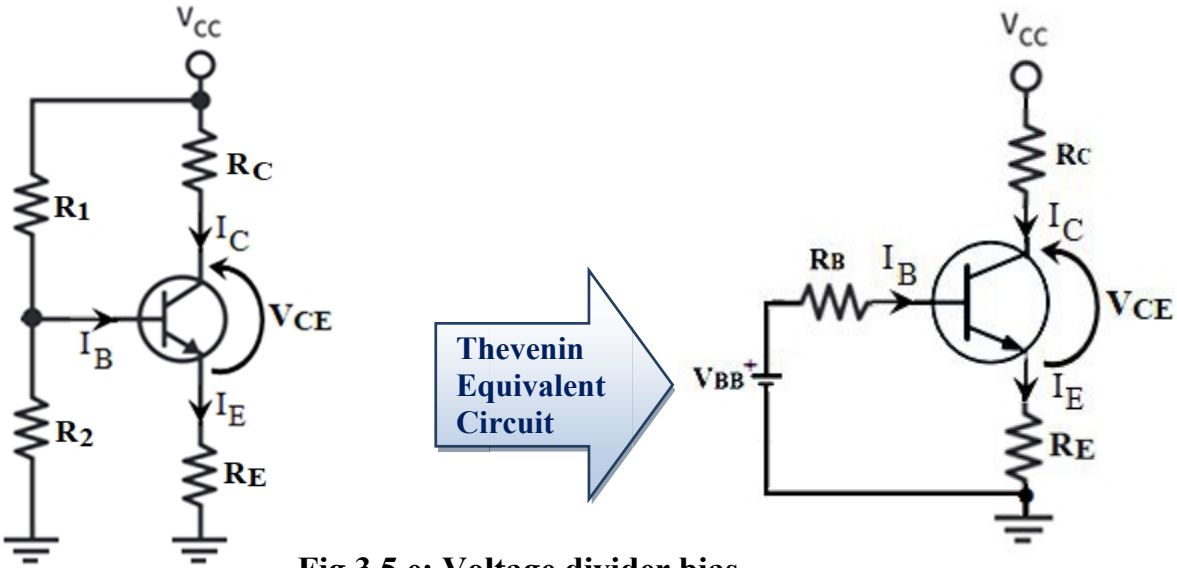


Fig.3.5.e: Voltage divider bias

Note: The voltage V_B can be approximated to VBB if the condition β*RE ≥ 10* R2 is satisfied.

6.5. Emitter follower /Common base configuration

This circuit is used in the case of common collector or **Common base** configuration.

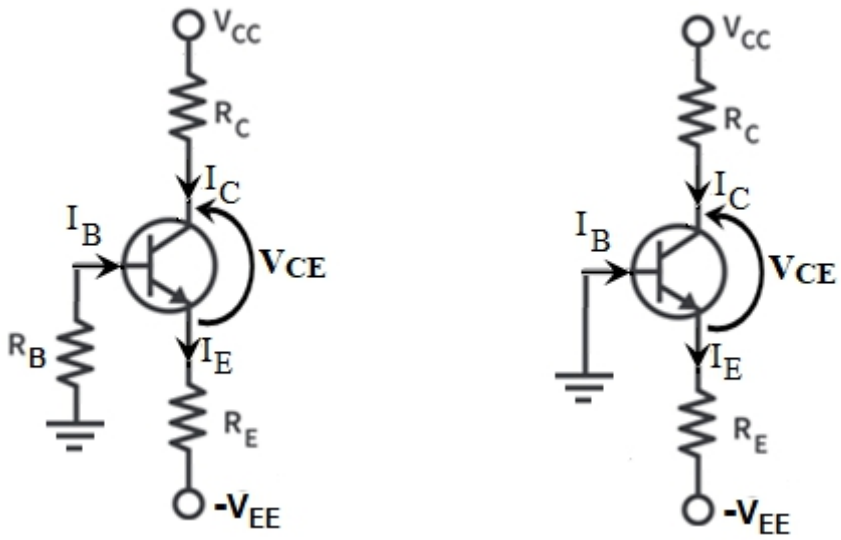


Fig.3.5.f: Emitter follower

The base current and the load line equations are:

$V_{EE} - V_{BE} - R_B I_B - R_E I_E = 0$

$$\mathbf{I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}}$$

$V_{CC} + V_{EE} - V_{CE} - R_C I_C - R_E I_E = 0$

7. Limits of operation

For each transistor there is a region of operation on the characteristics that will ensure that the maximum values (**$I_C$max; V_{CE}max, $P_C$max**) are not being exceeded. Those limits are given in the transistor specification sheet.

We have to be sure that the operating point **Q** falls into the following ranges.

$I_{CQ}<I_{C}max$

$V_{CEQ}<V_{CE}max$

$V_{CEQ} * I_{CQ}<P_{C}max$

Figure 3.6 gives the limit of operation described by the graphical method.

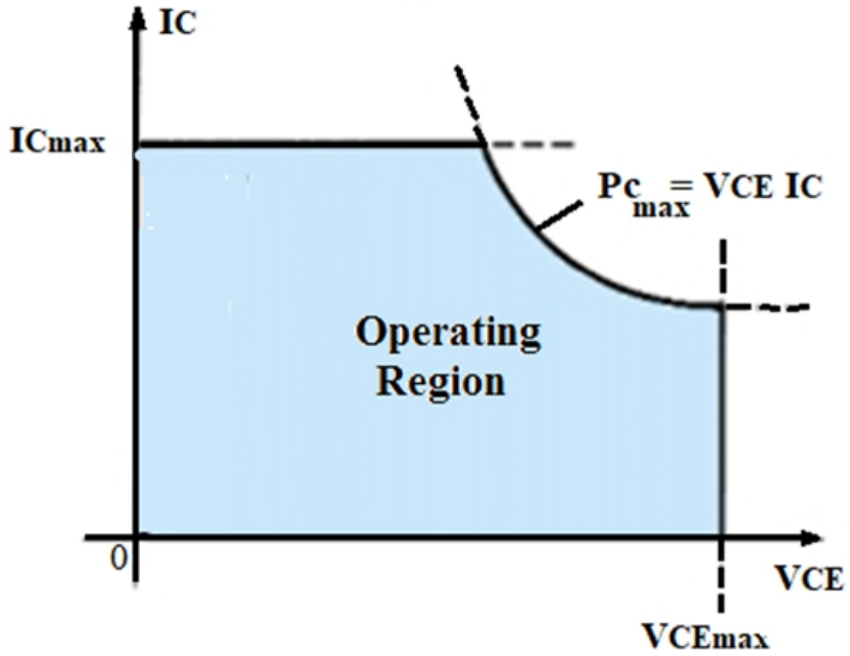


Fig.3.6: Limits of operation

Application:

The maximum ratings of a given BJT are:
$I_{C}max=30mA$; $V_{CE}max=15V$, $P_{C}max=200mW$.

1. What do you think about the operating point Q(**$I_{CQ}=25mA$; $V_{CEQ}=10V$**)?

$I_{CQ}<ICmax$

$V_{CEQ}<VCEmax$

$V_{CEQ} * I_{CQ}=250mW>P_{C}max \Rightarrow$ ***The operating point (Q) is not a safe operating point***.

2. Find the maximum value **V_{CEQmax}** allowed at the point **$I_{CQ}=25mA$.**

$V_{CEQmax} = P_{C}max / I_{CQ} = 200/ 25=8V$

V_{CEQ} Should be **<8V**

8. BJT: AC Large signal Analysis

The correct AC operation mode allows the output current to increase and decrease around the amplifiers Q-point without distortion as the input signal swings through a complete cycle. In other words, the output current flows for the full 360° of the input cycle.
Each voltage and current is assumed to be the superposition of a DC component (which is the operating point "Q").

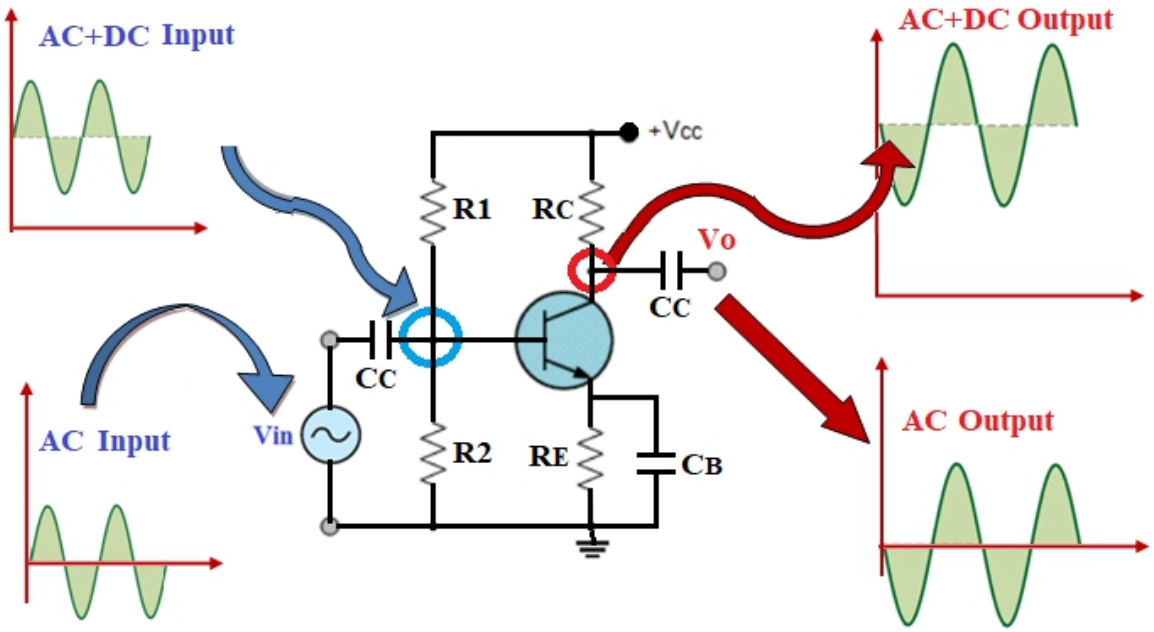


Fig.3.7: DC and AC signals in an amplifier based on BJT

Total signal	DC component	AC component
i_B =	I_{BQ} +	i_b
i_C =	I_{CQ} +	i_c
i_E =	I_{EQ} +	i_e
v_{BE} =	V_{BEQ} +	v_{be}
v_{CE} =	V_{CEQ} +	v_{ce}

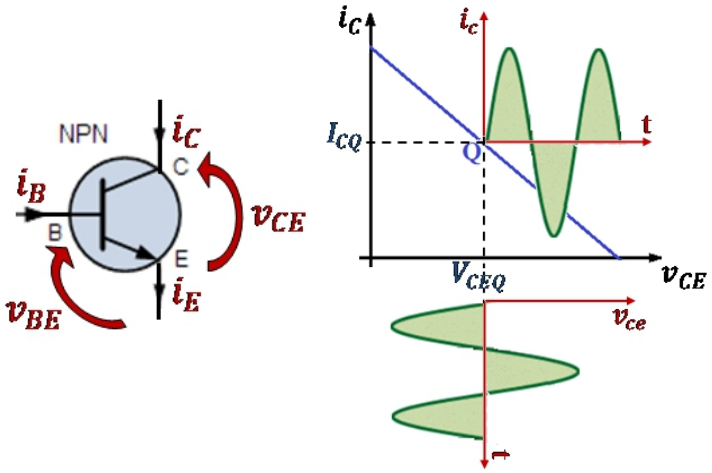


Table.3.2: Current and voltage signals in a BJT

8.1. Parameters of an amplifier circuit

a. Coupling Capacitor

Coupling capacitor (C_C in **Fig.1**) is connected in series to the signal path. In this way, it filters DC signals instead of AC signals (ie: it serves to block the DC currents, while permitting current at signal frequencies to pass).

b. Bypass Capacitor

Bypass capacitors are used to filter out noise and improve the overall performance of the circuit. One example circuit where a bypass capacitor is used is in a Common Emitter Transistor amplifier. Looking at its schematic, the common emitter amplifier has a bypass capacitor parallel to its emitter resistor. The emitter bypass capacitor, which is C_B in the **Fig.1**, provides an effective short to the AC signal around the emitter resistor, thus keeping the emitter at AC ground. With the bypass capacitor, the gain of the given amplifier will be at a maximum level.

c. Bias stability

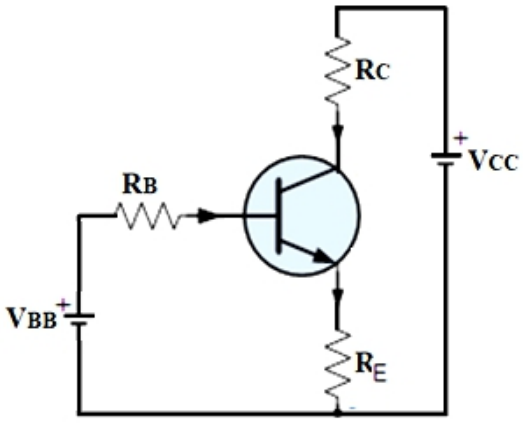
To minimize the effect of the changes of the β value on the Q point:
R_B should be $<<\beta R_E$

Or: $$R_B = \frac{\beta_{min} R_E}{10}$$

Example:

$80 \leq \beta \leq 120$, $V_{CC}=10V$, $I_{CQ}= 10mA$,
$V_{CEQ}=5V$, $R_C=400\Omega$.

Find the suitable values for R_E and R_B.



If $I_E \approx I_C$

$R_C+R_E= \frac{V_{CC}-V_{CEQ}}{I_{CQ}} = 500\Omega \Rightarrow R_E=100\Omega$

$$R_B = \frac{\beta_{min} R_E}{10}$$

$R_B=800\Omega$

Variation in "β" produces a negligible shift of the Q point.

8.2. AC Load line (Total signal load line)

If we consider the **pure AC signal**:

$$\boldsymbol{i_c = -\frac{1}{R_{AC}} v_{ce}} \quad \text{.....(1)}$$

Where : $\boldsymbol{R_{AC}}$ is the "AC" load or impedance given by the "AC" equivalent circuit.

Using the equations of table 1 and Eq.1:

$$\boldsymbol{i_C}\text{-}\ I_{CQ} = -\frac{1}{R_{AC}}\left(\boldsymbol{v_{CE}} - V_{CEQ}\right)$$

The final AC Load line **(of the total signal)** is given by:

$$\boldsymbol{i_C = -\frac{v_{CE}}{R_{AC}} + \frac{V_{CEQ}}{R_{AC}} + I_{CQ}} \quad \text{.....(2)}$$

Application 1

In an amplifier based on BJT of Fig.1.

Vcc=15V, R_C=1kΩ, R_E=500Ω, I_{BQ}= 40µA, β=100.

1. Write the DC and AC load lines and draw them.
2. Find the maximum voltage and current swing in the output (Vo(max) and i_c (max))
3. Find the maximum current swing in the base of the transistor.

The DC Load line (from the **DC circuit**)

$$I_C = \frac{1}{R_{DC}}(V_{DC} - V_{CE})$$

V_{DC} (is the DC power supply), in this example $V_{DC} = V_{CC.}$

The DC load: $R_{DC} = R_C + R_E$= 1.5kΩ

$$I_C = \frac{1}{1.5\text{k}\Omega}(15 - V_{CE})$$

The operating point Q:

$I_{CQ} = \beta I_{BQ}$= 4mA , $V_{CEQ} = V_{CC} - R_{DC} I_C$= 9V

The pure AC Load line (from the **AC circuit**)

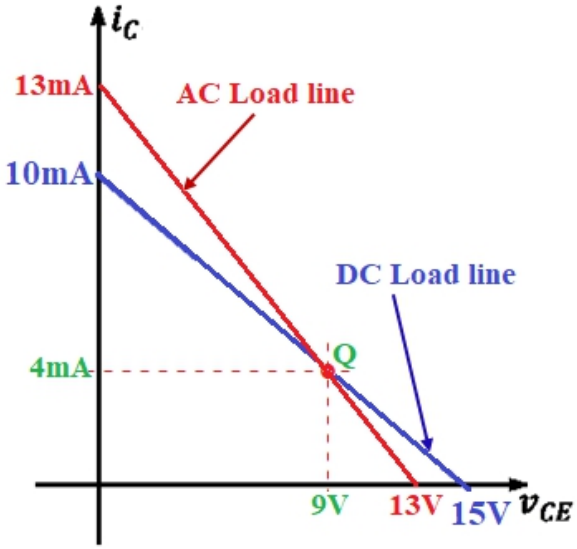
$$i_c = -\frac{1}{R_{AC}} v_{ce}$$

The AC load: $R_{AC} = R_C$= 1 kΩ

The final AC Load line **(of the total signal)** is given by:

$$i_C = -\frac{1}{R_{AC}}(v_{CE} - V_{CEQ}) + I_{CQ}$$

$$i_C = -\frac{1}{1k\Omega}(v_{CE} - 9) + 4 \quad (mA)$$



The maximum voltage swing in the output (Vo(max)):

Vo= v_{ce},

From the load line:

Vo(max) = v_{ce}(max) = min(9-0; 13-9)= 4V

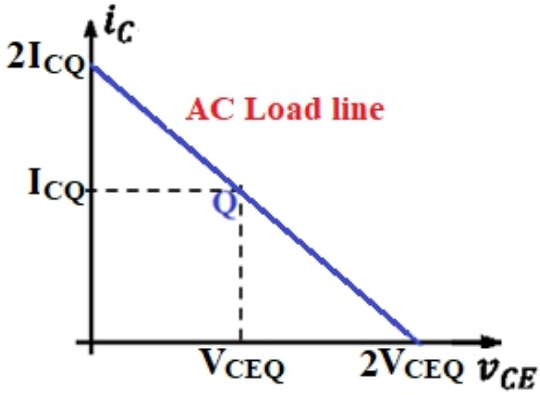
So: Vo= v_{ce} = 4 sin(ωt)

And : i_c(max) = min(4-0; 13-4)= 4mA ⇒ i_b(max)= 40µA.

8.3. Optimal operating point and Maximum symmetrical swing

To get a maximum symmetrical variation in collector current (a condition known as maximum symmetrical swing) the Q point should be placed in the middle of the AC load line (**the optimal position**) ⇒ Condition which will ensure linear operation over a maximum range of input signal.

In this case:



$$\begin{cases} \textbf{if } i_C = 0 \ ; \quad v_{CE} = 2V_{CEQ} \ldots\ldots\ldots\ldots\ldots\ldots (*) \\ \textbf{if } v_{CE} = 0 \ ; \quad i_C = 2I_{CQ} \ldots\ldots\ldots\ldots\ldots\ldots (**) \end{cases}$$

We replace (*) in Eq (2)

$$0 = -\frac{1}{R_{AC}}(2V_{CEQ} - V_{CEQ}) + I_{CQ} \Rightarrow$$

$$I_{CQ} = \frac{V_{CEQ}}{R_{AC}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

The DC Load line (from the **DC circuit**)

$$I_C = \frac{1}{R_{DC}}(V_{DC} - V_{CE})$$

Using the operating point Q:

$I_{CQ}R_{DC} = (V_{DC} - V_{CEQ})$ ……(4)

(3) in (4)

$V_{CEQ} = \frac{R_{AC}V_{DC}}{R_{DC}+R_{AC}}$ ……(5)

(5) in (3)

$I_{CQ} = \frac{V_{DC}}{R_{DC}+R_{AC}}$ ……(6)

Application 2

Using the circuit of application 1; find the new base current, I_{BQ}, in order to get an optimal operating point.

Sketch the new AC load line in this case.

R_{DC}= 1.5kΩ

R_{AC}= 1kΩ

V_{DC}= 15V

The optimal operating point:

$I_{CQ} = \frac{V_{DC}}{R_{DC}+R_{AC}} = \frac{15}{1.5+1}$ = 6mA

$I_{BQ} = I_{CQ}/B$= 60µA

$V_{CEQ} = \frac{R_{AC}V_{DC}}{R_{DC}+R_{AC}}$ = 6V

The equation of the new AC load line:

$$i_C = -\frac{1}{1k\Omega}(v_{CE} - 6) + 6 \quad (mA)$$