# Idaville HCC Platform Thermal Mechanical Overview

Intel Corporation
Data Center Platform Application Engineering
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# Revision History

| Revision | Date | Supplier |
|---|---|---|
| 1.0 | December 2020 | Initial release |
| 1.1 | March 2021 | Updated Ice Lake-D HCC SoC thermal specs.<br>Updated Ice Lake-D HCC non-uniform heating correction factors and die power guidance. |
| 1.2 | August 2021 | Updated Ice Lake-D Intel® PTU overview for system validations. |

# Idaville HCC Platform Thermal and Mechanical Overview (Ice Lake-D HCC SoC)

# Agenda

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- Ice Lake-D HCC SoC Package Mechanical Drawings
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- Ice Lake-D HCC SoC Reference Heatsink Design and Component Suppliers
- Ice Lake-D HCC SoC Loading Spec
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- Ice Lake-D HCC SoC $T_{CASE}$ Metrology
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- Lake-D HCC SoC $T_{CONTROL}$ and Fan Speed Control
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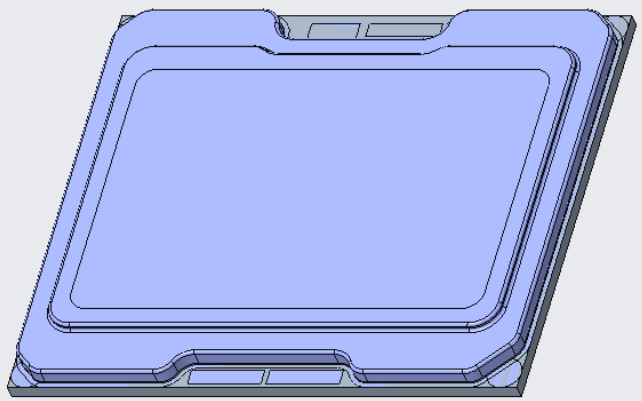
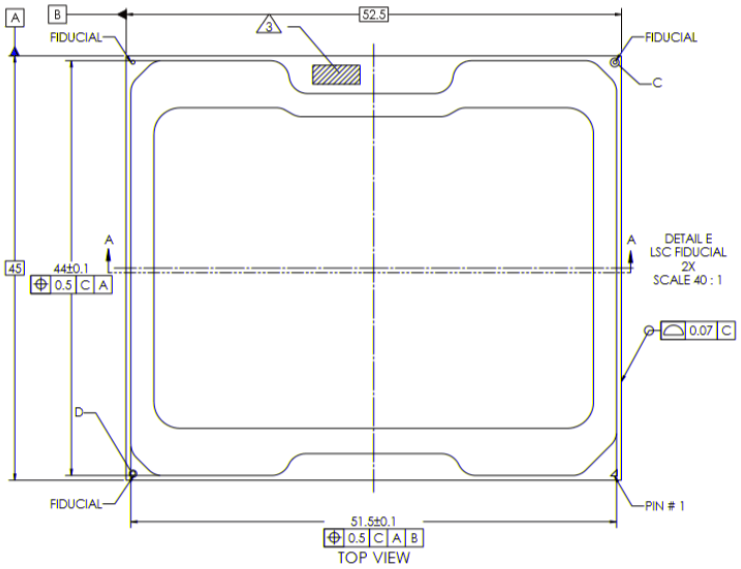
# Ice Lake-D HCC SoC Package Mechanical Model and Drawings

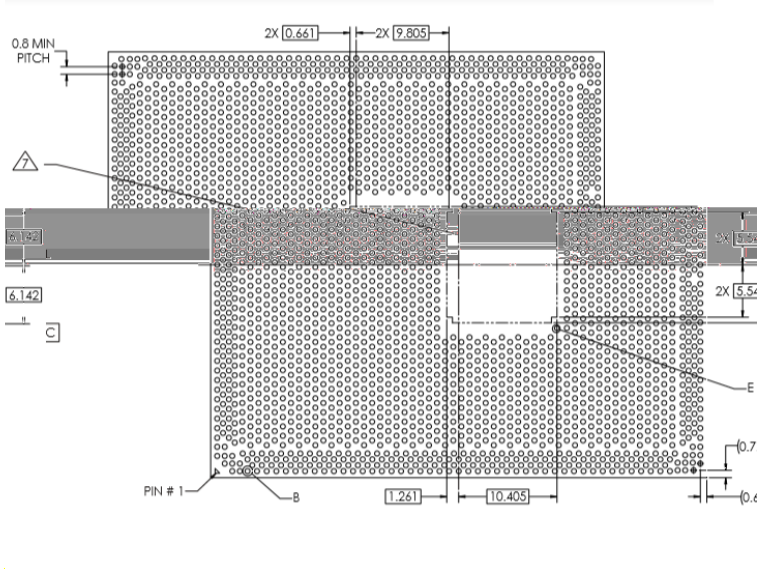
## (Document Numbers 627166 and 627168)

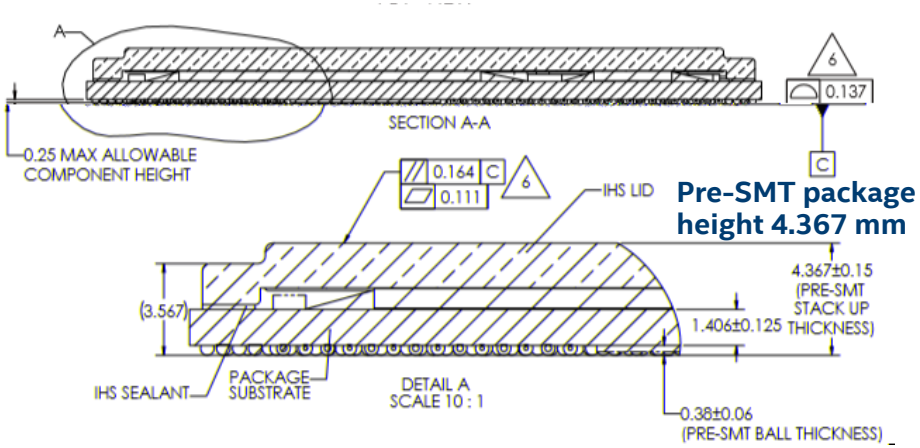
Drawing : J95556_R03

- The SoC is housed in a Flip-Chip Ball Grid Array (FC-BGA) package with Integrated Heat Spreader (IHS) that interfaces with the motherboard via 2579 solder balls when soldered down.





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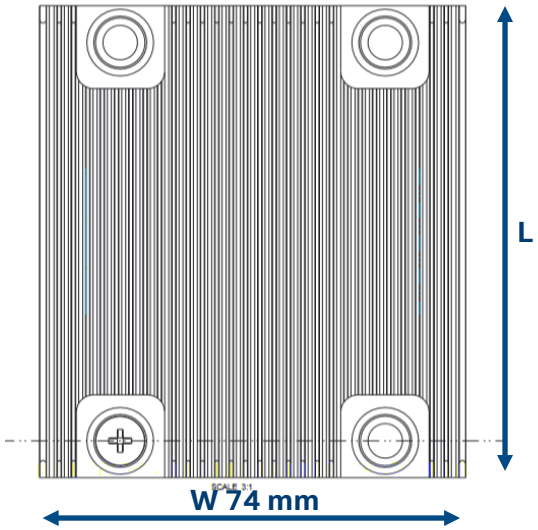
# Ice Lake-D HCC SoC Reference Heatsink and Backplate Mechanical Drawings

## (Document Numbers 630617 and 630619)

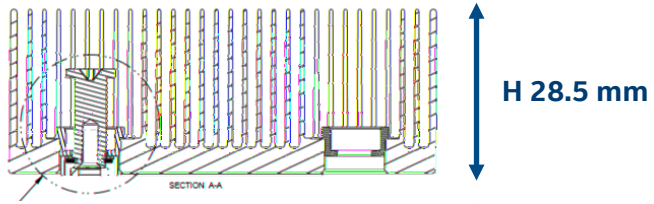
This new backplate design has different openings to allow space for board components.

This new backplate design for Ice Lake-D HCC is based on simulations and has not been validated. Customers must do their own validations before using the Ice Lake-D HCC SoC backplate assembly (K98682-001).

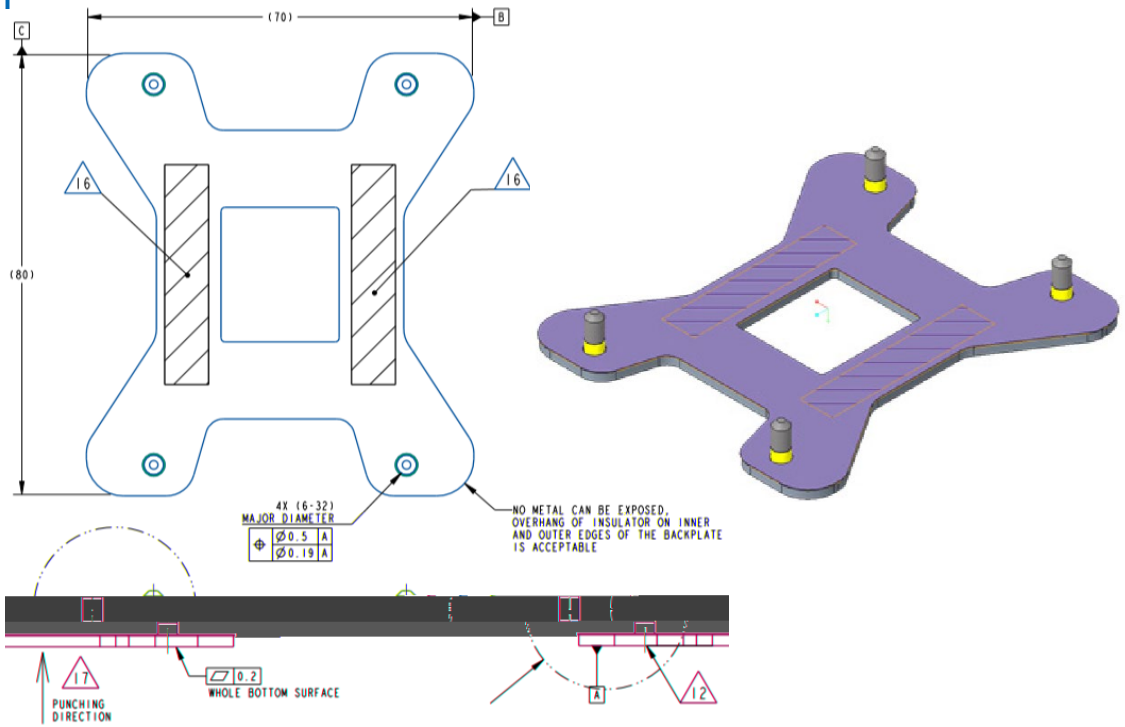



Drawing : J25479-001 and J25480-001

(Reuse of the Skylake-D ref. heatsink)




Drawing K98682-001




**Updated backplate tooling sample will be available in August. Intel will release the update drawing on RDC before end of July.**

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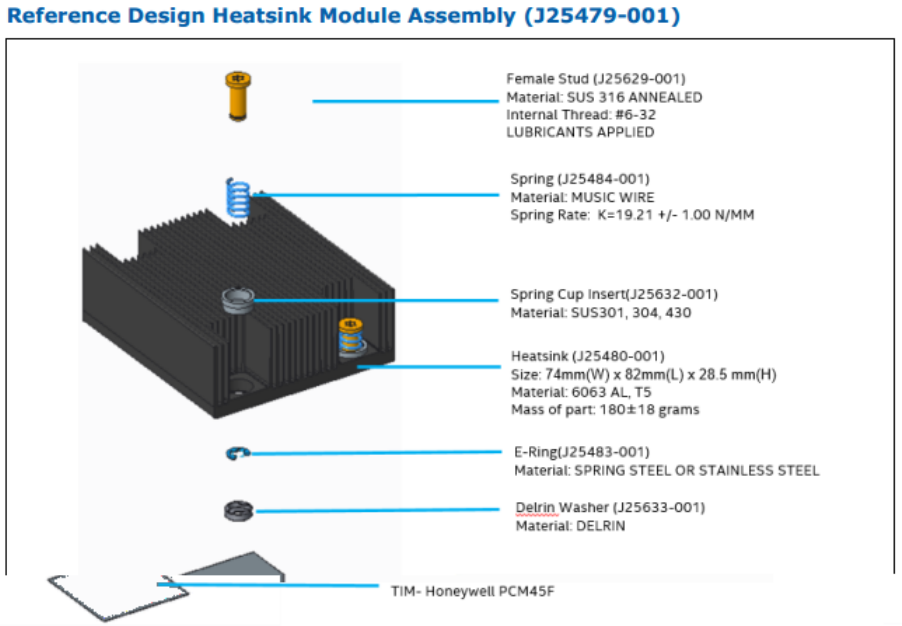
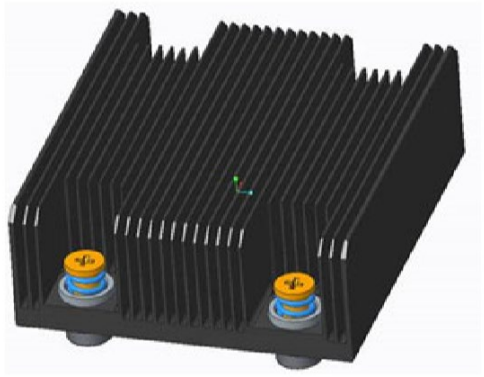
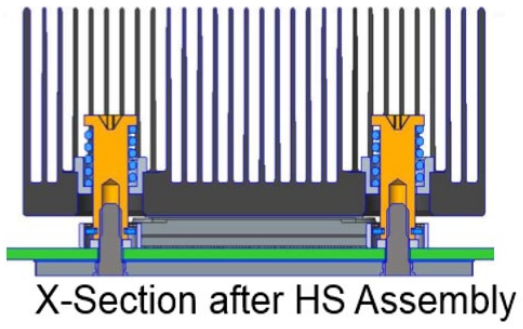
# Ice Lake-D HCC SoC Reference Heatsink Design
## (Document Number 627298)

1. The Ice Lake-D HCC reference heatsink is based on reuse of the Skylake-D reference heatsink assembly.




Delrin* washer





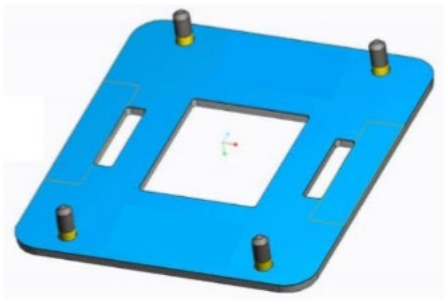

| Parameter | Value |
|---|---|
| Volumetric | 74 (W) x 82 (L) x 28.5 (H) mm |
| Base thickness | 4.5 mm |
| Fin description | 30 fins, 24 mm height<br>0.7 mm thickness<br>Pitch 2.49 mm |
| Heatsink mass | 198 g (180 +/- 18 g) |
| Type / Material | Extruded Aluminum |
| Backplate | Used to provide higher TIM force |
| Load design target (Time 0) | 47 lbf ~ 100 lbf |
| Thermal Interface Material | Honeywell* PCM45F |

# Ice Lake-D LCC/HCC SoC Backplate Design and Component Suppliers

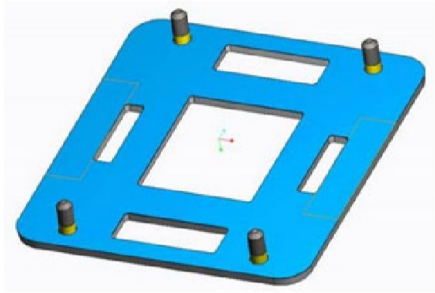
## (Document Numbers 568201, 616372, and 627298)

1. The new backplate design for Ice Lake-D LCC has additional openings to allow more space for board components.
2. The new backplate design for Ice Lake-D HCC has different openings to allow space for board components.
3. These new backplate designs for Ice Lake-D LCC and HCC are based on simulations and has not been validated. Customers must do their own validations before using Ice Lake-D LCC and HCC backplate assembly.

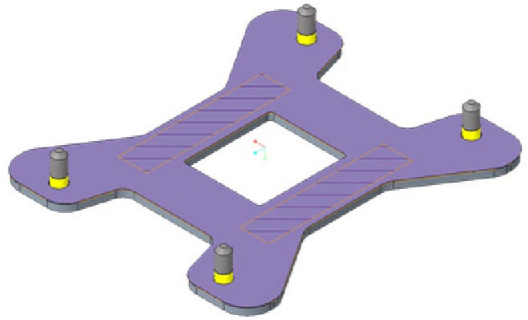
Skylake-D backplate assembly (J25634-001)



Ice Lake-D LCC backplate assembly (J94624-001)



Ice Lake-D HCC backplate assembly (K98682-001)



| Component | Intel P/N | Supplier | Supplier P/N |
|---|---|---|---|
| Skylake-D, Ice Lake-D LCC/HCC reference 1U heatsink assembly | J25479-001 | CCI | 0A16273101 |
| Skylake-D reference backplate assembly | J25634-001 | CCI | 0A16274101 |
| Ice Lake-D LCC reference backplate assembly | J94624-001 | CCI | 0A20115101 |
| Ice Lake-D HCC reference backplate assembly | K98682-001 | CCI | 0A20116101 |

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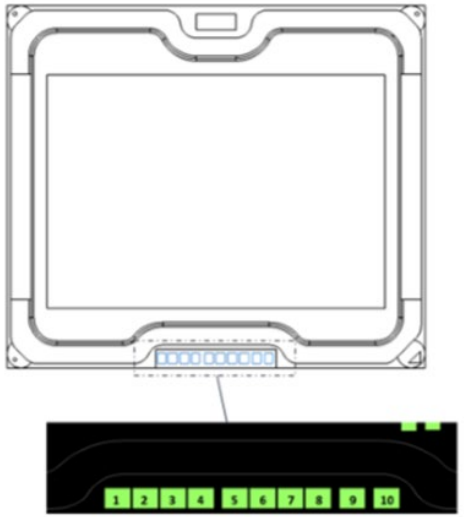
# Goat Rock TTV Thermal Operation and Power Settings
(Document Numbers 569587)

## Goat Rock TTV Thermal Specifications

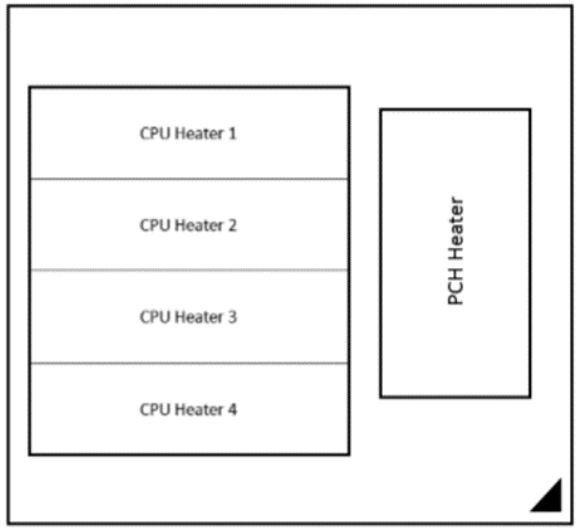
| Parameter | Specification |
|---|---|
| Nominal heater resistance (+/- 50%) CPU 1-4 Heater | 36.7 ohms at 25 ºC |
| Nominal heater resistance (+/- 50%) PCH Heater | 33.3 ohms at 25 ºC |
| Max. TTV case temperatures | Tc-max = 110 ºC |
| Max. heater power CPU | 120W |
| Max. heater power PCH | 30W |

## Top Side Pad Connection



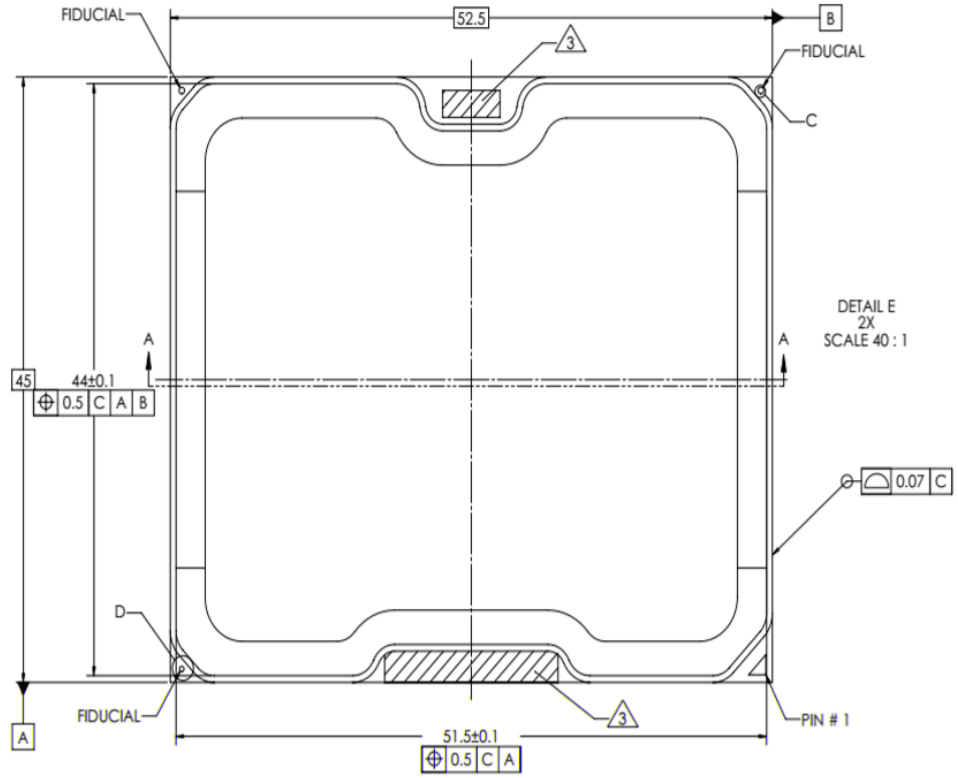

| Pin# | Net Name |
|---|---|
| 1 | CPU Heater 1_FH |
| 2 | CPU Heater 2_FH |
| 3 | CPU Heater 3_FH |
| 4 | CPU Heater 4_FH |
| 5 | CPU Heater 1_FL |
| 6 | CPU Heater 2_FL |
| 7 | CPU Heater 3_FL |
| 8 | CPU Heater 4_FL |
| 9 | PCH Heater_FH |
| 10 | PCH Heater_FL |

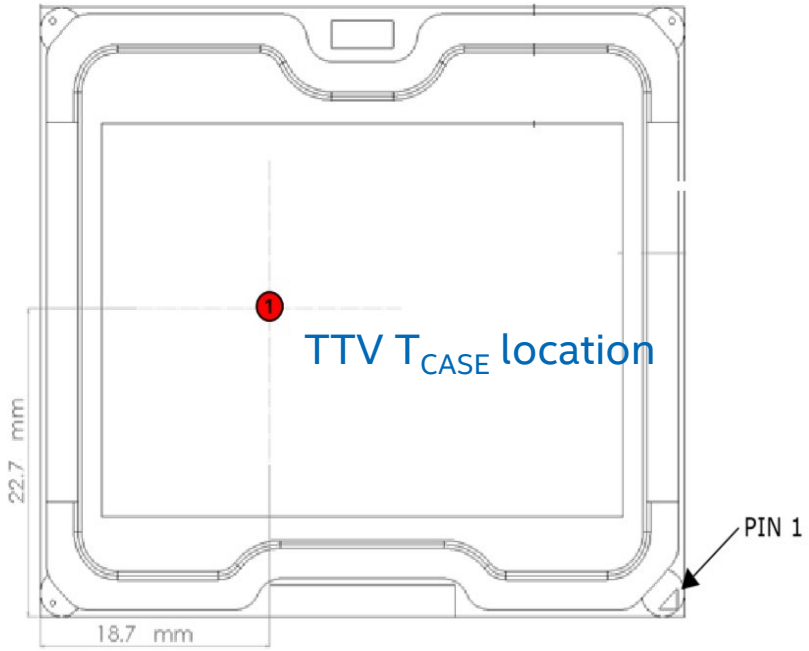
## Die Heater Representative



# Goat Rock TTV $T_{CASE}$ Location
## (Document Numbers 627298)

- The TTV $T_{CASE}$ is measured at specified location on the topside of the SoC IHS, centered over the CPU die.



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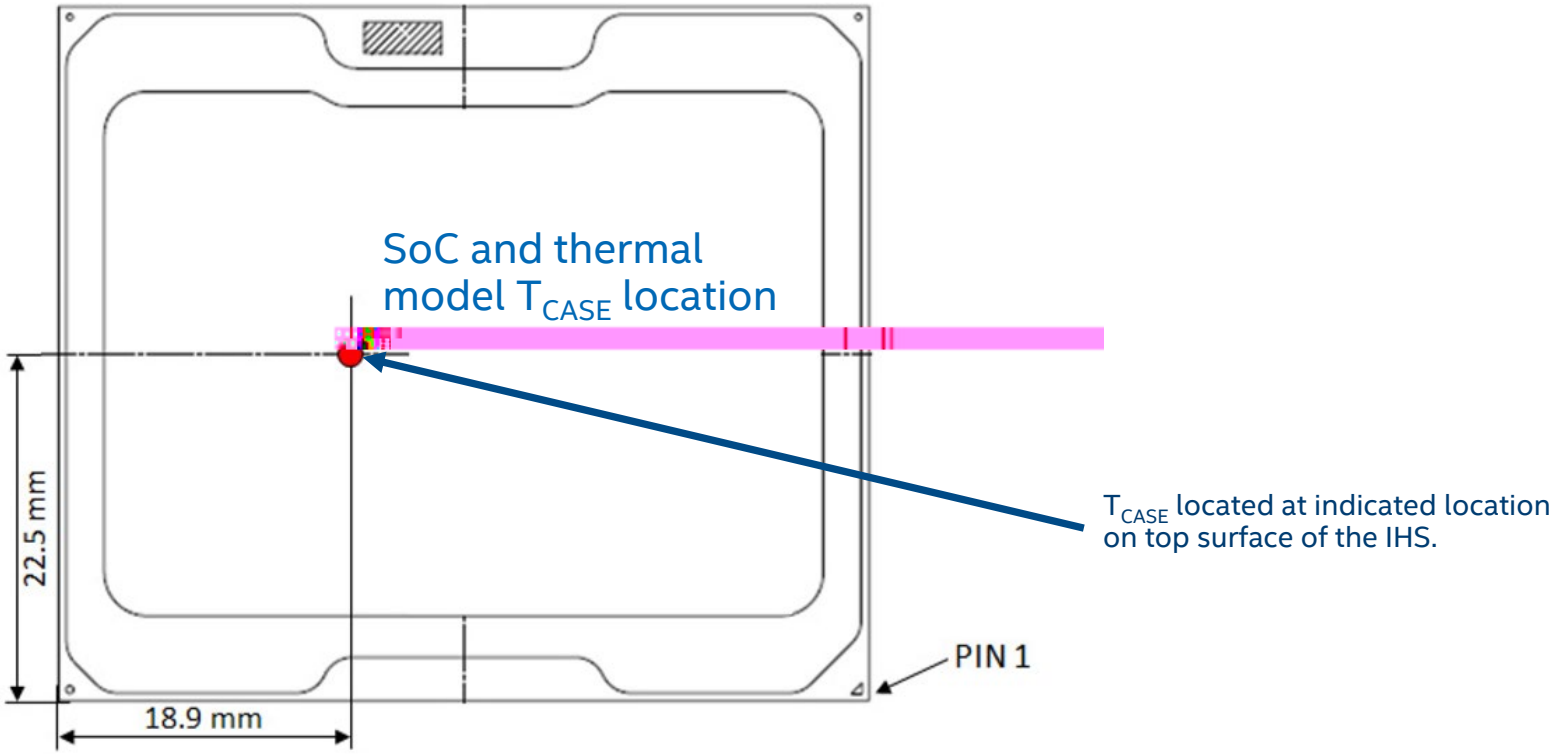
# Ice Lake-D HCC $T_{CASE}$ Metrology
## (Document Numbers 627298)

- The minimum and maximum case temperatures are measured at a specified location on the topside of the SoC IHS. The location is centered over the CPU die, not in the center of the SoC IHS.
- This location applies to Ice Lake-D HCC SoC product and thermal model.



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# Ice Lake-D HCC SoC Thermal Specs

## (Document Numbers 627298)

| SKU / Sample type | Core Count | Package TDP (W) | eTemp | $T_{CASE\_MAX}$ | DTSmax | $T_{CONTROL}$ | $T_{CASE\_MIN}$ |
|---|---|---|---|---|---|---|---|
| Preliminary | 20 | 119 | No | 77 | TBD | TBD | 0 |
| | 20 | 116 | No | 77 | TBD | TBD | 0 |
| | 20 | 112 | eTemp | 78 | TBD | TBD | -40 |
| | 18 | 114 | eTemp | 77 | TBD | TBD | -40 |
| | 18 | 92 | No | 80 | TBD | TBD | 0 |
| | 16 | 111 | No | 77 | TBD | TBD | 0 |
| | 16 | 110 | No | 77 | TBD | TBD | 0 |
| | 16 | 97 | eTemp | 79 | TBD | TBD | -40 |
| | 14 | 95 | No | 77 | TBD | TBD | 0 |
| | 12 | 92 | eTemp | 77 | TBD | TBD | -40 |
| | 12 | 91 | No | 78 | TBD | TBD | 0 |
| | 12 | 72 | eTemp | 82 | TBD | TBD | -40 |
| | 8 | 86 | No | 72 | TBD | TBD | 0 |
| | 8 | 83 | No | 73 | TBD | TBD | 0 |
| | 8 | 75 | No | 75 | TBD | TBD | 0 |
| | 4 | 64 | No | 78 | TBD | TBD | 0 |

Refer to the preliminary SKUs specs for simulation and TTV validation for thermal solution development.

# Ice Lake-D HCC Non-Uniform Heating Correction Factors

## (Document Numbers 627298)

| SKU / Sample type | Core Count | Package TDP (W) | eTemp | Ice Lake-D LCC Thermal Model | | Goat Rock TTV | |
|---|---|---|---|---|---|---|---|
| | | | | $CF_1$ (C/W) | $CF_2$ (C/W) | $CF_1$ (C/W) | $CF_2$ (C/W) |
| Preliminary | 20 | 119 | No | 0.017 | -0.002 | 0.030 | -0.005 |
| | 20 | 116 | No | 0.017 | -0.002 | 0.030 | -0.005 |
| | 20 | 112 | eTemp | 0.017 | -0.002 | 0.030 | -0.005 |
| | 18 | 114 | eTemp | 0.020 | -0.002 | 0.033 | -0.005 |
| | 18 | 92 | No | 0.019 | -0.002 | 0.032 | -0.005 |
| | 16 | 111 | No | 0.021 | -0.002 | 0.034 | -0.005 |
| | 16 | 110 | No | 0.021 | -0.002 | 0.034 | -0.005 |
| | 16 | 97 | eTemp | 0.021 | -0.002 | 0.034 | -0.005 |
| | 14 | 95 | No | 0.025 | -0.002 | 0.038 | -0.005 |
| | 12 | 92 | eTemp | 0.030 | -0.002 | 0.043 | -0.005 |
| | 12 | 91 | No | 0.030 | -0.002 | 0.043 | -0.005 |
| | 12 | 72 | eTemp | 0.026 | -0.002 | 0.039 | -0.005 |
| | 8 | 86 | No | 0.023 | -0.002 | 0.036 | -0.005 |
| | 8 | 83 | No | 0.020 | -0.002 | 0.033 | -0.005 |
| | 8 | 75 | No | 0.017 | -0.002 | 0.030 | -0.005 |
| | 4 | 64 | No | 0.017 | -0.002 | 0.030 | -0.005 |

**Die Power Guidance** for thermal modeling and TTV thermal testing.

Package TDP = CPU power + PCH power ; CPU power = Package TDP – 1 W ; PCH power =1 W

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# Ice Lake-D HCC Reference Documents

| Title | Doc. Number |
|---|---|
| *Ice Lake-D HCC SoC Package Mechanical Drawing* | 627166 |
| *Ice Lake-D HCC SoC Package Mechanical Model in STEP Format* | 627168 |
| *Ice Lake-D HCC SoC Reference Heatsink and Backplate Mechanical Drawings* | 630617 |
| *Ice Lake-D HCC SoC Reference Heatsink and Backplate Mechanical Models in STEP Format* | 630619 |
| *Ice Lake-D HCC SoC Thermal Model User Guide and Models* | 632170 |
| *Intel Xeon Processor D-2100 Product Family Thermal Test Vehicle [TTV] User Guide* | 569587 |
| *Installing a Thermocouple into an Integrated Heat Spreader for $T_{CASE}$ Measurement - Best Known Method (BKM)* | 612146 |
| *Ice Lake-D HCC SoC Thermal and Mechanical Specification and Design Guide (TMSDG)* | 627298 |
| *Idaville HCC With Ice Lake-D HCC SoC Platform Design Guide [PDG]* | 622027 |
| *Ice Lake-D SoC Intel Power Thermal Utility for Linux* | 634082 |
| *Ice Lake-D SoC Intel Power Thermal Utility for Windows* | 637933 |

# Ice Lake-D SoC Intel® Power Thermal Utility (Intel® PTU)

# Agenda

- Intel® Power Thermal Utility (Intel® PTU) Workloads
- Near-TDP Workload
  1. Purpose of The Near-TDP Workload
  2. Challenges of Reaching Near TDP with Intel® PTU
  3. PTU nTDP
- Intel® PTU Executables
- Intel® PTU for Linux*
  1. Software Installation
  2. Intel® PTU Monitor Data
  3. Command for Monitor and Data Log
  4. Command for Workload Generator
- FAQ

# Intel® Power Thermal Utility (Intel® PTU) Workloads

| Intel® PTU Workload | Instruction Sets | Voltage | Purpose |
|---|---|---|---|
| TDP Test | SSE AVX1 Pwr Virus | Nominal | TDP Thermal Test |
| Near-TDP Test | SSE AVX1 Pwr Virus | Over-Voltage ( pre-production ) | TDP Thermal Test with Increasing Core and Ring Voltage |
| Core IA/SSE Test | SSE AVX1 Pwr Virus | Nominal | Core AVX1 Test |
| Core AVX2 Test | AVX2 Pwr Virus | Nominal | Core AVX2 Test |
| Core AVX512 Test | AVX512 Pwr Virus | Nominal | Core AVX512 Test |
| Pmax Test | AVX512 Pwr Virus | Nominal | The Max Instantaneous Electrical Power Test |
| Turbo Test | AVX1/AVX2/AVX512 | Nominal | Core Turbo Frequency Test |

## All Intel® PTU Workloads' Power map NEVER EQUALS real world workload power map (current version does not model Uncore activity)

**Note:** Intel® Advanced Vector Extensions (Intel® AVX)
Intel® Advanced Vector Extensions 2 (Intel® AVX2)
Intel® Advanced Vector Extensions 512 (Intel® AVX-512)

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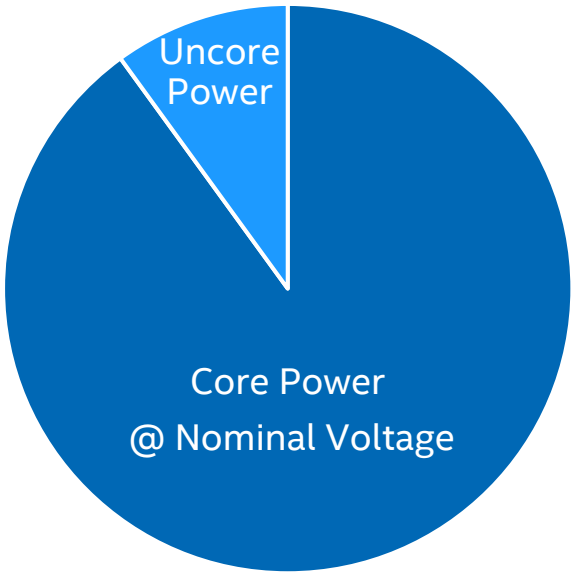
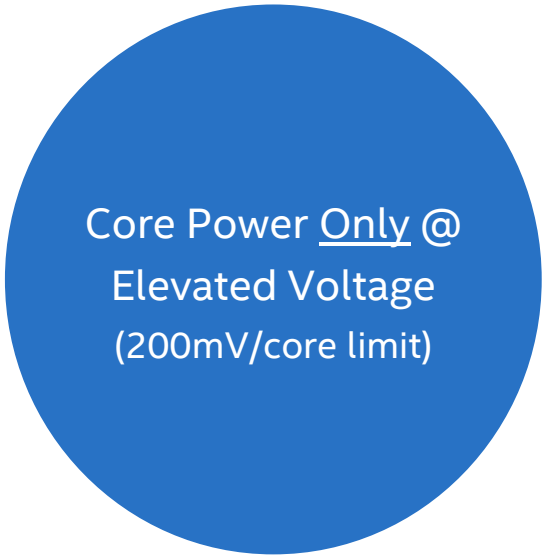
# Purpose of The Near-TDP Workload




**Real World TDP Workload**




**Goal of Intel® PTU's near-TDP Workload**

- Goal: To match total power dissipation for thermal validation.

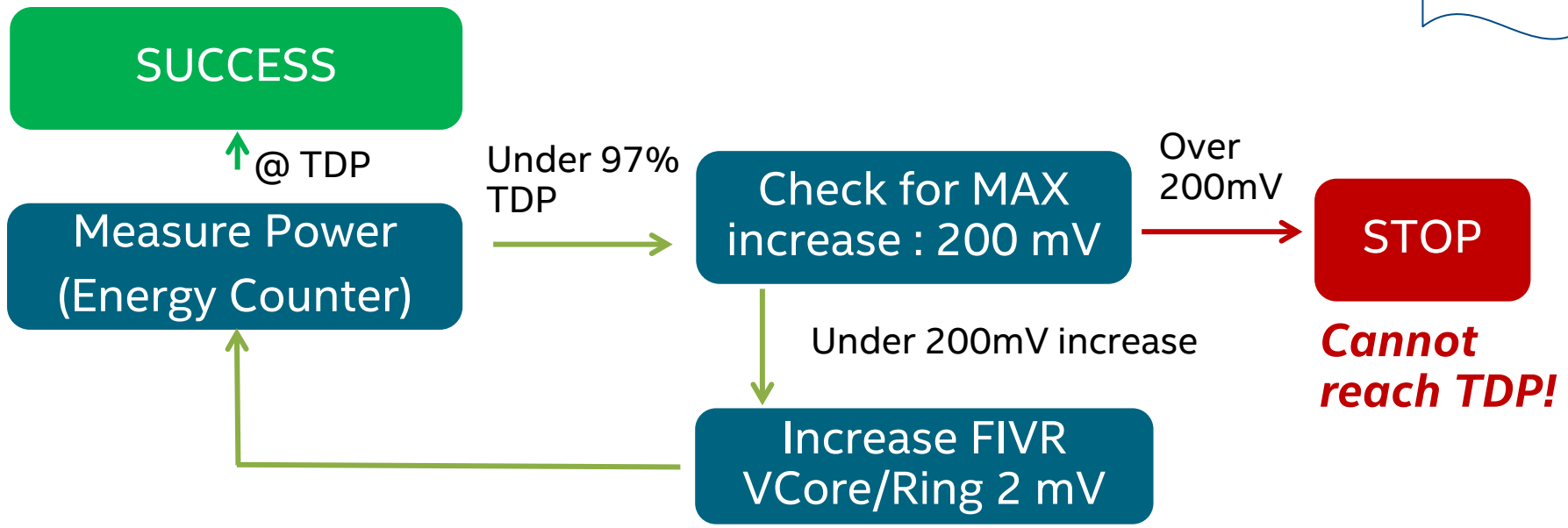
**Note:** Intel® Power Thermal Utility (Intel® PTU)

# Intel® Power Thermal Utility (Intel® PTU) nTDP (Near-TDP Workload)

- Intel® PTU nTDP is available on non-production parts only
- How does Intel® PTU nTDP work?
  - Increase Core and Ring voltage until the part reaches TDP
  - One shot only (TDP Test); no dynamic tuning

Most ES2 parts need between 100mV-200mV to get to TDP at P1

nTDP feature may reduce thermal margin by few C



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- Intel® Power Thermal Utility (Intel® PTU) Workloads
- Near-TDP Workload
  1. Purpose of The Near-TDP Workload
  2. Challenges of Reaching Near TDP with Intel® PTU
  3. PTU nTDP
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- Intel® PTU for Linux*
  1. Software Installation
  2. Intel® PTU Monitor Data
  3. Command for Monitor and Data Log
  4. Command for Workload Generator
- FAQ

# Intel® Power Thermal Utility (Intel® PTU) Executables

- Ice Lake-D SoC Intel® PTU for Linux* (Doc# 634082)

  (1) Command line interface.

  (2) 1 binary for workload generator, monitor and data log functions.

  (3) ./ptu –ct 1/2/3/4/5/6/7 is the workload generator.

  (4) –mon option will display the thermal, power and frequency data.

  → Needs two terminals to execute the workload generator and the monitor function.

- Ice Lake-D SoC Intel® PTU for Windows* (Doc# 637933)

  (1) GUI interface.

  (2) Full capabilities with workload generator, monitor and data log functions.

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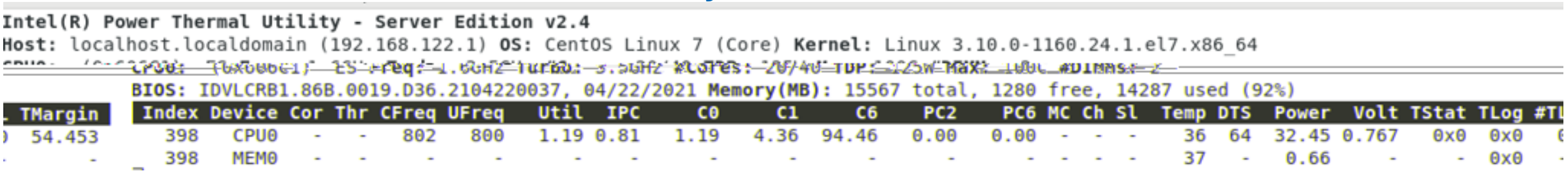
# Intel® Power Thermal Utility (Intel® PTU) Monitor Data




| | |
|---|---|
| Cfreq | Core Frequency. Intel® PTU uses combination of MSR registers (0x30a & 0x30b) and timer stamp counter (MSR 0x10) to figure out the current CPU operating frequency internally. |
| Ufreq | Uncore Frequency |
| IPC | IPC column shows the average number of retired instruction per cycle. Each core/thread has its own IPC. The CPU line shows the average IPC of all core threads. |
| CO/C1/C6 | core C-state residency |
| PC2/PC6 | package C-state residency |
| Temp | current die temp. (MSR 1b1h) |
| DTS | relative distance to a fixed temp DTSmax. (MSR 1b1h) |
| Power | current package power consumed of the CPU. (MSR 611h) |
| Volt | current P-state voltage. Each core has its own voltage (FIVR out reading). The CPU line shows the average voltage of all cores. |
| Tstat | Thermal status. Bit 0 is when your CPU is in thermal throttling. Usually, it happens when the DTS is 0.<br>Bit 1 is PROCHOT. This could come from external devices. Example: memory, PCH, platform, etc.<br>Bit 2 is Critical temperature. You will probably never see this; system will shut down the computer.<br>Bit 3 is Pmax assertion |
| Tlog | When there is Tstat set, most likely Tlog will have a copy as well. PTUmon will clear whenever it restart the program. |
| TMargin | ICX-D is SOC, Tmargin is the delta between the hottest die temp and Tcontrol. |

# Command for Monitor and Data Log

| Use Case | | Command |
|---|---|---|
| Monitor Function | Run PTU Mon to show both CPU and MEM | ./ptu –mon |
| | Run PTU Mon to show both CPU and MEM details | ./ptu –mon –l 1 |
| | Run PTU Mon to show both CPU and MEM in screen mode | ./ptu –mon –scr |
| | Run PTU Mon and specify the update interval in 1 second<br>Run PTU Mon and specify the update interval in 0.1 second | ./ptu –mon –i 1000000<br>./ptu –mon –i 100000 |
| Data Log Function | Run PTU Mon and save the log as **test1** file to the folder **/root/Desktop** | ./ptu –mon –log –logdir /root/Desktop/ -logname test1 |
| | Run PTU Mon and save the log as **test2.csv** file to the folder **/root/Desktop** | ./ptu –mon –log –logdir /root/Desktop/ -logname test2 –csv |
| | Run Turbo Test for IA/SSE turbo check and save the log as **SSE** file to the folder **/root/Desktop** | ./ptu –ct 8 –avx 1 –log –logdir /root/Desktop/ -logname SSE |
| | Run Turbo Test for AVX2 turbo check and save the log as **AVX2** file to the folder **/root/Desktop** | ./ptu –ct 8 –avx 2 –log –logdir /root/Desktop/ -logname AVX2 |
| | Run Turbo Test for AVX3 turbo check and save the log as **AVX3** file to the folder **/root/Desktop** | ./ptu –ct 8 –avx 3 –log –logdir /root/Desktop/ -logname AVX3 |

For more details, check Linux* PTU help. (./ptu –h)

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# FAQ (1/3)

- Q1: Intel® Power Thermal Utility (Intel® PTU) is able to show Processor Frequency, how does Intel® PTU calculate it? Which registers and formula does it use?
- A1: Intel® PTU uses combination of MSR registers (0x30a & 0x30b) and timer stamp counter (MSR 0x10) to figure out the current CPU operating frequency internally.
- Q2: CPU could not reach turbo frequency listed in DCL when Intel® PTU running TDP stress or heavy workload but CPU could reach turbo frequency when running lighter workload?
- A2: CPU turbo bins highly depends on the CPU package power and thermal headroom. When running heavy workload like TDP or 100% Core Power level, that would be less power thermal headroom for turbo bins. For more details, please refer to “debug handbook, doc# 611976”, CPU could not reach the maximum turbo frequency when using Intel® PTU to stress.

# FAQ (2/3)

- Q3: What's the stress mechanism of core Intel® Advanced Vector Extensions (Intel® AVX)?
- A3: CoreAVX uses high power instruction sets to stress and power can be exceeded/near TDP and as a result CPU might go into throttle mode. This test is not meant for processor thermal characterization.

- Q4: Why could not some CPU SKU reach TDP with Near TDP enabled?
- A4: Most of SKUs can be stressed to TDP power with Near TDP feature enabled in PTU, but a few SKUs such as LCC ones still may not be able to do so due to uncore idle.

# FAQ (3/3)

- Q5: Is there any limitation when stressing CPU and Memory simultaneously?
- A5: It is impossible to stress both CPU 100% (or significantly) and memory 100% (or significantly) at the same time from the architecture point of view. It is usually good to generate the preheats for downstream components.

- Q6: Intel® Power Thermal Utility (Intel® PTU) DIMM Power Accuracy?
- A6: The reading from VR and the Pcode calculation (read from Intel® PTU) for Broadwell reference system, the differences are less than 20% for the medium to the max DIMM power, and about 50% to 100% for the DIMM power consumption at idle. Different platform and DIMM power may have different tolerance.


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