6249828 MITSUBISHI(MICMPTR/MIPRC)
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MITSUBISHI MICROCOMPUTERS

M5L8049-XXXP, P-6
M5L8039P-11, P-6

SINGLE-CHIP 8-BIT MICROCOMPUTER

T-49-19-05

DESCRIPTION

The M5L8049-XXXP, P-6 and M5L8039P-11, P-6 are 8-bit parallel microcomputers fabricated on a single chip using high-speed N-channel silicon gate ED-MOS technology.

Speed \ ROM Type	Internal ROM Type	External ROM Type
11 MHz Type	M5L8049-XXXP	M5L8039P-11
6 MHz Type	M5L8049-XXXP-6	M5L8039P-6

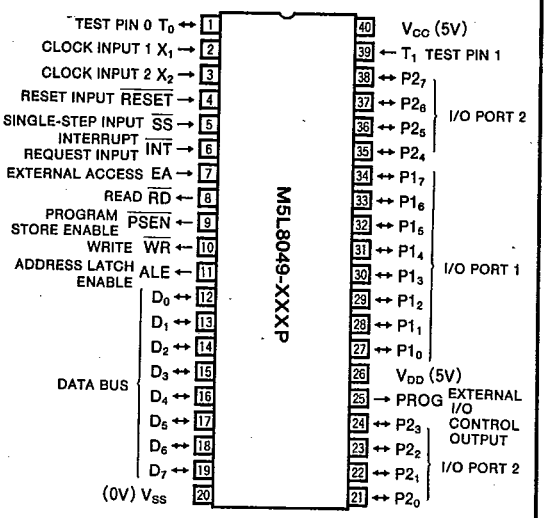
FEATURES

- Single 5V power supply
- Instruction cycle

11MHz	8MHz	6MHz
1.36μs(min)	1.875μs(min)	2.5μs(min)

- Basic machine instructions 96
  - 1-byte instructions: 68
  - 2-byte instructions: 28
- Direct addressing ..... up to 4096 bytes
- Internal RAM ..... 128 bytes
- Built-in timer/event counter ..... 8 bits
- I/O Ports ..... 27 lines
- Easily expandable Memory and I/O:
- Subroutine nesting ..... 8 levels
- External and timer/event counter interrupt . 1 level each
- External RAM ..... 256 bytes
- M5L8049-XXXP/M5L8039P-11, P-6 are interchangeable with i8049/i8039, i8039-6 in pin configuration and electrical characteristics.

PIN CONFIGURATION (TOP VIEW)

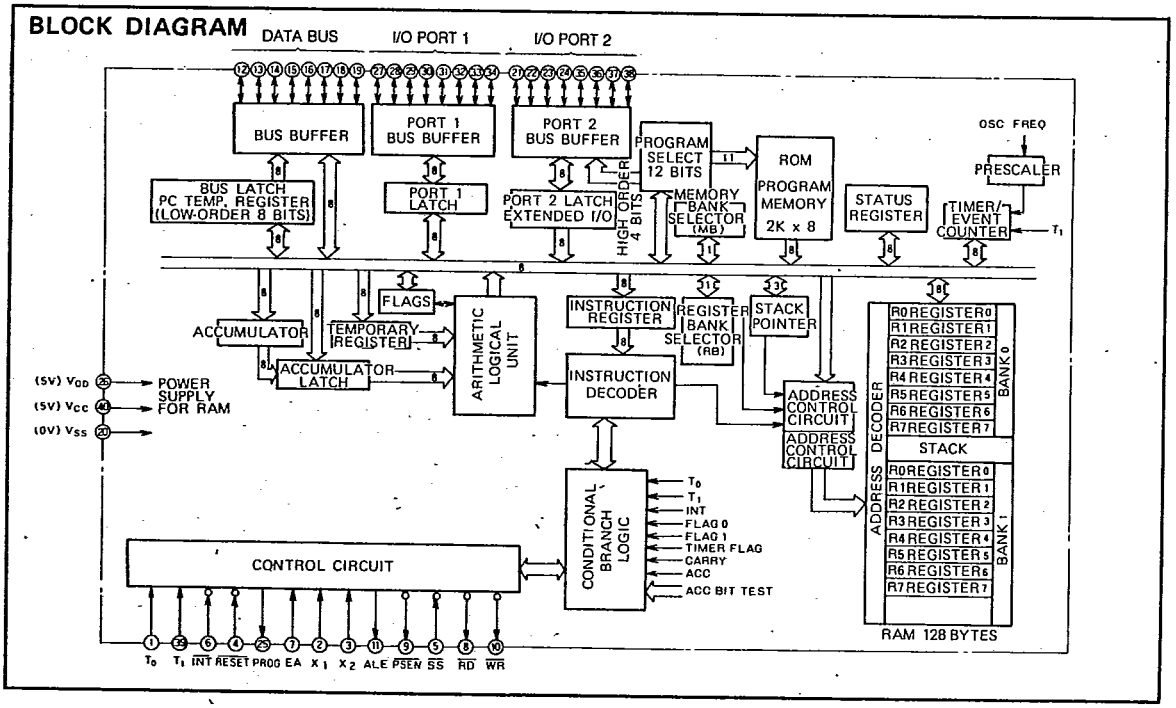


Outline 40P4

APPLICATION

- Control processor or CPU for a wide variety of applications

BLOCK DIAGRAM



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FUNCTION

The M5L8049-XXXP and M5L8039P are integrated 8-bit CPUs, with memory (ROM, RAM) and timer/event counter interrupt all contained on a single chip.

PIN DESCRIPTION

Pin	Name	Input or output	Function
V_{SS}	Ground		Normally connected to ground (0V).
V_{CC}	Main power supply		Connected to 5V power supply.
V_{DD}	Power supply		①Connected to 5V power supply. ②Used for memory hold when V_{CC} is cut.
T_0	Test pin 0	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JT0/JNT0).
		Output	②Used for outputting the internal clock signal (ENT0 CLK).
X_1, X_2	Crystal inputs	Input	External crystal oscillator or RC circuit input for generating internal clock signals. An external clock signal can be input through X_1 or X_2.
$\overline{RESET}$	Reset	Input	Control used to initialize the CPU.
$\overline{SS}$	Single step	Input	Control signal used in conjunction with ALE to stop the CPU through each instruction, in the single-step mode.
$\overline{INT}$	Interrupt	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JNI). ②Used for external interrupt to CPU.
EA	External access	Input	①Normally maintained at 0V. ②When the level is raised to 5V, external memory will be accessed even when the address is less than 400_{16} (2048). The M5L8039P is raised to 5V.
$\overline{RD}$	Read control	Output	Read control signal used when the CPU requests data from external data memory or external device to be transferred to the data bus. (MOVX A, @R_r, and INS A, BUS)
$\overline{PSEN}$	Program store enable	Output	Strobe signal to fetch external program memory.
$\overline{WR}$	Write control	Output	Write control signal used when the CPU sends data through the data bus to external data memory or external device. (MOVX @R_r, A and OUTL BUS, A)
ALE	Address latch enable	Output	A signal used for latching the address on the data bus. An ALE signal occurs once during each cycle.
D_0~D_7	Data bus	Input/output	①Provides true bidirectional bus transfer of instructions and data between the CPU and external memory. Synchronizing is done with signals $\overline{RD}$/$\overline{WR}$. The output data is latched.
			②When using external program memory, the output of the low-order 8 bits of the program counter are synchronized with ALE. After that, the transfer of the instruction code or data from the external program memory is synchronized with $\overline{PSEN}$.
			③The output of addresses for data using the external data memory is synchronized with ALE. After that, the transfer of data with the external data memory is synchronized with $\overline{RD}$/$\overline{WR}$. (MOVX A, @R_r, and MOVX @R_r, A)
$P2_0$~$P2_7$	Port 2	Input/output	①Quasi-bidirectional port. When used as an input port, FF_{16} must first be output to this port. After reset, when not used as an output port, nothing needs to be output.
		Output	②$P2_0$~$P2_3$ output high-order 4 bits of the program counter when using external program memory.
		Input/output	③$P2_0$~$P2_3$ serve as a 4-bit I/O expander bus for the M5L8243P.
PROG	Program	Output	Strobe signal for M5L8243P I/O expander.
$P1_0$~$P1_7$	Port 1	Input/output	Quasi-bidirectional port. When used as an input port, FF_{16} must first be output to this port. After reset, when not used as an output port, nothing needs to be output.
T_1	Test pin 1	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JT1/JNT1). ②When enabled, event signals are transferred to the timer/event counter (STRT CNT).

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5～7	V
V_{DD}	Supply voltage		−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
P_d	Power dissipation	Ta＝25℃	1.5	W
Topr	Operating free-air temperature range	M5L8049-XXXP-6 M5L8039P-6	−20～75	℃
		M5L8049-XXXP M5L8039-11	0～70	
Tstg	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH1}	High-level input voltage, except for X_1, X_2, $\overline{RESET}$	2		V_{CC}	V
V_{IH2}	High-level input voltage, X_1, X_2, $\overline{RESET}$	3.8		V_{CC}	V
V_{IL}	Low-level input voltage	−0.5		0.8	V

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, V_{CC}=V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OL1}	Low-level output voltage, BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE	I_{OL}=2mA			0.45	V
V_{OL2}	Low-level output voltage, except for the above and PROG	I_{OL}=1.6mA			0.45	V
V_{OL3}	Low-level output voltage PROG	I_{OL}=1mA			0.45	V
V_{OH1}	High-level output voltage, BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE	I_{OH}=−100μA	2.4			V
V_{OH2}	High-level output voltage, except for the above	I_{OH}=−50μA	2.4			V
I_I	Input leak current, T1, $\overline{INT}$	$V_{SS} \leqq V_{IN} \leqq V_{CC}$	−10		10	μA
I_{OZ}	Output leak current, BUS, TO, high-impedance state	$V_{SS}+0.45 \leqq V_{IN} \leqq V_{CC}$	−10		10	μA
I_{LI1}	Input current during low-level input, port	V_{IL}=0.8V		−0.2		mA
I_{LI2}	Input current during low-level input, $\overline{RESET}$, $\overline{SS}$	V_{IL}=0.8V		−0.05		mA
I_{DD}	Supply current from V_{DD}	Ta＝25℃		25	50	mA
$I_{DD}+I_{CC}$	Supply current from V_{DD} and V_{CC}	Ta＝25℃		100	170	mA

TIMING REQUIREMENTS (T_a=−20～75℃, V_{CC}=V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Limits									Unit
			M5L8049-XXXP M5L8039P-11 (Note 2)			M5L8049-XXXP-8 M5L8039P-8			M5L8049-XXXP-6 M5L8039P-6			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tc	Cycle time	t_{CY}	1.36		15.0	1.875		15.0	2.5		15.0	μs
th (PSEN-D)	Data hold time after $\overline{PSEN}$	t_{DR}	0		100	0		150	0		200	ns
th (R-D)	Data hold time after $\overline{RD}$	t_{DR}	0		100	0		150	0		200	ns
tsu (PSEN-D)	Data setup time after $\overline{PSEN}$	t_{RD}			200			350			500	ns
tsu (R-D	Data setup time after $\overline{RD}$	t_{RD}			200			350			500	ns
tsu (A-D)	Data setup time after address	t_{AD}			400			650			950	ns
tsu (PROG-D)	Data setup time after PROG	t_{PR}			650			700			810	ns
th (PROG-D)	Data hold time before PROG	t_{PF}	0		150	0		150	0		150	ns

Note 1 : The input voltage are V_{IL}=0.45V and V_{IH}=2.4V.
2 : Ta=0～70℃

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SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC} = V_{DD} = 5V±10%, V_{SS} = 0V, unless otherwise noted)

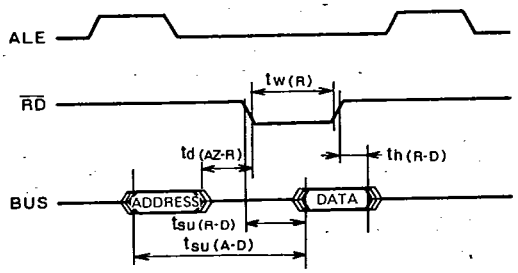
Symbol	Parameter	Alternative symbol	Limits						Unit
			M5L8049-XXXP M5L8039-11 (Note 2)			M5L8049-XXXP-6 M5L8039P-6			
			Min	Typ	Max	Min	Typ	Max	
tw (ALE)	ALE pulse width	t_{LL}	150			400			ns
td (A-ALE)	Delay time, address to ALE signal	t_{AL}	70			150			ns
tv (ALE-A)	Address valid time after ALE	t_{LA}	50			80			ns
tw (PSEN)	$\overline{PSEN}$ pulse width	t_{CC}	300			700			ns
tw (R)	$\overline{RD}$ pulse width	t_{CC}	300			700			ns
tw (W)	$\overline{WR}$ pulse width	t_{CC}	300			700			ns
td (Q-W)	Delay time, data to $\overline{WR}$ signal	t_{DW}	250			500			ns
tv (W-Q)	Data valid time after $\overline{WR}$	t_{WD}	40			120			ns
td (A-W)	Delay time, address to $\overline{WR}$ signal	t_{AW}	200			230			ns
td (AZ-R)	Delay time, address disable to $\overline{RD}$ signal	t_{AFC}	−10			0			ns
td (AZ-PSEN)	Delay time, address disable to $\overline{PSEN}$ signal	t_{AFC}	−10			0			ns
td (PC-PROG)	Delay time, port control to PROG signal	t_{CP}	100			110			ns
tv (PROG-PC)	Port control valid time after PROG	t_{PC}	60			130			ns
tp (Q-PROG)	Delay time, data to PROG signal	t_{DP}	200			220			ns
tv (PROG-Q)	Data valid time after PROG	t_{PD}	20			65			ns
tw(PROGL)	PROG low pulse width	t_{PP}	700			1510			ns
td (Q-ALE)	Delay time, data to ALE signal	t_{PL}	150			400			ns
tv (ALE-Q)	Data valid time after ALE	t_{LP}	20			150			ns

Note 3 : Conditions of measurement: control output C_L=80pF
data bus output, port output C_L=150pF

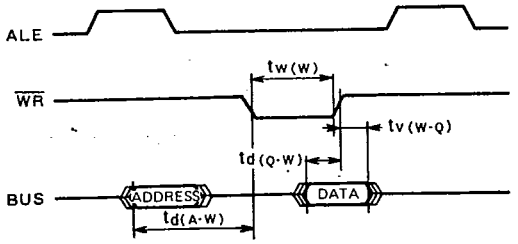
4 : Reference levels for the input/output voltages are low level=0.8V and high level=2V.

TIMING DIAGRAM

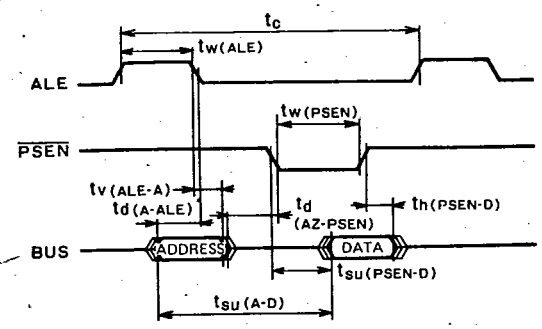
Read from External Data Memory



Write to External Data Memory



Instruction Fetch from External Program Memory



Port 2