Mandelbrot VHDL Viewer

Ian Roth

ECE8455 Advanced Digital Design Using FPGAs

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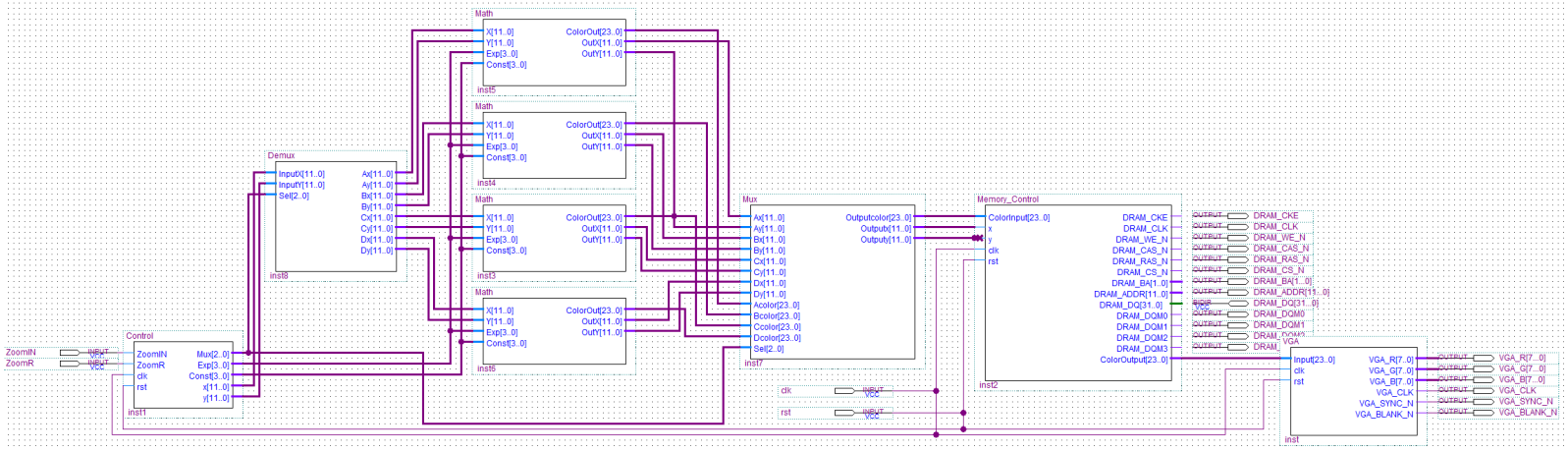
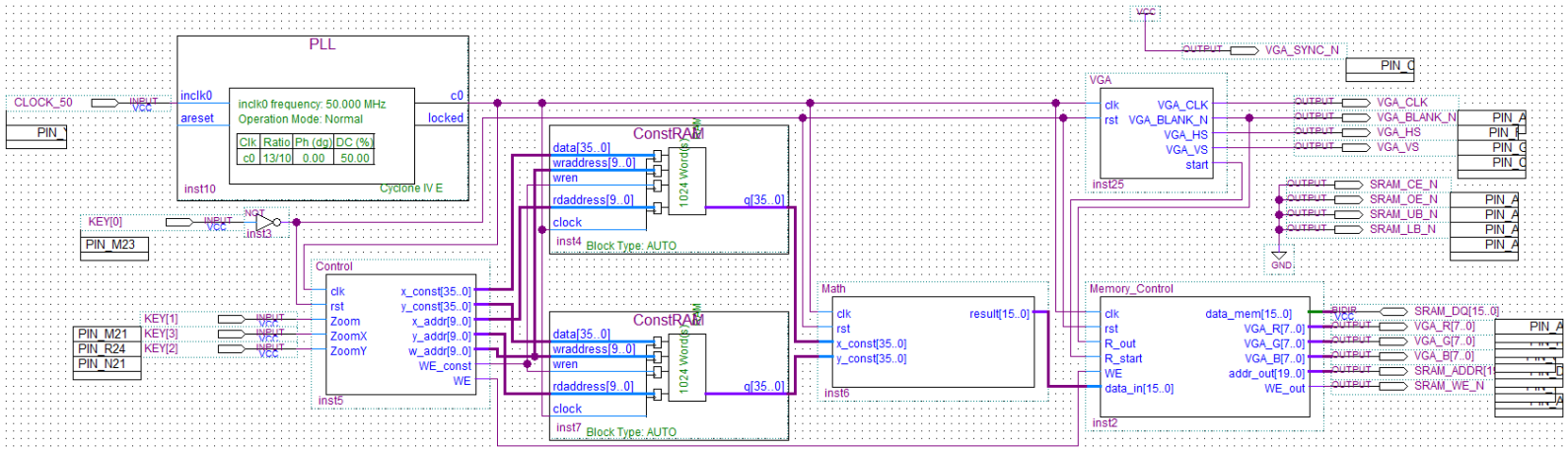
Introduction

The purpose of this project is to demonstrate the use of embedded 9 bit multipliers in a pipeline configuration for the generation of a fractal for VGA output. A Mandelbrot Set is the selected fractal and the output can be zoomed by the user. The completed system makes use of the VGA, SRAM, and push button components of the DE2-115 board.

Original Design



Revised Design



Considerations

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Pipelined design does not fully use multipliers.
Twice the 9 bit multipliers are needed for 36 bit fixed point arithmetic than the expected 4 per multiply.