ESE 516: Fall 2018
Project Part 1
Due October 31st

Use the following parameters for 0.5μm CMOS technology:
$V_{dd} = 5V$, $V_{Tn0} = 0.73V$, $k_n = \mu_n C_{ox} = 115\mu A/V^2$, $V_{Tp0} = -0.94V$ and $k_p = \mu_p C_{ox} = 37\mu A/V^2$.
To calculate transistor capacitances use the following parameters:
$C_{ox}=2.5\times10^{-3}F/m^2$, $L_S = L_D = 1.5\ \mu m$
NMOS: $C_j = 4.16\times10^{-4}F/m^2$, $C_{jsw} = 3.26\times10^{-10}F/m$, $C_{GD0} = C_{GS0} = 1.93\times10^{-10}F/m$.
PMOS: $C_j = 7.1\times10^{-4}F/m^2$, $C_{jsw} = 2.18\times10^{-10}F/m$, $C_{GD0} = C_{GS0} = 2.28\times10^{-10}F/m$.

Objective:
The goal of this part of the project is to estimate the small signal parameters of a transistor and to see how they depend on the sizing and biasing currents. You will investigate how different sizing of the transistors and different biasing currents affect the performance of the common-source amplifier, as well as the frequency response.

Report:
The project is done in a group of two students and only one report per group is required. In appendix of the report (at the end of report), please include schematic plots with annotated transistor sizes and results plots that demonstrate your claimed results.

Part 1.
Draw a schematic of a 4 terminal NMOSFET with W=4.8μm, L=1.2μm, that will allow you to sweep the voltages on the gate, drain, source and bulk. Print this schematic.

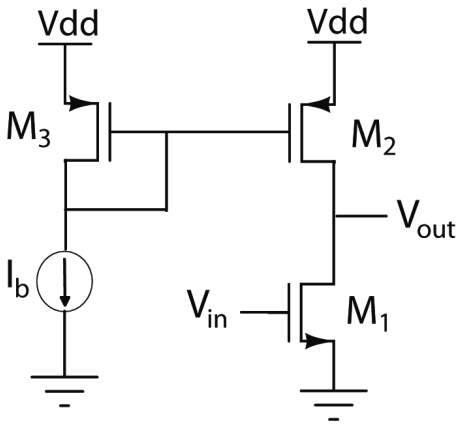
1. Holding the $V_{gs} = 0.9V$, $V_{sb} = 0V$, run a DC simulation that will sweep the V_{ds} of the transistor from 0V to 5V, in steps of 0.1mV. Plot I_{ds} vs V_{ds}. Extract the values of output resistance r_o. Print the graphs and explain clearly how you extracted the parameters.

2. Repeat the experiment 2. for different values of V_{gs} voltage (0.8, 1V and 1.1V). Extract the values of output resistance r_o. How r_o depends on the value of the current I_d in the saturation?

3. Repeat the experiment 2. with $V_{gs} = 0.9V$, but with different sizing of the transistor (W/L): (2.4μm/0.6μm), (9.6μm/2.4μm) (14.4μm/3.6μm). Is there a difference in value of output resistance?

Part 2.

Draw the schematic of the common-source amplifier shown in Figure 1. The sizing of transistors is following: W_1=7.2µm, L_1=1.8µm, W_2=W_3=7.2µm and L_2=L_3=3.6µm. The biasing current is I_b = 10µA.



1. Measure the gain of the amplifier using DC analysis and plot of $\partial V_{out}/\partial V_{in}$ and DC value of the input voltage V_{IN} that provides the maximum gain of the amplifier. The step of the voltage sweep around the DC voltage with the maximum gain has to be 10µV.

2. By keeping all the other parameters constant, change the width of the gain transistor W_1 to 3.6µm, 10.8µm, 14.4µm and 18µm. How does the change of width affect the gain of amplifier?

3. By keeping the constant W/L, change both the width and the length to (2.4µm/0.6µm), (4.8µm/1.2µm), (9.6µm/2.4µm) (14.4µm/3.6µm). Measure the gain. How is gain affected by changes in the length of the transistor?

4. Keep the sizing of the transistor as in Part 1 and change the biasing current to 1µA, 50µA, 100µA and 500µA. What is the effect of the change in the biasing current on the gain?

Part 3.

For the same common-source amplifier shown in Figure 1, with the sizing of transistors and same biasing current as in Part 2, provide input voltage as $V_{in} = V_{IN} + v_{in}$, where V_{IN} is DC value of the input voltage V_{IN} that provides the maximum gain of the amplifier found in Part 2 task 1.

1. Add a capacitor of size 10pF to the output node of the amplifier. Use AC analysis to find the first pole of the amplifier transfer function. Calculate the location of the pole. How the measured value compares to the calculated one?

2. Change the size of the capacitor to 10fF. Calculate and measure the location of the pole (Note: count in the internal capacitance of the amplifier at the output node).