ESE 516: Fall 2018
Project 2
Due December 17th

Use the following parameters for 0.5μm CMOS technology:
$V_{dd} = 5V$, $V_{Tn0} = 0.73V$, $k_n = \mu_n C_{ox} = 115\mu A/V^2$, $V_{Tp0} = -0.94V$ and $k_p = \mu_p C_{ox} = 37\mu A/V^2$.

Report:
The project is done in a group of two students and only one report per group is required. In appendix of the report (at the end of report), please include schematic plots with annotated transistor sizes and results plots that demonstrate your claimed results.

Problem 1.
Draw the two-stage amplifier shown in Figure 1. The sizing of the transistors is following:
$(W_1 / L_1) = (W_2 / L_2) = (14.4\mu m / 1.2\mu m)$, $(W_3 / L_3) = (W_4 / L_4) = (6\mu m / 3\mu m)$,
$(W_5 / L_5) = (7.2\mu m / 2.4\mu m)$, $(W_6 / L_6) = (28.8\mu m / 1.2\mu m)$ and $(W_7 / L_7) = (6\mu m / 3\mu m)$.
Set the biasing voltages V_B and V_{B1} so the currents of transistors M_5 and M_7 are $I_{D5} = 40\mu A$ and $I_{D7} = 240\mu A$.
Capacitors C_o and C_c are both equal to 1pF.
Use the following values for calculation of the output resistance: $\lambda_{n1} = \lambda_{n2} = 0.042\ V^{-1}$, $\lambda_{n5} = 0.026\ V^{-1}$, $\lambda_{n7} = 0.02\ V^{-1}$, $\lambda_{p3} = \lambda_{p4} = 0.015\ V^{-1}$ and $\lambda_{p6} = 0.007\ V^{-1}$.

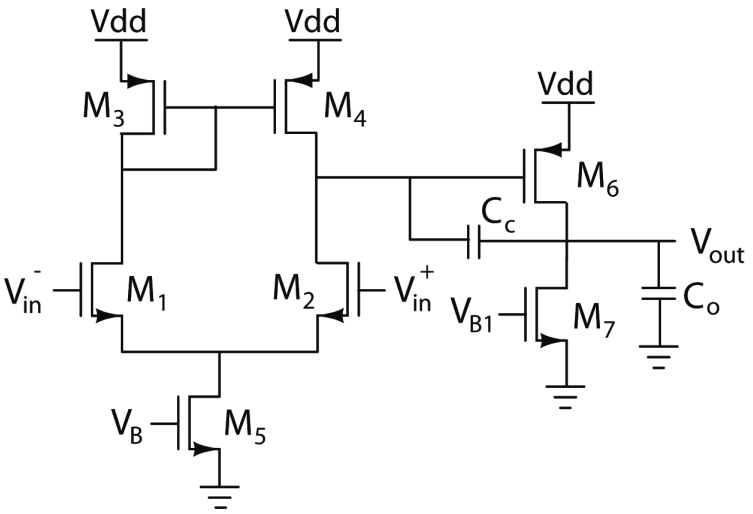

Figure 1.

1. Calculate the small-signal differential-mode and common-mode voltage gain for the shown amplifier, the input common-mode voltage range and the output voltage range.

2. Connect both inputs to the DC voltage source V_{IC} and using DC analysis plot the output voltage as the function of the voltage V_{IC}. What is the range of the voltage V_{IC} for which all transistors operate in saturation? How the calculated values compare to the values from the obtained plot? Measure the small-signal common-mode voltage gain. How the measured value compares to the calculated one?

3. Connect the differential voltage source v_{id} to the one of the inputs in series with the voltage source V_{IC}. Set both voltage sources V_{IC} to 2.5V. Sweep the voltage v_{id} from -0.25V to 0.25V with the voltage step of 0.001mV. Measure the small-signal differential-mode voltage gain. How the measured value compares to the calculated one? Estimate the output voltage range. Calculate the common-mode rejection ratio (CMRR).

4. Use AC analysis to plot the magnitude and phase of the transfer function of the amplifier. Calculate the location of the dominant pole. How the measured value compares to the calculated one? Calculate the other poles and zeros and estimate their locations from the plots of the magnitude and phase of the transfer function. Calculate the phase margin and compare it to the measured value. Calculate the GBW product.

5. Draw a schematic of a unity gain buffer shown in Figure 2, where the operational amplifier is the two-stage amplifier shown in Figure 1. Measure the settling time (output settles within 0.5% of the desired value), when the applied input voltage is a step voltage from 2V to 3V. How the measured settling time compares to the calculated value?

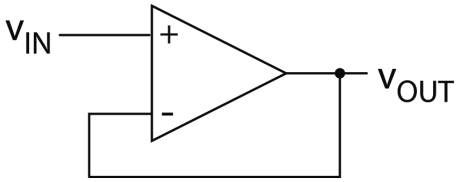

Figure 2.

Problem 2.
Draw the schematic of the differential folded-cascode amplifier shown in Figure 3.
The sizing of the transistors is following:
$(W_3 / L_3) = (W_4 / L_4) = (6\mu m / 3\mu m)$, $(W_5 / L_5) = (W_6 / L_6) = (4.8\mu m / 1.8\mu m)$,
$(W_7 / L_7) = (W_8 / L_8) = (4.8\mu m / 1.8\mu m)$, $(W_9 / L_9) = (W_{10} / L_{10}) = (3\mu m / 3\mu m)$ and
$(W_{11} / L_{11}) = (7.2\mu m / 3.6\mu m)$.

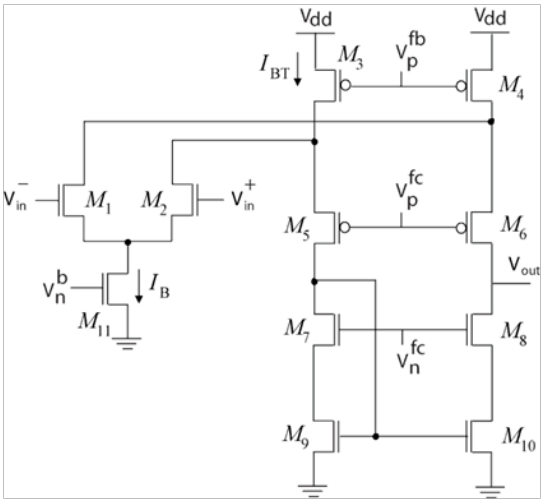

Figure 3. Folded-cascode operational amplifier.

1. Calculate the biasing current I_B and sizing of the transistors $(W_1 / L_1) = (W_2 / L_2)$ such that the settling time of the amplifier, when used as unity-gain buffer, is 20 ns when driving capacitance C_L = 1pF. Assume that the slewing time (t_{SR}) and linear settling time (t_{SS}) are equal and that the output voltage settles within four times of the time-constant of the amplifier ($t_{SS} = 4\,\tau$). Assume that the current $I_{BT} = 0.6\ I_B$. Set the biasing voltages V_n^b and V_p^{fb} so the currents of transistors M_{11} and M_3 are equal to calculated values of I_B and I_{BT}, respectively.
   Hint: Amplifier enters the linear settling when $V_{in}^+ - V_{in}^- = 1.4\ V_{ov1}$.
   Hint: For length of transistors of M_1 and M_2 use $L_1 = L_2 = 1.2\mu m$.

2. Find the biasing voltages V_p^{fc} and V_n^{fc} so that all transistors operate in saturation when common-mode voltage is applied at the inputs and the output voltage range is maximized.

3. With the calculated sizing of transistors and biasing voltages, simulate amplifier as unit gain buffer with the loading capacitance C_L = 1pF. How is the measured value of the settling time (within 0.5% of the final step value) different from the calculated value? Adjust values of biasing currents I_B and I_{BT} to satisfy the settling time constraint if it is not satisfied.

4. For the open-loop amplifier, connect both inputs to the DC voltage source V_{IC} and using DC analysis plot the output voltage as the function of the voltage V_{IC}. What is the DC voltage at the output when V_{IC} equals 2V? What is the small-signal common-mode voltage gain? What is the range of the voltage V_{IC} for which all transistors operate in saturation? How the values compare to the values obtained for two-stage amplifier in Part 1?

5. Connect the differential voltage source v_{id} to the one of the inputs in series with the voltage source V_{IC}. Set both voltage sources V_{IC} to 2.5V. Sweep the voltage v_{id} from -0.25V to 0.25V with the voltage step of 0.001mV. What is the small-signal differential-mode voltage gain? Estimate the output voltage range. Calculate the common-mode rejection ratio (CMRR). How the values compare to the values obtained for two-stage amplifier in Part 1? How the power of the amplifier in Part 1 and Part 2 compare?