Heaven's light is our guide

RAJSHAHI UNIVERSITY OF ENGINEERING AND TECHNOLOGY

Department Of Electrical & Computer Engineering

Course Title:

VLSI Design Sessional

Course Code:

ECE 4128

Submitted to:	Submitted by:
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Experiment No. 2

Name of the Experiment

Implementation of NMOS ratio less inverter.

Theory

An inverter is one of the most fundamental logic gates in digital electronics, producing an output that is the logical complement of its input. In transistor-based implementations, inverters can be built using CMOS technology (complementary PMOS and NMOS devices) or NMOS-only designs.

In NMOS logic, both pull-up and pull-down networks are implemented using NMOS transistors. A conventional NMOS inverter uses a load resistor connected between the supply voltage (V_{DD}) and the output node, with an NMOS transistor acting as the pull-down device to ground. However, using physical resistors in integrated circuits is area-inefficient and slow, especially for large-scale integration. To overcome this limitation, the resistor can be replaced by active load NMOS transistors, creating a ratio-less inverter. This design does not require precise transistor sizing ratios to set the logic threshold, unlike ratioed logic, and is simpler to fabricate in NMOS technology.

The 3-NMOS ratio-less inverter is a digital circuit that uses three NMOS transistors without any resistive load. In this configuration, one NMOS transistor acts as the main driver (T1) while the other two NMOS transistors (T2 and T3) serve as active load devices. The driver transistor receives the input signal at its gate, and its source is connected to ground. The active load transistors are connected between V_{DD} and the output node, with their gates biased to ensure they remain partially ON, thereby functioning as constant current sources.

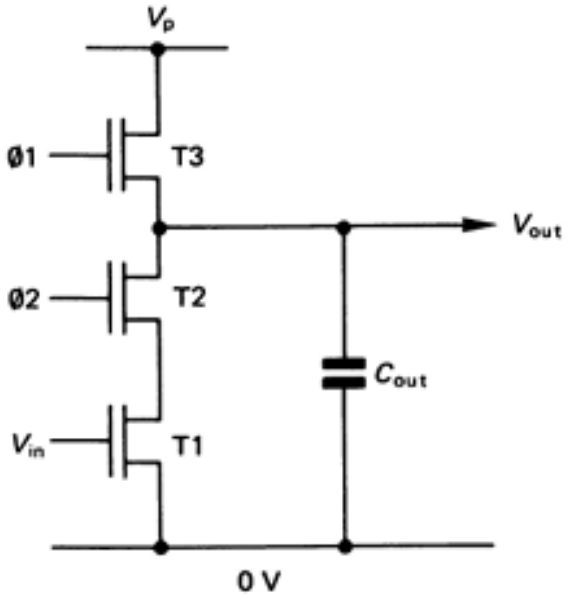

Figure 1: Schematic diagram of NMOS ratio less inverter.

Operation:

1. Input Low (Logic 0) – T1 is OFF, and the active load transistors (T2 and T3) conduct enough current to pull the output high to logic 1.
2. Input High (Logic 1) – T1 turns ON, forming a low-resistance path from the output to ground. The output is pulled to logic 0, while the active load still conducts slightly, leading to static power dissipation.

Required Tools

1. Microwind
2. MS Word

Circuit Diagram

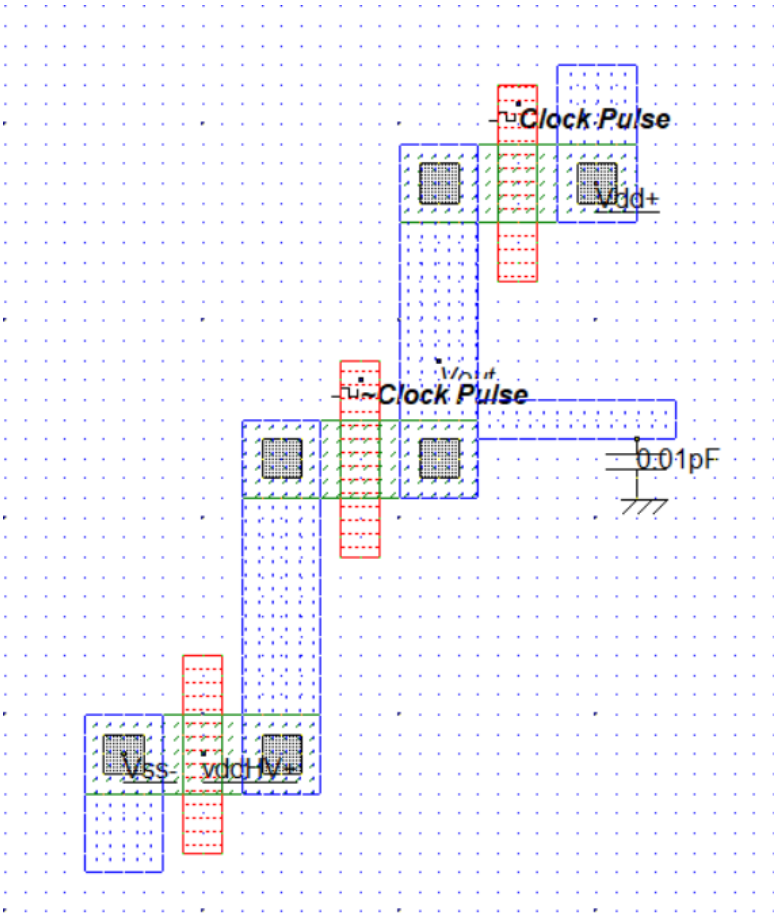

Figure 2: Circuit diagram of NMOS ratio less inverter.

Output

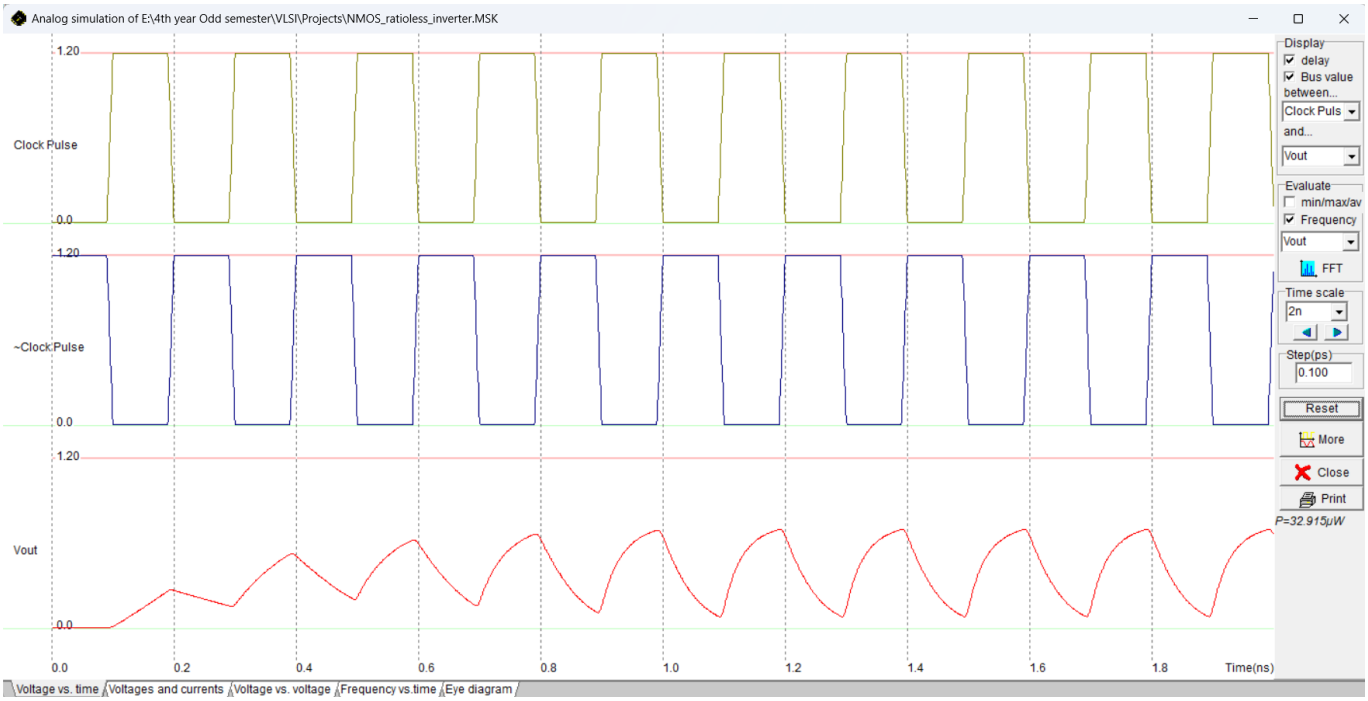

Figure 3: Voltage vs Time graph when Vin = 1

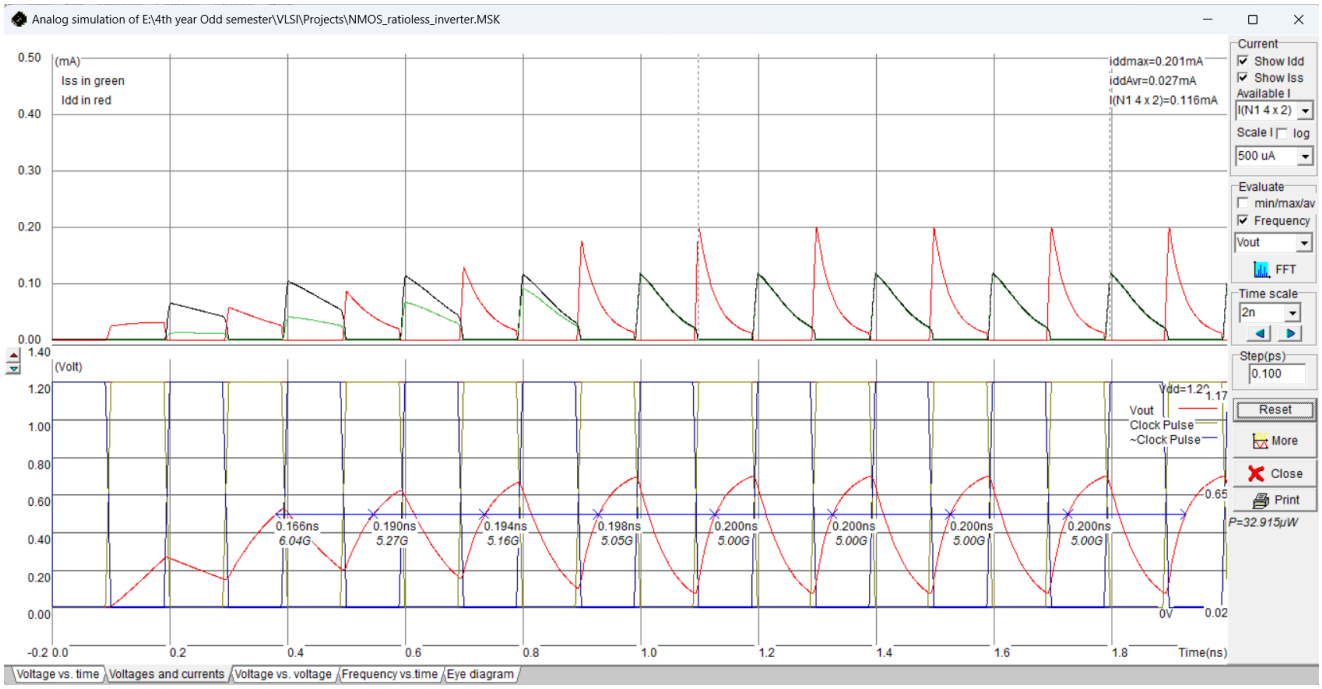

Figure 4: Voltage vs Current graph when Vin = 1

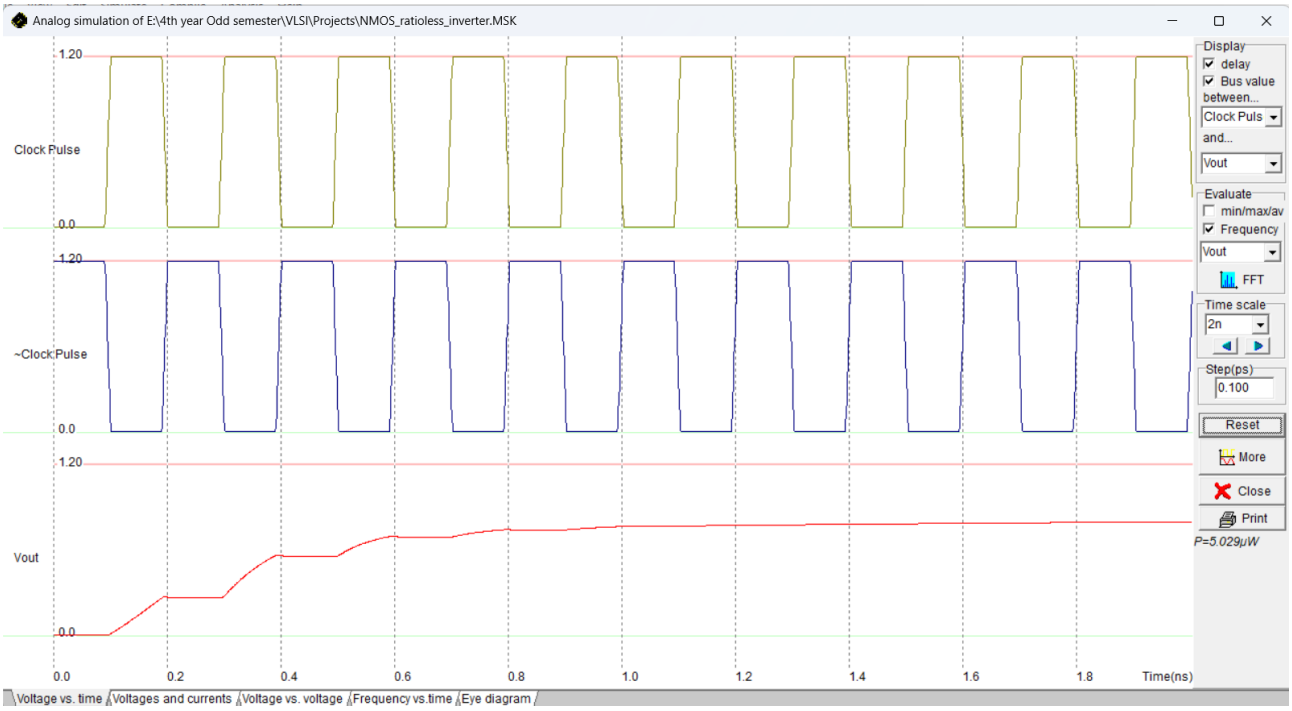

Figure 5: Voltage vs Time graph when Vin = 0

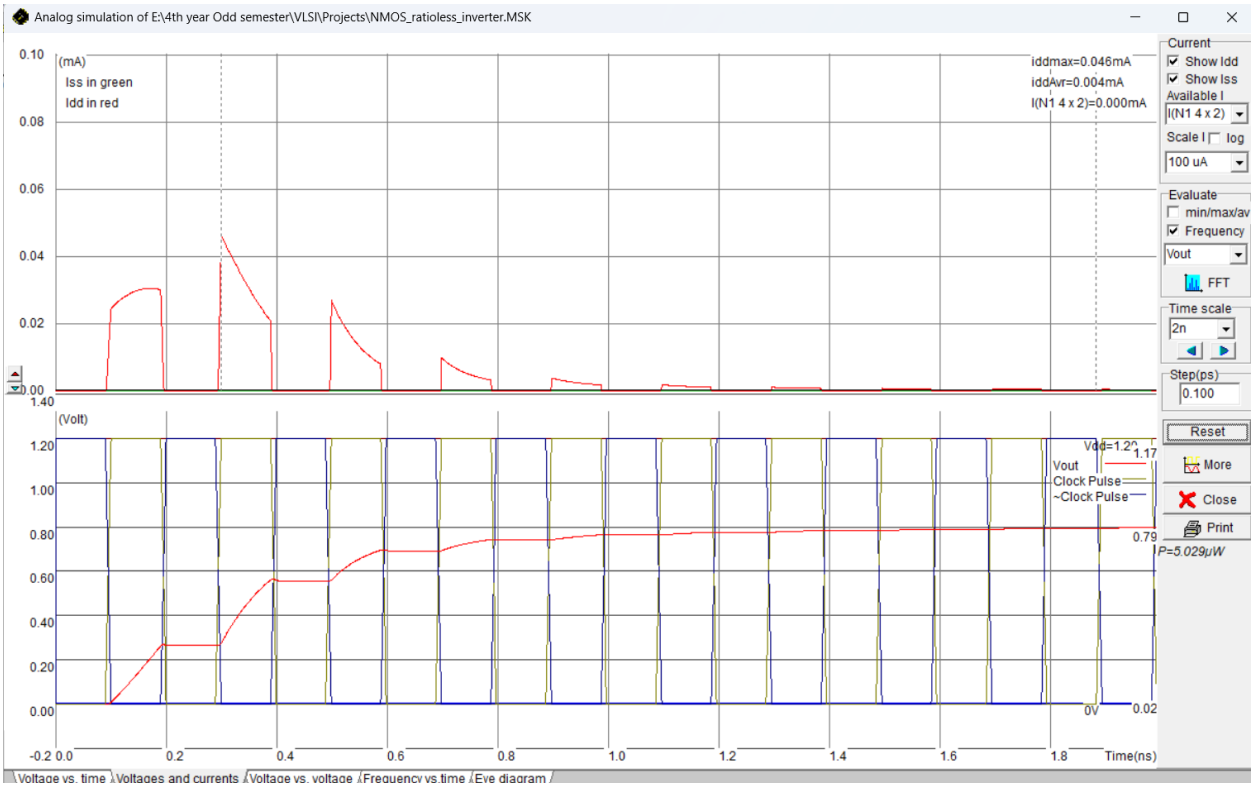

Figure 6: Voltage vs Current graph when Vin = 0

Discussion and Conclusion

In this experiment, a 3-NMOS ratio-less inverter was designed and simulated to examine its switching behavior and performance. The circuit used one NMOS driver transistor and two NMOS active load transistors, eliminating the need for resistors. Simulation confirmed the output was the logical inverse of the input: when the input was low, the active loads pulled the output high; when high, the driver pulled the output low.

The results showed slower rise times compared to fall times due to the weaker pull-up of the active loads, along with static power dissipation during the low output state caused by continuous current flow. These findings agree with theory, highlighting how transistor biasing and active load design affect switching speed, delay, and power consumption.

The inverter's switching threshold was found to be independent of transistor sizing ratios, a key feature of ratio-less designs. By removing resistors, the design is more suitable for NMOS IC fabrication. This study reinforced important concepts in transistor operation, active loading, and trade-offs between speed, power, and simplicity, offering useful insights for VLSI design.

Reference

[1] "MOS Inverter in VLSI Design." https://www.tutorialspoint.com/vlsi_design/vlsi_design_mos_inverter.htm (accessed Aug. 10, 2025).