Experiment No. 1

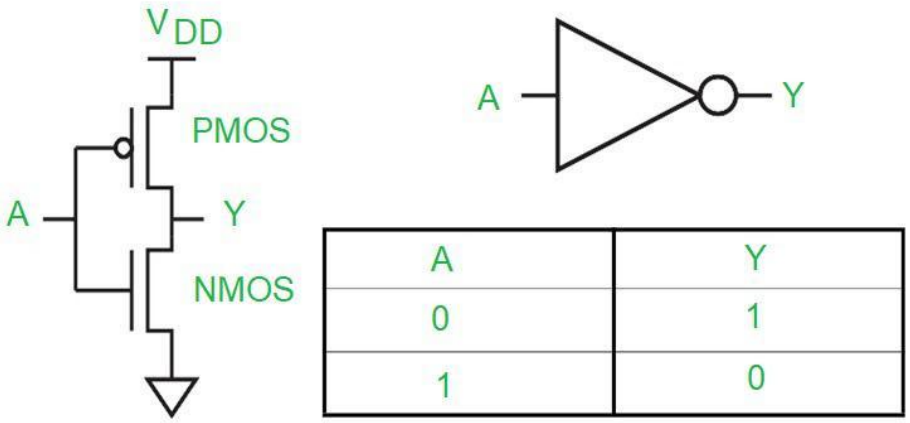
Name of the Experiment

Implementation of CMOS Inverter

Theory

A **CMOS inverter** is the most fundamental component in digital integrated circuits and serves as the basic building block for complex logic gates and memory cells. It is composed of two complementary transistors—a **pMOS** and an **nMOS**—arranged such that only one of them conducts at a time, ensuring minimal static power dissipation.

The **pMOS transistor** is connected to the supply voltage V_{DD}, while the **nMOS transistor** is connected to ground (V_{SS}). The input signal $V_{in}$is applied to both transistor gates, and the output $V_{out}$is taken from the node joining the drains of both transistors.



A	Y
0	1
1	0

1. Operation Principle

- **When $V_{in} = 0$:**
  The pMOS turns **ON** and connects $V_{out}$to V_{DD}, resulting in a logic HIGH output.
  The nMOS remains **OFF**.

$$V_{out} = V_{DD}(\text{logic } 1)$$

- **When $V_{in} = V_{DD}$:**
  The nMOS turns **ON** and connects $V_{out}$to ground, resulting in a logic LOW output.
  The pMOS remains **OFF**.

$$V_{out} = 0(\text{logic } 0)$$

This complementary behavior produces a full voltage swing and eliminates direct current flow between $V_{DD}$and ground, giving the CMOS inverter **high noise immunity and low static power consumption**.

2. Voltage Transfer and Switching Characteristics

The inverter's **Voltage Transfer Characteristic (VTC)** defines the relationship between the input voltage and the output voltage. The transition region, where both transistors conduct partially, determines the **switching threshold voltage** V_M, which ideally occurs near $V_{DD}/2$.

The performance parameters include:

- **Rise Time (t_r)** – Time for output to rise from 10% to 90% of V_{DD}
- **Fall Time (t_f)** – Time for output to fall from 90% to 10% of V_{DD}
- **Propagation Delay (t_p)** – Average of rise and fall transition delays

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

3. Effect of Load Capacitance

When a capacitive load C_L is connected at the output, it affects the charging and discharging process of the output node:

- During a HIGH-to-LOW transition, the nMOS transistor discharges the capacitor.
- During a LOW-to-HIGH transition, the pMOS charges the capacitor.

This results in finite rise and fall times, where:

$$t_r \approx 0.69 R_p C_L, t_f \approx 0.69 R_n C_L$$

Here, $R_p$and $R_n$are the effective resistances of pMOS and nMOS respectively.

Because holes in pMOS have lower mobility than electrons in nMOS ($\mu_p < \mu_n$), the pMOS device is typically made wider ($W_p \approx 2W_n$) to balance the rising and falling edge times.

4. Analytical Relationship

The propagation delay for a given load can be estimated using the empirical relation:

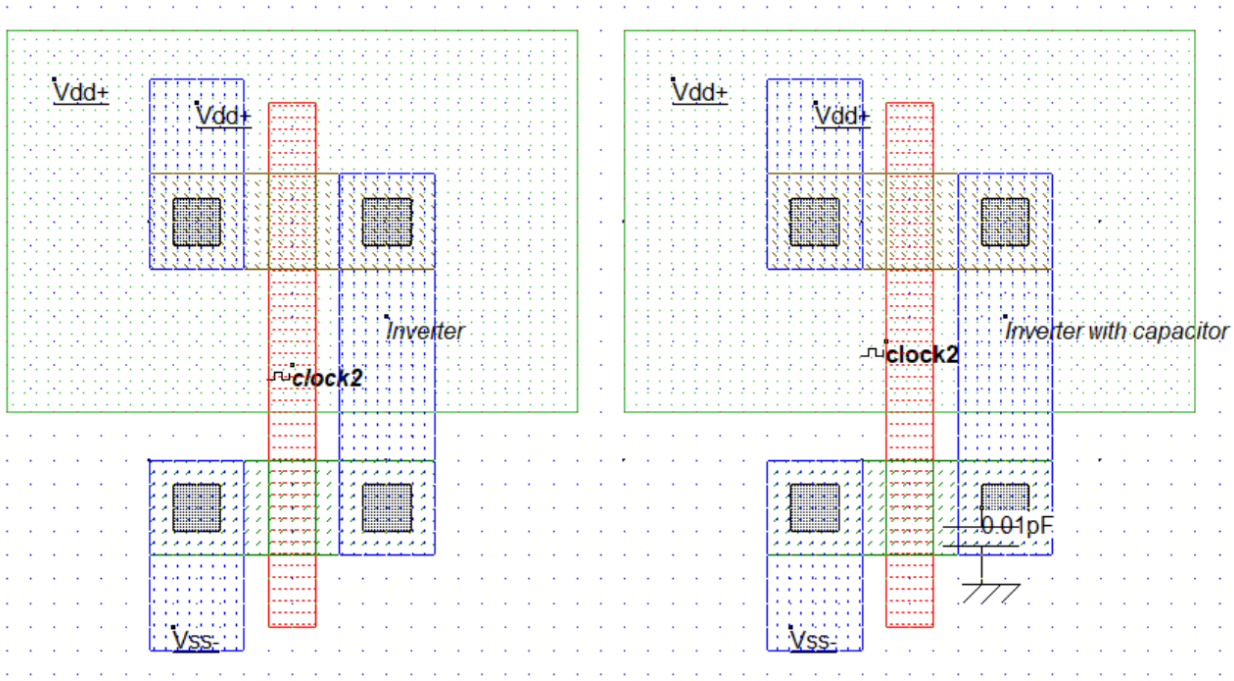
$$t_r(\text{ns}) = 35 \times C_{out}$$

where $C_{out}$is in picofarads (pF). Hence, increasing load capacitance or reducing transistor dimensions leads to slower output transitions.

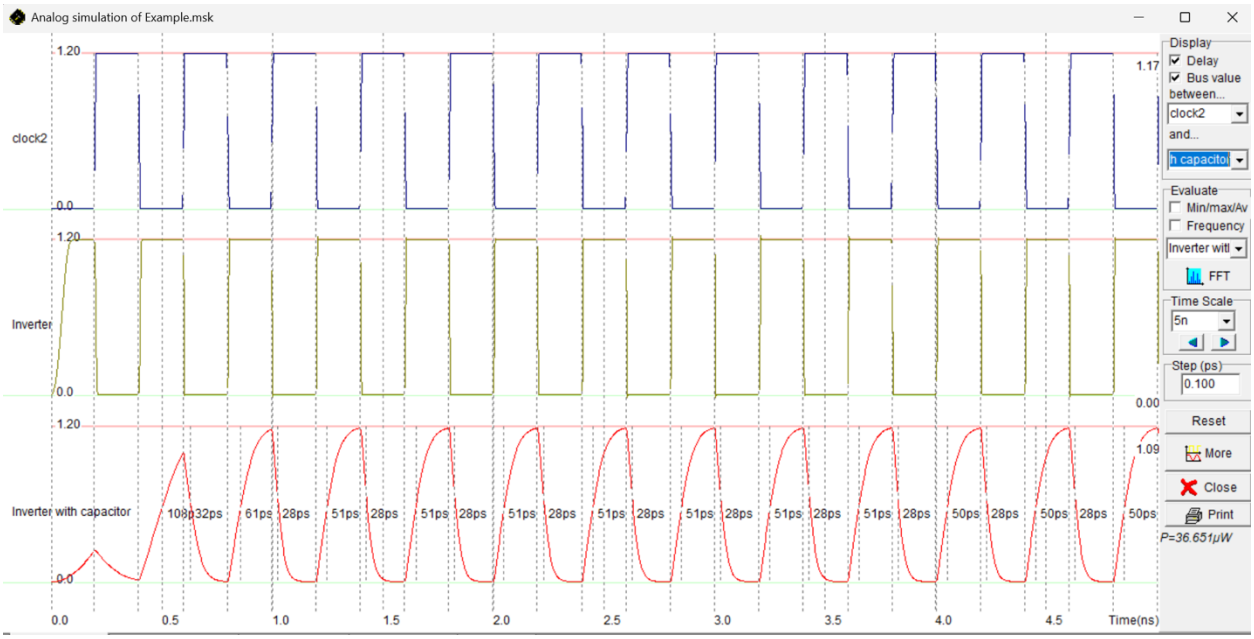
Required Tools

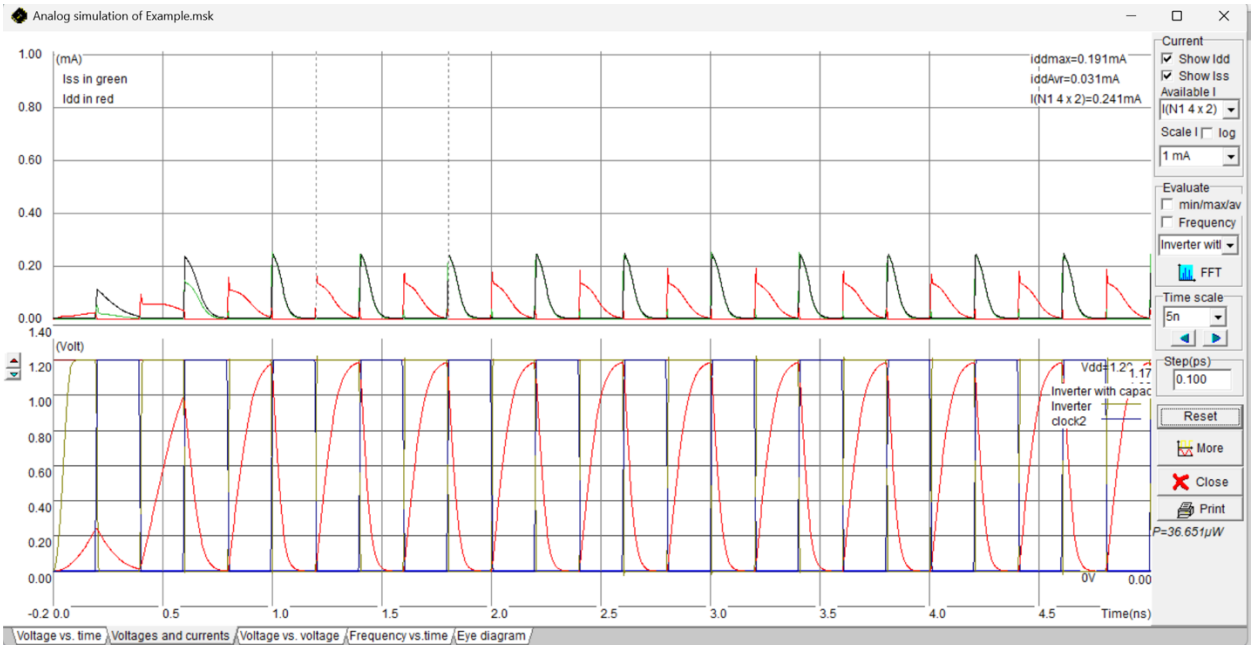
1. **MICROWIND** – for CMOS layout design and analog simulation
2. **MS Word** – for report preparation

Circuit Diagram



Output





Results

The CMOS inverter circuit was designed and simulated in **MICROWIND 3.1** using a supply voltage of **1.2 V**. Two cases were considered:

1. Inverter without load capacitance
2. Inverter with an external load capacitor of 0.01 pF

The simulation results showed the following characteristics:

- The output of the inverter was the **logical complement** of the input signal in both cases.
- The **waveforms without the capacitor** exhibited **sharp and ideal transitions**, indicating minimal propagation delay.
- When the **capacitor was added**, the rise and fall transitions became **slower**, and small current spikes were observed in the $I_{DD}$and I_{SS}traces due to charging and discharging of the load node.
- The **average power dissipation** recorded was approximately $P = 36.65\ \mu$W.

The second simulation (Voltage vs. Time plot) indicated that the output followed the input inversely, confirming the inverter's fundamental logic behavior. The delay measurements (10–60 ps) depended on the capacitive load and transistor drive strength.

Discussion and Conclusion

This experiment demonstrated the design and functional verification of a CMOS inverter at the transistor level using **MICROWIND**. The simulated results confirmed the theoretical operation of the inverter—producing a logical complement of the input signal with high voltage gain and full logic swing between 0 V and 1.2 V.

The addition of a load capacitor introduced visible rise and fall delays due to charging and discharging at the output node. This behavior matches the theoretical relation $t_r = 35 \times C_{out}$ ns, showing that delay increases with load capacitance. Moreover, current spikes in the waveform indicated short dynamic current flow during switching but negligible static power consumption when the state was stable.

The results validate the efficiency of CMOS technology, which provides high noise margin, low static power, and predictable switching performance. The experiment highlighted key factors—such as aspect ratio balancing, output loading, and transistor mobility—that influence the inverter's speed and reliability in VLSI design.

Reference

[1] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, Wiley-IEEE Press.
[2] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison-Wesley.
[3] S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, McGraw-Hill.
[4] MICROWIND and DSCH User Manuals, Microwind Inc.