Heaven's light is our guide

RAJSHAHI UNIVERSITY OF ENGINEERING AND TECHNOLOGY

Department Of Electrical & Computer Engineering

Course Title:

VLSI Design Sessional

Course Code:

ECE 4128

Submitted to:	Submitted by:
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RUET	ECE 2020-21

Experiment No. 1

Name of the Experiment

Implementation of CMOS Inverter.

Theory

A CMOS inverter is one of the most essential components in digital logic circuits, made up of a PMOS and an NMOS transistor arranged in a complementary fashion. The PMOS is connected to the supply voltage (VDD), while the NMOS is tied to ground. Both transistors share the same input (Vin), and the output is taken from the node between them. When the input is at logic 0 (low), the PMOS conducts and the NMOS remains off, producing a high (logic 1) output. In contrast, when the input is at logic 1 (high), the NMOS turns on, the PMOS switches off, and the output is pulled to logic 0. This complementary action minimizes static power dissipation, which is why CMOS technology is known for its high energy efficiency.

One key dynamic characteristic of CMOS inverters is the transition time, which includes the rise time (tr) and fall time (tf). These define how fast the output voltage changes in response to an input signal. Rise time is the duration for the output to move from about 10% to 90% of VDD, while fall time measures the transition from 90% down to 10% of VDD.

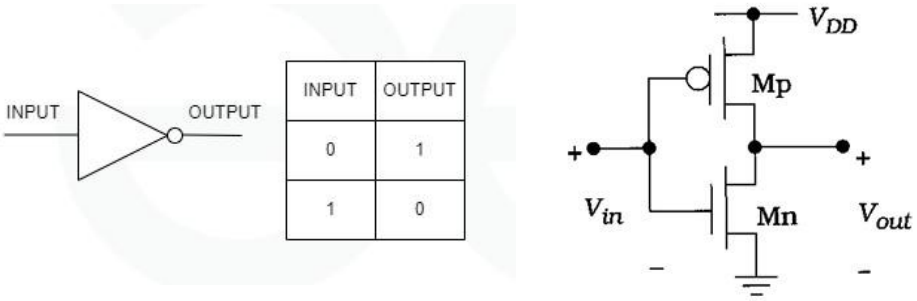

Figure 1: Schematic diagram of CMOS inverter.

The rise and fall times are influenced by the output load capacitance (Cout) and the transistor aspect ratios (W/L). Since PMOS transistors generally have lower carrier mobility (µp) compared to NMOS transistors (µn), the PMOS is typically designed wider—about twice the NMOS width—to balance the speed of rising and falling edges. This balance is achieved when:

$$\left(\frac{W_1}{L_1}\right) = \frac{\mu_p}{\mu_n}\left(\frac{W_2}{L_2}\right)$$

where T1 represents the NMOS and T2 represents the PMOS. This relationship ensures symmetrical switching times.

The propagation delay caused by the output capacitance can be estimated as:

$$t_r = t_f = \frac{35 \cdot C_{\text{out}}}{(W/L)_1} \text{ ns}$$

where Cout is in picofarads, and W_1/L_1 is the NMOS aspect ratio. This indicates that higher output capacitance or smaller transistor dimensions lead to slower transitions.

Required Tools

1. Microwind
2. MS Word

Circuit Diagram

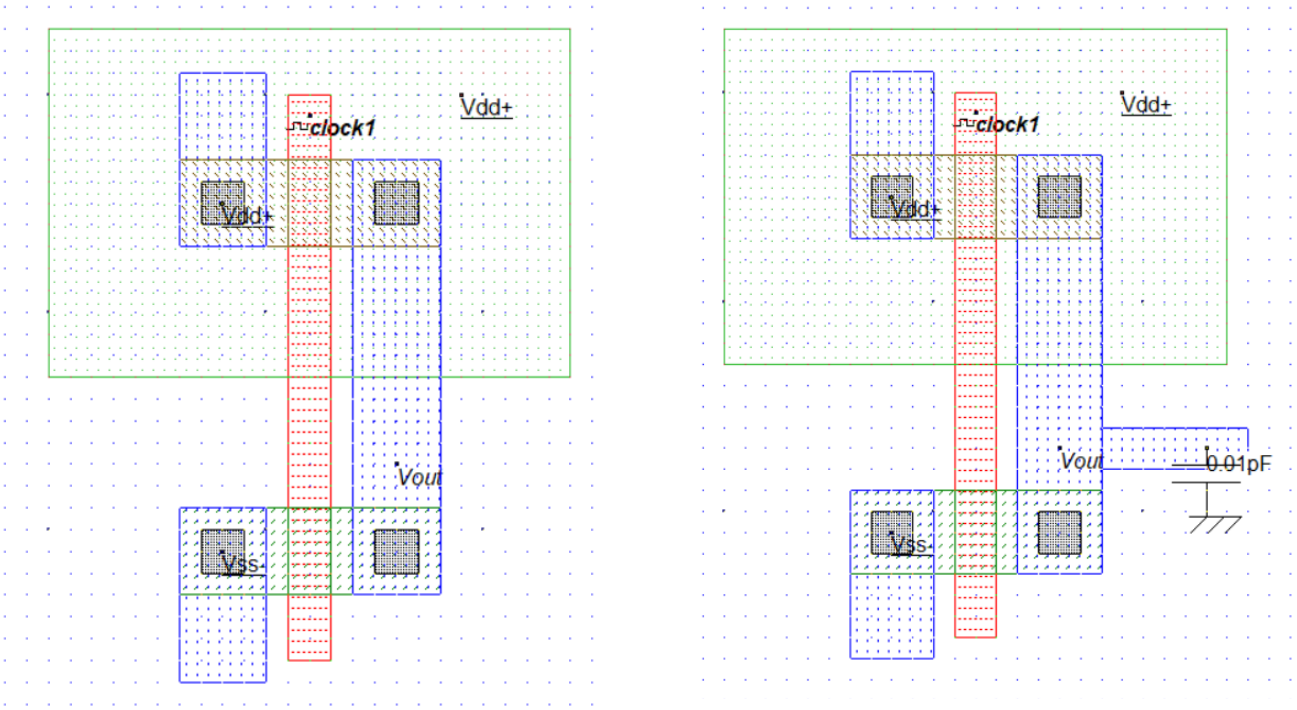

Figure 2: The CMOS inverter circuit with and without capacitor.

Output

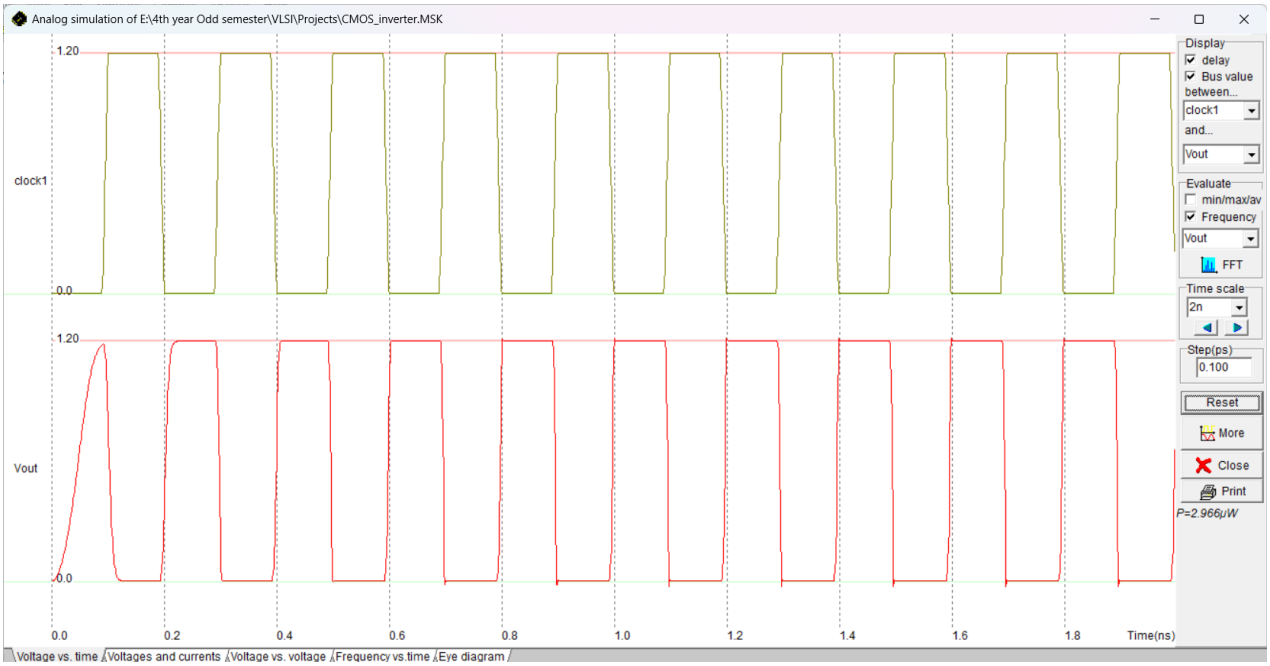

Figure 3: Voltage vs Time graph without capacitor.

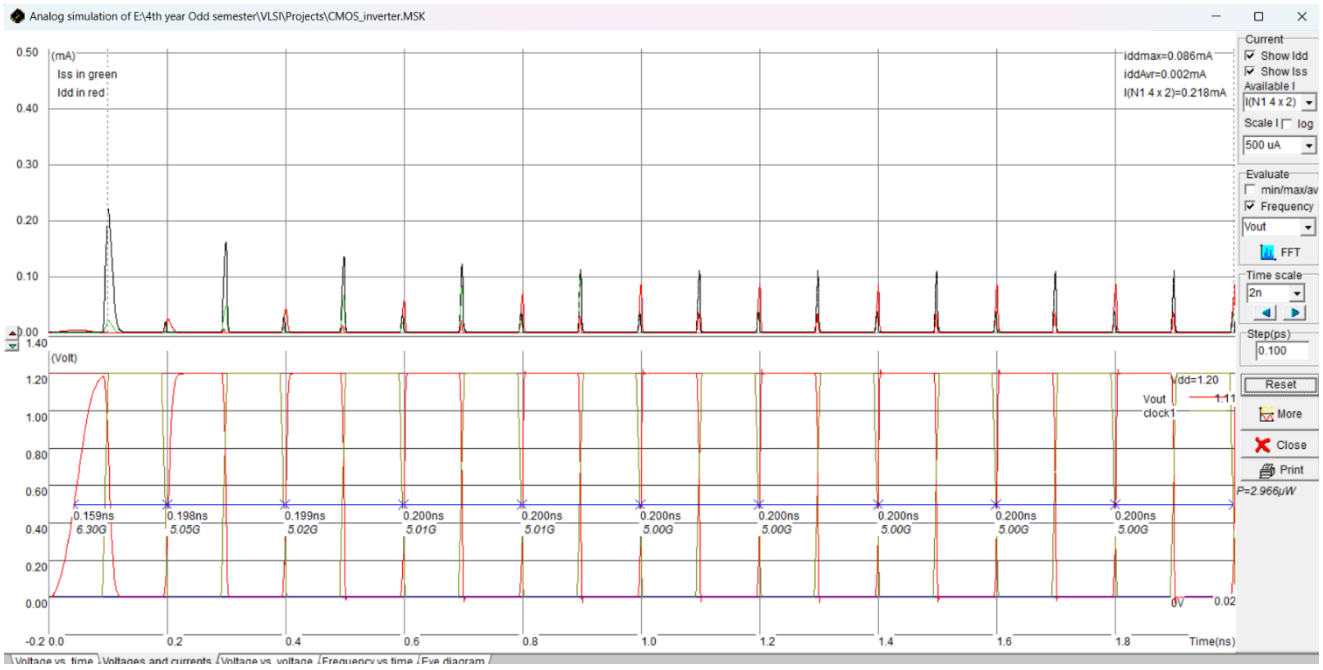

Figure 4: Voltage vs Current graph without capacitor.

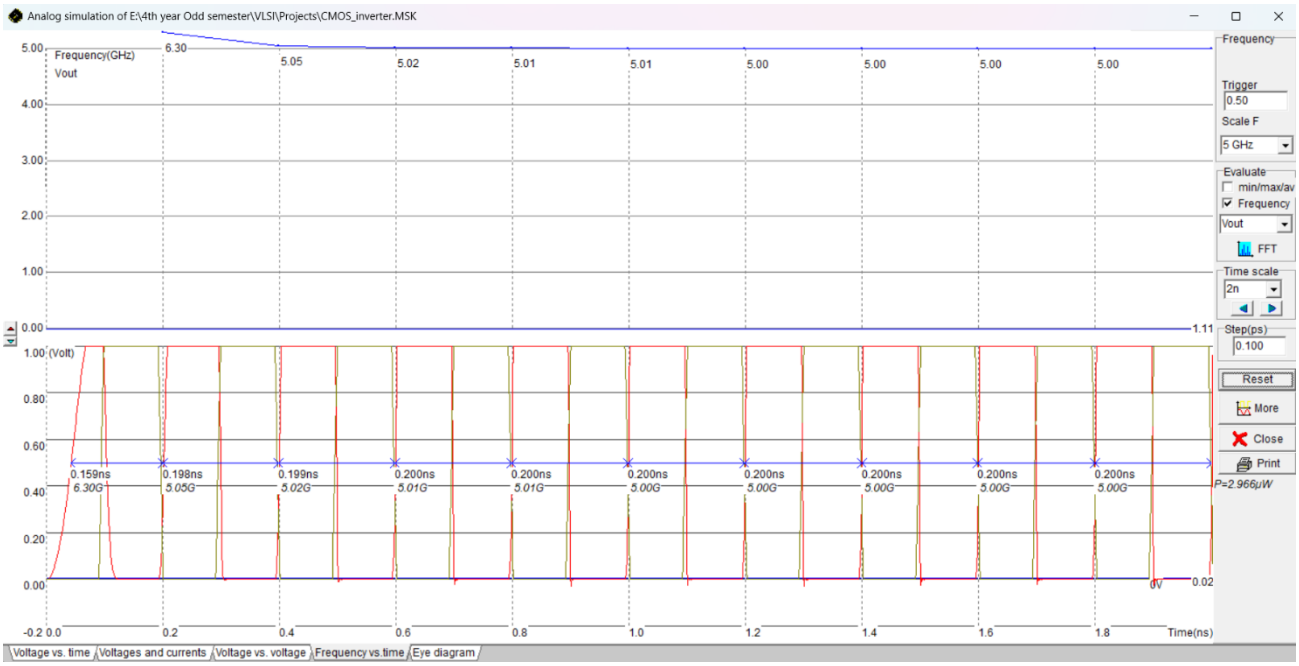

Figure 5: Frequency vs Time graph without capacitor.

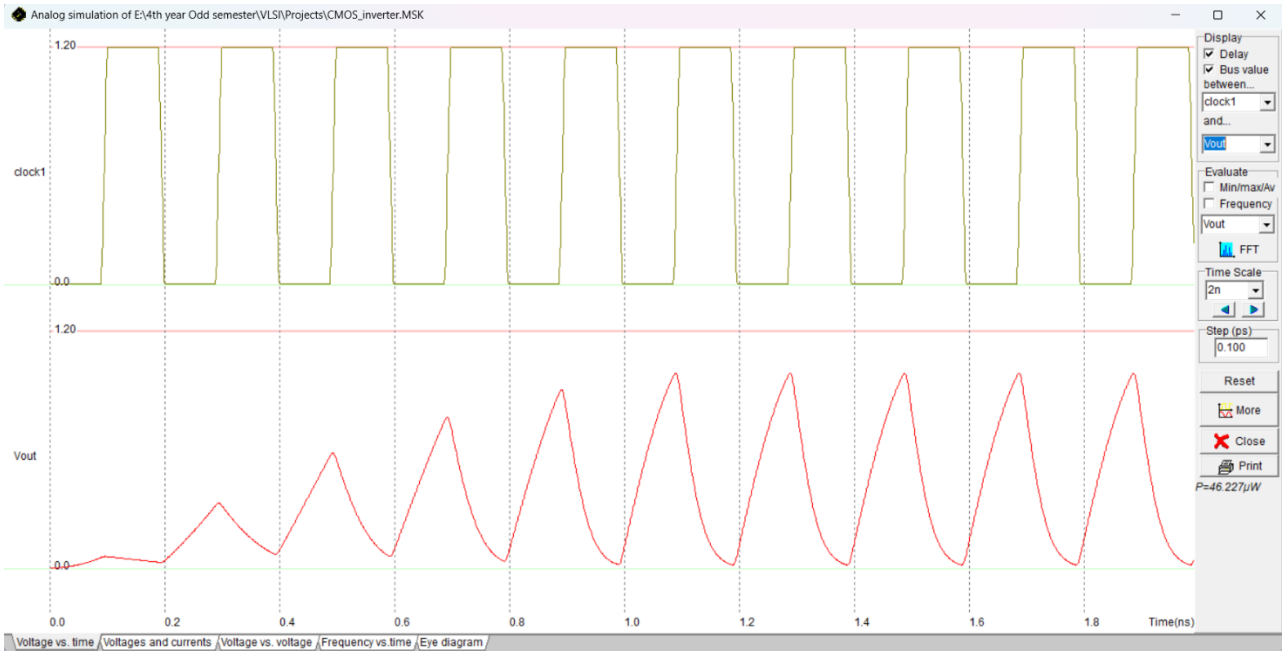

Figure 6: Voltage vs Time graph with capacitor.

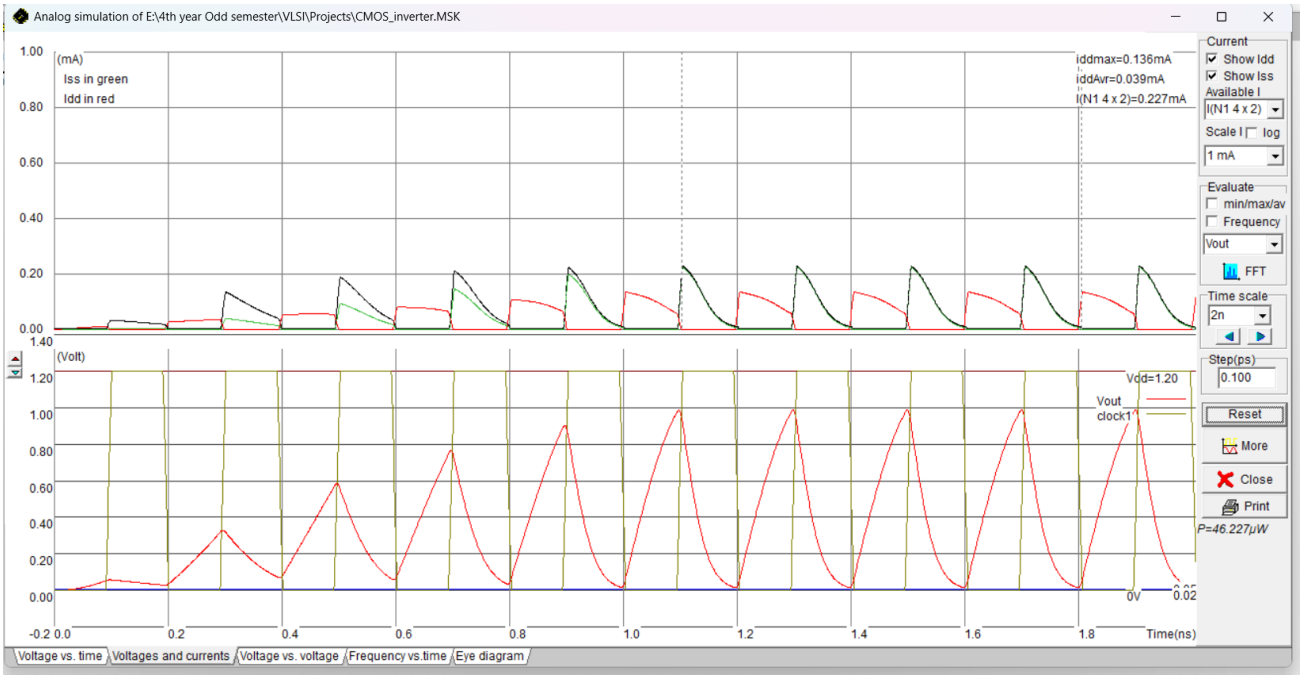

Figure 7: Voltage vs Current graph with capacitor.

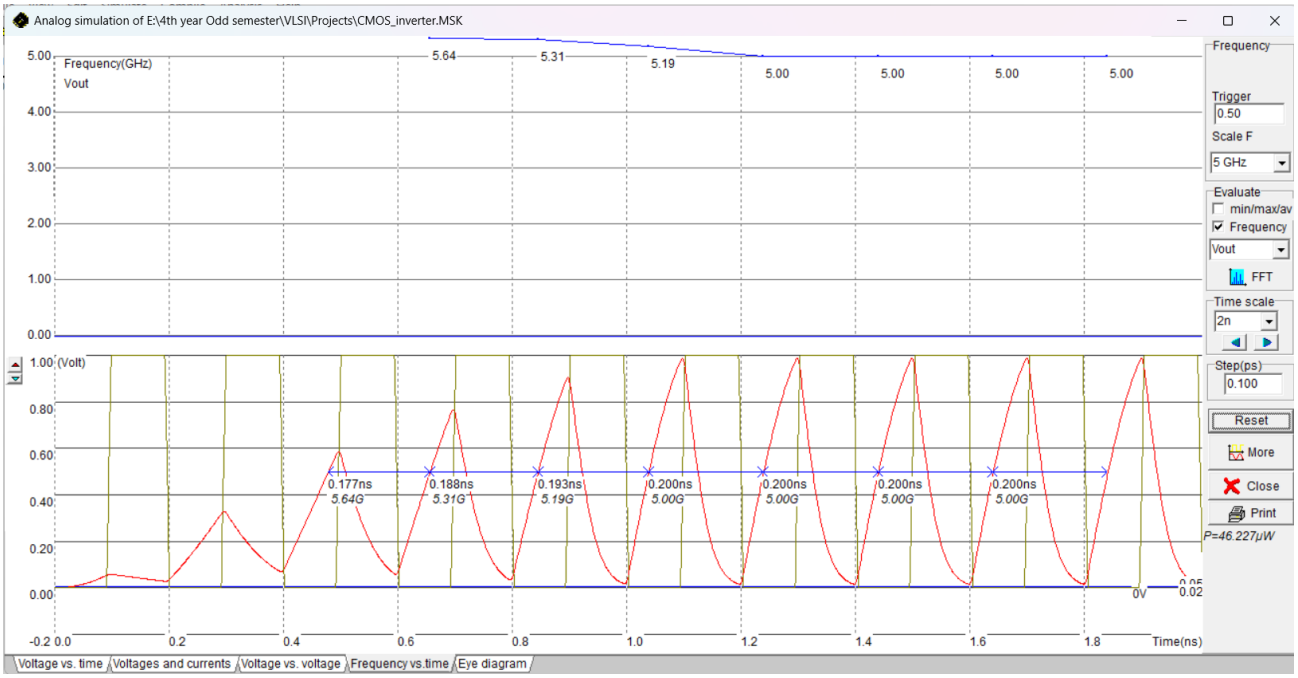

Figure 8: Frequency vs Time graph with capacitor.

Discussion and Conclusion

In this work, a CMOS inverter was designed and simulated in Microwind to study its switching characteristics under a clocked input alternating between 0 V and 1.2 V. The simulations confirmed the inverter's fundamental operation, where the output consistently produced the logical complement of the input. Waveform observations—covering voltage vs. time, current vs. voltage, and frequency vs. time—were carried out for cases with and without an output capacitive load.

Introducing a load capacitor revealed distinct rise and fall times, attributed to the charging and discharging of the output node, as described by the relation tr=35·Coutns. Without the capacitor, transitions were sharp and nearly ideal; with the capacitor, slight delays and current spikes became evident. These behaviors align with theoretical principles of CMOS design, particularly the influence of load capacitance and the importance of balancing transistor sizing to compensate for PMOS–NMOS mobility differences. Proper adjustment of aspect ratios ensured symmetrical rise and fall edges, improving timing performance.

Overall, the experiment validated both theoretical and practical aspects of CMOS inverter behavior. It demonstrated how dynamic parameters—such as load capacitance, transistor aspect ratio, and carrier mobility—directly affect propagation delay, switching speed, and power characteristics. This study not only confirmed expected inverter functionality but also emphasized design considerations crucial for efficient and reliable VLSI implementation.

Reference

[1] GeeksforGeeks," [Online]. Available: https://www.geeksforgeeks.org/electronicsengineering/cmos-inverter/. [Accessed 10 August 2025].

[2] "L. E. Brackenbury, Design of VLSI Systems - A Practical Introduction, Macmillan Education Ltd..