

## Exp No.: 05

### Name of the Experiment:

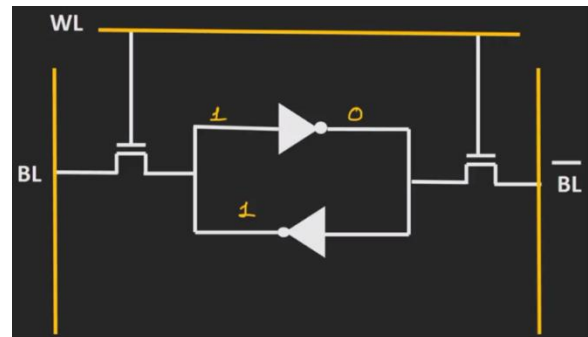
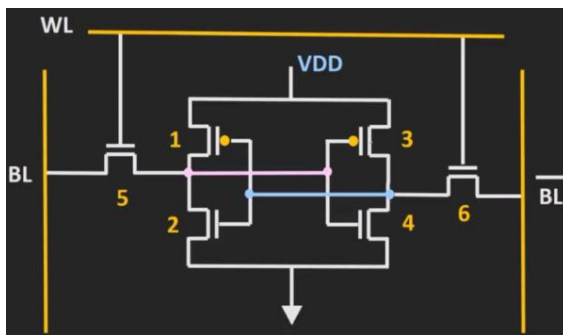
Simulation of 1-bit 6T SRAM Using MICROWIND

### Theory

A **6T SRAM (Six-Transistor Static Random Access Memory)** cell is a bistable storage element capable of storing a single bit of data indefinitely if power is supplied. Unlike DRAM, it does not require periodic refreshing because the data is retained by cross-coupled feedback inverters.

### Internal Structure

The 6T SRAM cell consists of six MOSFETs — four transistors form **two cross-coupled CMOS inverters**, and two additional **access (pass) transistors** control connectivity between the cell and the **bit lines (BL and  $\overline{BL}$ )**.



- **Transistors M1 & M2:** form the first CMOS inverter.
- **Transistors M3 & M4:** form the second CMOS inverter.
- **Transistors M5 & M6:** act as **access transistors**, controlled by the **word line (WL)**, enabling read and write operations through the bit lines.

The **two stable nodes** usually denoted  $Q$  and  $\bar{Q}$ , store complementary voltage levels — one representing logic '1' and the other logic '0'.

The feedback connection between these inverters ensures that the state of one inverter reinforces the opposite state in the other, maintaining bi-stability without refresh cycles. Thus, the term “**static**” is used in contrast to DRAM, which needs refresh operations.

### Working Principle

When power is supplied, the cross-coupled inverters maintain one of two stable states:

$$(Q, \bar{Q}) = (1,0) \text{ or } (0,1)$$

The access transistors (M5, M6) connect these nodes to the bit lines when the word line (WL) is asserted high, allowing data transfer during read or write operations.

## 1. Write Operation

To write a bit into the SRAM cell:

1. The **word line (WL)** is activated high, turning **M5** and **M6** ON.
2. The **bit lines (BL and  $\overline{BL}$ )** are driven externally with the data to be stored (e.g., BL = 1,  $\overline{BL}$  = 0 for writing logic 1).
3. The corresponding inverter pair flips to store the desired logic value at  $Q$  and  $\bar{Q}$ .
4. After writing, the **WL** is deactivated (LOW), isolating the cell and preserving the stored value.

The **strong feedback** of the inverter pair maintains the written value even after WL is deactivated.

## 2. Read Operation

During read:

1. Both **bit lines (BL and  $\overline{BL}$ )** are **pre-charged** to logic HIGH.
2. The **word line (WL)** is activated high, enabling the access transistors.
3. Depending on the stored bit, a small voltage difference appears between BL and  $\overline{BL}$  :
  - If  $Q = 1$ , BL remains high,  $\overline{BL}$  slightly drops.
  - If  $Q = 0$ , BL drops,  $\overline{BL}$  remains high.
4. A **sense amplifier** detects this differential voltage and outputs the stored data.

The read process must be designed so that it **does not disturb** the cell's stored value — a critical factor in SRAM stability.

## 3. Static Operation (No Refresh Needed)

Since the 6T SRAM cell retains data as long as power is supplied through the feedback loop of cross-coupled inverters, it does **not require refresh cycles** like DRAM. Hence, it is more power-efficient during idle states and provides faster access times.

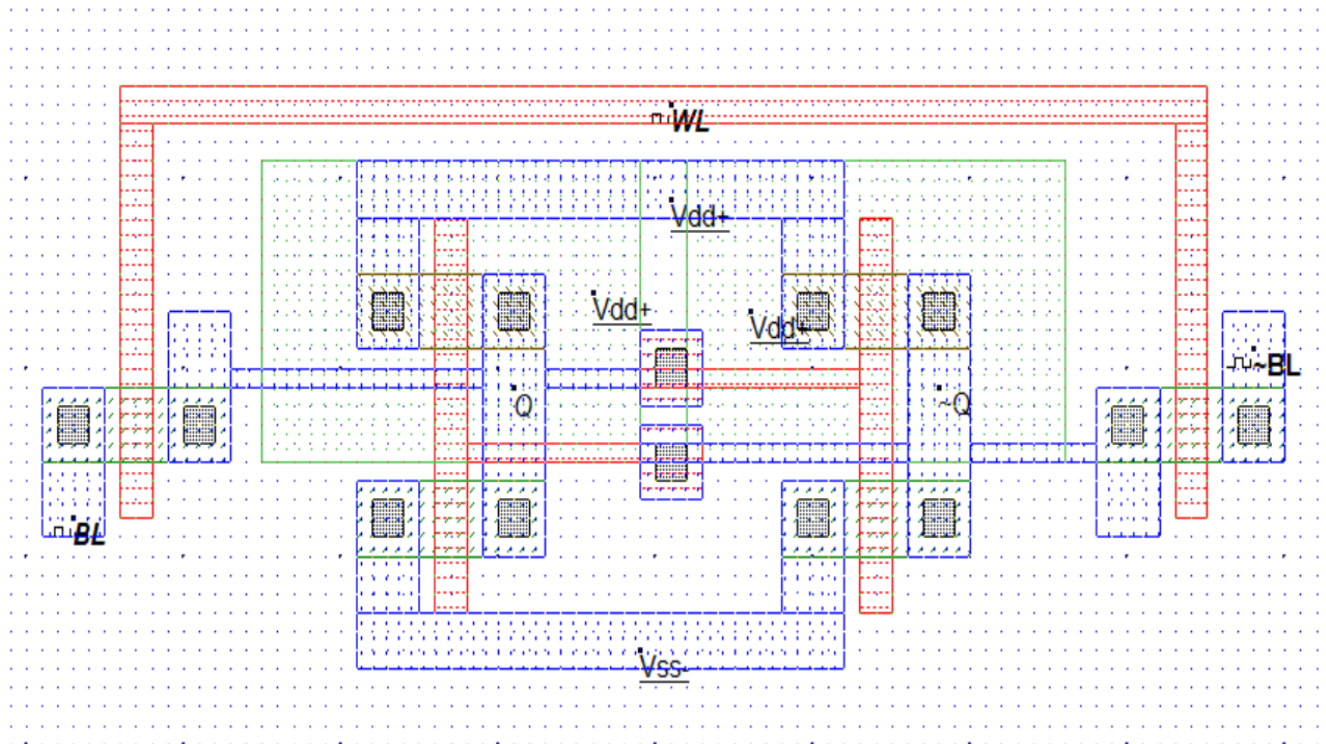
## Comparison: SRAM vs DRAM

Feature	SRAM	DRAM
Storage Element	6 Transistor Flip-Flop	1 Transistor + 1 Capacitor
Refresh Cycle	Not required	Required
Speed	Faster	Slower
Power Consumption	Higher during switching, negligible static	Moderate but periodic refresh
Density	Low	High
Cost per bit	Higher	Lower

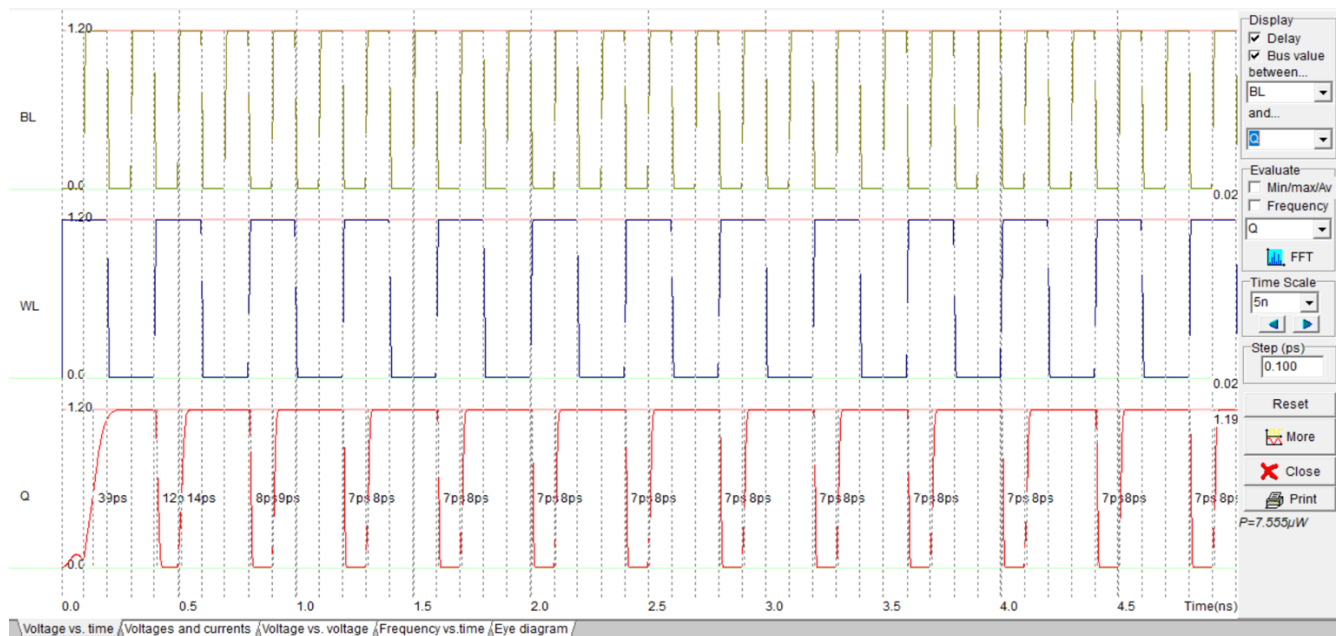
## Required Tools

- **MICROWIND** – for transistor-level layout and simulation
- **DSCH** – for logic schematic design (optional)
- **Word Processor** – for report preparation

## Circuit Diagram:



## Output:



## Results

The simulated 6T SRAM cell demonstrated correct **read and write** functionality. When BL and BL' were set according to the desired data and WL was asserted high, the cross-coupled inverters successfully latched the correct logic level. During the read phase, the voltage difference between BL and BL' corresponded accurately to the stored value.

The transient analysis in MICROWIND showed stable operation with no data loss after WL was deactivated, confirming static retention. The observed delay for switching was within a few picoseconds, and the power dissipation remained minimal except during bit transitions.

## Discussion & Conclusion

The experiment verified the working principle of a 1-bit 6T SRAM cell using MICROWIND simulation. The design maintained bistable states through cross-coupled inverters and demonstrated robust static operation without refresh. Simulation results confirmed reliable write and read cycles with proper differential sensing on BL and  $\overline{BL}$ . The cell provided fast response time and low dynamic power, illustrating the efficiency of CMOS-based static memory structures in VLSI design.

## References

1. Class Lecture Notes on SRAM Cell (Department of ECE, RUET).
2. R. Jacob Baker, *CMOS: Circuit Design, Layout, and Simulation*, Wiley-IEEE.
3. Neil H. E. Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison-Wesley.
4. MICROWIND/DSCH User Manuals, Microwind Inc.