Exp No.: 03

Name of the Experiment:

Design and Observation of CMOS Characteristics for **NAND** and **NOR** Gates

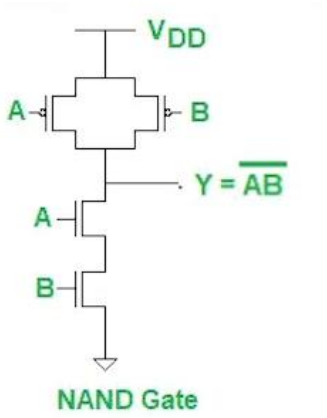
Theory

A CMOS logic gate is formed by a complementary pair of networks: a **pull-down network (PDN)** of nMOS devices that conducts for output 0, and a **pull-up network (PUN)** of pMOS devices that conducts for output 1. Series connections realize logical AND; parallel connections realize logical OR. The PUN is the dual of the PDN.

CMOS 2-input NAND

The Boolean function is

$$Y_{\text{NAND}} = \overline{A \cdot B}$$

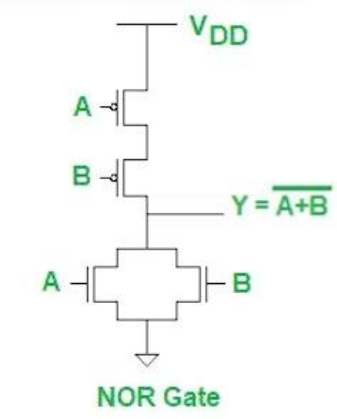


- **PDN (nMOS):** devices for A and B **in series** implement $A \cdot B$.
- **PUN (pMOS):** devices for A and B **in parallel** implement $\bar{A} + \bar{B}$. The output only falls when both inputs are high; for any other combination, at least one pMOS is on and the output is held high.

CMOS 2-input NOR

The Boolean function is

$$Y_{\text{NOR}} = \overline{A + B}$$



- **PDN (nMOS):** devices for $A$and B**in parallel** implement $A + B$.
- **PUN (pMOS):** devices for $A$and B**in series** implement $\bar{A} \cdot \bar{B}$. The output only rises when both inputs are low; otherwise at least one nMOS pulls it down.

Truth Tables

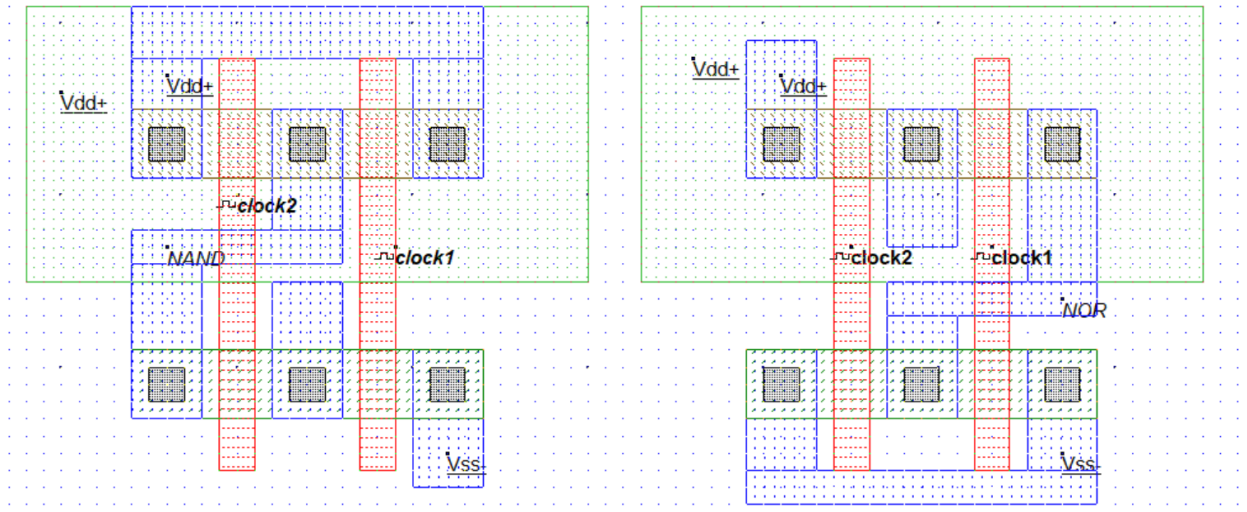
A	B	Y_{NAND}	Y_{NOR}
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

Key expectations include rail-to-rail swings, negligible static power, and propagation delay dominated by the longest conducting series path (NAND worst-case fall; NOR worst-case rise).

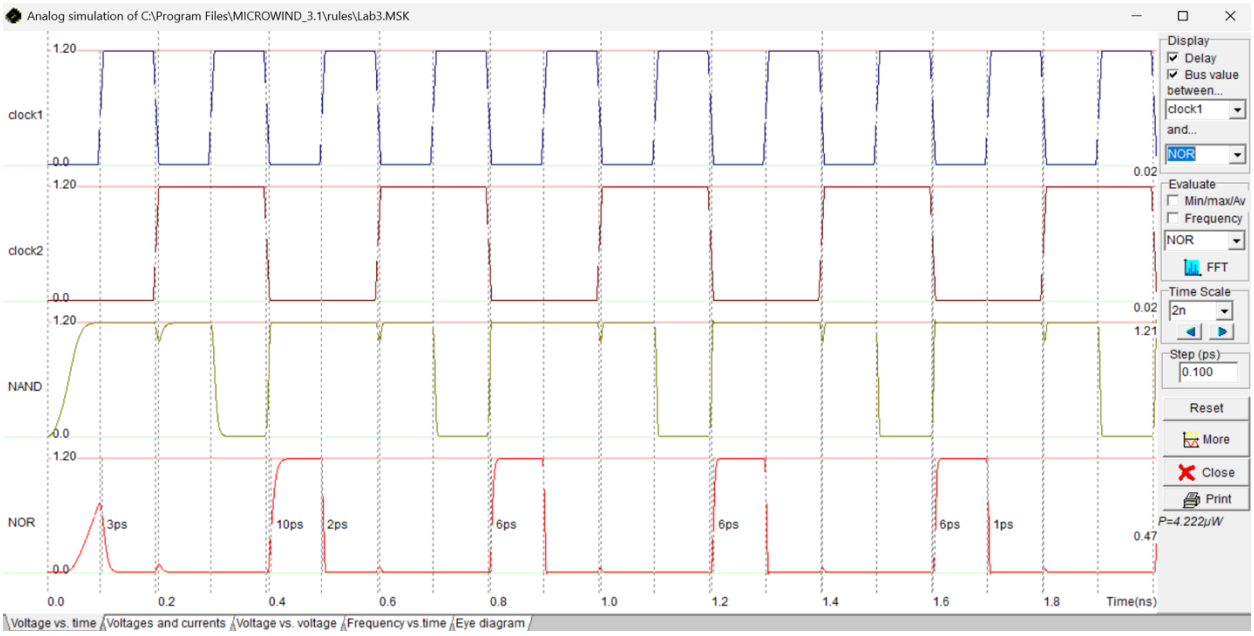
Required Tools

- **MICROWIND** – CMOS layout and analog simulation
- **DSCH** – schematic / logic capture (optional)
- **Word Processor** – documentation

Circuit Diagram



Output



Results

Inputs were driven by two clocks (**clock1**, **clock2**). The displayed supply rail was approximately **1.2 V**, time scale **2 ns/div**, and simulation **step = 0.1 ps**.

- **NAND output:** stayed high except when both inputs were high, when it transitioned low—consistent with $\overline{A \cdot B}$. Measured propagation-delay annotations on edges were around **3–10 ps** depending on direction and input vector ordering.
- **NOR output:** stayed low except when both inputs were low, when it transitioned high—consistent with $\overline{A + B}$. Delay markers indicated **~1–6 ps** on the shown events.
- The simulator's power readout indicated $P \approx 4.222\ \mu$Waverage under the applied toggling activity.

These observations match the theoretical truth tables and the dual series/parallel topology of CMOS NAND/NOR.

Discussion & Conclusion

The NAND and NOR gates were realized with complementary CMOS pull-up and pull-down networks and verified in transient simulation. The outputs exhibited correct logic behavior with rail-to-rail levels, while measured delays (≈1–10 ps) reflected the expected dependence on transistor stacking: the NAND's worst-case fall delay was larger due to series nMOS, and the NOR's worst-case rise delay was larger due to series pMOS. The reported average power of about 4.2 μWconfirmed low dynamic consumption and negligible static current. Hence, the CMOS implementations satisfied functional correctness and demonstrated characteristic delay asymmetries inherent to NAND/NOR structures.

References

1. R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, Wiley-IEEE.
2. N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison-Wesley.
3. MICROWIND/DSCH User Manuals, Microwind Inc.