

## Exp No.: 04

### Name of the Experiment:

Design and Observation of CMOS Circuit Characteristics for

$$Y_1 = (A + \bar{B})C, Y_2 = A\bar{B} + ABC$$

### Theory

CMOS logic implements Boolean expressions by forming dual pull-up (pMOS) and pull-down (nMOS) networks. The nMOS network conducts for logic '0' outputs, and the pMOS network conducts for logic '1'. Series-connected transistors represent logical AND, and parallel connections represent logical OR. The pMOS network is always the dual of the nMOS structure.

**For  $Y_1 = (A + \bar{B})C$ :**

Applying De Morgan's law,

$$Y_1 = (A + \bar{B}) + \bar{C} = (\bar{A} \cdot \bar{B}) + \bar{C}.$$

Hence, the nMOS pull-down network corresponds to the term  $(A + B)C$  (an OR followed by AND), while the pMOS pull-up network is its dual, implementing  $(\bar{A} \cdot \bar{B}) + \bar{C}$ .

**For  $Y_2 = A\bar{B} + ABC$ :**

Factoring out A,

$$Y_2 = A(\bar{B} + BC).$$

Using the identity  $X + YZ = (X + Y)(X + Z)$  with  $X = \bar{B}$ ,  $Y = B$ , and  $Z = C$ ,

$$\bar{B} + BC = (\bar{B} + B)(\bar{B} + C) = 1 \cdot (\bar{B} + C) = \bar{B} + C.$$

Thus,

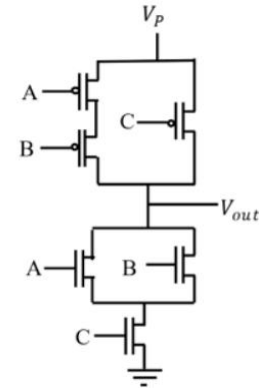
$$Y_2 = A(\bar{B} + C).$$

The nMOS network therefore consists of a series device for A feeding a parallel branch for  $\bar{B}$  and C; the pMOS network is its dual.

For each logic equation, the corresponding CMOS transistor arrangements are summarized as follows:

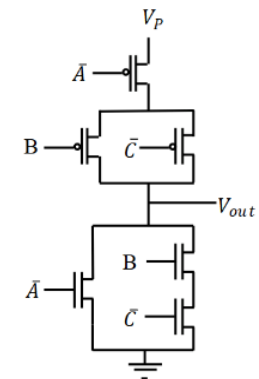
1. For  $\overline{(A + B)C}$  :

- **nMOS Network (Pull-Down):**
  - A and B are connected **in parallel** to realize  $(A + B)$ .
  - This parallel combination is connected **in series** with C, implementing  $(A + B)C$ .
- **pMOS Network (Pull-Up):**
  - A and B are connected **in series** to realize  $(\bar{A} \cdot \bar{B})$ .
  - This series path is connected **in parallel** with a single pMOS transistor for  $\bar{C}$ .



2. For  $Y_2 = A(\bar{B} + C)$ :

- **nMOS Network (Pull-Down):**
  - A transistor for A is placed **in series** with a parallel branch of two transistors representing  $\bar{B}$  and C.
  - This forms  $A(\bar{B} + C)$ .
- **pMOS Network (Pull-Up):**
  - A transistor for A is placed **in parallel** with a series combination of B and  $\bar{C}$ , realizing the dual structure.



These configurations ensure complementary switching, minimal static current, and correct logic inversion for all input combinations.

### Truth Table

A	B	C	$(A + \bar{B})C$	$A(\bar{B} + C)$
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1

## Required Tools

- **MICROWIND** – for CMOS layout design and simulation
- **DSCH** – for schematic verification (optional)
- **Word Processor** – for documentation and report preparation

## Circuit Diagram

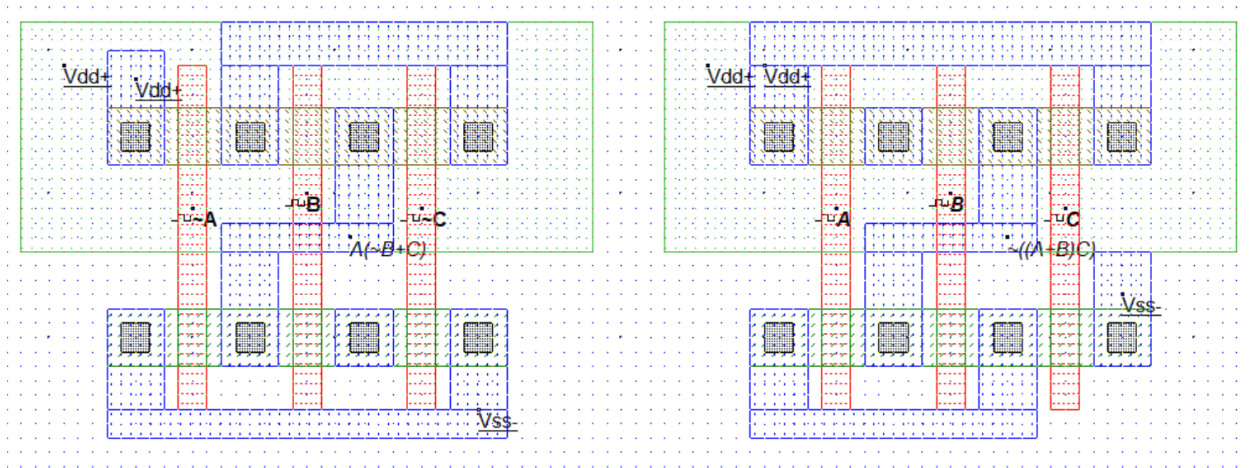


Figure 1: The Circuit Diagram of both equation

## Output

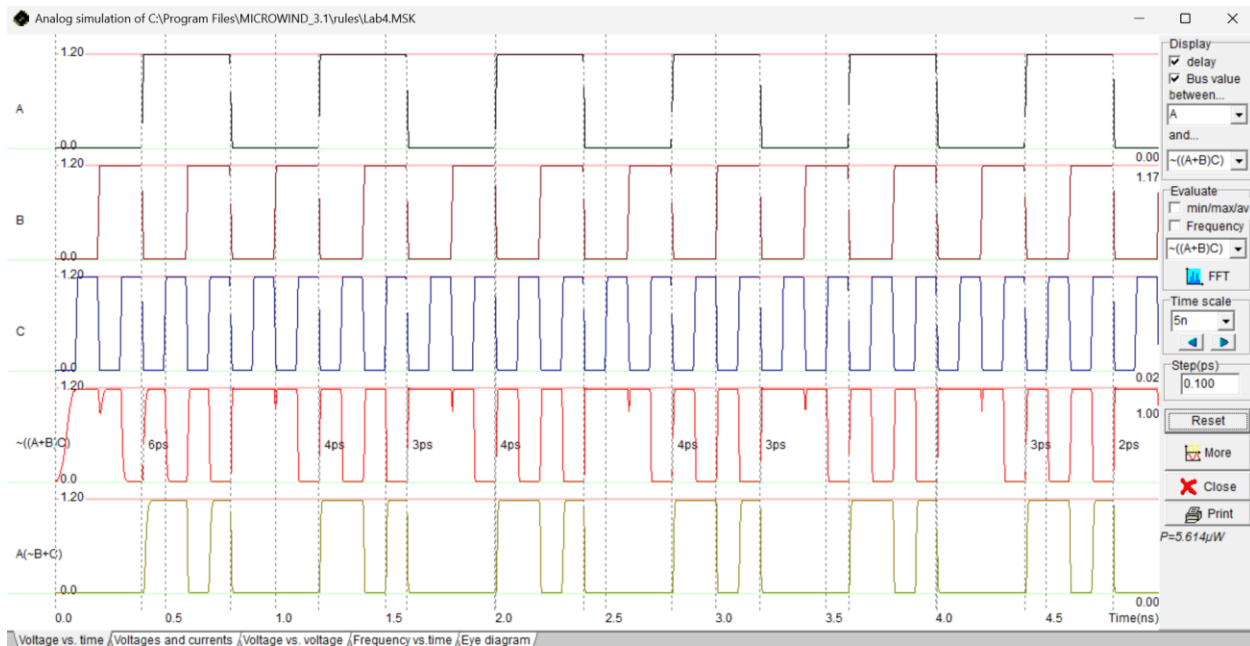


Figure 2: Output of both equations

## Results

The MICROWIND simulation confirms that both circuits perform according to their logical definitions.

- For  $Y_1 = (A + \bar{B})C$ , the output remains at logic high when  $C = 0$ , and transitions to logic low when  $C = 1$  and either  $A$  or  $B$  is high, consistent with the truth table.
- For  $Y_2 = A(\bar{B} + C)$ , the output transitions to logic high whenever  $A = 1$  and either  $B = 0$  or  $C = 1$ , verifying the correctness of the simplification.

Observed propagation delays ranged from **2 ps – 6 ps**, indicating high-speed switching. The simulation reported an average power dissipation of approximately,  $5.614\mu\text{W}$  consistent with expected CMOS dynamic power behavior.

## Discussion & Conclusion

Both CMOS circuits were successfully implemented and simulated according to the given Boolean equations. Logical correctness was verified from the simulated waveforms, and the timing results matched theoretical expectations. The experiment demonstrated how complex logic functions can be realized through systematic transformation of Boolean equations into CMOS transistor networks. The layouts achieved low power dissipation and symmetrical transition characteristics, confirming the efficiency of CMOS design methodology.

## References

1. S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, McGraw-Hill.
2. R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, Wiley-IEEE Press.
3. *MICROWIND and DSCH User Manuals*, Microwind Inc.