**Experiment No. 6**

**Experiment Name:** Implementation of Half Adder Circuit Using MICROWIND

**Theory:**

A **Half Adder** is one of the fundamental building blocks in digital arithmetic circuits. It performs the addition of two single-bit binary numbers and generates two outputs: **Sum (S)** and **Carry (C)**. The circuit does not account for any carry input; hence, it is termed a *Half Adder*.

If the two input bits are denoted by and , then the Boolean expressions for the outputs are:

Here, the **Sum** is obtained using an **Exclusive-OR (XOR)** function, and the **Carry** is produced by an **AND** function.

**Logic Representation**

| **A** | **B** | **SUM (S)** | **CARRY (C)** |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**CMOS Implementation**

The Half Adder can be realized using CMOS logic by combining the transistor-level layouts of **XOR** and **AND** gates.

* The **XOR circuit** is designed using a combination of NAND, NOR, and inverter structures to ensure correct logical toggling.
* The **AND circuit** is realized using a pair of series-connected nMOS transistors and parallel-connected pMOS transistors.

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**Working Principle:**

* When both inputs (A, B) are LOW → SUM = 0, CARRY = 0.
* When either input is HIGH → SUM = 1, CARRY = 0.
* When both inputs are HIGH → SUM = 0, CARRY = 1.

**Dynamic Characteristics:**  
The propagation delay is given by

where is the equivalent resistance of the conducting transistors and is the total load capacitance.

This delay increases with larger output capacitance or smaller transistor sizes. Proper aspect ratio selection () ensures fast switching and balanced rise/fall times.

**Required Tools:**

1. **MICROWIND 3.1** – for transistor-level layout and analog simulation
2. **DSCH 3.5** – for schematic entry and verification
3. **MS Word** – for documentation

**Circuit Diagram:**

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**Output:**

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**Result:**

The Half Adder circuit was successfully designed and simulated using **MICROWIND** with a supply voltage of **1.2 V**. The input signals and were driven by clock pulses, and the outputs (SUM and CARRY) were observed.

* The **SUM (S)** output matched the XOR logic, becoming HIGH only when one input was HIGH.
* The **CARRY (C)** output followed the AND logic, remaining HIGH only when both inputs were HIGH.
* The voltage transitions were sharp and consistent, showing correct logical behavior.
* The measured **propagation delay** was in the range of a few picoseconds (ps), confirming fast switching.
* The observed **average power consumption** was in the **micro-watt (µW)** range, consistent with low-power CMOS operation.

**Discussion and Conclusion:**

This experiment successfully implemented a **1-bit Half Adder circuit** using **CMOS technology** in MICROWIND. The design combined XOR and AND functionalities to produce the correct SUM and CARRY outputs according to the Half Adder truth table.

The simulation confirmed the expected operation, showing precise logical transitions, negligible static current, and stable voltage levels. The delay and power results validated CMOS advantages — low power, full voltage swing, and high noise margin.

Hence, this experiment demonstrated the transistor-level realization of a basic arithmetic unit, reinforcing fundamental principles of CMOS digital design and its role in VLSI circuit implementation.

**References:**

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