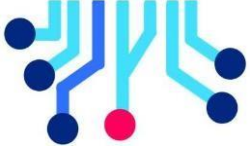
Digital Design Verification

Assignment # 02 – FIFO Layered Testbench

Release: 1.0

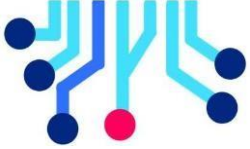
Date: 1-Aug-2024

NUST Chip Design Centre (NCDC), Islamabad, Pakistan



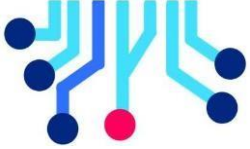
Revision History

Revision Number	Revision Date	Revision By	Nature of Revision	Approved By
1.0	01/08/2024	Qamar Moavia, M. Abdullah	Complete Assignment	-



Contents

Contents 2
Objective 3
Tools 3
Submission Instructions for Assignment 3
DUT Specification (Synchronous FIFO) 3
Task1: Creating Verification Plan for FIFO 4
Task 2: FIFO Verification 5



Objective

The objective of this assignment is

- To apply concepts learned in Labs to verify the provided FIFO designs.

Tools

- SystemVerilog
- Cadence Xcelium

Submission Instructions for Assignment

Submit Verification plan and all the layered testbench files. Make sure all the components and classes are in separate files.

DUT Specification (Synchronous FIFO)

Read the specification first and then follow the instructions to fully verify all the provided FIFO designs.

1. Introduction

Let's first specify the design and operation of a Synchronous FIFO memory. A Synchronous FIFO is a type of memory buffer used to store data temporarily while transferring it between two systems or processes that operate at the same clock frequency.

2. Key Features

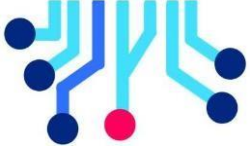
- **Data Width:** Configurable (8-bit, 16-bit, 32-bit, etc.)
- **FIFO Depth:** Configurable (16, 32, 64, 128, etc.)
- **Synchronous Operation:** All operations are synchronized with the clock signal.
- **Flags:** Full, Empty.
- **Reset:** Asynchronous reset to initialize the FIFO.

3. Functional Description

The FIFO memory consists of a series of registers organized in a circular buffer. Data is written into the FIFO via the write interface and read from the FIFO via the read interface. The FIFO operates synchronously, with all operations occurring on the rising edge of the clock signal.

4. Interface Signals

Signal Name	Direction	Width	Description
clk	Input	1	Clock signal
rst_n	Input	1	Asynchronous reset (active low)
wr_en	Input	1	Write enable
rd_en	Input	1	Read enable
data_in	Input	DATA_WIDTH	Data input is parametrized
data_out	Output	DATA_WIDTH	Data output is parametrized
full	Output	1	Full flag (indicates FIFO is full)
empty	Output	1	Empty flag (indicates FIFO is empty)



5. Operations

Reset Operation
FIFO is reset asynchronously whenever the rst_n signal transitions from high to low. On reset fifo will become empty indicated by high empty flag. Data_out can have any value on the reset.

Write Operation
Data is written into the FIFO on the rising edge of the clock when wr_en is asserted high and the FIFO is not full (full is low).

Read Operation
Data is read from the FIFO on the rising edge of the clock when rd_en is asserted high and the FIFO is not empty (empty is low).
Note: Both Write and Read Operation can be performed on FIFO at the same time.

6. Flag Descriptions

Full Flag (full)
The full flag is asserted (set to high) when the FIFO is full. Once this flag is set, FIFO write operation will be disabled. The flag will only be deserted (set to low) when data is read from the FIFO through fifo read operation or the reset operation occurs.

Empty Flag (empty)
The empty flag is asserted (set to high) when the FIFO is empty. Once this flag is set, FIFO read operation will be disabled. The flag will only be deserted (set to low) only when data is written to the FIFO through fifo write operation.

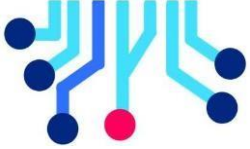
7. Configurable Parameters

Parameter	Description	Default Value
DATA_WIDTH	Width of the data bus	8
DEPTH	Depth of the FIFO	8

Task1: Creating Verification Plan for FIFO

1. Understand the FIFO functionality first through specifications mentioned above.
2. Create a detailed verification plan by stating objectives, listing features to verify, outlining specific test cases, and specifying whether the stimulus will be random or directed.
   Example Feature: Full Flag
   Test Cases:
   - Fill the FIFO to its maximum capacity and check if the full flag is asserted.
   - Add one more item to the full FIFO and ensure no data is written and the full flag remains asserted.
   - Read one item from the full FIFO and verify the full flag is de-asserted.

   Stimulus: Directed tests with specific data patterns.
3. Add coverage goals in the verification plan by defining what needs to be covered (e.g., all possible states, transitions, boundary conditions), create coverage bins by categorizing different scenarios and conditions that need to be tested, and include assertions for key properties to ensure thorough validation.



Task 2: FIFO Verification

1. Follow verification plan to create a Layered Testbench Environment to Verify the FIFO Design.
2. Execute the verification plan by creating test cases mentioned in the plan. As your environment is already set, you will only be modifying the Generator code in this subtask.
3. Verify the FIFO with at least three different parameter configurations (e.g., different DEPTH and DATA_WIDTH values).
4. Run the simulation with the provided design file **fifo.sv**.
5. Debug as needed until you are happy that design is verified.
6. In case of any error or assertion failure clearly mention that in the comment section of verification plan. Additionally, attach the waveform and provide a detailed error description.
7. Finally add the Complete Coverage report in the verification plan.