Lab # 43 Report
Register Level Modeling

Github: https://github.com/imranAlVLSI/Lab-43-Register-Level-Modeling

Task 1: Generation

Understand the basic registers model description such as register block name, it address, register name, access policy, registers sub-fields register size etc, from the given yapp_router_regs.xml file.

Q: What is the access policy of the control register (ctrl_reg)?

A: ____RW_____

Q: What is the access policy of the address 0 register (addr0_cnt_reg)?

A: ____RO_____

Using cadence reg_verifier tool generated a register model with following arguments

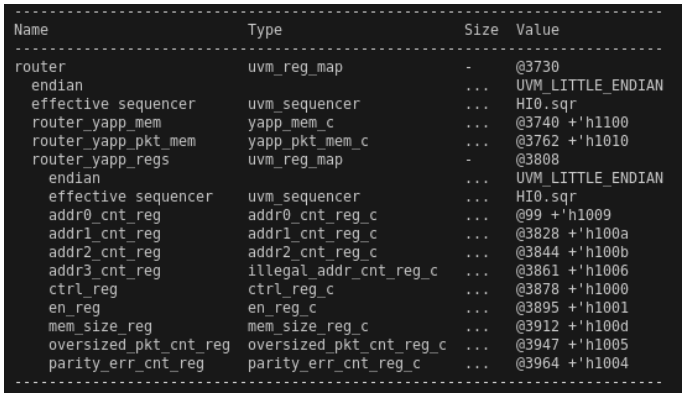
reg_verifier

-domain uvmreg	Create a UVM register model
-top yapp_router_regs.xml	Input IP-XACT file
-dut yapp_router_regs	Top component name in IP-XACT file
-out_file yapp_router_regs	Output filename
-quicktest	Generate quick test
-cov	Generate coverage code
-pkg yapp_router_reg_pkg	Package name

Cadence reg_verifier tool generated the following files

Yapp_router_regs_config.dat	Configuration information
yapp_router_regs_hdlpaths.dat	Path information for backddoor access
Yapp_router_regs_rdb.sv	Register Model
Cdns_uvmreg_utils_pkg.sv	Cadence utility package
quicktest.sv	UVM test to verify model

Generated quicktest can be used to create, print and reset the register model. After modification of qt_test run_phase and placing the model.print() after the model.reset() and adding model.default.print after this, printing the address map of HBUS interface using run_test



```
----------------------------------------------------------------------------
Name                      Type                    Size  Value
----------------------------------------------------------------------------
router                    uvm_reg_map             -     @3730
  endian                                          ...   UVM_LITTLE_ENDIAN
  effective sequencer     uvm_sequencer           ...   HI0.sqr
  router_yapp_mem         yapp_mem_c              ...   @3740 +'h1100
  router_yapp_pkt_mem     yapp_pkt_mem_c          ...   @3762 +'h1010
  router_yapp_regs        uvm_reg_map             -     @3808
    endian                                        ...   UVM_LITTLE_ENDIAN
    effective sequencer   uvm_sequencer           ...   HI0.sqr
    addr0_cnt_reg         addr0_cnt_reg_c         ...   @99 +'h1009
    addr1_cnt_reg         addr1_cnt_reg_c         ...   @3828 +'h100a
    addr2_cnt_reg         addr2_cnt_reg_c         ...   @3844 +'h100b
    addr3_cnt_reg         illegal_addr_cnt_reg_c  ...   @3861 +'h1006
    ctrl_reg              ctrl_reg_c              ...   @3878 +'h1000
    en_reg                en_reg_c                ...   @3895 +'h1001
    mem_size_reg          mem_size_reg_c          ...   @3912 +'h100d
    oversized_pkt_cnt_reg oversized_pkt_cnt_reg_c ...   @3947 +'h1005
    parity_err_cnt_reg    parity_err_cnt_reg_c    ...   @3964 +'h1004
----------------------------------------------------------------------------
```

Hierarchy of Register Block(router_yapp_regs)

```
data:"'{kind:UVM_READ, addr:'h1004, data:'h0, n_bits:8, byte_en:'hff, status:UVM_IS_OK}"
UVM_INFO ./quicktest.sv(35) @ 265: HI0.drv [DRV] sending item complete
----------------------------------------------------------------------------------------------------------------------------------------------------------------
Name                                Type                                                                                Size  Value
----------------------------------------------------------------------------------------------------------------------------------------------------------------
model                               yapp_router_regs_vendor_Cadence_Design_Systems_library_Yapp_Registers_version_1_5   -     @3717
  router_yapp_regs                  yapp_regs_c                                                                         -     @3783
    addr0_cnt_reg                   addr0_cnt_reg_c                                                                     -     @99
      non_reserved_auto_added_field uvm_reg_field                                                                       ...    RO addr0_cnt_reg[7:0]=8'h00
    addr1_cnt_reg                   addr1_cnt_reg_c                                                                     -     @3828
      non_reserved_auto_added_field uvm_reg_field                                                                       ...    RO addr1_cnt_reg[7:0]=8'h00
    addr2_cnt_reg                   addr2_cnt_reg_c                                                                     -     @3844
      non_reserved_auto_added_field uvm_reg_field                                                                       ...    RO addr2_cnt_reg[7:0]=8'h00
    addr3_cnt_reg                   illegal_addr_cnt_reg_c                                                              -     @3861
      non_reserved_auto_added_field uvm_reg_field                                                                       ...    RO addr3_cnt_reg[7:0]=8'h00
    ctrl_reg                        ctrl_reg_c                                                                          -     @3878
      plen                          uvm_reg_field                                                                       ...    RW ctrl_reg[5:0]=6'h3f
    en_reg                          en_reg_c                                                                            -     @3895
      router_en                     uvm_reg_field                                                                       ...    RW en_reg[0:0]=1'h1
      parity_err_cnt_en             uvm_reg_field                                                                       ...    RW en_reg[1:1]=1'h0
      oversized_pkt_cnt_en          uvm_reg_field                                                                       ...    RW en_reg[2:2]=1'h0
      addr0_cnt_en                  uvm_reg_field                                                                       ...    RW en_reg[4:4]=1'h0
      addr1_cnt_en                  uvm_reg_field                                                                       ...    RW en_reg[5:5]=1'h0
      addr2_cnt_en                  uvm_reg_field                                                                       ...    RW en_reg[6:6]=1'h0
      addr3_cnt_en                  uvm_reg_field                                                                       ...    RW en_reg[7:7]=1'h0
    mem_size_reg                    mem_size_reg_c                                                                      -     @3912
      non_reserved_auto_added_field uvm_reg_field                                                                       ...    RO mem_size_reg[7:0]=8'h00
    oversized_pkt_cnt_reg           oversized_pkt_cnt_reg_c                                                             -     @3947
      non_reserved_auto_added_field uvm_reg_field                                                                       ...    RO oversized_pkt_cnt_reg[7:0]=8'h00
    parity_err_cnt_reg              parity_err_cnt_reg_c                                                                -     @3964
      non_reserved_auto_added_field uvm_reg_field                                                                       ...    RO parity_err_cnt_reg[7:0]=8'h00
  router_yapp_mem                   yapp_mem_c                                                                          -     @3740
    n_bits                          integral                                                                            32    'd8
    size                            integral                                                                            32    'd256
  router_yapp_pkt_mem               yapp_pkt_mem_c                                                                      -     @3762
    n_bits                          integral                                                                            32    'd8
    size                            integral                                                                            32    'd64
    router                          uvm_reg_map                                                                         0     id=@3730 seqr=HI0.sqr offset=0x0 size=0x1200 baseaddr=0x0
      router_yapp_regs              uvm_reg_map                                                                         0     id=@3808 seqr=HI0.sqr offset=0x1000 size=0x5 baseaddr=0x1000
----------------------------------------------------------------------------------------------------------------------------------------------------------------
```

Q: What is the reset value of the plen field of ctrl_reg?
A: 63
What is the size of the yapp_pkt_mem?
A: 32
What is the access policy of addr3_cnt_reg?
A: Read_Only
Q: What is the address of mem_size_reg?
A: 0x100d
Q: What is the starting address of the packet memory?
A: 0x1010

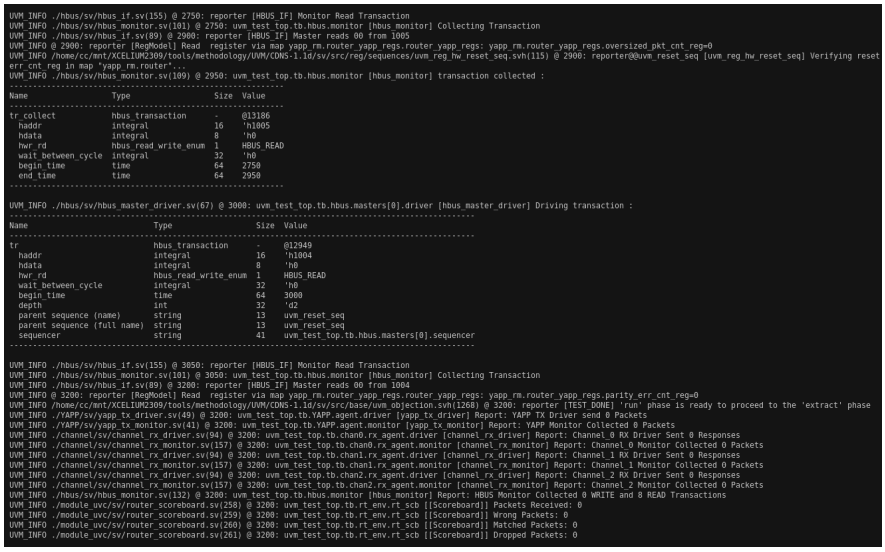
Task 2: Integration

Added register model files generated by the Cadence reg_verifier into the module_uvc/tb directory. Created the handles for the register model and adapter in the main testbench and constructed configured and locked the configuration of register model in the build_phase and In the connect phase, set the sequencer and adapter for the model address map, added the pkg files in the tb_top module.

```
class router_tb extends uvm_env;
    virtual function void build_phase(uvm_phase phase);

        // register model integration
        yapp_rm = yapp_router_regs_vendor_Cadence_Design_Systems_library_Yap
        yapp_rm.build();
        yapp_rm.lock_model();
        yapp_rm.set_hdl_path_root("hw_top.dut");
        // set the suto predict ON
        yapp_rm.default_map.set_auto_predict(1);

        reg2hbus = hbus_reg_adapter::type_id::create("reg2hbus", this);
```

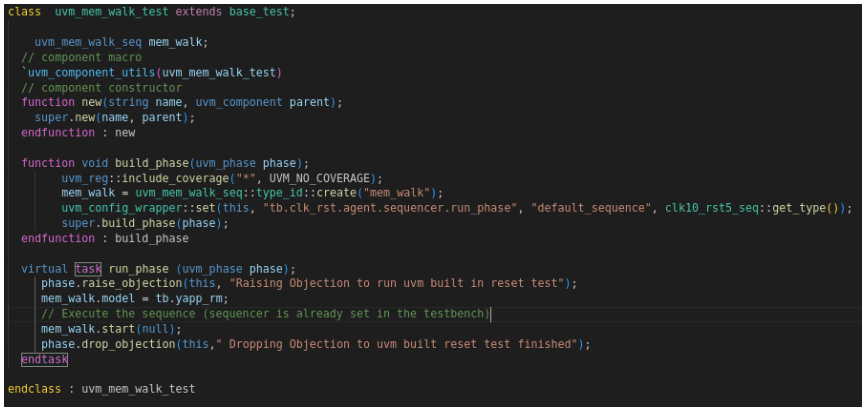
```
yapp_rm.default_map.set_sequencer(hbus.masters[0].sequencer, reg2hbus);
```

Running the **uvm_reset_test**



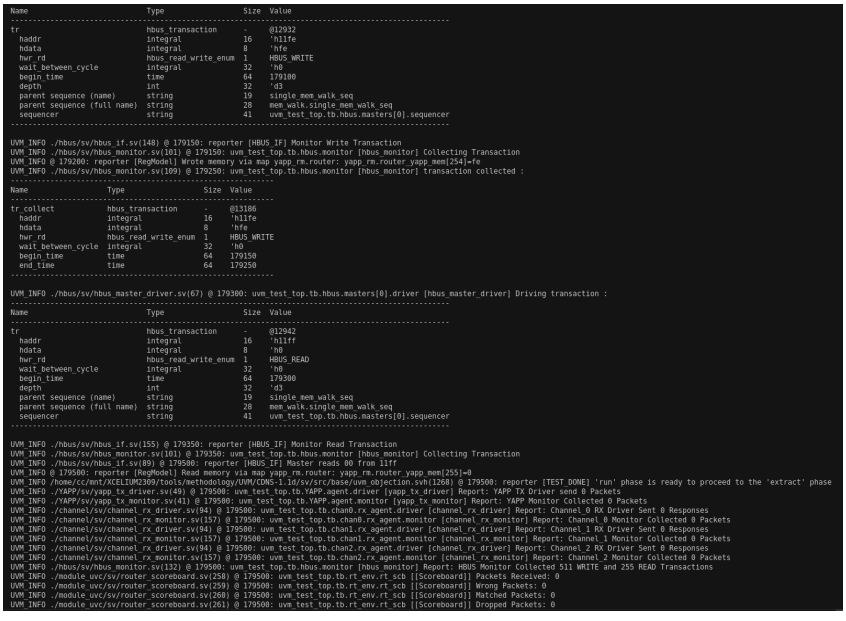
```
UVM_INFO ./hbus/sv/hbus_if.sv(155) @ 2750: reporter [HBUS_IF] Monitor Read Transaction
UVM_INFO ./hbus/sv/hbus_monitor.sv(101) @ 2750: uvm_test_top.tb.hbus.monitor [hbus_monitor] Collecting Transaction
UVM_INFO ./hbus/sv/hbus_if.sv(89) @ 2900: reporter [HBUS_IF] Master reads 00 from 1005
UVM_INFO @ 2900: reporter [RegModel] Read  register via map yapp_rm.router_yapp_regs.router_yapp_regs: yapp_rm.router_yapp_regs.oversized_pkt_cnt_reg=0
UVM_INFO /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDNS-1.1d/sv/src/reg/sequences/uvm_reg_hw_reset_seq.svh(115) @ 2900: reporter@@uvm_reset_seq [uvm_reg_hw_reset_seq] Verifying reset
err_cnt_reg in map 'yapp_rm.router'...
UVM_INFO ./hbus/sv/hbus_monitor.sv(109) @ 2950: uvm_test_top.tb.hbus.monitor [hbus_monitor] transaction collected :
-------------------------------------------------------------
Name                  Type                  Size  Value
-------------------------------------------------------------
tr_collect            hbus_transaction      -     @13186
  haddr               integral              16    'h1805
  hdata               integral              8     'h0
  hwr_rd              hbus_read_write_enum  1     HBUS_READ
  wait_between_cycle  integral              32    'h0
  begin_time          time                  64    2750
  end_time            time                  64    2950
-------------------------------------------------------------

UVM_INFO ./hbus/sv/hbus_master_driver.sv(67) @ 3000: uvm_test_top.tb.hbus.masters[0].driver [hbus_master_driver] Driving transaction :
-----------------------------------------------------------------------------------------------
Name                        Type                  Size  Value
-----------------------------------------------------------------------------------------------
tr                          hbus_transaction      -     @12949
  haddr                     integral              16    'h1004
  hdata                     integral              8     'h0
  hwr_rd                    hbus_read_write_enum  1     HBUS_READ
  wait_between_cycle        integral              32    'h0
  begin_time                time                  64    3000
  depth                     int                   32    'd2
  parent sequence (name)    string                13    uvm_reset_seq
  parent sequence (full name)  string             13    uvm_reset_seq
  sequencer                 string                41    uvm_test_top.tb.hbus.masters[0].sequencer
-----------------------------------------------------------------------------------------------

UVM_INFO ./hbus/sv/hbus_if.sv(155) @ 3050: reporter [HBUS_IF] Monitor Read Transaction
UVM_INFO ./hbus/sv/hbus_monitor.sv(101) @ 3050: uvm_test_top.tb.hbus.monitor [hbus_monitor] Collecting Transaction
UVM_INFO ./hbus/sv/hbus_if.sv(89) @ 3200: reporter [HBUS_IF] Master reads 00 from 1004
UVM_INFO @ 3200: reporter [RegModel] Read  register via map yapp_rm.router_yapp_regs.router_yapp_regs: yapp_rm.router_yapp_regs.parity_err_cnt_reg=0
UVM_INFO /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 3200: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO ./YAPP/sv/yapp_tx_driver.sv(49) @ 3200: uvm_test_top.tb.YAPP.agent.driver [yapp_tx_driver] Report: YAPP TX Driver send 0 Packets
UVM_INFO ./YAPP/sv/yapp_tx_monitor.sv(41) @ 3200: uvm_test_top.tb.YAPP.agent.monitor [yapp_tx_monitor] Report: YAPP Monitor Collected 0 Packets
UVM_INFO ./channel/sv/channel_rx_driver.sv(94) @ 3200: uvm_test_top.tb.chan0.rx_agent.driver [channel_rx_driver] Report: Channel_0 RX Driver Sent 0 Responses
UVM_INFO ./channel/sv/channel_rx_monitor.sv(157) @ 3200: uvm_test_top.tb.chan0.rx_agent.monitor [channel_rx_monitor] Report: Channel_0 Monitor Collected 0 Packets
UVM_INFO ./channel/sv/channel_rx_driver.sv(94) @ 3200: uvm_test_top.tb.chan1.rx_agent.driver [channel_rx_driver] Report: Channel_1 RX Driver Sent 0 Responses
UVM_INFO ./channel/sv/channel_rx_monitor.sv(157) @ 3200: uvm_test_top.tb.chan1.rx_agent.monitor [channel_rx_monitor] Report: Channel_1 Monitor Collected 0 Packets
UVM_INFO ./channel/sv/channel_rx_driver.sv(94) @ 3200: uvm_test_top.tb.chan2.rx_agent.driver [channel_rx_driver] Report: Channel_2 RX Driver Sent 0 Responses
UVM_INFO ./channel/sv/channel_rx_monitor.sv(157) @ 3200: uvm_test_top.tb.chan2.rx_agent.monitor [channel_rx_monitor] Report: Channel_2 Monitor Collected 0 Packets
UVM_INFO ./hbus/sv/hbus_monitor.sv(132) @ 3200: uvm_test_top.tb.hbus.monitor [hbus_monitor] Report: HBUS Monitor Collected 0 WRITE and 0 READ Transactions
UVM_INFO ./module_uvc/sv/router_scoreboard.sv(258) @ 3200: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Packets Received: 0
UVM_INFO ./module_uvc/sv/router_scoreboard.sv(259) @ 3200: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Wrong Packets: 0
UVM_INFO ./module_uvc/sv/router_scoreboard.sv(260) @ 3200: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Matched Packets: 0
UVM_INFO ./module_uvc/sv/router_scoreboard.sv(261) @ 3200: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Dropped Packets: 0
```

Created a uvm_mem_walk_test using built_in uvm_mem_walk_seq



```
class  uvm_mem_walk_test extends base_test;

    uvm_mem_walk_seq mem_walk;
  // component macro
  `uvm_component_utils(uvm_mem_walk_test)
  // component constructor
  function new(string name, uvm_component parent);
    super.new(name, parent);
  endfunction : new

  function void build_phase(uvm_phase phase);
        uvm_reg::include_coverage("*", UVM_NO_COVERAGE);
        mem_walk = uvm_mem_walk_seq::type_id::create("mem_walk");
        uvm_config_wrapper::set(this, "tb.clk_rst.agent.sequencer.run_phase", "default_sequence", clk10_rst5_seq::get_type());
        super.build_phase(phase);
  endfunction : build_phase

  virtual task run_phase (uvm_phase phase);
    phase.raise_objection(this, "Raising Objection to run uvm built in reset test");
    mem_walk.model = tb.yapp_rm;
    // Execute the sequence (sequencer is already set in the testbench)
    mem_walk.start(null);
    phase.drop_objection(this," Dropping Objection to uvm built reset test finished");
  endtask

endclass : uvm_mem_walk_test
```

Running the **uvm_mem_walk_test**



```
Name                        Type                  Size  Value
-----------------------------------------------------------------------------------------------
tr                          hbus_transaction      -     @12932
  haddr                     integral              16    'h11fe
  hdata                     integral              8     'hfe
  hwr_rd                    hbus_read_write_enum  1     HBUS_WRITE
  wait_between_cycle        integral              32    'h0
  begin_time                time                  64    179100
  depth                     int                   32    'd3
  parent sequence (name)    string                19    single_mem_walk_seq
  parent sequence (full name)  string             28    mem_walk.single_mem_walk_seq
  sequencer                 string                41    uvm_test_top.tb.hbus.masters[0].sequencer
-----------------------------------------------------------------------------------------------

UVM_INFO ./hbus/sv/hbus_if.sv(148) @ 179150: reporter [HBUS_IF] Monitor Write Transaction
UVM_INFO ./hbus/sv/hbus_monitor.sv(101) @ 179150: uvm_test_top.tb.hbus.monitor [hbus_monitor] Collecting Transaction
UVM_INFO @ 179200: reporter [RegModel] Wrote memory via map yapp_rm.router: yapp_rm.router_yapp_mem[254]=fe
UVM_INFO ./hbus/sv/hbus_monitor.sv(109) @ 179250: uvm_test_top.tb.hbus.monitor [hbus_monitor] transaction collected :
-------------------------------------------------------------
Name                  Type                  Size  Value
-------------------------------------------------------------
tr_collect            hbus_transaction      -     @13186
  haddr               integral              16    'h11fe
  hdata               integral              8     'hfe
  hwr_rd              hbus_read_write_enum  1     HBUS_WRITE
  wait_between_cycle  integral              32    'h0
  begin_time          time                  64    179150
  end_time            time                  64    179250
-------------------------------------------------------------

UVM_INFO ./hbus/sv/hbus_master_driver.sv(67) @ 179300: uvm_test_top.tb.hbus.masters[0].driver [hbus_master_driver] Driving transaction :
-----------------------------------------------------------------------------------------------
Name                        Type                  Size  Value
-----------------------------------------------------------------------------------------------
tr                          hbus_transaction      -     @12942
  haddr                     integral              16    'h11ff
  hdata                     integral              8     'h0
  hwr_rd                    hbus_read_write_enum  1     HBUS_READ
  wait_between_cycle        integral              32    'h0
  begin_time                time                  64    179300
  depth                     int                   32    'd3
  parent sequence (name)    string                19    single_mem_walk_seq
  parent sequence (full name)  string             28    mem_walk.single_mem_walk_seq
  sequencer                 string                41    uvm_test_top.tb.hbus.masters[0].sequencer
-----------------------------------------------------------------------------------------------

UVM_INFO ./hbus/sv/hbus_if.sv(155) @ 179350: reporter [HBUS_IF] Monitor Read Transaction
UVM_INFO ./hbus/sv/hbus_monitor.sv(101) @ 179350: uvm_test_top.tb.hbus.monitor [hbus_monitor] Collecting Transaction
UVM_INFO ./hbus/sv/hbus_if.sv(89) @ 179500: reporter [HBUS_IF] Master reads 00 from 11ff
UVM_INFO @ 179500: reporter [RegModel] Read memory via map yapp_rm.router: yapp_rm.router_yapp_mem[255]=0
UVM_INFO /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 179500: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO ./YAPP/sv/yapp_tx_driver.sv(49) @ 179500: uvm_test_top.tb.YAPP.agent.driver [yapp_tx_driver] Report: YAPP TX Driver send 0 Packets
UVM_INFO ./YAPP/sv/yapp_tx_monitor.sv(41) @ 179500: uvm_test_top.tb.YAPP.agent.monitor [yapp_tx_monitor] Report: YAPP Monitor Collected 0 Packets
UVM_INFO ./channel/sv/channel_rx_driver.sv(94) @ 179500: uvm_test_top.tb.chan0.rx_agent.driver [channel_rx_driver] Report: Channel_0 RX Driver Sent 0 Responses
UVM_INFO ./channel/sv/channel_rx_monitor.sv(157) @ 179500: uvm_test_top.tb.chan0.rx_agent.monitor [channel_rx_monitor] Report: Channel_0 Monitor Collected 0 Packets
UVM_INFO ./channel/sv/channel_rx_driver.sv(94) @ 179500: uvm_test_top.tb.chan1.rx_agent.driver [channel_rx_driver] Report: Channel_1 RX Driver Sent 0 Responses
UVM_INFO ./channel/sv/channel_rx_monitor.sv(157) @ 179500: uvm_test_top.tb.chan1.rx_agent.monitor [channel_rx_monitor] Report: Channel_1 Monitor Collected 0 Packets
UVM_INFO ./channel/sv/channel_rx_driver.sv(94) @ 179500: uvm_test_top.tb.chan2.rx_agent.driver [channel_rx_driver] Report: Channel_2 RX Driver Sent 0 Responses
UVM_INFO ./channel/sv/channel_rx_monitor.sv(157) @ 179500: uvm_test_top.tb.chan2.rx_agent.monitor [channel_rx_monitor] Report: Channel_2 Monitor Collected 0 Packets
UVM_INFO ./hbus/sv/hbus_monitor.sv(132) @ 179900: uvm_test_top.tb.hbus.monitor [hbus_monitor] Report: HBUS Monitor Collected 511 WRITE and 255 READ Transactions
UVM_INFO ./module_uvc/sv/router_scoreboard.sv(258) @ 179500: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Packets Received: 0
UVM_INFO ./module_uvc/sv/router_scoreboard.sv(259) @ 179500: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Wrong Packets: 0
UVM_INFO ./module_uvc/sv/router_scoreboard.sv(260) @ 179500: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Matched Packets: 0
UVM_INFO ./module_uvc/sv/router_scoreboard.sv(261) @ 179500: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Dropped Packets: 0
```

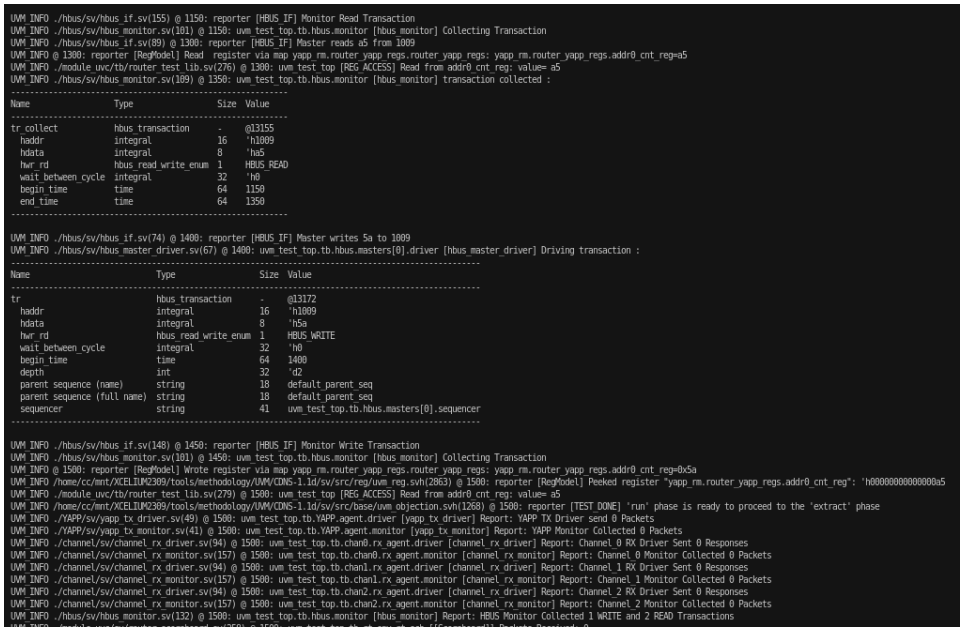
Task 3: Simulation

Reg_access_test:

Created a handle of register block and assigned this handle to the register block instance using hierarchical pathname.

```
class reg_access_test extends base_test;

    yapp_regs_c yapp_regs;
    uvm_status_e status;
  // component macro
  `uvm_component_utils(reg_access_test)

  // component constructor
  function new(string name, uvm_component parent);
    super.new(name, parent);
  endfunction : new

  function void build_phase(uvm_phase phase);
        uvm_reg::include_coverage("*", UVM_NO_COVERAGE);
        uvm_config_wrapper::set(this, "tb.clk_rst.agent.sequencer.run_phase", "default_sequence", clk10_rst5_seq::get_type());
        super.build_phase(phase);
  endfunction : build_phase
bit [7:0] rdata;
  virtual task run_phase (uvm_phase phase);
    phase.raise_objection(this, "Raising Objection to run uvm built in reg_access_test");
    //RW register Check
    yapp_regs.en_reg.write(status, 8'hA5);
    yapp_regs.en_reg.peek(status, rdata);
    `uvm_info("REG_ACCESS", $sformatf("Read from register en_reg: value= %0h", rdata), UVM_NONE)
    yapp_regs.en_reg.poke(status, 8'h5A);
    yapp_regs.en_reg.read(status, rdata);
    `uvm_info("REG_ACCESS", $sformatf("Read from register en_reg: value= %0h", rdata), UVM_NONE)

    //RO register check
    yapp_regs.addr0_cnt_reg.poke(status, 8'hA5);
    yapp_regs.addr0_cnt_reg.read(status, rdata);
    `uvm_info("REG_ACCESS", $sformatf("Read from addr0_cnt_reg: value= %0h", rdata), UVM_NONE)
    yapp_regs.addr0_cnt_reg.write(status, 8'h5A);
    yapp_regs.addr0_cnt_reg.peek(status, rdata);
    `uvm_info("REG_ACCESS", $sformatf("Read from addr0_cnt_reg: value= %0h", rdata), UVM_NONE)

    phase.drop_objection(this," Dropping Objection to uvm built reset test finished");

  endtask

  function void connect_phase(uvm_phase phase);
    yapp_regs = tb.yapp_rm.router_yapp_regs;
  endfunction

endclass: reg_access_test
```

Running reg_access_test:



Functional Verification:
Reg_function_test:

```
class reg_function_test extends base_test;
    `uvm_component_utils(reg_function_test)

    yapp_tx_sequencer yapp_sequencer;
    yapp_012_seq yapp012;
    yapp_regs_c yapp_regs;

    function new(string name = "reg_function_test", uvm_component parent);
        super.new(name, parent);
    endfunction

    function void build_phase(uvm_phase phase);
        yapp012 = yapp_012_seq::type_id::create("yapp012", this);
        uvm_config_wrapper::set(this, "tb.clk_rst.agent.sequencer.run_phase", "default_sequence", clk10_rst5_seq::get_type());
        uvm_config_wrapper::set(this, "tb.chan?.rx_agent.sequencer.run_phase", "default_sequence", channel_rx_resp_seq::get_type());
        super.build_phase(phase);
    endfunction

    task run_phase(uvm_phase phase);
        bit [7:0] rdata;
        uvm_status_e status;
        phase.raise_objection(this, "Raising Objection to run reg_function_test");

        yapp_regs.en_reg.write(status, 8'h01);
        yapp_regs.en_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from register en_reg: value= %0h", rdata), UVM_NONE)
        yapp012.start(yapp_sequencer);
        yapp_regs.addr0_cnt_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from addr0_cnt_reg: value= %0h", rdata), UVM_NONE)
        yapp_regs.addr1_cnt_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from addr1_cnt_reg: value= %0h", rdata), UVM_NONE)
        yapp_regs.addr2_cnt_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from addr2_cnt_reg: value= %0h", rdata), UVM_NONE)
        yapp_regs.addr3_cnt_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from addr3_cnt_reg: value= %0h", rdata), UVM_NONE)

        yapp_regs.en_reg.write(status, 8'hff);
        yapp012.start(yapp_sequencer);
        yapp012.start(yapp_sequencer);

        yapp_regs.addr0_cnt_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from addr0_cnt_reg: value= %0h", rdata), UVM_NONE)
        yapp_regs.addr1_cnt_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from addr1_cnt_reg: value= %0h", rdata), UVM_NONE)
        yapp_regs.addr2_cnt_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from addr2_cnt_reg: value= %0h", rdata), UVM_NONE)
        yapp_regs.addr3_cnt_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from addr3_cnt_reg: value= %0h", rdata), UVM_NONE)

        yapp_regs.parity_err_cnt_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from parity_err_cnt_reg: value= %0h", rdata), UVM_NONE)
        yapp_regs.oversized_pkt_cnt_reg.read(status, rdata);
        `uvm_info("REG_FUNCTION_TEST", $sformatf("Read from oversized_pkt_cnt_reg: value= %0h", rdata), UVM_NONE)

        phase.drop_objection(this, "Dropping Objection to run reg_function_test finished");
    endtask

    function void connect_phase(uvm_phase phase);
        yapp_sequencer = tb.YAPP.agent.sequencer;
        yapp_regs = tb.yapp_rm.router_yapp_regs;
    endfunction

endclass: reg_function_test
```

Running reg_function_test:

```
UVM_INFO ./hbus/sv/hbus_if.sv(89) @ 35300: reporter [HBUS_IF] Master reads 02 from 1009
UVM_INFO @ 35300: reporter [RegModel] Read  register via map yapp_rm.router_yapp_regs.router_yapp_regs: yapp_rm.router_yapp_regs.addr0_cnt_reg=2
UVM_INFO ./module uvc/tb/router_test_lib.sv(341) @ 35300: uvm_test_top [REG_FUNCTION_TEST] Read from addr0_cnt_reg: value= 2
UVM_INFO ./hbus/sv/hbus_monitor.sv(109) @ 35350: uvm_test_top.tb.hbus.monitor [hbus_monitor] transaction collected :
----------------------------------------------------------
Name                Type                    Size  Value
----------------------------------------------------------
tr_collect          hbus_transaction        -     @13173
  haddr             integral                16    'h1009
  hdata             integral                8     'h2
  hwr_rd            hbus_read_write_enum    1     HBUS_READ
  wait_between_cycle  integral              32    'h0
  begin_time        time                    64    35150
  end_time          time                    64    35350
----------------------------------------------------------

UVM_INFO ./hbus/sv/hbus_master_driver.sv(67) @ 35400: uvm_test_top.tb.hbus.masters[0].driver [hbus_master_driver] Driving transaction :
-----------------------------------------------------------------------------------------------------------
Name                        Type                    Size  Value
-----------------------------------------------------------------------------------------------------------
tr                          hbus_transaction        -     @12874
  haddr                     integral                16    'h100a
  hdata                     integral                8     'h0
  hwr_rd                    hbus_read_write_enum    1     HBUS_READ
  wait_between_cycle        integral                32    'h0
  begin_time                time                    64    35400
  depth                     int                     32    'd2
  parent sequence (name)    string                  18    default_parent_seq
  parent sequence (full name)  string               18    default_parent_seq
  sequencer                 string                  41    uvm_test_top.tb.hbus.masters[0].sequencer
-----------------------------------------------------------------------------------------------------------

UVM_INFO ./hbus/sv/hbus_if.sv(155) @ 35450: reporter [HBUS_IF] Monitor Read Transaction
UVM_INFO ./hbus/sv/hbus_monitor.sv(101) @ 35450: uvm_test_top.tb.hbus.monitor [hbus_monitor] Collecting Transaction
UVM_INFO ./channel/sv/channel_rx_monitor.sv(144) @ 35550: uvm_test_top.tb.chan2.rx_agent.monitor [channel_rx_monitor] Channel_2 Packet collected :
-----------------------------------------------------
Name                Type                Size  Value
-----------------------------------------------------
packet_collected    channel_packet      -     @12864
  length            integral            6     'h12
  addr              integral            2     'h2
  payload           da(integral)        18    -
    [0]             integral            8     'hb4
    [1]             integral            8     'h30
    [2]             integral            8     'h55
    [3]             integral            8     'hc3
    [4]             integral            8     'h35
    ...             ...                 ...   ...
    [13]            integral            8     'h31
    [14]            integral            8     'h2
    [15]            integral            8     'hd4
    [16]            integral            8     'ha7
    [17]            integral            8     'h66
  parity            integral            8     'h0
  parity_type       parity_e            1     BAD_PARITY
  packet_delay      integral            32    'd0
  begin_time        time                64    33550
  end_time          time                64    35550
-----------------------------------------------------

UVM_ERROR ./module uvc/sv/router_scoreboard.sv(111) @ 35550: uvm_test_top.tb.rt_env.rt_scb [router_scoreboard] Packet Matched
UVM_INFO ./hbus/sv/hbus_if.sv(89) @ 35600: reporter [HBUS_IF] Master reads 02 from 100a
UVM_INFO @ 35600: reporter [RegModel] Read  register via map yapp_rm.router_yapp_regs.router_yapp_regs: yapp_rm.router_yapp_regs.addr1_cnt_reg=2
UVM_INFO ./module uvc/tb/router_test_lib.sv(343) @ 35600: uvm_test_top [REG_FUNCTION_TEST] Read from addr1_cnt_reg: value= 2
UVM_INFO ./hbus/sv/hbus_monitor.sv(109) @ 35650: uvm_test_top.tb.hbus.monitor [hbus_monitor] transaction collected :
----------------------------------------------------------
```

```
INFO ./hbus/sv/hbus_if.sv(155) @ 36650: reporter [HBUS_IF] Monitor Read Transaction
INFO ./hbus/sv/hbus_monitor.sv(101) @ 36650: uvm_test_top.tb.hbus.monitor [hbus_monitor] Collecting Transaction
INFO ./hbus/sv/hbus_if.sv(89) @ 36800: reporter [HBUS_IF] Master reads 00 from 1005
INFO @ 36800: reporter [RegModel] Read  register via map yapp_rm.router_yapp_regs.router_yapp_regs: yapp_rm.router_yapp_regs.oversized_pkt_cnt_reg=0
INFO ./module_uvc/tb/router_test_lib.sv(352) @ 36800: uvm_test_top [REG_FUNCTION_TEST] Read from oversized_pkt_cnt_reg: value= 0
INFO /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 36800: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
INFO ./YAPP/sv/yapp_tx_driver.sv(49) @ 36800: uvm_test_top.tb.YAPP.agent.driver [yapp_tx_driver] Report: YAPP TX Driver send 9 Packets
INFO ./YAPP/sv/yapp_tx_monitor.sv(41) @ 36800: uvm_test_top.tb.YAPP.agent.monitor [yapp_tx_monitor] Report: YAPP Monitor Collected 9 Packets
INFO ./channel/sv/channel_rx_driver.sv(94) @ 36800: uvm_test_top.tb.chan0.rx_agent.driver [channel_rx_driver] Report: Channel_0 RX Driver Sent 3 Responses
INFO ./channel/sv/channel_rx_monitor.sv(157) @ 36800: uvm_test_top.tb.chan0.rx_agent.monitor [channel_rx_monitor] Report: Channel_0 Monitor Collected 3 Packets
INFO ./channel/sv/channel_rx_driver.sv(94) @ 36800: uvm_test_top.tb.chan1.rx_agent.driver [channel_rx_driver] Report: Channel_1 RX Driver Sent 3 Responses
INFO ./channel/sv/channel_rx_monitor.sv(157) @ 36800: uvm_test_top.tb.chan1.rx_agent.monitor [channel_rx_monitor] Report: Channel_1 Monitor Collected 3 Packets
INFO ./channel/sv/channel_rx_driver.sv(94) @ 36800: uvm_test_top.tb.chan2.rx_agent.driver [channel_rx_driver] Report: Channel_2 RX Driver Sent 3 Responses
INFO ./channel/sv/channel_rx_monitor.sv(157) @ 36800: uvm_test_top.tb.chan2.rx_agent.monitor [channel_rx_monitor] Report: Channel_2 Monitor Collected 3 Packets
INFO ./hbus/sv/hbus_monitor.sv(132) @ 36800: uvm_test_top.tb.hbus.monitor [hbus_monitor] Report: HBUS Monitor Collected 2 WRITE and 10 READ Transactions
INFO ./module_uvc/sv/router_scoreboard.sv(258) @ 36800: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Packets Received: 9
INFO ./module_uvc/sv/router_scoreboard.sv(259) @ 36800: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Wrong Packets: 0
INFO ./module_uvc/sv/router_scoreboard.sv(260) @ 36800: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Matched Packets: 9
INFO ./module_uvc/sv/router_scoreboard.sv(261) @ 36800: uvm_test_top.tb.rt_env.rt_scb [[Scoreboard]] Dropped Packets: 0
```

Errors after enabling the automatic checking of read values against the mirrored value in register model

```
UVM_INFO ./hbus/sv/hbus_if.sv(155) @ 57550: reporter [HBUS_IF] Monitor Read Transaction
UVM_INFO ./hbus/sv/hbus_monitor.sv(101) @ 57550: uvm_test_top.tb.hbus.monitor [hbus_monitor] Collecting Transaction
UVM_INFO ./hbus/sv/hbus_if.sv(89) @ 57700: reporter [HBUS_IF] Master reads 02 from 100a
UVM_ERROR /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDNS-1.1d/sv/src/reg/uvm_reg.svh(2892) @ 57700: reporter [RegModel] Register "yapp_rm.router_yapp_regs.addr1_cnt_reg" value read from DUT (0x0000000000000002) does not match mirrored v
UVM_INFO /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDNS-1.1d/sv/src/reg/uvm_reg.svh(2911) @ 57700: reporter [RegModel] Field non_reserved_auto_added_field (yapp_rm.router_yapp_regs.addr1_cnt_reg[7:0]) mismatch read='h2 mirrored='h0
UVM_INFO @ 57700: reporter [RegModel] Read  register via map yapp_rm.router_yapp_regs.router_yapp_regs: yapp_rm.router_yapp_regs.addr1_cnt_reg=2
UVM_INFO ./module_uvc/tb/router_test_lib.sv(343) @ 57700: uvm_test_top [REG_FUNCTION_TEST] Read from addr1_cnt_reg: value= 2
UVM_INFO ./hbus/sv/hbus_monitor.sv(109) @ 57750: uvm_test_top.tb.hbus.monitor [hbus_monitor] transaction collected :
```

Register Introspection:

```
// Get all registers in the register model
tb.yapp_rm.get_registers(regs);

// Select RW and RO registers using array selection
foreach (regs[i]) begin
    if (regs[i].get_rights() == "RW")
        rw_regs.push_back(regs[i]);
    else if (regs[i].get_rights() == "RO")
        ro_regs.push_back(regs[i]);
end

// Print names of RW registers
`uvm_info("REG_INTROSPECT", "RW Registers:", UVM_LOW)
foreach (rw_regs[i])
    `uvm_info("REG_INTROSPECT", $sformatf("  %s", rw_regs[i].get_name()), UVM_LOW)

// Print names of RO registers
`uvm_info("REG_INTROSPECT", "RO Registers:", UVM_LOW)
foreach (ro_regs[i])
    `uvm_info("REG_INTROSPECT", $sformatf("  %s", ro_regs[i].get_name()), UVM_LOW)
```

```
UVM_INFO ./hbus/sv/hbus_if.sv(155) @ 40050: reporter [HBUS_IF] Monitor Read Transaction
UVM_INFO ./hbus/sv/hbus_monitor.sv(101) @ 40050: uvm_test_top.tb.hbus.monitor [hbus_monitor] Collecting Transaction
UVM_INFO ./hbus/sv/hbus_if.sv(89) @ 40200: reporter [HBUS_IF] Master reads 00 from 1005
UVM_INFO @ 40200: reporter [RegModel] Read  register via map yapp_rm.router_yapp_regs.router_yapp_regs: yapp_rm.router_yapp_regs.oversized_pkt_cnt_reg=0
UVM_INFO ./module_uvc/tb/router_test_lib.sv(355) @ 40200: uvm_test_top [REG_FUNCTION_TEST] Read from oversized_pkt_cnt_reg: value= 0
UVM_INFO ./module_uvc/tb/router_test_lib.sv(370) @ 40200: uvm_test_top [REG_INTROSPECT] RW Registers:
UVM_INFO ./module_uvc/tb/router_test_lib.sv(372) @ 40200: uvm_test_top [REG_INTROSPECT]   ctrl_reg
UVM_INFO ./module_uvc/tb/router_test_lib.sv(372) @ 40200: uvm_test_top [REG_INTROSPECT]   en_reg
UVM_INFO ./module_uvc/tb/router_test_lib.sv(375) @ 40200: uvm_test_top [REG_INTROSPECT] RO Registers:
UVM_INFO ./module_uvc/tb/router_test_lib.sv(377) @ 40200: uvm_test_top [REG_INTROSPECT]   addr0_cnt_reg
UVM_INFO ./module_uvc/tb/router_test_lib.sv(377) @ 40200: uvm_test_top [REG_INTROSPECT]   addr1_cnt_reg
UVM_INFO ./module_uvc/tb/router_test_lib.sv(377) @ 40200: uvm_test_top [REG_INTROSPECT]   addr2_cnt_reg
UVM_INFO ./module_uvc/tb/router_test_lib.sv(377) @ 40200: uvm_test_top [REG_INTROSPECT]   addr3_cnt_reg
UVM_INFO ./module_uvc/tb/router_test_lib.sv(377) @ 40200: uvm_test_top [REG_INTROSPECT]   mem_size_reg
UVM_INFO ./module_uvc/tb/router_test_lib.sv(377) @ 40200: uvm_test_top [REG_INTROSPECT]   oversized_pkt_cnt_reg
UVM_INFO ./module_uvc/tb/router_test_lib.sv(377) @ 40200: uvm_test_top [REG_INTROSPECT]   parity_err_cnt_reg
UVM_INFO /home/cc/mnt/XCELIUM2309/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 40200: reporter [TEST_DONE] 'run' phase is ready to
```