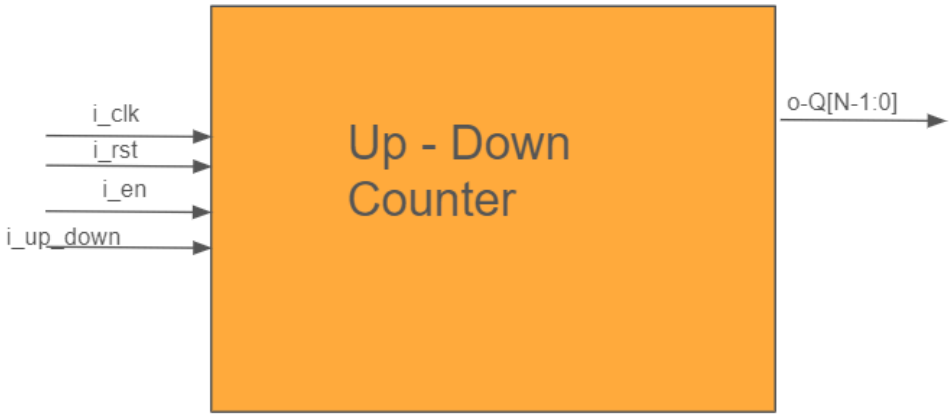
Specification for Mod-N Conditional Up-Down Counter

Block diagram :



1. Introduction
The mod-N conditional up-down counter is a digital counter that counts up or down based on a control signal and wraps around after reaching a maximum count of N-1.
It is commonly used in applications where counting in a specific range with directional control is required.

2. Features
- Counts from 0 to N-1
- Up and down counting capability based on control signal
- Synchronous operation with a clock signal
- Conditional counting based on an enable signal
- Reset functionality to initialize the counter

3. Inputs
1. Clock (i_clk) : The primary clock signal for synchronizing the counter.
2. Reset (i_rst) : An asynchronous signal that resets the counter to 0 when asserted.
3. Enable (i_en) : A signal that enables counting when asserted. When deasserted, the counter holds its value.
4. Up/Down (i_up_down) : A control signal that determines the counting direction. When asserted (high), the counter counts up; when deasserted (low), the counter counts down.

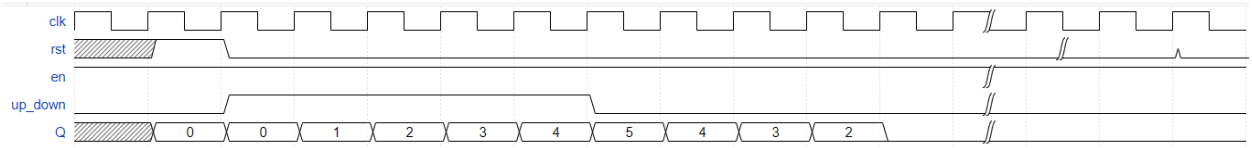
4. Outputs
1. Count (o_Q): The current value of the counter, ranging from 0 to N-1.

5. Operation

- Counting Up: When `up_down` is high and `en` is asserted, the counter increments its value on each rising edge of the clock.
- Counting Down: When `up_down` is low and `en` is asserted, the counter decrements its value on each rising edge of the clock.
- Wrap Around :
  - When counting up and the counter reaches N-1, it wraps around to 0 on the next clock edge.
  - When counting down and the counter reaches 0, it wraps around to N-1 on the next clock edge.
- Hold : When `en` is deasserted, the counter holds its current value regardless of the clock edges.
- Reset : When `rst` is asserted, the counter is asynchronously reset to 0, overriding all other signals.

6. Timing Diagram

The timing diagram should illustrate the behavior of the counter under various conditions, including counting up, counting down, holding, and resetting.



7. State Diagram

A state diagram should be provided to illustrate the transitions between states based on the `up_down`, `en`, and `rst` signals.

TBD - can some take it up and draw and send.

8. Verification

- Functional Simulation : Verify the counter functionality through simulation by applying various test vectors to check the counting up, counting down, hold, and reset functionalities.
- Timing Analysis : Ensure that the counter meets the required timing constraints in the target technology.

9. Applications

- Frequency dividers
- Digital clocks
- State machines
- Event counters