MCAC102: Computer System architecture **Roll No. .....**

Time: One Hour **Max. Marks: 20**

Instruction: All questions are compulsory. Each question carries 4 marks.

Q1) Design a common bus system for four registers of 4 bit each using three state-buffers and a decoder.

Q2) Design an 8-bit combinational circuit shifter.

Q3) Implement 16x1 Multiplexer using lower order Multiplexers. (eg. Lower than 8x1)

Q4) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages.

S	$C_{in} = 0$	$C_{in} = 1$
0	$D = A + B$ (add)	$D = A + 1$ (increment)
1	$D = A - 1$ (decrement)	$D = A + \overline{B} + 1$ (subtract)

Q5) Design and Describe the flowchart for the Register and I/O reference instruction with timing signal.