MASTER OF COMPUTER APPLICATIONS
MCAC102: COMPUTER SYSTEMS ARCHITECTURE

Unique Paper Code: 223421102
Semester I
January 2024
Year of Admission: 2023

Time: Three Hours **Max. Marks: 70**

ROLL NO. 2323476800005L

Attempt all questions. Write your answer with question no.

Attempt all parts of a question together.

Unless stated otherwise, the symbols have their usual meanings.

Make suitable assumptions, if required.

Q1.	(a) Decode the following instructions and show their execution using block diagrams: (i) 11000011000001 (ii) 01001001001100 **(b)** Give an example of a situation that would require a (i) branch instruction, (ii) a call subroutine instruction and (iii) program interrupt.	**5+5= 10**
Q2.	Describe the Strobe control method of asynchronous data transfer with the help of a diagram. What are its limitations? How can they be addressed?	**10**
Q3.	(a) Simplify the given expression using Boolean algebra: (i) F = XY'Z + X'Y'Z + W'XY + WX'Y + WXY (ii) F = X'Y + YZ' + YZ + XY'Z' **(b)** Design the Binary Ripple carry adder.	**5+5= 10**
Q4.	Give the diagram of a DMA controller. Why are the read and write control lines in a DMA controller bidirectional? Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose are they used as outputs?	**10**
Q5.	(a) Evaluate the following arithmetic statement in assembly language instruction $X = A + B[C * D + E(F + G)]$ (i) Using three address instructions. (ii) Using two address instructions. (iii) Using one address instructions. (iv) Using zero address operation instructions. Use the symbols *ADD* and *MUL* for arithmetic operations; *MOV* for the transfer-type operation; and *LOAD* and *STORE* for transfers to and from *AC* register and memory. Assume that memory operands are stored at memory addresses *A, B, C, D, E, F, G* and the result must be stored in memory at address *X*. **(b)** Write the assembly language program to find the average of the five numbers.	**5+5= 10**
Q6.	(a) Design a circuit associated with the accumulator and give its different microoperation. **(b)** What is a datapath? With a neat diagram, describe one, two and three -bus organization (datapath) of CPU.	**4+6= 10**
Q7.	(a) Give the sequence of microinstructions for push and pop operations. Also give the relevant diagrams. **(b)** How is the memory table used for mapping a virtual address and in a paged system? Illustrate with diagrams.	**4+6= 10**

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