Report

Risc Pipeline Processor

EE309 Microprocessors

Contents

OVERVIEW:

Built a 16-bit, 6-stage, 8-register pipelined RISC processor capable of executing 14 instructions in 3 distinct formats an 8-register system with 6 stages: fetch, decode, register read, execute, memory access, and write-back architecture with advanced hazard management and data forwarding techniques for better performance

COMPONENTS:

ARITHMETIC LOGIC UNIT (ALU):

It does Addition, Subtraction, NAND and XOR operations.

Port Name	Port type	Length(bits)	Function
ALU_A	input	16	First input vector
ALU_B	input	16	Second input vector
ALU_C	output	16	Output vector
ctrl	input	2	Denotes operation
c	output	1	Denotes occurrence of carry
z	output	1	Indicates if the output is zero

MEMORY:

An Array of 512 vectors, each of which is of length 16-bit. It is where most of the data we work on are stored.

Port Name	Port Type	Length(bits)	Function
clk	input	1	clock vector for looping
MWR	input	1	Memory write enabling
reset	input	1	Resetting
m_adrs	input	16	Address of concerned location
m_Din	input	16	Data input to the memory

m_Dout	output	16	Data output from the memory

REGISTER:

Registers are a type of computer memory used to accept, store quickly, and transfer data and instructions used at once by the CPU. It is a 16-bit Register. It has

Port Name	Port Type	Length(bits)	Function
clk	input	1	clock vector for looping
WR_E	input	1	Register writes enabling
reset	input	1	Resetting
regin	input	16	Data input to Register
regout	output	16	Data output to Register

REGISTER FILE:

A register file is an array of processor registers. The Register file is a simple method of using a single name to access multiple different registers depending on the operating mode.

Port Name	Port Type	Length(bits)	Function
clk	input	1	clock vector for looping
WR_E	input	1	Register writes enabling to write in the register
RD_E	input	1	Register read enabling to read data from register
reset	input	1	Resetting
A1	input	3	Address input to register for data output from D1
A2	input	3	Address input to register for data output from A2
A3	input	3	Address input to write data D3 in given registers.
D3	input	16	Register with address A3 stores the Data input
D1	output	16	Data output from Register

D2	output	16	Data output from Register
R7_PC	output	16	Gives output as data stored in R7

SIGN EXTENDER (SE6):

Sign Extender is the operation to increase the number of bits of a binary number while preserving the number's sign and value. It converts 6-bit numbers to 16 Bit numbers.

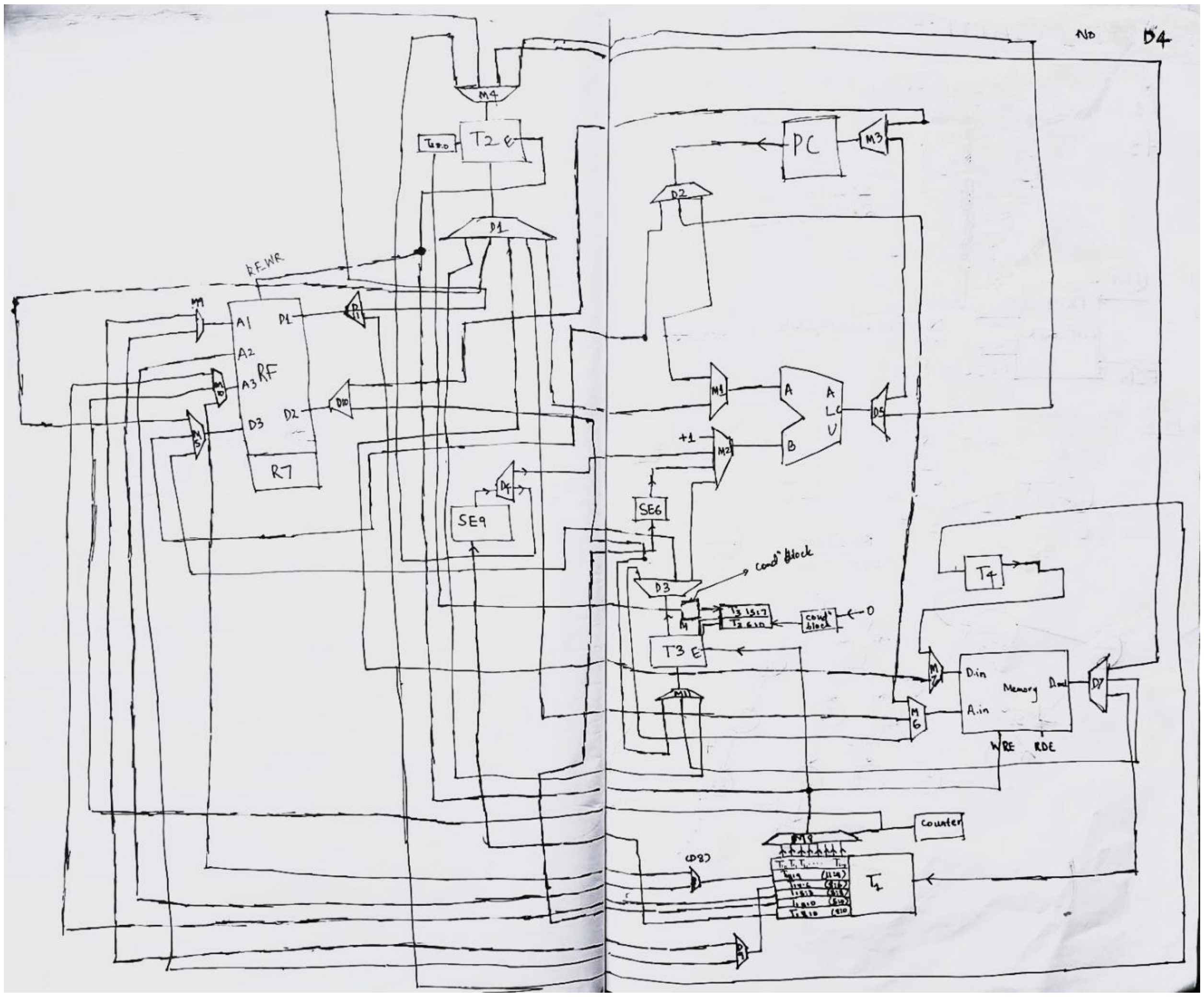
Port Name	Port Type	Length(bits)	Function
SE6_I	input	6	Data input is 6 bits.
SE6_O	output	16	Data input converted to 16 bits output.

SIGN EXTENDER (SE9):

Sign Extender is the operation to increase the number of bits of a binary number while preserving the number's sign and value. It converts 9-bit numbers to 16 Bit numbers.

Port Name	Port Type	Length(bits)	Function
SE6_I	input	9	Data input as 9 bits.
SE6_O	output	16	Data input converted to 16 bits output.

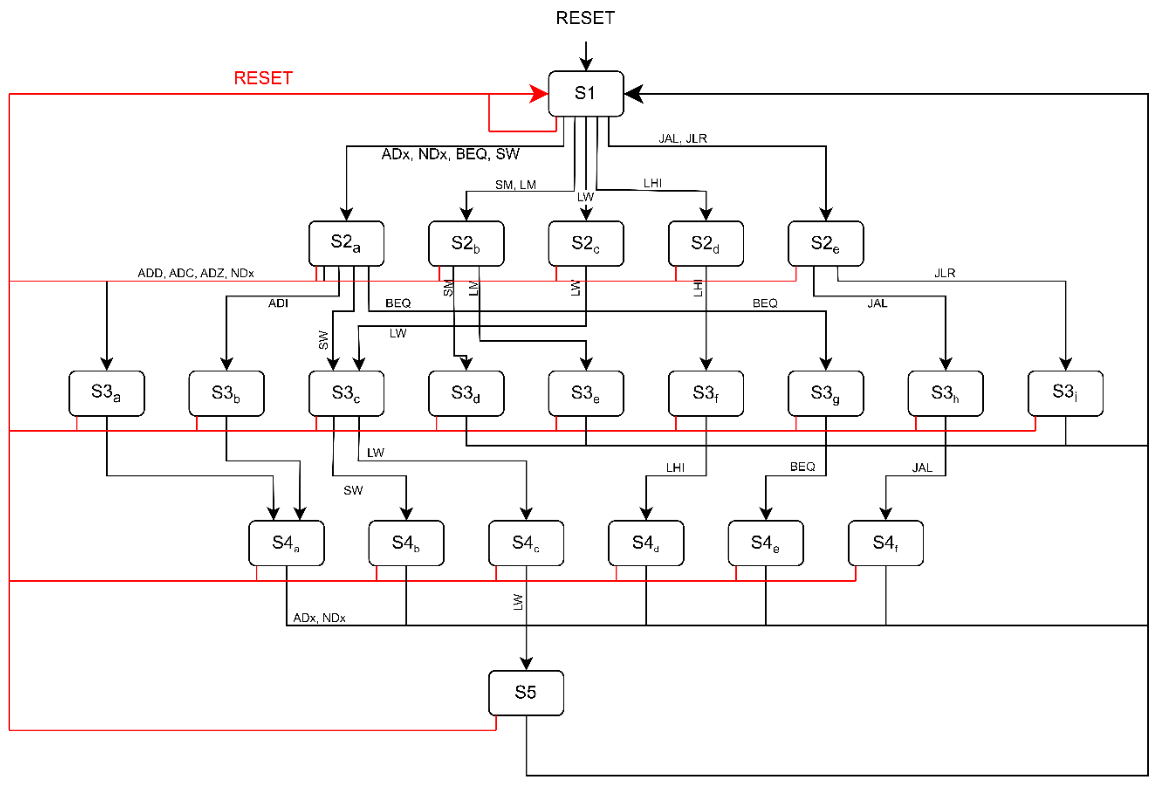
DATAPATH DIAGRAM:



STATE TRANSITION TABLE:

Previous state	Next state	Condition
Any State	S_1	Reset
S_1	S_{2A}	(Inp(15)).(Inp(14)).(! Inp(13)).(! Inp(12)) or (! Inp(15)).(! Inp(14)).(! Inp(12)) or (! Inp(15))(! Inp(13)).(Inp(12))
S_1	S_{2B}	(! Inp(15)).(Inp(14)).(Inp(13))
S_1	S_{2C}	(! Inp(15)).(Inp(14)).(! Inp(13)).(! Inp(12))
S_1	S_{2D}	(! Inp(15)).(! Inp(14)).(Inp(13)).(Inp(12))
S_1	S_{2E}	(Inp(15)).(! Inp(14)).(! Inp(13))
S_{2A}	S_{3A}	(! Inp(15)).(! Inp(14)).(! Inp(12))
S_{2A}	S_{3B}	(! Inp(15)).(! Inp(14)).(! Inp(13)).(Inp(12))
S_{2A}	S_{3C}	(! Inp(15)).Inp(14)).(! Inp(13)).(Inp(12))
S_{2A}	S_{3G}	(Inp(15)).(Inp(14)).(! Inp(13)).(! Inp(12))
S_{2B}	S_{3D}	(! Inp(15)).(Inp(14)).(Inp(13)).(Inp(12))
S_{2B}	S_{3E}	(! Inp(15)).(Inp(14)).(Inp(13)).(! Inp(12))
S_{2C}	S_{3C}	X
S_{2D}	S_{3F}	X
S_{2E}	S_{3H}	(Inp(15)).(! Inp(14)).(! Inp(13)).(! Inp(12))
S_{2E}	S_{3I}	(Inp(15)).(! Inp(14)).(! Inp(13)).(Inp(12))
S_{3A}	S_{4A}	X
S_{3B}	S_{4A}	X
S_{3C}	S_{4B}	(! Inp(15)).(Inp(14)).(! Inp(13)).(Inp(12))
S_{3C}	S_{4C}	(! Inp(15)).(Inp(14)).(! Inp(13)).(! Inp(12))
S_{3D}	S1	X
S_{3E}	S1	X
S_{3F}	S_{4d}	X
S_{3G}	S_{4e}	X
S_{3H}	S_{4g}	X
S_{3I}	S_1	X
S_{4C}	S_5	X
S_5	S1	X

STATE TRANSITION DIAGRAM:


RESET
RESET
S1
ADx, NDx, BEQ, SW
SM, LM
LW
LHI
JAL, JLR
S2a
S2b
S2c
S2d
S2e
ADD, ADC, ADZ, NDx
ADI
BEQ
SW
LW
SM
LM
LW
LHI
BEQ
JAL
JLR
S3a
S3b
S3c
S3d
S3e
S3f
S3g
S3h
S3i
LW
SW
LHI
BEQ
JAL
S4a
S4b
S4c
S4d
S4e
S4f
ADx, NDx
LW
S5