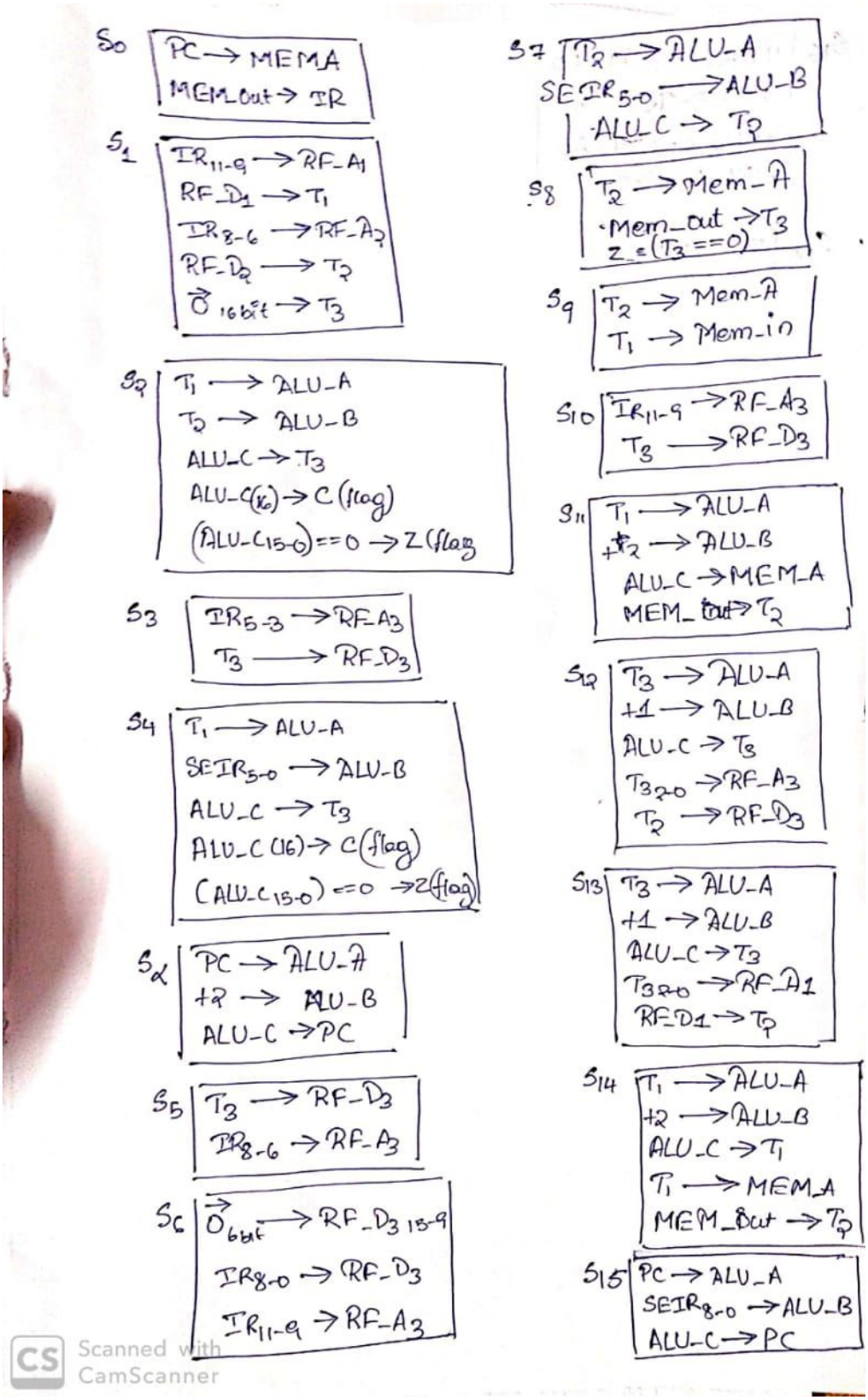
Digital Project Design

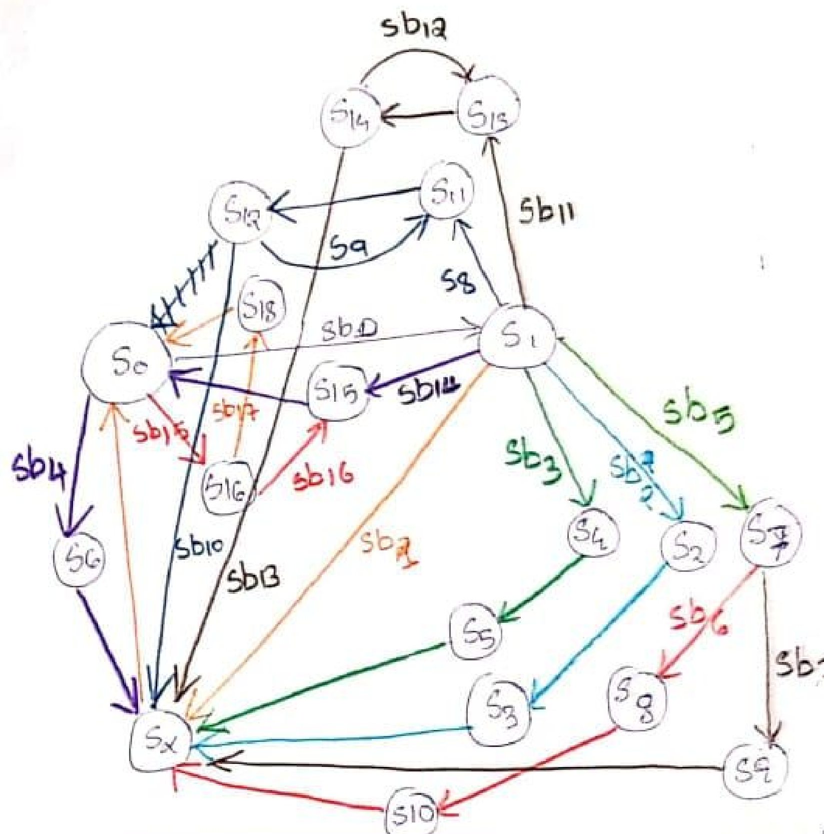
Data Path



S16 $IR_{11-9} \rightarrow RF\_A_3$
$PC \rightarrow RF\_D_3$
$IR_{8-6} \rightarrow RF\_A_2$
$RF\_D_2 \rightarrow T_2$

S18 $T_2 \rightarrow PC$

State Diagram



Sb0 – $\overline{op = 0011 \text{ or } 1000 \text{ or } 1001}$ or [(RF_D xor RF_D) op=1100]

Sb1 – (opcode = 0000 or 0010) ($\overline{IR=10}\,\overline{C}$ or $\overline{(IR=01)}\,\overline{Z}$)

Sb2 – ~~[op = 0000 or 0010]~~ (op = 0000 / 0010) ($(IR_{10}=10)\overline{C} + (IR_{10}=01)Z + (IR_{10}=00)$)

Sb3 – [op = 0001]

Sb4 – [op = 0011]

Sb5 – [op = 0100 or 0101]

Sb6 – [op = 0100]

Sb7 – [op = 0101]

Sb8 – [op = 0110]

Sb9 – $\overline{T_{2-0} = 111}$

Sb10 = $T_{2-0} = 111$

Sb11 = [op = 0111]

Sb12 = $\overline{T_{2-0} = 000}$

Sb13 = $T_{2-0} = 000$

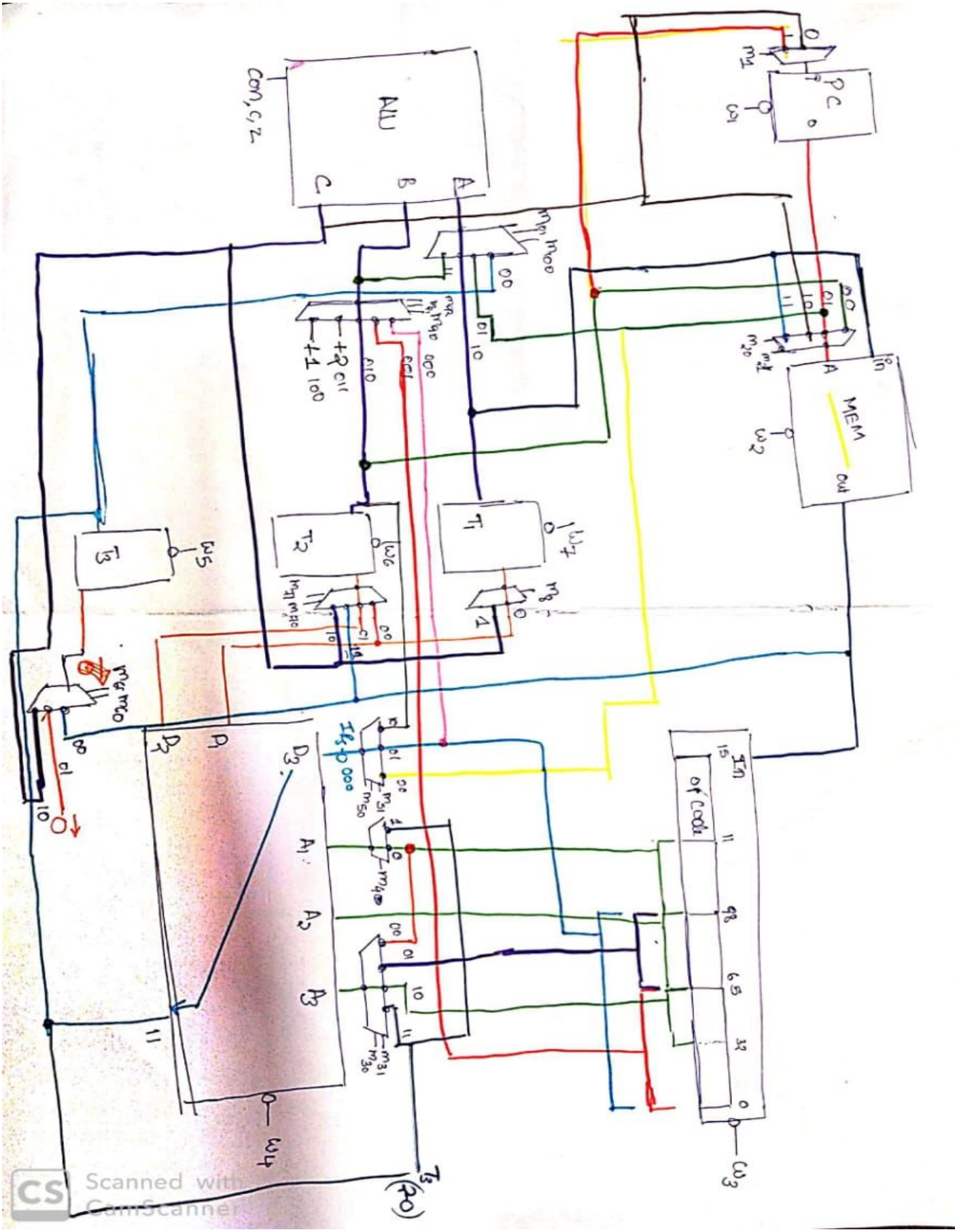
Sb14 = [~~op = 1000~~] [$\overline{RF\_D_1 \text{ xor } RF\_D_2}$] op=1100

Sb15 = [op = 1000 or 1001]

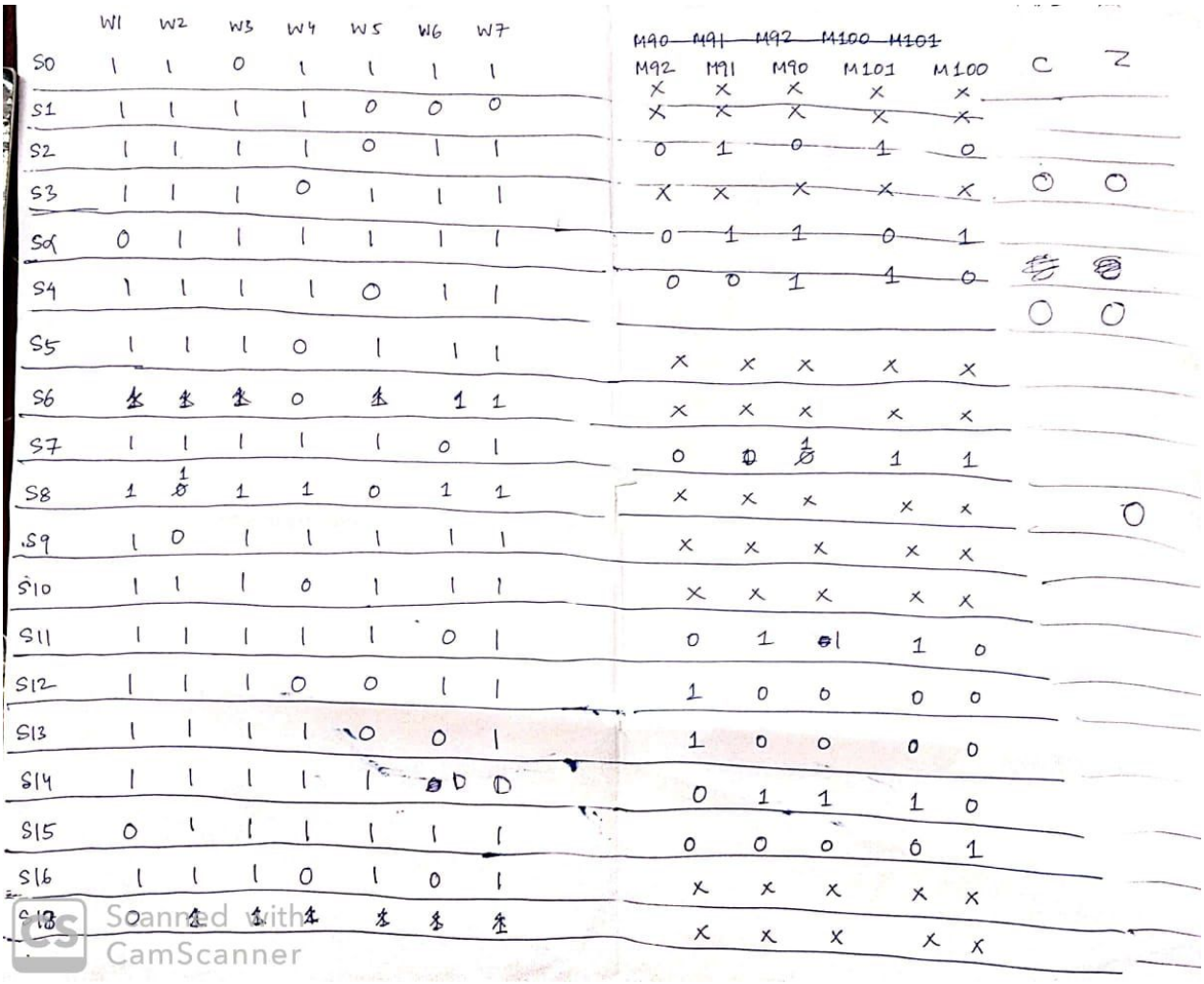
Sb16 = [op = 1000]

~~[illegible]~~ Sb17 = [op = 1001]

Circuit Diagram



Control Pin Assignment



	W1	W2	W3	W4	W5	W6	W7	M92	M91	M90	M101	M100	C	Z
S0	1	1	0	1	1	1	1	X	X	X	X	X		
S1	1	1	1	1	0	0	0	X	X	X	X	X		
S2	1	1	1	1	0	1	1	0	1	0	1	0		
S3	1	1	1	0	1	1	1	X	X	X	X	X	0	0
S4	0	1	1	1	1	1	1	0	1	1	0	1		
S4	1	1	1	1	0	1	1	0	0	1	1	0		
S5	1	1	1	0	1	1	1	X	X	X	X	X	0	0
S6	X	X	X	0	X	1	1	X	X	X	X	X		
S7	1	1	1	1	1	0	1	0	0	1	1	1		
S8	1	0	1	1	0	1	1	X	X	X	X	X	0	
S9	1	0	1	1	1	1	1	X	X	X	X	X		
S10	1	1	1	0	1	1	1	X	X	X	X	X		
S11	1	1	1	1	1	0	1	0	1	1	1	0		
S12	1	1	1	0	0	1	1	1	0	0	0	0		
S13	1	1	1	1	0	0	1	1	0	0	0	0		
S14	1	1	1	1	1	0	0	0	1	1	1	0		
S15	0	1	1	1	1	1	1	0	0	0	0	1		
S16	1	1	1	0	1	0	1	X	X	X	X	X		
S17	X	X	X	X	X	X	X	X	X	X	X	X