Programmable Timer/Counter

GENERAL DESCRIPTION

The XR-2240 Programmable Timer/Counter is a monolithic controller capable of producing ultra-long time delays without sacrificing accuracy. In most applications, it provides a direct replacement for mechanical or electromechanical timing devices and generates programmable time delays from micro-seconds up to five days. Two timing circuits can be cascaded to generate time delays up to three years.

As shown in Figure 1, the circuit is comprised of an internal time-base oscillator, a programmable 8-bit counter and a control flip-flop. The time delay is set by an external R-C network and can be programmed to any value from 1 RC to 255 RC.

In astable operation, the circuit can generate 256 separate frequencies or pulse-patterns from a single RC setting and can be syncronized with external clock signals. Both the control inputs and the outputs are compatible with TTL and HCMOS logic levels.

FEATURES

Timing from micro-seconds to days
Programmable delays: 1RC to 255 RC
Wide supply range; 4V to 15V
TTL and DTL compatible outputs
High accuracy: 0.5%
External Sync and Modulation Capability
Excellent Supply Rejection: 0.2%/V

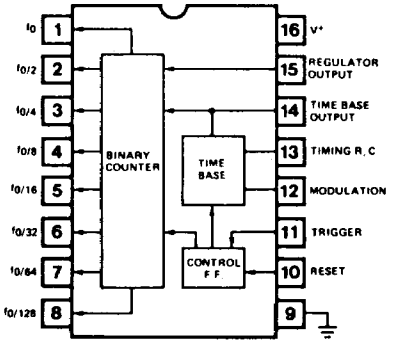
APPLICATIONS

Precision Timing	Frequency Synthesis
Long Delay Generation	Pulse Counting/Summing
Sequential Timing	A/D Conversion
Binary Pattern Generation	Digital Sample and Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mw/°C
Plastic Package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2240M	Ceramic	−55°C to +125°C
XR-2240N	Ceramic	0°C to +70°C
XR-2240CN	Ceramic	0°C to +70°C
XR-2240P	Plastic	0°C to +70°C
XR-2240CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2240 is a combination timer/counter capable of generating accurate timing intervals ranging from microseconds through several days. The time base works as an astable multivibrator with a period equal to RC. The eight bit counter can divide the time base output by any integer value from 1 to 255. The wide supply voltage range of 4.5 to 15 V, TTL and HCMOS logic compatibility, and 0.5% accuracy allow wide applicability. The counter may operate independently of the time base. Counter outputs are open collector and may be wire or connected.

The circuit is triggered or reset with positive going pulses. By connecting the reset pin (Pin 10) to one of the counter outputs, the time base will halt at timeout. If none of the outputs are connected to the reset, the circuit will continue to operate in the astable mode. Activating the trigger terminal (Pin 11) while the timebase is stopped will set all counter outputs to the low state and start the timebase.

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, $R = 10\ k\Omega$, $C = 0.1\ \mu F$, unless otherwise noted.

PARAMETERS	XR-2240 MIN	XR-2240 TYP	XR-2240 MAX	XR-2240C MIN	XR-2240C TYP	XR-2240C MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4		15	4		15	V	For $V^+ < 4.5V$, Short Pin 15 to Pin 16
Supply Current								
Total Circuit		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Counter Only		1			1.5		mA	See Figure 3
Regulator Output, V_R	4.1	4.4		3.9	4.4		V	Measured at Pin 15, $V^+ = 5V$
	6.0	6.3	6.6	5.8	6.3	6.8	V	$V^+ = 15V$, See Figure 4
TIME BASE SECTION								See Figure 2
Timing Accuracy*		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ $0°C \le T \le 75°C$
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \ge 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	$R = 1\ k\Omega$, $C = 0.007\ \mu F$
Modulation Voltage Level								Measured at Pin 12
	3.00	3.50	4.0	2.80	3.50	4.20	V	V^+ 5V
		10.5			10.5		V	$V^+ = 15V$
TRIGGER/RESET CONTROLS								
Trigger								Measures at Pin 11, $V_{RS} = 0$
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time**		1			1		μsec.	
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time**		0.8			0.8		μsec.	
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Measured at Pin 14
Input:								
Impedance		20			20		kΩ	
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 8
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10\ pF$
Fall Time		180			180		nsec.	
Sink Current	3	5		2	4		mA	$V_{OL} \le 0.4V$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$

*Timing error solely introduced by XR-2240, measured as % of ideal time-base period of T = 1.00 RC.
**Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at pin 1.

Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	

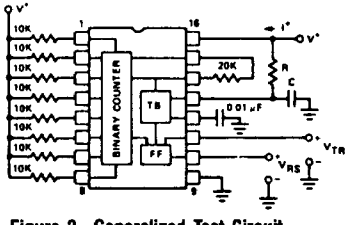


Figure 2. Generalized Test Circuit

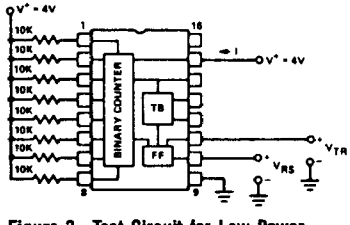


Figure 3. Test Circuit for Low-Power Operation (Time-Base Powered Down)

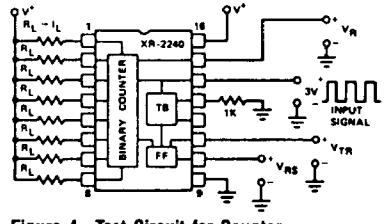


Figure 4. Test Circuit for Counter Section

PRINCIPLES OF OPERATION

The timing cycle for the XR-2240 is initiated by applying a positive-going trigger pulse to pin 11. The trigger input actuates the time-base oscillator, enables the counter section, and sets all the counter outputs to "low" state. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to pin 10.

Figure 5 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is at reset state, both the time-base and the counter sections are disabled and all the counter outputs are at "high" state.

In most timing applications, one or more of the counter outputs are connected back to the reset terminal, as shown in Figure 6, with S_1 closed. In this manner, the circuit will start timing when a trigger is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S_1 open), the circuit would operate in its astable or free-running mode, subsequent to a trigger input.

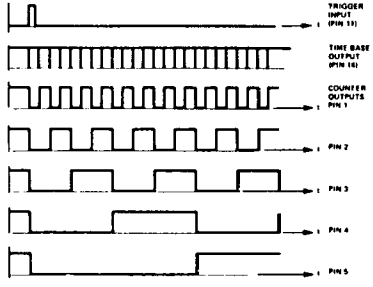


Figure 5. Timing Diagram of Output Waveforms

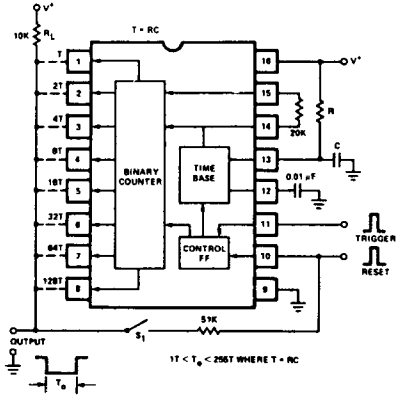


Figure 6. Generalized Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

PROGRAMMING CAPABILITY

The binary counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-or" connection. The combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be *summed* by simply shorting them together to a common output bus as shown in Figure 6. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_0, would be 32T. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_0 = (1 + 16 + 32)\,T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be: $1T \leq T_0 \leq 255T$, where $T = RC$.

TRIGGER AND RESET CONDITIONS

When power is applied to the XR-2240 with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously trigger overrides reset.

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

The binary counter outputs are buffered "open-collector" type stages, as shown in Figure 15. Each output is capable of sinking ≈ 5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 5.

The counter outputs can be used individually, or can be connected together in a "wired-or" configuration, as described in the Programming section.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11. The threshold level for these controls is approximately two diode drops (≈1.4V) above ground.

Minimum pulse widths for reset and trigger inputs are shown in Figure 10. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle. Figure 12 should be referenced for time between reset and trigger.

MODULATION AND SYNC INPUT (PIN 12)

The period T of the time-base oscillator can be modulated by applying a dc voltage to this terminal (see Figure 13). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12, as shown in Figure 16. Recommended sync pulse widths and amplitudes are also given in the figure.

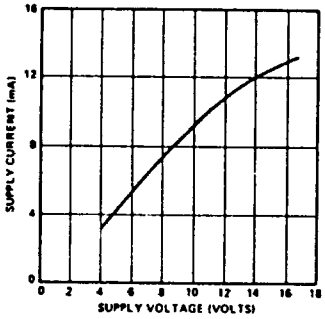


Figure 7. Supply Current vs. Supply Voltage in Reset Condition (Supply Current Under Trigger Condition is ≈0.7 mA less)

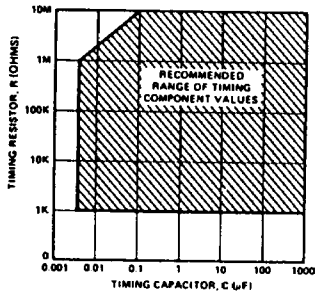


Figure 8. Recommended Range of Timing Component Values.

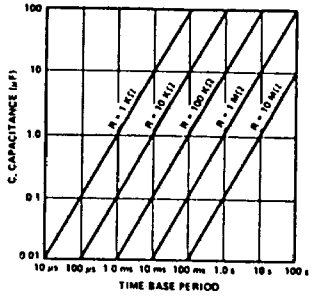


Figure 9. Time-Base Period, T, as a Function of External RC

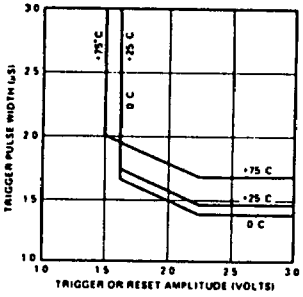


Figure 10. Minimum Trigger and Reset Pulse Widths at Pins 10 and 11

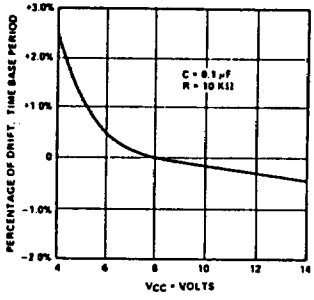


Figure 11. Power Supply Drift

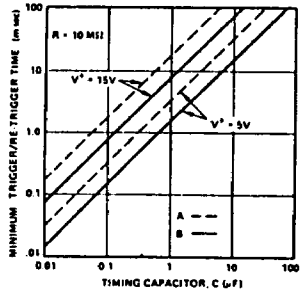


Figure 12.
A) Minimum Trigger Delay Time Subsequent to Application of Power
B) Minimum Re-trigger Time, Subsequent to a Reset Input

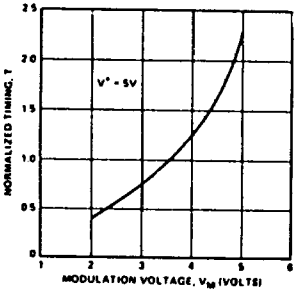
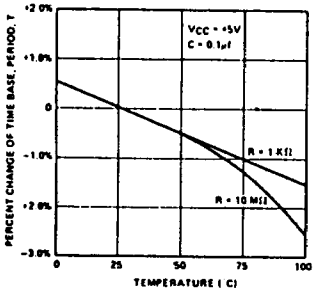


Figure 13. Normalized Change in Time-Base Period As a Function of Modulation Voltage at Pin 12



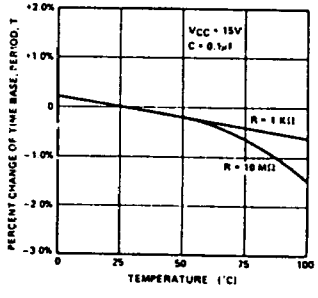


Figure 14. Temperature Drift of Time-Base Period, T

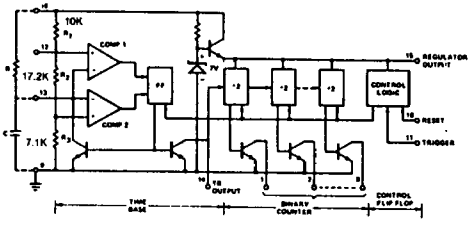


Figure 15. Simplified Circuit Diagram of XR-2240

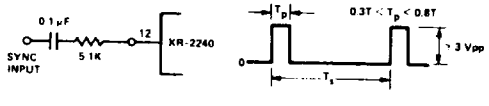


Figure 16. Operation with External Sync Signal.
(a) Circuit for Sync Input
(b) Recommended Sync Waveform

HARMONIC SYNCHRONIZATION

Time-base can be synchronized with *integer multiples or harmonics* of input sync frequency, by setting the time-base period, T, to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m) \text{ where}$$

$$m \text{ is an integer, } 1 \leq m \leq 10.$$

Figure 17 gives the typical pull-in range for harmonic synchronization, for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

TIMING TERMINAL (PIN 13)

The time-base period T is determined by the external R-C network connected to this pin. When the time-base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC. A 1KΩ resistor to ground should be placed on this pin to disable the timebase.

TIME-BASE OUTPUT (PIN 14)

Time-Base output is an open-collector type stage, as shown in Figure 15 and requires a 20 KΩ pull-up resistor to Pin 15 for proper operation of the circuit. At reset state, the time-base output is at "high" state. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 5.

Time-base output is internally connected to the binary counter section and also serves as the input for the external clock signal when the circuit is operated with an external time-base.

The counter input triggers on the negative-going edge of the timing or clock pulses applied to pin 14. The trigger threshold for the counter section is ≈ +1.5 volts. The counter section can be disabled by clamping the voltage level at pin 14 to ground.
Note:
*Under certain operating conditions such as high supply voltages ($V^+ > 7V$) and small values of timing capacitor ($C < 0.1\ \mu F$) the pulse-width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a **620 pF** capacitor from pin 14 to ground.*

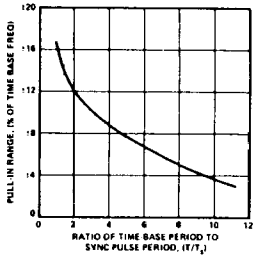


Figure 17. Typical Pull-In Range for Harmonic Synchronization

REGULATOR OUTPUT (PIN 15)

This terminal can serve as a V^+ supply to additional XR-2240 circuits when several timer circuits are cascaded (See Figure 20), to minimize power dissipation. For circuit operation with external clock, pin 15 can be used as the V^+ terminal to power-down the internal time-base and reduce power dissipation. The output current shall not exceed 10 mA.

When the internal time-base is used with $V^+ \leq 4.5V$, pin 15 should be short to pin 16. For wide temperature application and if V+ = 5 VDC pin 15 should be tied to pin 16.

APPLICATIONS INFORMATION

PRECISION TIMING (Monostable Operation)

In precision timing applications, the XR-2240 is used in its monostable or "self-resetting" mode. The generalized circuit connection for this application is shown in Figure 18.

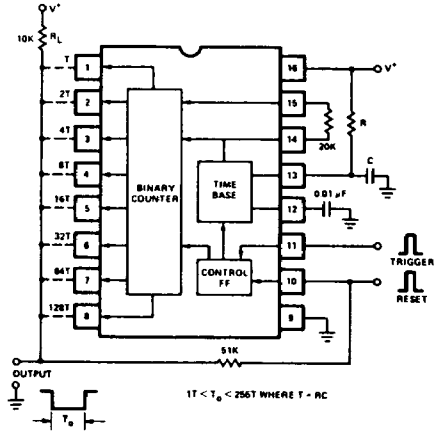


Figure 18. Circuit for Monostable Operation (T_0 = NRC where $1 \leq N \leq 255$)

The output is normally "high" and goes to "low" subsequent to a trigger input. It stays low for the time duration T_0 and then returns to the high state. The duration of the timing cycle T_0 is given as:

$$T_O = NT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at pin 13 (See Figure 9). N is an integer in the range of:

$$1 \leq N \leq 255$$

as determined by the combination of counter outputs (pins 1 through 8) connected to the output bus, as described below.

PROGRAMMING OF COUNTER OUTPUTS: The binary counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-or" connection where

the combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output bus as shown in Figure 18. For example if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_0, would be 32T. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_0 = (1 + 16 + 32)\,T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be: $1T \leq T_0 \leq 255T$.

ULTRA-LONG DELAY GENERATION

Two XR-2240 units can be cascaded as shown in Figure 19 to generate extremely long time delays. In this application, the reset and the trigger terminals of both units are tied together and the time base of Unit 2 disabled. In this manner, the output would normally be high when the system is at reset. Upon application of a trigger input, the output would go to a low stage and stay that way for a total of $(265)^2$ or 65,536 cycles of the time-base oscillator.

PROGRAMMING: Total timing cycle of two cascaded units can be programmed from $T_0 = 256RC$ to $T_0 = 65{,}536RC$ in 256 discrete steps by selectively shorting any one or the combination of the counter outputs from Unit 2 to the output bus.

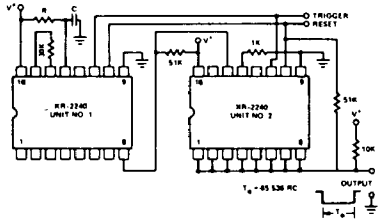


Figure 19. Cascaded Operation for Long Delay Generation

LOW-POWER OPERATION

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption, by using the circuit connection of Figure 20. In this case, the V^+ terminal (pin 16) of Unit 2 is left open-circuited, and the second unit is powered from the regulator output of Unit 1, by connecting pin 15 of both units.

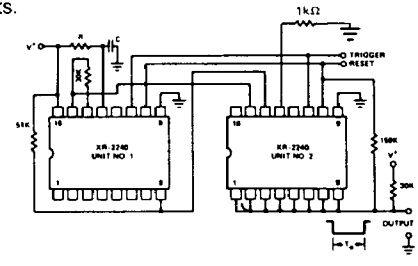


Figure 20. Low-Power Operation of Cascaded Timers

ASTABLE OPERATION

The XR-2240 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 10) from the counter outputs. Two typical circuit connections for this mode of operation are shown in Figure 21. In the circuit connection of Figure 21(a), the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its rest state. The circuit of Figure 21(a) is essentially the same as that of Figure 6, with the feedback switch S_1 open.

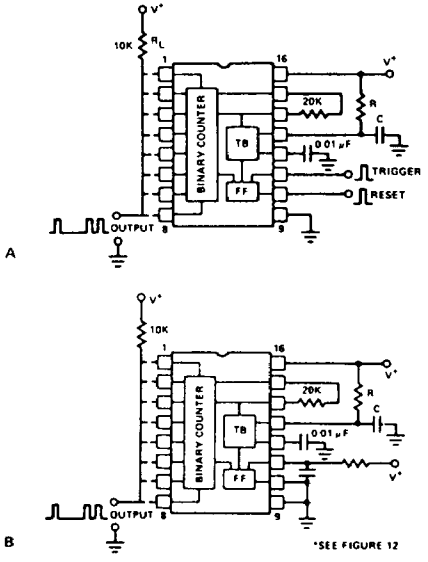


Figure 21. Circuit Connections for Astable Operation
(a) Operation with External Trigger and Reset Controls
(b) Free-running or Continuous Operation

The circuit of Figure 21(b) is designed for continuous operation. The circuit self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

In astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators; or they can be interconnected to generate complex pulse patterns.

BINARY PATTERN GENERATION

In astable operation, as shown in Figure 21, the output of the XR-2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 5 which shows the phase relations between the counter outputs. Figure 22 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected

to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

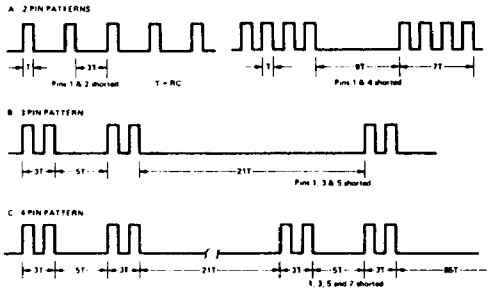


Figure 22. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

OPERATION WITH EXTERNAL CLOCK

The XR-2240 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 14. The recommended circuit connection for this application is shown in Figure 23. The internal time-base can be deactivated by connecting a 1 KΩ resistor from pin 13 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be ≥ 1 μS. **The external clock must have a duty cycle of 50% or more.**

For operation with supply voltages of 6V or less, the internal time-base section can be powered down by open-circuiting pin 16 and connecting pin 15 to V+. In this configuration, the internal time-base does not draw any current, and the over-all current drain is reduced by ≈ 3 mA. **The pulse width of the trigger must be at least 60% of the period of the external clock for reliable operation.**

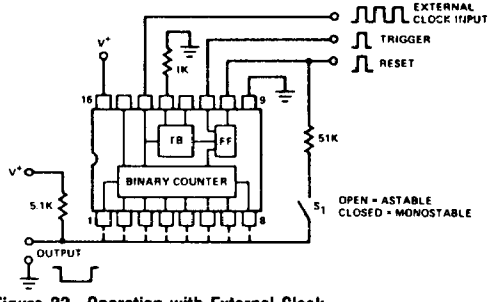


Figure 23. Operation with External Clock

FREQUENCY SYNTHESIZER

The programmable counter section of XR-2240 can be used to generate 255 discrete frequencies from a given time base setting using the circuit connection of Figure 24. The output of the circuit is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) T where N is the programmed count in the counter.

The modulus N is the *total count* corresponding to the counter outputs connected to the output bus. Thus, for example, if pins 1, 3 and 4 are connected together to the output bus, the total count is: N = 1 + 4 + 8 = 13; and the period of the output waveform is equal to (N + 1) T or 14T. In this manner, 256 different frequencies can be synthesized from a given time-base setting.

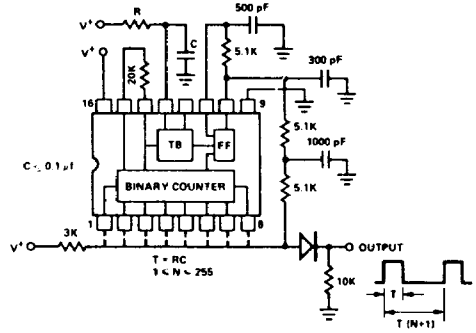


Figure 24. Frequency Synthesis from Internal Time-Base

SYNTHESIS WITH HARMONIC LOCKING: The harmonic synchronization property of the XR-2240 time-base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in Figure 25. (See Figures 16 and 17 for external sync waveform and harmonic capture range.) If the time base is synchronized to (m)th harmonic of input frequency where 1 ≤ m ≤ 10, as described in the section on "Harmonic Synchronization", the frequency f_O of the output waveform in Figure 25 is related to the input reference frequency f_R as:

$$f_O = f_R \frac{m}{(N + 1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of 1 ≤ N ≤ 255, the circuit of Figure 25 can produce 1500 separate frequencies from a single fixed reference.

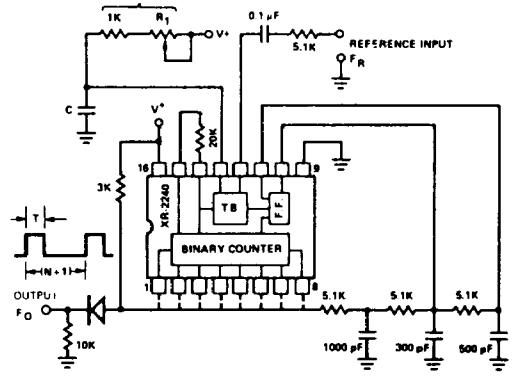


Figure 25. Frequency Synthesis by harmonic Locking to an External Reference

One particular application of the circuit of Figure 25 is generating frequencies which are not harmonically related to a reference input. For example, by choosing the external R-C to set m = 10 and setting N = 5, one can obtain a 100 Hz output frequency synchronized to 60 Hz power line frequency.

STAIRCASE GENERATOR

The XR-2240 Timer/Counter can be interconnected with an external operational amplifier and a precision resistor ladder to form a staircase generator, as shown in Figure 26. Under reset condition, the output is low. When a trigger is applied, the op. amp. output goes to a high state and generates a negative going staircase of 256 equal steps. The time duration of each step is equal to the time-base period T. The staircase can be stopped at any desired level by applying a "disable" signal to pin 14, through a steering diode, as shown in Figure 26. The count is stopped when pin 14 is clamped at a voltage level less than 1.4V.

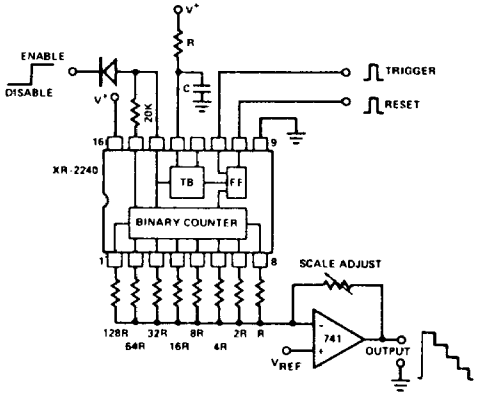


Figure 26. Staircase Generator

DIGITAL SAMPLE/HOLD

Figure 27 shows a digital sample and hold circuit using the XR-2240. The principle of operation of the circuit is similar to the staircase generator described in the previous section. When a "strobe" input is applied, the RC low-pass network between the reset and the trigger inputs of XR-2240 causes the timer to be first reset and then triggered by the same strobe input. This strobe input also sets the output of the bistable latch to a high state and activates the counter.

The circuit generates a staircase voltage at the output of the op. amp. When the level of the staircase reaches that of the analog input to be sampled, comparator changes state, activates the bistable latch and stops the count. At this point, the voltage level at the op. amp. output corresponds to the sampled analog input. Once the input is sampled, it will be held until the next strobe signal. Minimum re-cycle time of the system is ≈6 msec.

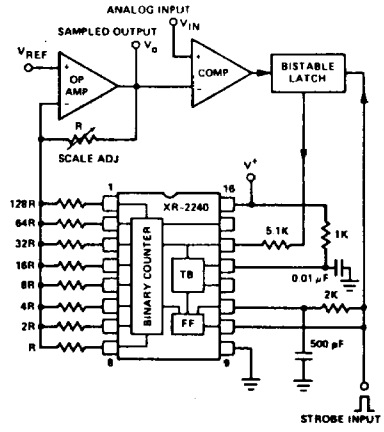


Figure 27. Digital Sample and Hold Circuit

ANALOG-TO-DIGITAL CONVERTER

Figure 28 shows a simple 8-bit A/D converter system using the XR-2240. The operation of the circuit is very similar to that described in connection with the digital sample/hold system of Figure 15. In the case of A/D conversion, the digital output is obtained in parallel format from the binary counter outputs, with the output at pin 8 corresponding to the most significant bit (MSB). The re-cycle time of the A/D converter is ≈6 msec.

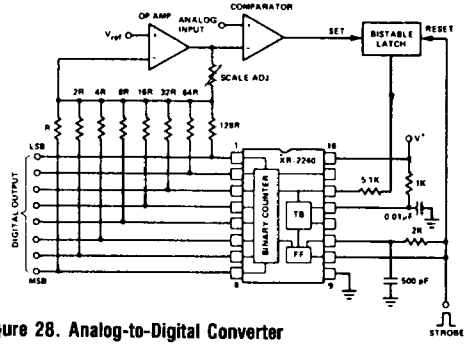
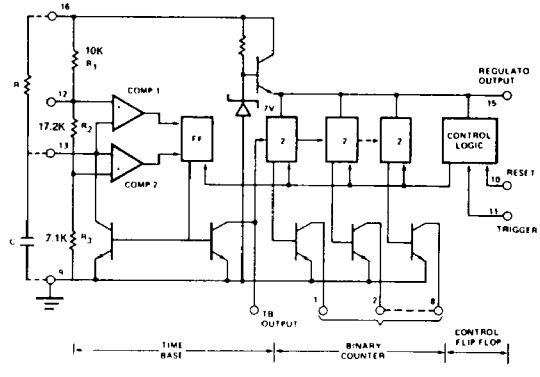


Figure 28. Analog-to-Digital Converter



EQUIVALENT SCHEMATIC DIAGRAM