# Course Title: Processing & Fabrication Technology Course No.: EEE 707

VLSI Class lecture -5

# **Introduction to Wafer Cleaning**

# Wafer cleaning and photoresist stripping

- ICs are so sensitive to contaminate.
- The wafer fabrication process may be broadly broken up into front end of line (FEOL) and back end of line (BEOL).
- The FEOL is focused on the fabrication of the different devices that make up the circuit.
- ▶ BEOL is focused on interconnecting the devices.
- In FEOL cleaning, the surfaces being cleaned are typical silicon (Si) of silicon dioxide (SiO₂).
- In BEOL cleaning, metal layers are present on the wafers and the allowable cleaning solutions are limited versus FEOL cleaning.

# Front-end-of-line (FEOL)

- The front-end-of-line (FEOL) is the first portion of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) are patterned in the semiconductor. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers.
- ▶ FEOL contains all processes of CMOS fabrication needed to form fully isolated CMOS elements:
  - Selecting the type of wafer to be used; Chemical-mechanical planarization and cleaning of the wafer.
  - Shallow trench isolation (STI)
  - Well formation
  - Gate module formation
  - Source and drain module formation

# **Back-end-of-line (BEOL)**

- ▶ The back end of line (BEOL) is the second portion of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) get interconnected with wiring on the wafer.
- BEOL generally begins when the first layer of metal is deposited on the wafer. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chipto-package connections.
- After the last FEOL step, there is a wafer with isolated transistors (without any wires). In BEOL part of fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed. For modern IC process, more than 10 metal layers can be added in the BEOL.

# **Wafer Surface Types**

Generally, Cleaning surfaces are two types:

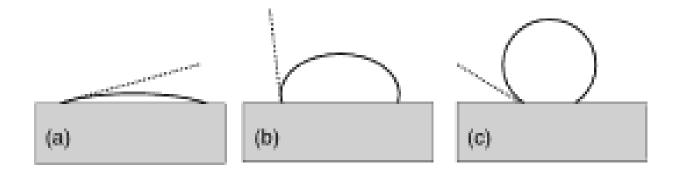
- Hydrophilic
- Hydrophobic

# **Hydrophilic and Hydrophobic Surfaces**

- ▶ Hydrophilic surfaces are easily wet by cleaning solutions and during drying any particles on the surface tend to stay in solution until the solution is removed from the surface.
  - SiO<sub>2</sub> surfaces are hydrophilic.
- Hydrophobic surface are more difficult to clean, cleaning solution do not wet as well and during drying the solutions tend to "bead" up on the surface leaving particles on the surface instead of keeping the particles in solution.
  - Si surface free of oxide are hydrophobic.

### Hydrophilic and Hydrophobic Surfaces...

Hydrophilic surfaces have contact angles (CA) < 90°, and Hydrophobic surfaces > 90°. High contact angles indicate low surface energies and vice versa.



(a) Hydrophilic surface, 20°, (b) Hydrophobic surface, 95°, (c) Ultra hydrophobic surface, 150°

#### The RCA Clean

- In 1970 the first systematically developed wafer cleaning process for bare and oxidized Si was published by Werner Kern of RCA. The clean that Kern disclosed had been in use at RCA since 1965 and went on to become known as the "RCA clean". The most widely used clean in the industry.
- The RCA clean is a FEOL clean.

#### The RCA Clean...

- ▶ The original RCA clean sequence is:
  - ▶ Standard clean 1 (SC1) 5 volumes of  $H_2O$ , 1 volume Hydrogen peroxide ( $H_2O_2$ ) 30%, 1 volume Ammonium hydroxide ( $NH_4OH$ ) 29% at 70-80C.
  - Ultrapure water rinse
  - ▶ Standard clean 2 (SC2) 6 volumes  $H_2O$ , 1 volume  $H_2O_2$  30%, 1 volume Hydrochloric (HCl) 37% at 70C.
  - Ultrapure water rinse and dry.
- ▶ The SC1 clean removes organic residues and particles. The SC1 clean works by forming and dissolving hydro oxide films. The SC2 clean removes alkali metal and hydroxides Li, Al, Ti, Zn, Cr, Fe, Ag, Pd, Au, S, Cu, Ni, Co, Mg, Nb, Te, W, Na, Fe (leaves Cl residues).

#### The RCA Clean...

- Several variants of the RCA clean have been used in the industry. Prior to 1997 a typical implementation would be:
  - Sulfuric peroxide (SPM) 4 volumes of sulfuric acid ( $H_2SO_4$ ) 98%, 1 volume  $H_2O_2$  30% at 130°C for 10 to 15 minutes.
  - Ultrapure water rinse
  - ▶ Dilute hydrofluoric acid (DHF) 50 volumes H<sub>2</sub>O, 1 volume hydrofluoric acid (HF) 49% at room temperature for 10 seconds.
  - Ultrapure water rinse
  - SC1 for 20 minutes
  - Ultrapure water rinse
  - SC2 for 15 minutes
  - Ultrapure water rinse and dry
- In the preceding sequences the SPM performs bulk organic removal and chemically oxidizes the wafer surface. The DHF removes the chemical oxide, SC1 removes particles and SC2 removes metals.

#### **IMEC Clean**

- ▶ IMEC (Interuniversity Microelectronics Center) has done a great deal of research into cleaning technologies. One of the major findings of the IMEC work is that dilute versions of SC1 and SC2 are still effective cleans. Dilute chemistries can be result in significant reductions in chemical consumption and thus lower costs and environmental impact. IMEC has developed a roadmap of cleaning technology.
- ▶ The IMEC roadmap:
  - RCA clean
  - Dilute clean
  - Reduced clean (IMEC)
  - Reduce clean (IMEC Ozone)
  - Next Generation cleans

#### **IMEC Clean...**

RCA
Clean
<b>↓</b>
Dilute
clean
<b>↓</b>
Reduced
clean (IMEC)
<b>1</b>
Reduced Clean
(IMEC-Ozone)
<b>1</b>
Single tank
<b>↓</b>

Single wafer

wet clean

H <sub>2</sub> SO <sub>4</sub>	Rinse	HF	Rinse	Meg	Rinse	HCI	Meg
+				NH₄OH		+ H <sub>2</sub> O <sub>2</sub>	Rinse
H <sub>2</sub> O <sub>2</sub>				+ H <sub>2</sub> O <sub>2</sub>			
H <sub>2</sub> SO <sub>4</sub>	Rinse	HF	Rinse	Meg	Rinse	Dilute	Meg
+				dilute		HCl	Rinse
O <sub>3</sub>				NH₄OH		+ H <sub>2</sub> O <sub>2</sub>	
				+ H <sub>2</sub> O <sub>2</sub>			
H <sub>2</sub> SO <sub>4</sub>	Rinse	HF	Rinse +	Rinse +			
+		+	oxide	Marango			
O <sub>3</sub>		HCI	re-grow	ni			
				Dry			
H <sub>2</sub> O	HF	Rinse +	Rinse +				
+	+	oxide	Marangon				
$O_3$	HCl	re-	i				
		grow	Dry				
Single	tank						
clean							
Single v	wafer						

Dry

Marang -oni Dry

Hybrid wet/dry cleans in cluster tool configuration

clean

#### **Contaminants**

The contaminants of concern during IC fabrication can be grouped into five general categories:

- Particles
- 2. Metals
- 3. Organics
- Native oxide
- 5. Micro-roughness

# **Cleaning Chemicals**

Chemical	Formula			
Acetic acid	CH₃COOH			
Ammonium Fluoride	NH <sub>4</sub> F			
Ammonium Hydroxide	NH <sub>4</sub> OH			
Hydrochloric acid	HCI			
Hydrofluoric acid	HF			
Hydrogen peroxide	$H_2O_2$			
Isopropyl alcohol, IPA or 2-Propanol	CH <sub>3</sub> CHOHCH <sub>3</sub>			
Methanol	CH <sub>3</sub> OH			
Nitric acid	HNO <sub>3</sub>			
Sulfuric acid	H <sub>2</sub> SO <sub>4</sub>			

# **Evolution of cleaning**

The requirements outlined in table (Cleaning Chemical) are driving continual improvements in cleaning chemistries. The need to reach ever higher level of cleanliness without surface damage are difficult to achieve. Standard SC1 chemistries remove particles well but also remove silicon (Si) and can roughen the surface. Dilute chemistries, new chemistries, highly optimized megasonics and drying techniques are also required. There is also a continuing push to move to dry cleaning techniques for easier process integration and waste reduction.

# Introduction to Metallization and Passivation

#### Metallization

- Metallization is the process of building wires to connect the devices. Conventional metallization uses aluminum. Aluminum can be deposited either by evaporation or sputtering.
- ▶ Evaporation is performed by passing a high electrical current through a thick aluminum wire in a vacuum chamber. Some of the aluminum atoms are vaporized and deposited on the wafer.
- Sputtering is achieved by generating gas plasma by ionizing an inert gas using an RF or DC electric field. The ions are focused on an aluminum target and the plasma dislodges metal atoms, which are then deposited on the wafer.

#### Metallization...

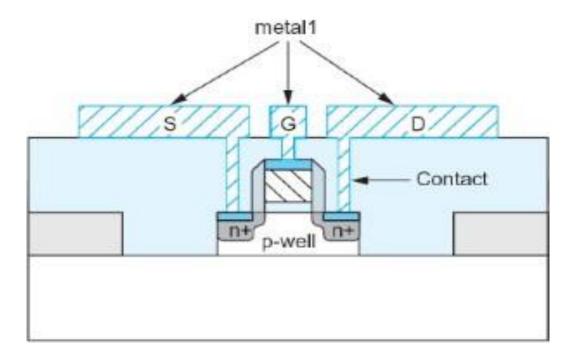


Figure: Aluminum (Al) metallization

#### **Passivation**

The final processing step is to add a protective glass layer called passivation or over glass that prevents the ingress of contaminants. Openings in the passivation layer allow connection to I/O pads and test probe points if needed. After passivation, further steps can be performed such as bumping, which allows the chip to be directly connected to a circuit board using plated solder bumps in the pad openings.