Department of Electrical and Electronic Engineering
Shahjalal University of Science and Technology

EEE 222: Electronic Circuit Simulation Laboratory
EXPERIMENT NO. 04

Name of the Experiment: STUDY OF CHARACTERISTICS OF FIELD EFFECT TRANSISTORS (FET) AND ITS APPLICATION IN CMOS INVERTER.

OBJECTIVE

The objective of this experiment is to simulate

- DC characteristics of Junction Field-Effect Transistor (JFET).
- DC characteristics of Enhancement-type Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET).
- DC characteristics of CMOS Inverter.

THE JUNCTION FIELD EFFECT TRANSISTOR (JFET)

As with other FET types, the JFET is available in 2 polarities: n-channel and p-channel. The basic structure of a n channel JFET is shown in Figure 1. The p-channel can be fabricated simply by reversing all the semiconductor types.

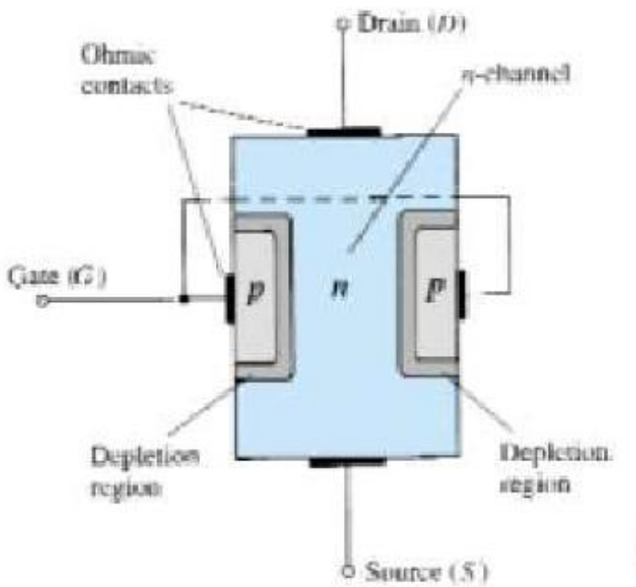


Figure 1: The Junction Field Effect Transistor (JFET)

The n region is the channel and the p-type regions are electrically connected together the gate. Thus the JFET is a 3 terminal device. When VGS=0V, the application of VDS causes current to flow from the drain to the source. When a negative VGS is applied, the depletion region of the gate-channel junction widens and the channel becomes correspondingly narrower; thus the channel resistance increases and the current ID decreases for a given VDS. One way to think of a JFET is as a resistance whose value is controlled by VGS. If VGS is increased in the negative direction, eventually a value is reached at which the depletion region occupies the entire channel. The channel has in effect disappeared (i.e. the channel is pinched), as shown in Figure 2.

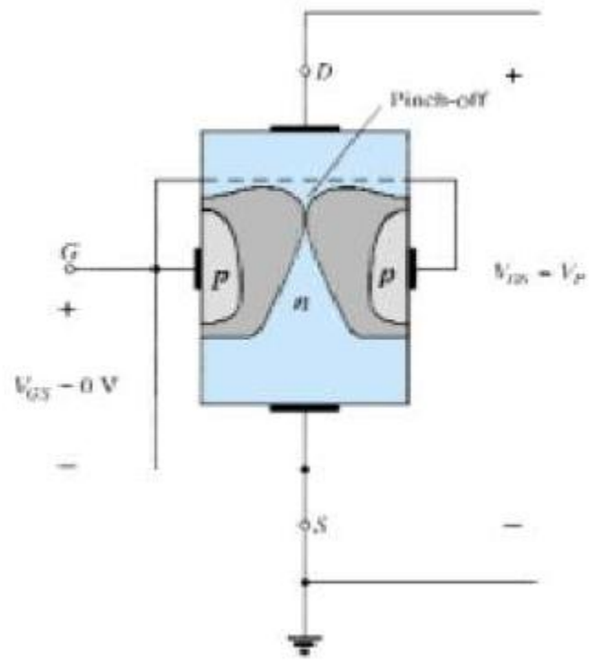


Figure 2: Pinch-off (V_{GS}=0V, V_{DS}=V_P)

The JFET characteristics are displayed in Figure 3 and Figure 4, for threshold voltage Vt=Vp=-4V, IDSS=8mA. Although Figure 4, shows ID to be independent of VDS in the saturation region, this is an ideal situation. In fact JFETs also suffer from channel-length modulation. For JFETs the threshold voltage is usually called the pinch-off voltage and is denoted by Vp, thus Vp=Vt. For n-channel JFET Vp is negative.

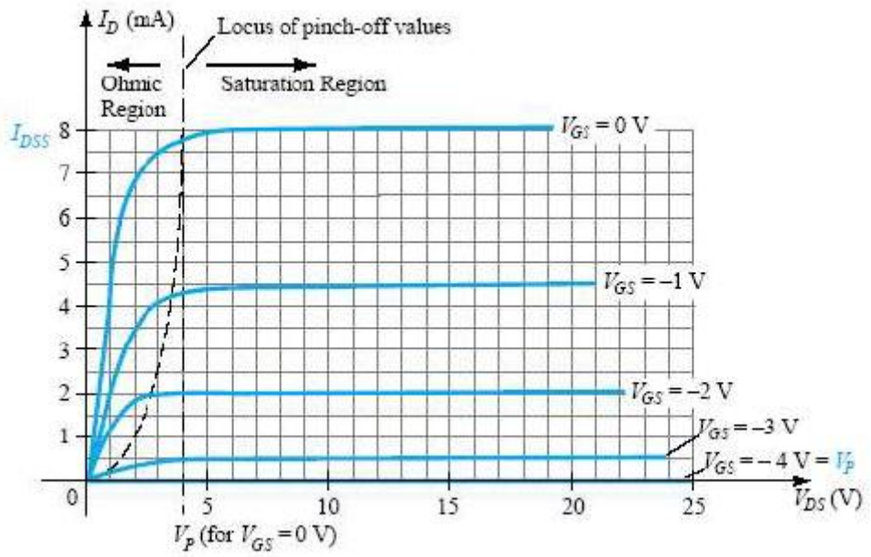


Figure 3: n-Channel JFET characteristics with I_{DSS}=8mA and Vp = - 4V

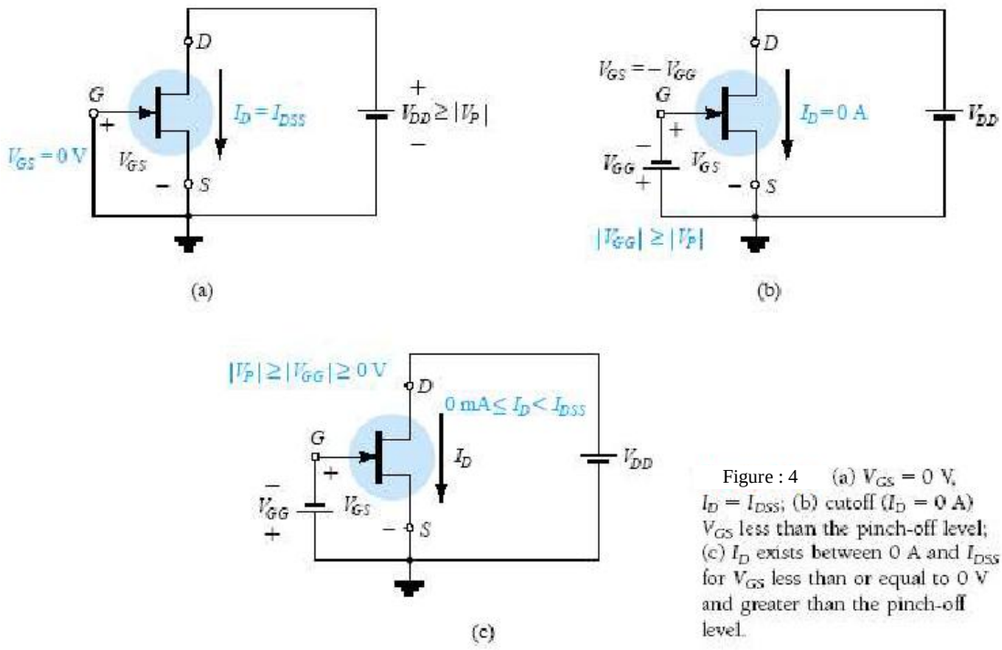


Figure : 4 (a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D exists between 0 A and I_{DSS} for V_{GS} less than or equal to 0 V and greater than the pinch-off level.

- The n-channel transistor is turned off (**cutoff region**) when vGS <= Vp. When 0 >= vGS > Vp, and vDS is positive the transistor is on.
- The transistor is said to be in the **triode region** when vDS< vGS – Vp.
- The transistor is said to be in the **saturation region** (**pinch-off**) when vDS>= vGS – Vp

The MOSFET Transistor

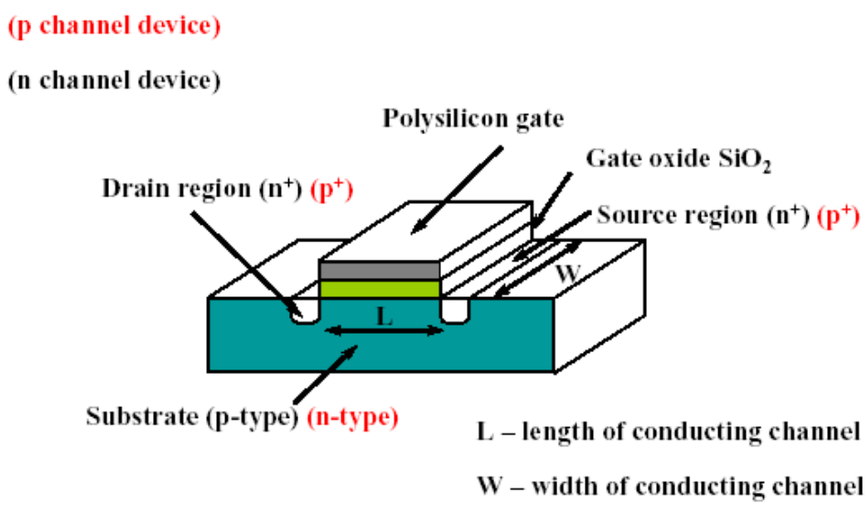
- Abbreviation of Metal Oxide Silicon Field Effect Transistor
- A three terminal device
  - Source: source of charge carriers (current)
  - Drain: sink of charge carriers (current)
  - Gate: potential (voltage) on gate controls current flow.

The basic component in a CMOS circuit is the MOSFET transistor. This transistor consists of a drain contact and a source contact with a channel in between which is doped such that it will not conduct when a potential is applied between the drain and source. It cannot conduct because it has no charge carriers of the type produced by the source electrode. If a suitable potential (voltage) is applied between the gate electrode and the source then charge is induced in the channel by the electric field set up across the gate oxide layer. This charge consists of the same type of carriers as in the source and hence the device can conduct.

By using n-type impurities in the source (electron donors) we need to induce a negative charge in the channel (initially p type material). This gives an n-channel device. On the other hand we can dope the source with p-type impurities and produce holes which act as positive charge carriers. We thus need a positive charge induced in the channel (originally n-type material) to make it conduct. This is a pchannel device.

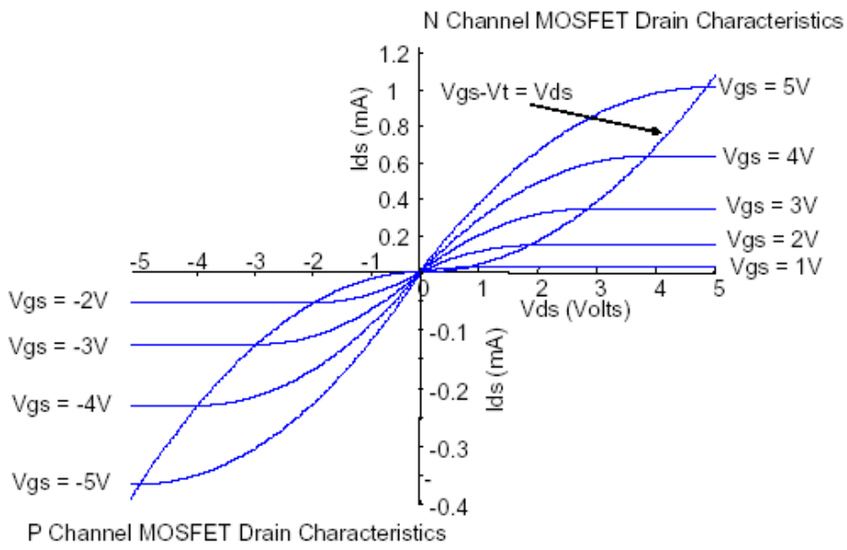
As the device is normally off and a voltage is required on the gate to make it conduct this type of MOSFET is known as an enhancement mode device. Depletion mode devices exist (normally conduct until turned off by a voltage on the gate) and these can be useful in logic circuits but not as switching elements.

Basic structure of the MOSFET



Here we see the basic construction of a MOSFET. Note the gate electrode sits above the channel and is separated from it by a thin layer of oxide. When a positive voltage is applied to the gate a negative charge is induced in the channel. If the source and drain are n-type material then they need a negative charge in the channel to make the device conduct. This is an n-channel device and the channel will initially be p-type and hence have no negative charge carriers to allow it to conduct.
The opposite is true for p-channel devices as indicated in the diagram. The major geometrical parameters (dimensions) of importance are the length of the channel
(L), the width of the channel (W) and the thickness of the gate oxide t_{ox}.

MOSFET Characteristics



If we vary the voltage between the drain and source electrode whilst keeping the gate electrode at some fixed voltage, we get the current flow shown in the graphs above.

Note that the n-channel device needs a positive voltage on its gate relative to the source to make it conduct. On the other hand the p-channel device needs a negative voltage on its gate to make it conduct. Its charge carriers are positive and hence the drain needs to be negative relative to the source in order to attract the carriers and produce a current flow. The complementary nature of these characteristics is what we exploit in a CMOS gate (Complementary Metal Oxide Silicon).

When $V_{GS} \geq V_T$, the transistor is ON. Now dependent on the value of drain voltage V_{DS}, MOSFET either operates in triode or saturation region. Before saturation, $(V_{GS}-V_{DS}) \geq V_T$ and

$$I_D \cong U_n C_o \left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V^2{}_{DS}\right]$$

In saturation region $(V_{GS}-V_{DS}) \leq V_T$ and

$$I_D = U_n C_o (\frac{W}{L})(V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

where $\lambda = \frac{1}{V_A}$ and V_A is the Early voltage, U_n is the electron mobility ($cm^2/V.s$),
C_o is the oxide capacitance per unit, W is the width of the gate and L is the Channel length.

PROCEDURE

DC Characteristics of JFET J2N3819

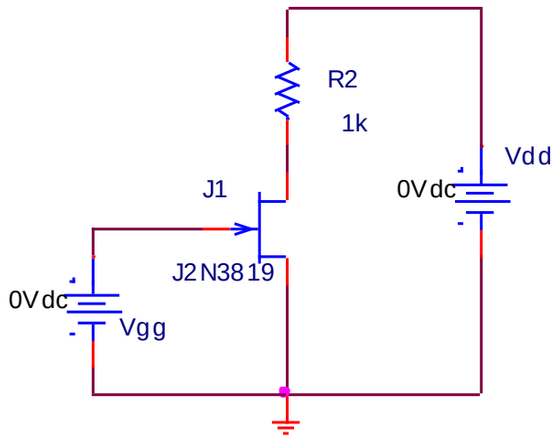


Fig.1. Circuit for DC analysis of JFET

1.1. Draw the circuit shown in Fig. 1 in PSpice schematics.

Plot of Transfer Curve of JFET

1.2. Set Vdd = 10V.

1.3. Set DC Sweep (linear) of Vgg from -5 to 0.7 volts in 0.01 volt steps.

1.4. Place a voltage marker on the drain of JFET. Run the simulation.

1.5. The transfer Curve will appear on the screen.

Plot of Output Characteristics of JFET

1.6. Here, for determining the output characteristics a nested DC Sweep of Vdd and Vgg is required. For achieving this, Select **Setup Analysis** and then **DC Sweep** from the pop-up window. Sweep first Vdd from 0 to 20V in 0.1V increments. Then click on the **Nested Sweep** button for sweeping Vgg from -4 to 0V in 1V increments. Mark the **Enable Nested Sweep** box.

1.7. After placing a current marker in the drain of the JFET, run the simulation.

1.8. Change the X-axis settings. [Plot → Axis settings → Axis variable. Then select V(J1:d) as axis variable]

1.9. Output characteristic of the JFET will appear in the probe.

1.10. Determine the pinch-off voltage of JFET for different Vgg.

DC Characteristics of Enhancement type (n)MOSFET IRF540

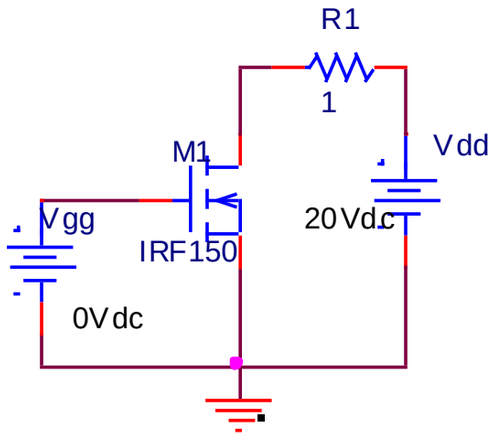


Fig.2. Circuit for DC analysis of Enhancement type (n)MOSFET

2.1. Draw the circuit shown in Fig. 2 in PSpice schematics.

Plot of Transfer Curve of n-MOSFET

2.2. Set DC Sweep (linear) of Vgg from 0 to 5 volts in 0.01 volt steps.

2.3. Place a voltage marker on the drain of n-MOSFET. Run the simulation.

2.4. The transfer Curve will appear on the screen.

2.5. Determine the threshold voltage of n-MOSFET.

Plot of Output Characteristics of n-MOSFET

2.6. Here, for determining the output characteristics a nested DC Sweep of Vdd and Vgg is required. For achieving this, Select **Setup Analysis** and then **DC Sweep** from the pop-up window. Sweep first Vdd from 0 to 20V in 0.1V increments. Then click on the **Nested Sweep** button for sweeping Vgg from 3 to 10V in 1V increments. Mark the **Enable Nested Sweep** box.

2.7. After placing a current marker in the drain of the MOSFET, run the simulation.

2.8. Change the X-axis settings. [Plot → Axis settings → Axis variable. Then select V(M1:d) as axis variable]

2.9. Output characteristic of the n-MOSFET will appear in the probe.

2.10. Determine the pinch-off voltage and early voltage of n-MOSFET for different Vgg.

DC Characteristics of Enhancement type (p)MOSFET IRF9140

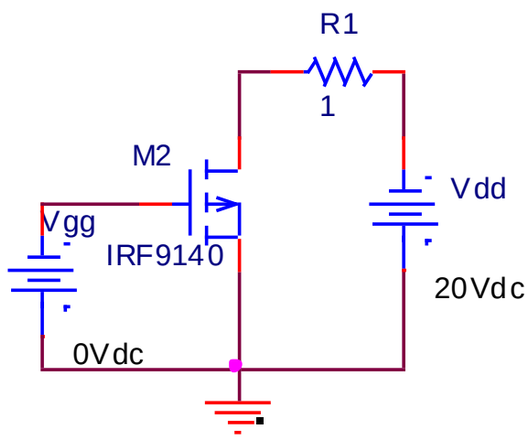


Fig.3. Circuit for DC analysis of Enhancement type (p)MOSFET

3.1. Draw the circuit shown in Fig. 3 in PSpice schematics.

Plot of Transfer Curve of p-MOSFET

3.2. Set DC Sweep (linear) of Vgg from 0 to 5 volts in 0.01 volt steps. [Note that the polarity of sources are reversed for p-MOSFET.]

3.3. Place a voltage marker on the drain of p-MOSFET. Run the simulation.

3.4. The transfer Curve will appear on the screen.

3.5. Determine the threshold voltage of p-MOSFET.

Plot of Output Characteristics of p-MOSFET

3.6. Here, for determining the output characteristics a nested DC Sweep of Vdd and Vgg is required. For achieving this, Select **Setup Analysis** and then **DC Sweep** from the pop-up window. Sweep first Vdd from 0 to 20V in 0.1V increments. Then click on the **Nested Sweep** button for sweeping Vgg from 0 to 5V in 1V increments. Mark the **Enable Nested Sweep** box.

3.7. After placing a current marker in the drain of the MOSFET, run the simulation.

3.8. Change the X-axis settings. [Plot → Axis settings → Axis variable. Then select V1(M2:d) as axis variable]

3.9. Output characteristic of the p-MOSFET will appear in the probe.

3.10. Determine the pinch-off voltage and early voltage of p-MOSFET for different Vgg.

DC Characteristics of Complementary MOS (CMOS) Inverter

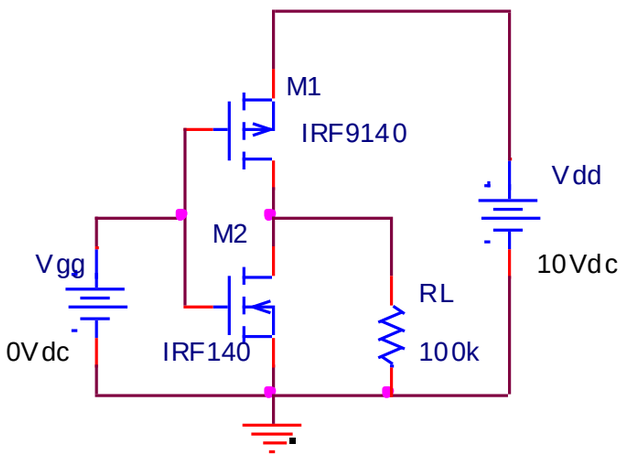


Fig.4. Circuit for DC analysis of CMOS Inverter

4.1. Draw the circuit shown in Fig. 3 in PSpice schematics. [Note that the MOSFETs selected for this inverter circuit has complementary, i.e. that have similar properties like rise time, fall time, etc. Also note that the p-MOSFET's source is connected to positive terminal of DC source and n-MOSFET's source connected to ground for proper operation of the circuit.]

Plot of Transfer Curve of CMOS Inverter

4.2. Set DC Sweep (linear) of Vgg from 0 to 10 volts in 0.01 volts steps.

4.3. Place a voltage marker across the load resistance. Run the simulation.

4.4. The transfer Curve will appear on the screen.