Fig. 2.7 (*a*) shows two of the output characteristic curves, 1 for $I_B = 0$ and 2 for $I_B \neq 0$. The initial part of curve 2 , characterised by low V_{CE}, is called the saturation region. In this region, the transistor acts like a switch. The flat part of curve 2, indicated by increasing V_{CE} and almost constant I_C, is the active region. In this region, transistor acts like an amplifier. Almost vertically rising curve is the breakdown region which must be avoided at all costs.

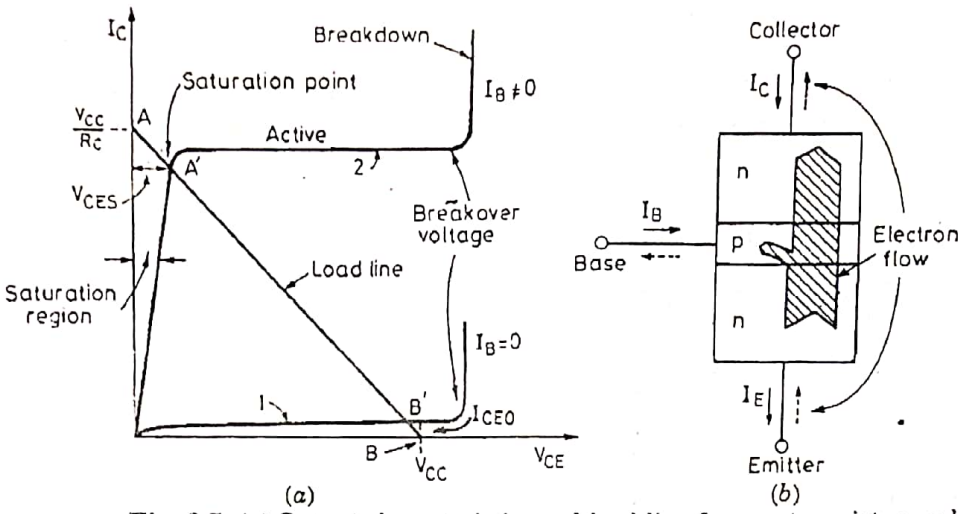

Fig. 2.7. (*a*) Output characteristics and load line for *npn* transistor and (*b*) electron flow in an *npn* transistor.

For load resistor R_C, Fig. 2.6 (*a*), the collector current I_C is given by

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

This is the equation of load line. It is shown as line AB in Fig. 2.7 (*a*). A load line is the locus of all possible operating points. Ideally, when transistor is on, V_{CE} is zero and $I_C = V_{CC}/R_C$. This collector current is shown by point *A* on the vertical axis. When the transistor is off, or in the cut-off region, V_{CC} appears across collector-emitter terminals and there is no collector current. This value is indicated by point *B* on the horizontal axis. For the resistive load, the line joining points *A* and *B* is the load line.

Relation between α and β. Most of the electrons, proportional to I_E, given out by emitter, reach the collector as shown in Fig. 2.7 (*b*). In other words, collector current I_C, though less than emitter current I_E, is almost equal to I_E. A symbol α is used to indicate how close in value these two currents are. Here α, called *forward current gain*, is defined as

$$\alpha = \frac{I_C}{I_E} \qquad ...(2.6)$$

As $I_C < I_E$, value of α varies from 0.95 to 0.99.

In a transistor, base current is effectively the input current and collector current is the output current. The ratio of collector (output) current I_C to base (input) current I_B is known as the *current gain* β.

$$\therefore \quad \beta = \frac{I_C}{I_B} \qquad ...(2.7)$$

As I_B is much smaller, β is much more than unity ; its value varies from 50 to 300. In another system of analysis, called h parameters, h_{FE} is used in place of β.

$$\beta = h_{FE} = \frac{I_C}{I_B} \qquad ...(2.7)$$

Use of KCL in Fig. 2.6 (*a*) gives

$$I_E = I_C + I_B \qquad ...(2.8)$$

Remember that emitter current is the largest of the three currents, collector current is almost equal to, but less than, emitter current. Base current has the least value. Dividing both sides of Eq. (2.8) by I_C, we get

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or
$$\beta = \frac{\alpha}{1 - \alpha} \qquad ...(2.9)$$

and
$$\alpha = \frac{\beta}{\beta + 1} \qquad ...(2.10)$$

Transistor Switch. Transistor operation as a switch means that transistor operates either in the saturation region or in the cut-off region and nowhere else on the load line. As an ideal switch, the transistor operates at point A in the saturated state as closed switch with $V_{CE} = 0$ and at point B in the cut-off state as an open switch with $I_C = 0$, Fig. 2.7 (*a*). In practice, the large base current will cause the transistor to work in the saturation region at point A' with small saturation voltage V_{CES}. Here subscript S is used to denote saturated value. Voltage V_{CES} represents on-state voltage drop of the transistor which is of the order of about 1 V. When the control, or base, signal is reduced to zero, the transistor is turned off and its operation shifts to B' in the cut-off region, Fig. 2.7 (*a*). A small leakage current I_{CEO} flows in the collector circuit when the transistor is off.

For Fig. 2.6 (*a*), KVL for the circuit consisting of V_B, R_B and emitter gives

$$V_B - R_B I_B - V_{BE} = 0$$

or
$$I_B = \frac{V_B - V_{BE}}{R_B} \qquad ...(2.11)$$

Also, from Fig. 2.6 (*a*), $V_{CC} = V_{CE} + I_C R_C$

or
$$V_{CE} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C$$

$$= V_{CC} - \frac{\beta R_C}{R_B}(V_B - V_{BE}) \qquad ...(2.12)$$

Also $V_{CE} = V_{CB} + V_{BE}$

or
$$V_{CB} = V_{CE} - V_{BE} \qquad ...(2.13)$$

If V_{CES} is the collector-emitter saturation voltage, then collector current I_{CS} is given by

$$I_{CS} = \frac{V_{CC} - V_{CES}}{R_C} \qquad ...(2.14)$$

and the corresponding value of minimum base current, that produces saturation, is

$$I_{BS} = \frac{I_{CS}}{\beta} \qquad ...(2.15)$$

If base current is less than I_{BS}, the transistor operates in the active region, *i.e* . somewhere between the saturation and cut-off points. If base current is more than I_{BS}, V_{CES} is almost zero and collector current from Eq. (2.14) is given by $I_{CS} = V_{CC}/R_C$ This shows that collector current at saturation remains substantially constant even if base current is increased.

With base current more than I_{BS}, *hard drive* of transistor is obtained. With hard saturation, on-state losses of transistor increase. Normally, the practical circuit is designed for hard-drive of transistor and therefore, base current I_B is greater than I_{BS} given by Eq. (2.15). The ratio of I_B and I_{BS} is defined as the overdrive factor (ODF).

$$\therefore \qquad ODF = \frac{I_B}{I_{BS}} \qquad ...(2.16)$$

ODF may be as high as 4 or 5.

The ratio of I_{CS} to I_B is called *forced current gain* β_f where

$$\beta_f = \frac{I_{CS}}{I_B} < \text{natural current gain } \beta \text{ or } h_{FE} \qquad ...(2.17)$$

The total power loss in the two junctions of a transistor is

$$P_T = V_{BE} I_B + V_{CE} I_C \qquad ...(2.18)$$

Under saturated state, V_{BES} is greater than V_{CES}, this means BEJ is forward biased. Further Eq. (2.13) shows that V_{CB} is negative under saturated conditions, therefore, CBJ is also forward biased. In other words, under saturated conditions, both junctions in a power transistor are forward biased.

Example 2.1. *A bipolar transistor shown in Fig. 2.6 (a) has current gain* $\beta = 40$. *The load resistance* $R_C = 10\ \Omega$, *dc supply voltage* $V_{CC} = 130$ V *and input voltage to base circuit,* $V_B = 10$ V. *For* $V_{CES} = 1.0$ V *and* $V_{BES} = 1.5$ V, *calculate.*

(*a*) *the value of* R_B *for operation in the saturated state,*

(*b*) *the value of* R_B *for an over drive factor 5,*

(*c*) *forced-current gain and*

(*d*) *power loss in the transistor for both parts (a) and (b).*

Solution. Here $\beta = 40$, $R_C = 10\ \Omega$, $V_{CC} = 130$ V, $V_B = 10$ V, $V_{CES} = 1.0$ V and $V_{BES} = 1.5$ V

(*a*) From Eq. (2.14), for operation in the saturated state,

$$I_{CS} = \frac{V_{CC} - V_{CES}}{R_C} = \frac{130 - 1.0}{10} = 12.90 \text{ A}$$

From Eq. (2.15), base current that produces saturation,

$$I_{BS} = \frac{I_{CS}}{\beta} = \frac{12.90}{40} = 0.3225 \text{ A}$$

Value of R_B for $I_{BS} = 0.3225$ A is given by Eq. (2.11) as,

$$R_B = \frac{V_B - V_{BES}}{I_{BS}} = \frac{10 - 1.5}{0.3225} = 26.357\ \Omega$$

(*b*) Base current with overdrive, from Eq. (2.16), is

$$I_B = ODF \times I_{BS} = 5 \times 0.3225 = 1.6125 \text{ A}$$

$$\therefore \quad R_B = \frac{10 - 1.5}{1.6125} = 5.27\ \Omega$$

(*c*) Forced current gain, from Eq. (2.17), is

$$\beta_f = \frac{I_{CS}}{I_B} = \frac{12.90}{1.6125} = 8 \text{ which is less than the natural current gain } \beta = 40.$$

(*d*) Power loss in transistor, from Eq. (2.18), is

$$P_T = V_{BES} I_{BE} + V_{CES} I_{CS}$$

For normal base drive, $P_T = 1.5 \times 0.3225 + 1.0 \times 12.9 = 13.384$ W

With overdrive, $P_T = 1.5 \times 1.6125 + 1.0 \times 12.9 = 15.32$ W

It is seen from above that power loss with hard drive of transistor is more.

2.5.1.2. BJT Switching Performance. When base current is applied, a transistor does not turn on instantly because of the presence of internal capacitances. Fig. 2.9 shows the various switching waveforms of an *npn* power transistor with resistive load between collector and emitter, Fig. 2.8.

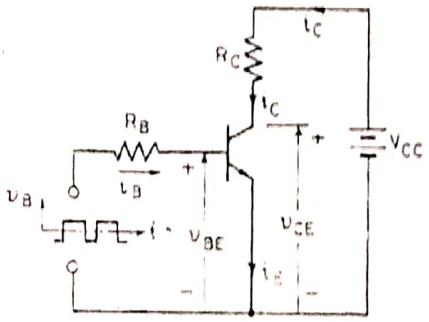

Fig. 2.8. *npn* transistor with resistive load.

When input voltage v_B to base circuit is made $-V_2$ at t_0, junction *EB* or *EBJ* is reverse biased, $v_{BE} = -V_2$, the transistor is off, $i_B = I_C = 0$ and $v_{CE} = V_{CC}$, Fig. 2.9. At time t_1, input voltage v_B is made $+V_1$ and i_B rises to I_{B1} as shown in Fig. 2.9. After t_1, base-emitter voltage v_{BE} begins to rise gradually from $-V_2$ and collector current i_c begins to rise from zero (actually a small leakage current I_{CEO} exists as shown in Fig. 2.7 (*a*)) and collector- emitter voltage v_{CE} starts falling from its initial value V_{CC}. After some time delay t_d, called delay time, the collector current rises to 0.1 I_{CS}, v_{CE} falls from V_{CC} to 0.9 V_{CC} and v_{BE} reaches $V_{BES} = 0.7$ V. This delay time is required to charge the base-emitter capacitance to $V_{BES} = 0.7$ V. Thus, *delay time* t_d is defined as the time during which the collector current rises from zero to 0.1 I_{CS} and collector-emitter voltage falls from V_{CC} to 0.9 V_{CC}.

After delay time t_d, collector current rises from 0.1 I_{CS} to 0.9 I_{CS} and v_{CE} falls from 0.9 V_{CC} to 0.1 V_{CC} in time t_r. This time t_r is known as rise time which depends upon transistor junction capacitances. *Rise time* t_r is defined as the time during which collector current rises from 0.1 I_{CS} to 0.9 V_{CC} and collector-emitter voltage falls from 0.9 V_{CC} to 0.1 V_{CC}. This shows that total turn-on time $t_{on} = t_d + t_r$. Value of t_{on} is of the order of 30 to 300 nano seconds. The transistor remains in the on, or saturated, state so long as input voltage stays at V_1, Fig. 2.9 (*a*).

In case transistor is to be turned off, then input voltage v_B and input base current i_B are reversed. At time t_2, input voltage v_B to base circuit is reversed from V_1 to $-V_2$. At the same time, base current changes from I_{B1} to $-I_{B2}$ as shown in Fig. 2.9 (*b*). Negative base current I_{B2} removes excess carriers from the base. The time t_s required to remove these excess carriers is

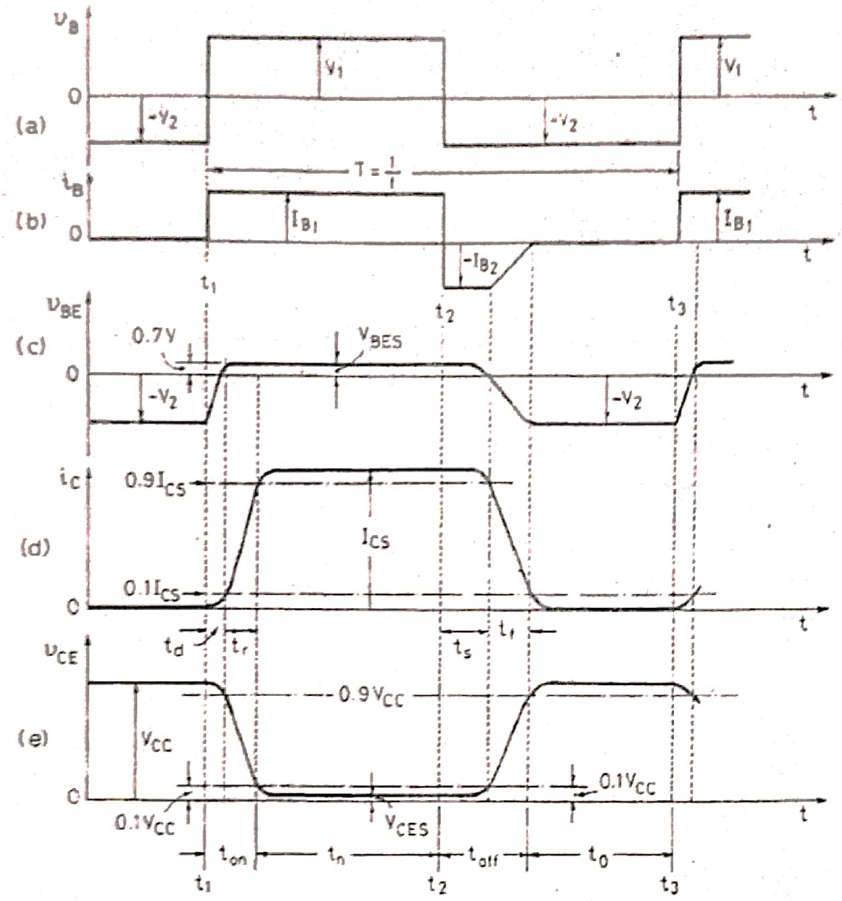

Fig. 2.9. Switching waveforms for *npn* power transistor of Fig. 2.8.

called storage time and only after t_s, base current I_{B2} begins to decrease towards zero. Transistor comes out of saturation only after t_s. *Storage time* t_s is usually defined as the time during which collector current falls from I_{CS} to 0.9 I_{CS} and collector-emitter voltage v_{CE} rises from V_{CES} to 0.1 V_{CC}, Fig. 2.9 (*d*) and (*e*). Negative input voltage enhances the process of removal of excess carriers from base and hence reduces the storage time and therefore, the turn-off time.

After t_s, collector current begins to fall and collector-emitter voltage starts building up. Time t_f, called *fall time*, is defined as the time during which collector current drops from 0.9 I_{CS} to 0.1 I_{CS} and collector-emitter voltage rises from 0.1 V_{CC} to 0.9 V_{CC}, Fig. 2.9 (*d*) and (*e*). Sum of storage time and fall time gives the transistor turn-off time t_{off} i.e. $t_{off} = t_s + t_f$. The various waveforms during transistor switching are shown in Fig. 2.9. In this figure, t_n = conduction period of transistor, t_0 = off period, $T = 1/f$ is the periodic time and f is the switching frequency.

2.5.1.3. Safe Operating Area. The safe operating area (SOA or SOAR) of a power transistor specifies the safe operating limits of collector current I_C versus collector-emitter voltage V_{CE}. For reliable operation of the transistor, the collector current and voltage must always lie within this area. Actually, two types of safe operating areas are specified by the manufacturers. FBSOA and RBSOA.

The forward-base safe operating area (FBSOA) pertains to the transistor operation when base-emitter junction is forward biased to turn-on the transistor. For a power transistor, Fig. 2.10 shows typical FBSOA for its dc as well as single-pulse operation. The scale for I_C and V_{CE} are logarithmic. Boundary *AB* is the maximum limit for dc and continuous current for V_{CE} less than about 80 V. For V_{CE} for more than 80 V, collector current has to be reduced to boundary BC so as to limit the junction temperature to safe values. For still higher V_{CE}, current should further be reduced so as to avoid secondary breakdown limit. Boundary CD defines this secondary breakdown limit. Boundary DE gives the maximum voltage capability for this particular transistor.

For pulsed operation, power transistor can dissipate more peak power so long as average power loss is within safe limits of junction temperature. In Fig. 2.10 ; 5 ms, 500 μs etc. indicate pulse widths for which transistor is on. It is seen that FBSOA increases as pulse-width is decreased.

It should be noted that FBSOA curves, as given by the manufacturers, are for a case temperature of 25°C and for dc and single-pulse operation. In order to take into consideration the actual working temperature and repetitive nature of the pulses, these curves must be modified with the help of thermal impedance of the device.

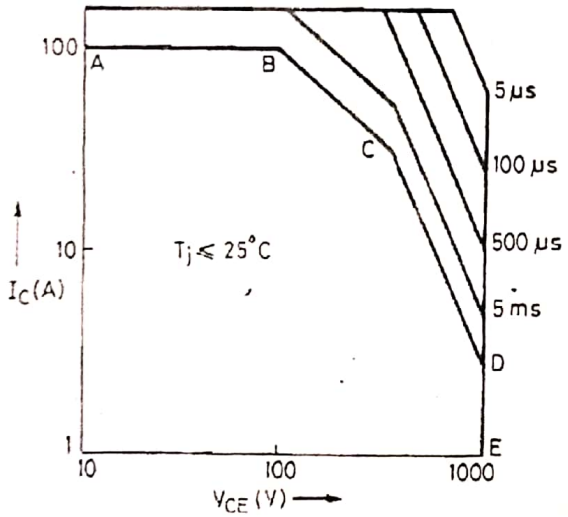

Fig. 2.10. Typical forward biased safe operating area (FBSOA) for a power transistor (logarithmic scale)

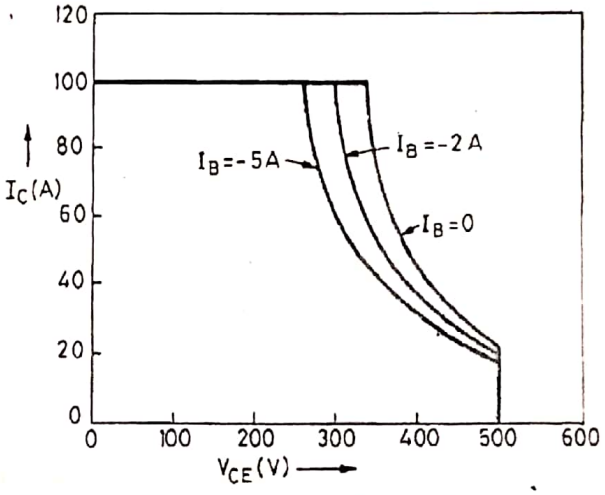

Fig. 2.11. Typical reverse-block safe operating area (RBSOA) for a power transistor.

During turn-off, a transistor is subjected to high current and high voltage with base-emitter junction reverse biased. Safe operating area for transistor during turn-off is specified as reverse blocking safe operating area (RBSOA). This RBSOA is a plot of collector current versus collector-emitter voltage as shown in Fig. 2.11. RBSOA specifies the limits of transistor operation at turn-off when the base current is zero or when the base-emitter junction is reverse biased (*i.e.* with base current negative). With increased reverse bias, area RBSOA decreases in size as shown in Fig. 2.11.

Example 2.2. *For a power transistor, typical switching waveforms are shown in Fig. 2.12(a). The various parameters of the transistor circuit are as under :*

$V_{CC} = 220$ V, $V_{CES} = 2$ V, $I_{CS} = 80$ A, $t_d = 0.4$ μs, $t_r = 1$ μs, $t_n = 50$ μs,

$t_s = 3$ μs, $t_f = 2$ μs, $t_o = 40$ μs, $f = 5$ kHz. *Collector to emitter leakage current itlaic*= 2 mA.

Determine average power loss due to collector current during t_{on} *and* t_n. *Find also the peak instantaneous power loss due to collector current during turn-on time.*

Solution. During delay time, the time limits are $0 \le t \le t_d$. Fig. 2.12 (a) shows that in this time, $i_C(t) = I_{CEO}$ and $v_{CE}(t) = V_{CC}$.

$\therefore$ Instantaneous power loss during delay time is

$$P_d(t) = i_C v_{CE} = I_{CEO} V_{CC} = 2 \times 10^{-3} \times 220 = 0.44 \text{ W}$$

Average power loss during delay time with $0 \le t \le t_d$ is given by

$$P_d = \frac{1}{T}\int_0^{t_d} i_C(t) \cdot v_{CE}(t)\, dt$$

$$= \frac{1}{T}\int_0^{t_d} I_{CEO} \cdot V_{CC}\, dt = f \cdot I_{CEO} \cdot V_{CC} \cdot t_d$$

$$= 5 \times 10^3 \times 2 \times 10^{-3} \times 220 \times 0.4 \times 10^{-6} = 0.88 \text{ mW}$$

where $f = \frac{1}{T}$ = frequency of transistor switching

During rise time, $0 \le t \le t_r$,

$$i_C(t) = \frac{I_{CS}}{t_r} \cdot t$$

and $$v_{CE}(t) = \left[V_{CC} - \frac{V_{CC} - V_{CES}}{t_r} \cdot t\right]$$

$\therefore$ Average power loss during rise time is

$$P_r = \frac{1}{T}\int_0^{t_r} \frac{I_{CS}}{t_r} \cdot t \left[V_{CC} - \frac{V_{CC} - V_{CES}}{t_r} \cdot t\right] dt$$

$$= f \cdot I_{CS} \cdot t_r \left[\frac{V_{CC}}{2} - \frac{V_{CC} - V_{CES}}{3}\right]$$

$$= 5 \times 10^3 \times 80 \times 1 \times 10^{-6} \left[\frac{220}{2} - \frac{220 - 2}{3}\right] = 14.933 \text{ W}$$

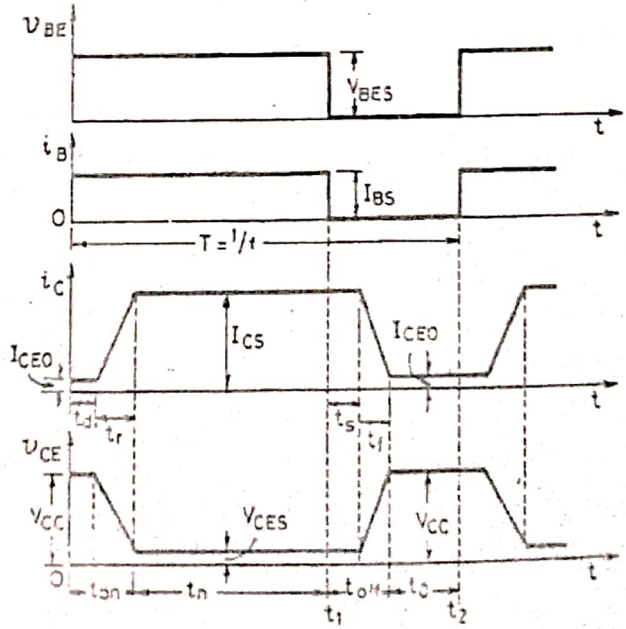

Fig. 2.12. (a) Switching waveforms for Examples 2.2 and 2.3.

Instantaneous power loss during rise time is

$$P_r(t) = \frac{I_{CS}}{t_r} \cdot t \left\{ V_{CC} - \frac{V_{CC} - V_{CES}}{t_r} \cdot t \right\}$$

$$= \frac{I_{CS} \cdot t}{t_r} V_{CC} - \frac{I_{CS} \cdot t^2}{t_r^2} [V_{CC} - V_{CES}] \quad ...(i)$$

$\frac{d P_r(t)}{dt} = 0$ gives time t_m at which instantaneous power loss during t_r would be maximum. It is seen from Eq. (*i*) that

$$t_m = \frac{V_{CC} \cdot t_r}{2 [V_{CC} - V_{CES}]} = \frac{220 \times 1 \times 10^{-6}}{2 [220 - 2]} = 0.5046 \ \mu s$$

Peak instantaneous power loss P_{rm} during rise time is obtained by substituting the value of $t = t_m$ in Eq. (*i*).

$$\therefore \quad P_{rm} = \frac{I_{CS}}{t_r} \cdot \frac{V_{CC}^2 \cdot t_r}{2 [V_{CC} - V_{CES}]} - \frac{I_{CS}}{t_r^2} \frac{(V_{CC} \cdot t_r)^2 [V_{CC} - V_{CES}]}{4 [V_{CC} - V_{CES}]^2}$$

$$= \frac{I_{CS} \cdot V_{CC}^2}{4 [V_{CC} - V_{CES}]} = \frac{80 \times 220^2}{4 [220 - .2]} = 4440.4 \text{ W}$$

Total average power loss during turn-on

$$P_{on} = P_d + P_r = 0.00088 + 14.933 = 14.9339 \text{ W}$$

During conduction time, $0 \le t \le t_n$

$$i_C(t) = I_{CS} \text{ and } V_{CE}(t) = V_{CES}$$

Instantaneous power loss during t_n is

$$P_n(t) = i_C \cdot v_{CE} = I_{CS} \cdot V_{CES} = 80 \times 2 = 160 \text{ W}$$

Average power loss during conduction period is

$$P_n = \frac{1}{T} \int_0^{t_n} i_C \cdot v_{CE} \cdot dt = f I_{CS} \cdot V_{CES} \cdot t_n$$

$$= 5 \times 10^3 \times 80 \times 2 \times 50 \times 10^{-6} = 40 \text{ W}.$$

Example 2.3. *Repeat Example 2.2 for obtaining average power loss during turn-off time and off-period, and also peak instantaneous power loss during fall time due to collector current. Sketch the instantaneous power loss for period T as a function of time.*

Solution. During storage time, $0 \le t \le t_s$,

$$i_C(t) = I_{CS} \text{ and } v_{CE}(t) = V_{CES}$$

Instantaneous power loss during t_s is

$$P_s(t) = i_C(t) v_{CE}(t)$$

$$= I_{CS} \cdot V_{CES} = 80 \times 2 = 160 \text{ W}$$

Average power loss during t_s is

$$P_s = \frac{1}{T} \int_0^{t_s} I_{CS} \cdot V_{CES} \cdot dt = f \cdot I_{CE} \cdot V_{CES} \cdot t_s$$

$$= 5 \times 10^3 \times 80 \times 2 \times 3 \times 10^{-6} = 2.4 \text{ W}$$