Department of Electrical and Electronic Engineering
Shahjalal University of Science and Technology

EEE 222: Electronic Circuit Simulation Laboratory
EXPERIMENT NO. 05

PART- A

Name of the Experiment: STUDY OF JFET SMALL SIGNAL AMPLIFIER.

OBJECTIVE

The objective of this experiment is to simulate for studying the performance of the Common Source (CS) and Common Drain (CD) JFET small signal amplifiers.

INTRODUCTION

The input impedance of the JFET is very high since the gate-to-channel junction is always reverse biased. FET's are therefore useful in the design of high-input-impedance amplifiers. In this experiment we shall study two configurations of FET amplifiers: the common-source circuit, and the common-drain or source follower. In addition to its application in amplifier design, JFETs are very useful as voltage controlled resistances.

In the triode, region, the I_D-V_{DS} characteristics have high slope and approximate straight lines for small V_{DS}. Furthermore, these straight lines pass through the origin. This linear resistance region of operation enables the application of the JFET as an analog switch. Switching of analog signals is required in many applications such as the multiplexing of a number of signal sources, onto single pair of wires, and the chopping of a low frequency square wave. The latter technique is used in the design of a special type of highly stable amplifiers (called chopper-stabilized amplifiers).

1. The JFET as an Amplifier

To understand the basis for the operation of the JFET as an Amplifier, consider the circuit of Figure 1.

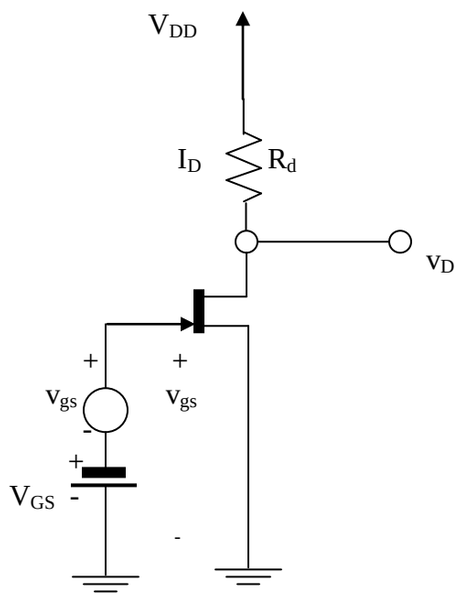


Fig.1.

$$v_{GS} = V_{GS} + v_{gs} \tag{1}$$

Assuming that the FET will remain in pinch off at all times, which is achieved by keeping v_{DS} higher than v_{GS} by at least $|Vp|$ (pinch-off voltage), that is

$$v_{DS} \geq v_{GS} + |V_p| \tag{2}$$

It can be shown that

$$I_D = I_{DSS}(1-\frac{V_{GS}}{V_p})^2 \quad (3)$$

And for

$$\frac{v_{gs}}{V_P} << 1 \quad (4)$$

$$i_d = (\frac{2I_{DSS}}{-V_P})(1-\frac{V_{GS}}{V_P})v_{gs} \quad (5)$$

Thus, the signal current is linearly related to the signal voltage v_{gs}, which is a requirement in a linear amplifier and which is obtained under the small signal condition of equation (4). The constant relating i_d to v_{gs} is the trans-conductance g_m,

$$g_m = \frac{i_d}{v_{gs}} = (\frac{2I_{DSS}}{-V_p})(1-\frac{V_{GS}}{V_p}) \quad (6)$$

Recalling that for n-channel FET's V_p is a negative number and V_{GS} is also negative, it is seen that gm is positive; a comforting result. Note that gm is determined by the FET parameters I_{DSS} and V_p, as well as by the DC operating point. We may write.

$$g_m = (\frac{2I_{DSS}}{-V_P})\sqrt{\frac{I_D}{I_{DSS}}} \quad (7)$$

It follows that gm will be highest if the FET is biased at V_{GS}= 0 (or, $I_D = I_{DSS}$). This maximum value of g_m is denoted g_{mo} and is given by.

$$g_{mo} = (\frac{2I_{DSS}}{-V_P}) \quad (8)$$

2. **The Common Source Amplifier**

Fig. 2 shows the common source amplifier where the FET is biased using a combination of fixed bias and self-bias. The fixed bias voltage V_{GG} is derived from V_{DD} via the voltage divider R_{G1}, R_{G2}.

$$V_{GG} = V_{DD}\frac{R_{G2}}{R_{G1}+R_{G2}} \quad (9)$$

The self-bias is obtained by connecting a resistance R_S in the source load. We shall assume that a DC drain current I_D is established and that the value of R_d is such that the FET remains in pinch-off at all times. The signal V_i is obtained from a source having a resistance 'R' and is coupled to the gate through a capacitor C_1 should be chosen such that its reactance is very small at the frequency band of interest.

The output voltage signal at the drain is coupled to a load resistance R_L through another capacitor C_2. The value of C_s should be chosen such that its reactance is very small at the frequencies of interest. At low frequencies C_S will no longer be a perfect signal bypass.

To evaluate the gain of the common source amplifier we ignore all capacitive effects. The input resistance R_{in} is given by (see Fig. 2),

$$R_{in} = R_{G1} // R_{G2} = \frac{R_{G1}R_{G2}}{R_{G1}+R_{G2}} \quad (10)$$

Thus, we may use the voltage divider rule to evaluate the signal v_{gs},

$$v_{gs} = v_i\frac{R_{in}}{R+R_{in}} \quad (11)$$

The drain current signal i_d will be $i_d = g_m v_{gs}$, and will flow into and effective load resistance R_L given by,

$$R'_L = R_d // R_L // r_o \quad (12)$$

Thus, the stage gain is given by,

$$\frac{v_o}{v_i} = -(\frac{R_{in}}{R + R_{in}}) g_m R'_L \tag{13}$$

3. **The Common Drain Amplifier**

Fig. 3 shows the JFET used in a source follower (common-drain) configuration. Because of its high impedance the JFET is an ideal device for such an application. Note, however, that since the signal is capacitively coupled to the gate, a resistor R_G had to be introduced in order to provide DC continuity for the gat. The input resistance of the source follower will be approximately equal to GG. Thus, the signal voltage at the gate will be,

$$v_g = v_i \frac{R_G}{R + R_G} \tag{14}$$

And the output voltage is obtained as,

$$v_o = v_g \frac{R_S \,//\, R_L}{(1/g_m) + R_S \,//\, R_L} \tag{15}$$

Equations (14) and (15) can be combined to obtain the gain,

$$\frac{v_o}{v_i} = \frac{R_G}{R + R_G} \frac{R_S \,//\, R_L}{(1/g_m) + R_S \,//\, R_L} \tag{16}$$

Thus the gain is less than, but usually close to unity.

To calculate the output resistance of the source follower we ground the signal source, the result is

$$R_{out} = R_S \,//(1/g_m) \tag{17}$$

Which is usually quite small.

PROCEDURE

Small Signal Analysis of JFET as CS amplifier

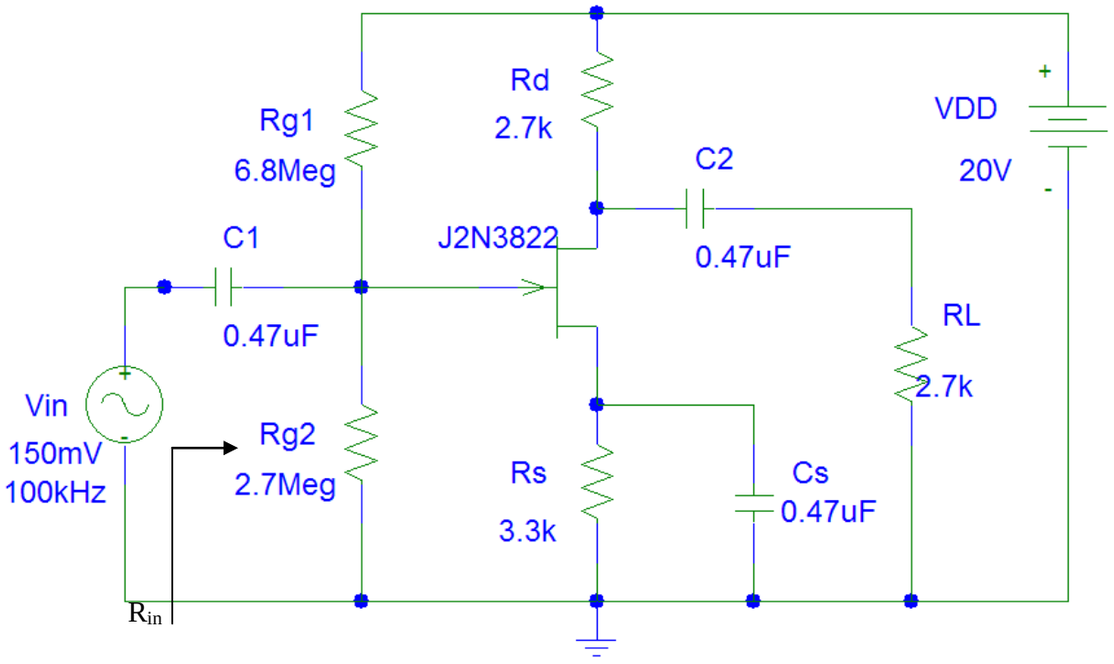


Fig.2. Circuit for Small signal analysis using JFET as CS Amplifier

1.1. Draw the circuit shown in Fig. 2.

1.2. By choosing **Setup analysis**, mark **Bias Point Detail** and **Transient.**

1.3. Choose appropriate step and stop time.

1.4. Run the simulation and click on the **Enable Bias Voltage Display** and **Enable Bias Current Display** icons. Note I_{DSQ} and V_{GSQ}. Compare this with theoretical values.

1.5. Draw the small signal equivalent circuit [Homework]

1.6. Obtain the voltage gain for the circuit (v_0/v_s) from the display in probe.

1.7. Remove C_S and calculate the voltage gain. Compare it with the result of step 6. What is the effect of C_S on the gain?

1.8. Reconnect C_S and connect a resistance of 100 kΩ of in series with the source. Calculate the new voltage gain.

1.9. From step 6 and 8 calculate input resistance of the amplifier.

1.10. With C_S connected, set the load resistance R_L = 1MΩ and calculate the voltage gain. Use the result of step 8 to calculate the output resistance.

Small Signal Analysis of JFET as CD amplifier

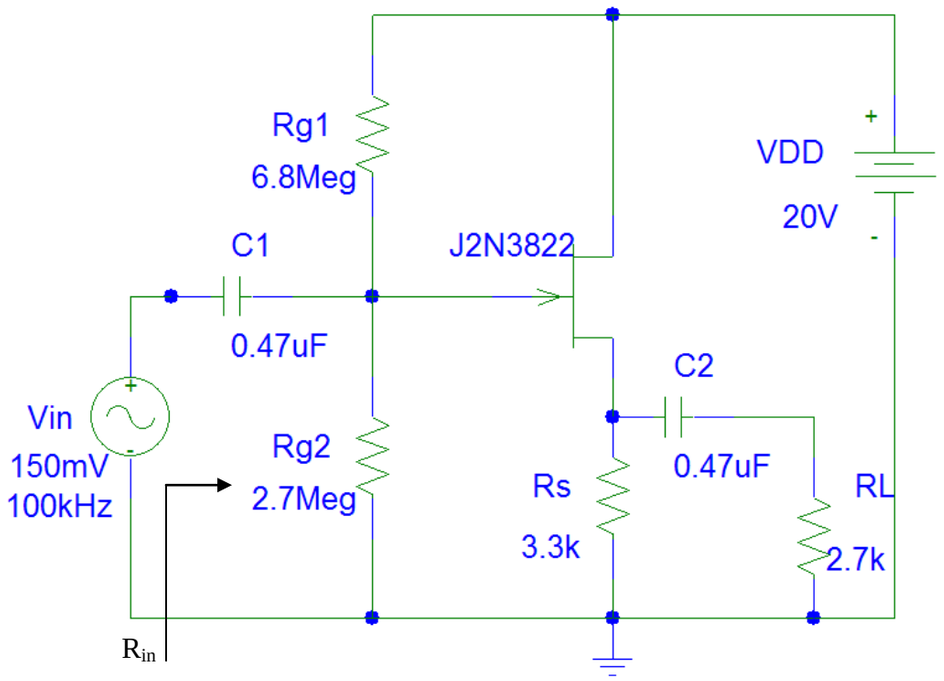


Fig.3. Circuit for Small signal analysis using JFET as CD Amplifier

2.1. Draw the circuit shown in Fig. 3.

2.2. By choosing **Setup analysis**, mark **Bias Point Detail** and **Transient.**

2.3. Choose appropriate step and stop time.

2.4. Run the simulation and click on the **Enable Bias Voltage Display** and **Enable Bias Current Display** icons. Note I_{DSQ} and V_{GSQ}. Compare this with theoretical values.

2.5. Draw the small signal equivalent circuit [Homework]

2.6. Obtain the voltage gain for the circuit (v_0/v_s) from the display in probe.

2.7. Simulate the circuit of Fig. 3 for obtaining the gain-frequency characteristic for the frequency range 10Hz-1MHz.

PART- B

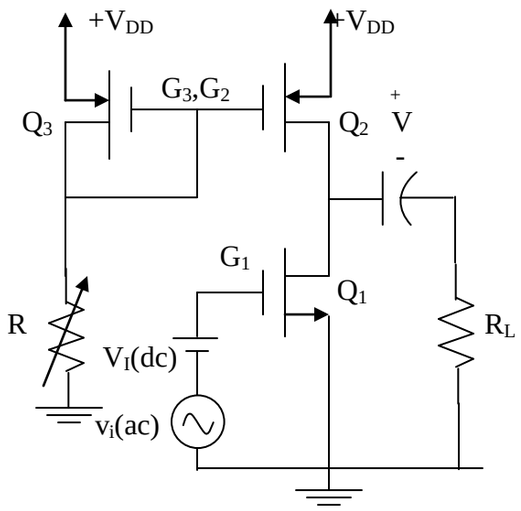
Name Of The Experiment: STUDY OF BIASING AND FREQUENCY RESPONSE OF AN INTEGRATED CIRCUIT MOS AMPLIFIER.

OBJECTIVE

To familiarize with biasing of Integrated MOSFET and frequency response of a Current Source (CS) Amplifier.

THEORY

A typical common source amplifier is shown in Fig. 4.



Q_2 and Q_3 are p MOSFET. Consider Q_3 and Q_2 are identical

Fig.4.

When Q_3 operates in saturation

$$I_{REF} = I_{D3} = \frac{\mu_P C_{ox}}{2}\left(\frac{W}{L}\right)_3 [V_{SG3} - |V_{tp}|]^2 (1 + \lambda V_{DS3}) \quad (1)$$

When Q_2 is in saturation

$$I_{D2} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_2 [V_{SG2} - |V_{tp}|]^2 (1 + \lambda V_{DS2}) \quad (2)$$

Here, $V_{SG3} = V_{SG2} = V_{SG}$ (3)

Now for, $I_{D2} = I_{REF}$, $V_{DS3} = V_{DS2} = V_{GS3} = V_{GS} = -V$ (4)

But $V_0 = V_{DD} - V_{SD2} = V_{DD} - V$ (5)

We can write

$$V_0 = V_{DD} - V_{SG} \quad (6)$$

Q_1 also must operate in saturation.

$$I_{D1} = I_{REF} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_I - V_{tn})^2 (1 + \lambda v_0) \quad (7)$$

A-C EQUIVALENT CIRCUIT

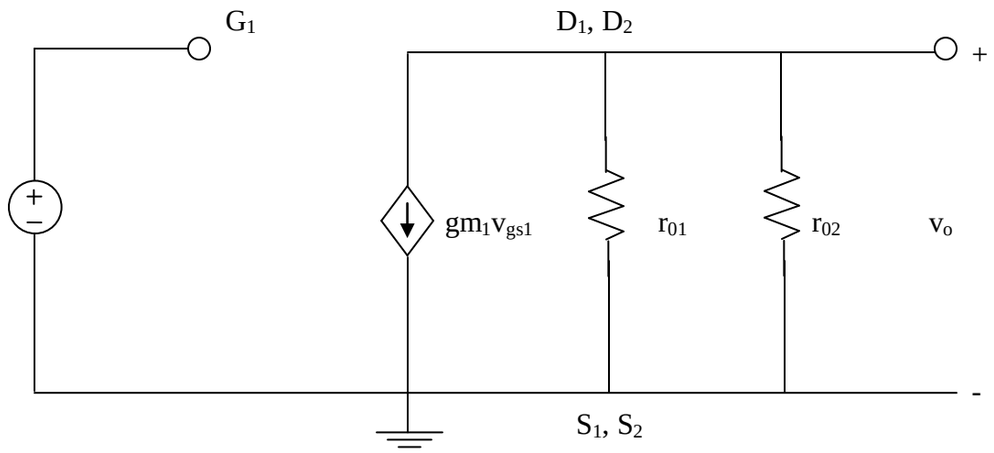


Fig.5.

It can be shown that, $V_0 = -gm_1 v_{gs1}(r_{01} \| r_{02})$

Hence, $A_V = \frac{v_o}{v_{gs1}} = \frac{v_o}{v_I} = -gm_1(r_{01} \| r_{02})$ (8)

where, $gm_1 = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{REF}}$

$r_{01} = \frac{|V_{A1}|}{I_{REF}}$ and $r_{02} = \frac{|V_{A2}|}{I_{REF}}$ [V_A is the early voltage]

We can also write,

$$A_v = -\frac{\sqrt{2\mu_n} C_{ox}\left(\frac{W}{L}\right)_1}{\frac{1}{|V_{A1}|} + \frac{1}{|V_{A2}|}} \cdot \frac{1}{\sqrt{I_{REF}}} \quad (9)$$

Therefore, $A_V \propto \frac{1}{\sqrt{I_{REF}}}$.

PROCEDURE

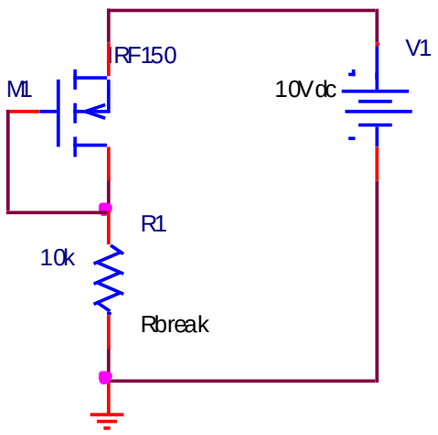


Fig.6.

a) Draw the circuit in Fig. 6. Set value of Rbreak to 10kΩ.

b) Note the value of V_{GS}, V_{DS} and I_D for determining the value of early voltage, V_A.

c) Replace the p-MOSFET (IRF9140) with n-MOSFET (IRF140). Following the steps in (b-d), find the value of early voltage for the n-MOSFET.

d) Draw the circuit in Fig.7. Set value of Rbreak to 10kΩ.

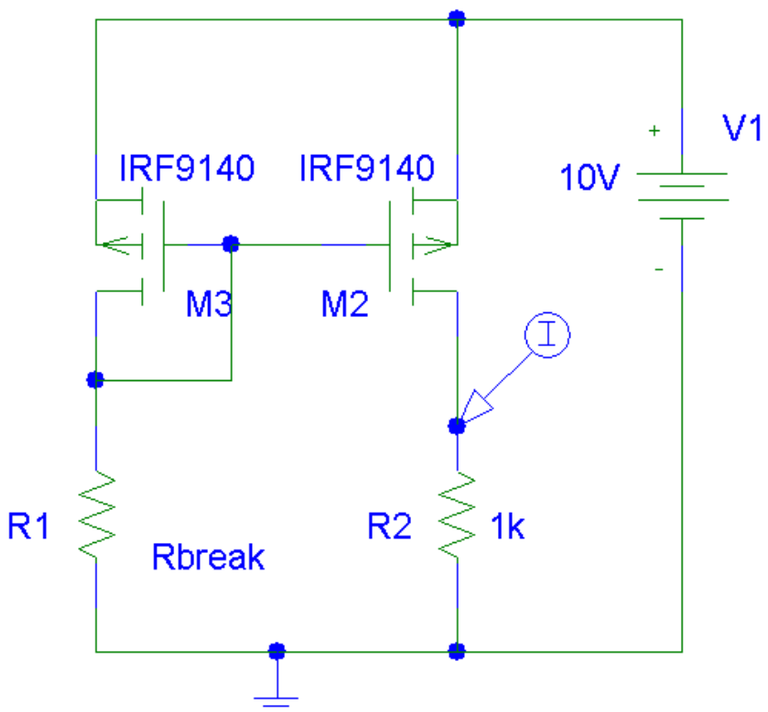


Fig.7.

e) Vary the resistance R1 from 0.1 kΩ to 20 kΩ. [For varying R1, choose **Rbreak** from part list, then from DC sweep select **Model Parameter** as sweep variable type. Use RES as **Model type**, Rbreak as **Model name** and R as **Param. Name.** Vary R from 0.1 to 2 in steps of 0.1.]

f) Determine the value of R1 (= R x 10kΩ) for which the value of I_{R2} is 1mA. Replace Rbreak with a resistance having the determined value.

g) Note V_{DS3}, V_{DS2}, V_{GD2}.

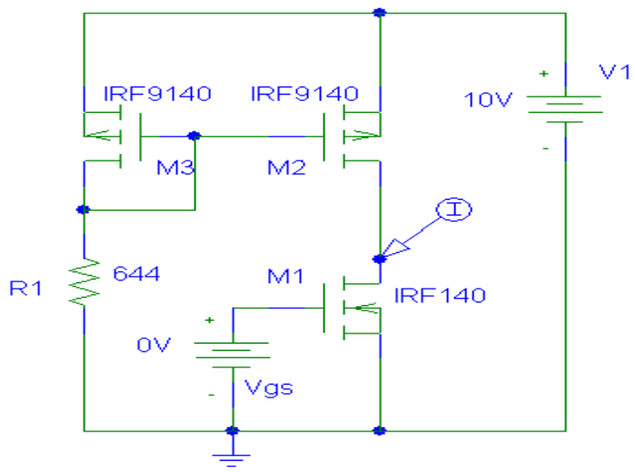


Fig.8.

h) Draw the circuit in Fig.8.

i) Vary Vgs from 0 to 5 V, and obtain the value of Vgs (= V_1) for which I_{M1} is 1mA.

j) Set Vgs = V_1.

k) Insert sinusoidal signal $V_i \cong 5$mV peak between Vgs and the gate of M1.

l) Vary only frequency of the input signal from 1Hz and observe output wave.

m) Measure -3 dB frequency.

n) Determine r_{01} and r_{02}.