Department of Electrical and Electronic Engineering
Shahjalal University of Science and Technology

EEE 222: Electronic Circuit Simulation Laboratory
EXPERIMENT NO. 02

Name of the Experiment: STUDY OF CHARACTERISTICS OF BIPOLAR JUNCTION TRANSISTOR (BJT).

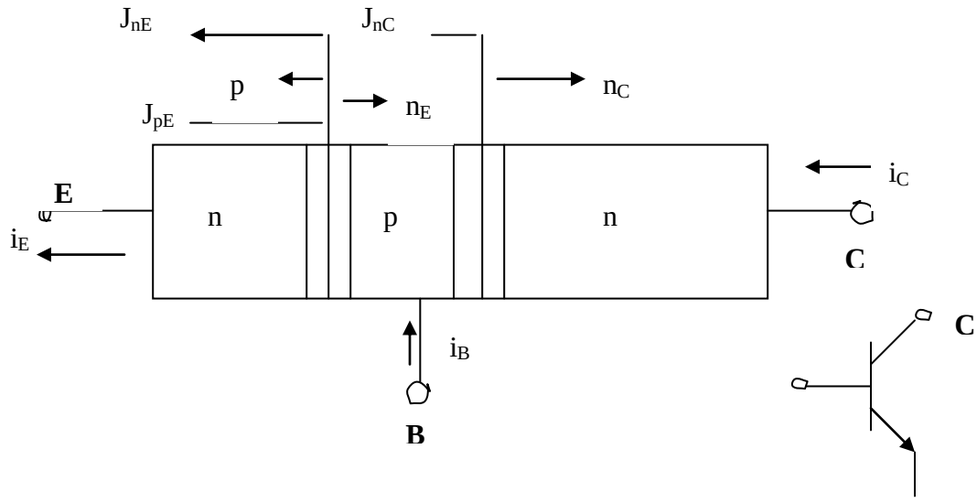
OBJECTIVE

The objective of this experiment is to simulate

- DC characteristics of BJT in Common Emitter (CE) and Common Base (CB) configuration.
- Biasing of BJT.
- Small signal Analysis using BJT.

THEORY

Transistor has two p-n junctions (see figure below). One junction is called emitter junction and other is called collector junction. When transistor is used as an amplifier, it is operated in active mode. In active mode, emitter junction is forward biased and collector junction is reverse biased.



Emitter current is given by

$$I_E = I_{nE} + I_{pE}$$

we can also write

$$I_E = I_C + I_B = [(1 + \beta)/\beta]I_C$$

Where $\beta = I_C / I_B$ is called common emitter current gain.

In good transistor $I_C >> I_B$ i.e. $\beta >> 1$. I_C can also be expressed as $I_C = \alpha I_E$.
where $\alpha = \beta/(1+\beta)$. α is called common base current gain. For good transistor, α is close to unity.
Proper dc biasing of a transistor is a prerequisite for proper operation as an amplifier. The purpose of the biasing is to fix the I_C (dc) and V_{CE} (dc) . But I_C is a function of temperature, V_{BE} and β. It is always desirable to design a biasing circuit where I_C is insensitive to change in β.

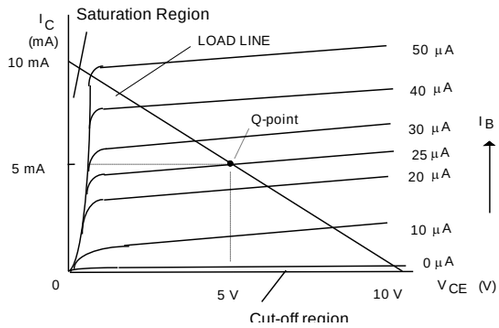
When E-B junction is forward biased and C-B junction is reverse biased, the transistor operates in active mode. For saturation mode of operation, both junction are forward-biased. Cut-off region operation requires that both E-B and C-B junctions be reverse biased. The inverted active operation occurs when E-b is reverse-biased and C-B is forward biased.

Output Characteristics & Load Line

- Static OUTPUT CHARACTERISTICS define steady state conditions
  $\rightarrow$ family of curves of I_C vs V_{CE} for increasing I_B
- Graphical design procedure gives

→ performance under non-linear conditions
→ start & finish points in analytical procedure

- For $V_i = 0$, $I_B = 0$
  → no current flows through R_L thus $I_C = 0$
  → so $V_S = V_{CE}(max)$
- For $V_i >> V_{BE}$, (say $V_i = V_s$), I_B is high and I_C is at maximum
  → nearly all volts dropped across R_S
  $\therefore V_{CE} = 0$ & $I_C(max) = V_S/R_L$
  $\Rightarrow$ Transistor is said to be SATURATED
- A LOAD LINE drawn from $I_C(max)$ to $V_{CE}(max)$
- Slope of load line is $-(1/R_L)$



Biasing of BJT

In order to characterize the operation of a particular transistor, a complete set of characteristic equations is needed. Typically, these curves look like those in Figure. These curves show that in the active region of operation, the collector current is constant and depends on the base current.

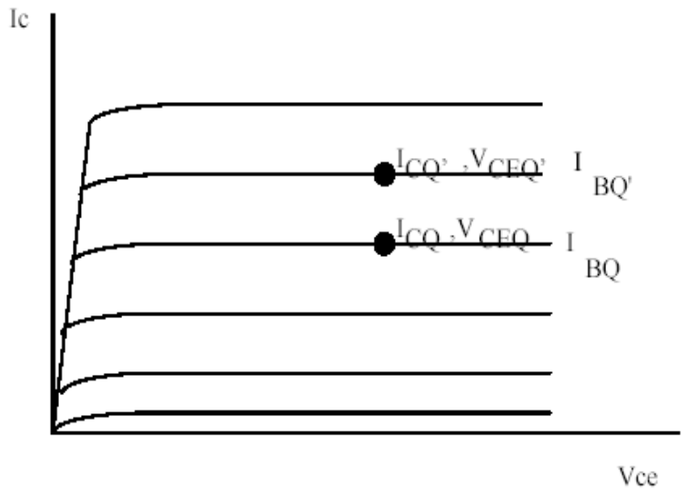


Figure: Characteristic curves for the BJT transistor.

These curves can be used to calculate the large signal current gain, β_{DC} (or h_{FE}) and the small signal current gain, β_{AC} (or h_{fe}). These values are in general calculated for a given bias point I_{CQ}, V_{CEQ} using the following equations:

$$\beta_{DC} = \frac{I_{CQ}}{I_{BQ}}$$

$$\beta_{AC} = \left| \frac{I_{CQ} - I_{CQ'}}{I_{BQ} - I_{BQ'}} \right|$$

From this, one can see that the large signal gain depends only on the Q point and the small signal gain depends only on small deviations around the Q point. In order to use a transistor in an amplifying circuit it has to be biased. In other words, a Q point has to be set in order to place the device in the active region of operation. There are several methods which can be used bias a transistor. Figures a and b demonstrate two possibilities. The first scheme (Figure a) is called a fixed bias scheme. In a fixed biasing the base current is set through a base resistor and the emitter of the transistor is grounded. This scheme is not used in practice since the Q point depends very strongly on β.

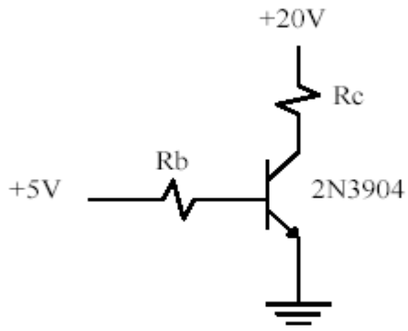


Figure (a): Fixed bias circuit

A second possibility, which is commonly used, is the self biasing scheme. Here the base voltage is set through a voltage divider and the emitter is tied to ground through a resistor. If designed correctly, this scheme is relatively independent of β.

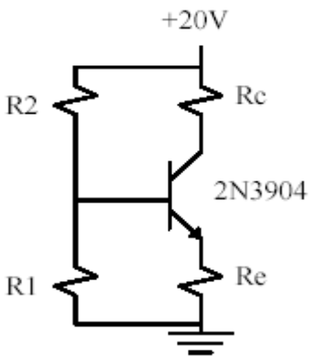
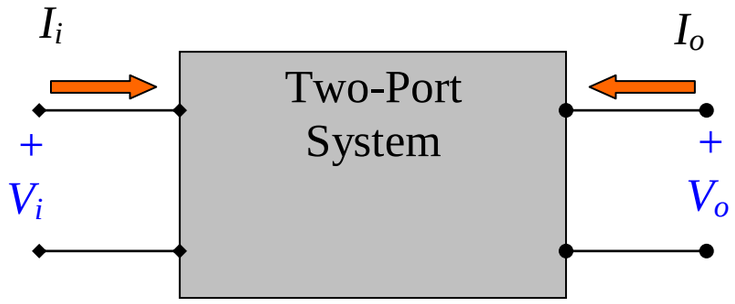


Figure b: Self bias circuit

Small signal analysis:

Two Port Systems

Many electronic components can be represented by a two port "**black box**"



Within the "black box" a mathematical representation of the behaviour can be constructed. Important characteristics of interested to electronic designers are:

Z_i	=	Input Impedance	=	V_i/I_i
Z_o	=	Output Impedance	=	V_o/I_o
A_v	=	Voltage Gain	=	V_o/V_i
A_i	=	Current Gain	=	I_o/I_i

Gain in dB=$20\log_{10}(v_{out}/v_{in})$
At cut-off $(v_{out}/v_{in})=1/\sqrt{2}$
So, at cut-off gain in dB is -3.

PROCEDURE

DC Characteristics of BJT Q2N2222

Output Characteristics

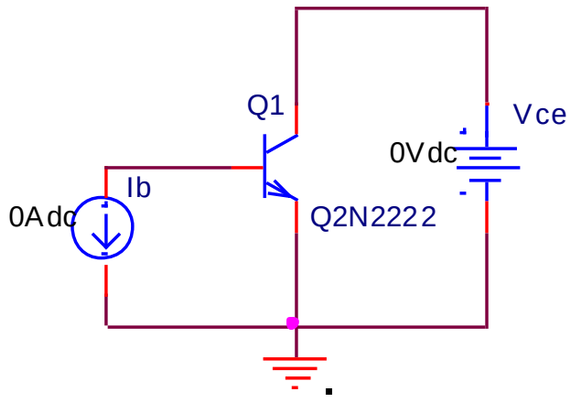


Fig.2. Circuit for DC analysis of BJT in CE configuration

1.1. Draw the circuit shown in Fig. 1 in PSpice schematics.

1.2. Here, for determining the output characteristics a nested DC Sweep of V_{CE} and I_B is required. For achieving this, Select **Setup Analysis** and then **DC Sweep** from the pop-up window. Sweep first V_{CE} from 0 to 10V in 0.1V increments. Then click on the **Nested Sweep** button for sweeping I_B from 0A to 1 mA in 0.2mA increments. Mark the **Enable Nested Sweep** box.

1.3. After placing a current marker in the collector of the BJT (as shown in Fig. 1), run the simulation.

1.4. Output characteristic of the BJT will appear in the probe.

1.5. [Home work] Draw a circuit for obtaining output characteristics of Q2N2222 in CB configuration and simulate it using appropriate sources and nested sweeps.

Plot of DC Current Gain β

β vs. collector current (I_C) and β vs. base current (I_B)

a) Circuit for this analysis is shown in Fig. 1. **Set** V_{CE}= 5V.

b) Sweep I_B from 10μA to 1 mA in **DECADES** with 20 points per decade.

c) Determine the DC current gain (I_C/I_B) vs. I_B curve.

d) Determine the DC current gain (I_C/I_B) vs. I_C curve (normally given in data sheets of IC supplied by the manufacturer).

e) Find, from second plot, the maximum DC current gain. Find the corresponding I_C. Determine Common Emitter (CE) current gain (α) at calculated I_C.

DC Current gain vs. Temperature

f) Circuit for this analysis is shown in Fig. 1. Consider V_{CE} = 5V.

g) Sweep for I_B from 100μA to 1 mA in **DECADES** with 20 points per decade. Click on the **Nested Sweep** button and set values –25, 25, 125 Celsius. Mark in the **Enable Nested Sweep** box.

h) Run the simulation. Generate a plot of DC current gain versus collector current.

NOTE: If you find difficulty in identifying the curves, you should run each case separately and verify the identity of each curve.

Biasing of BJT

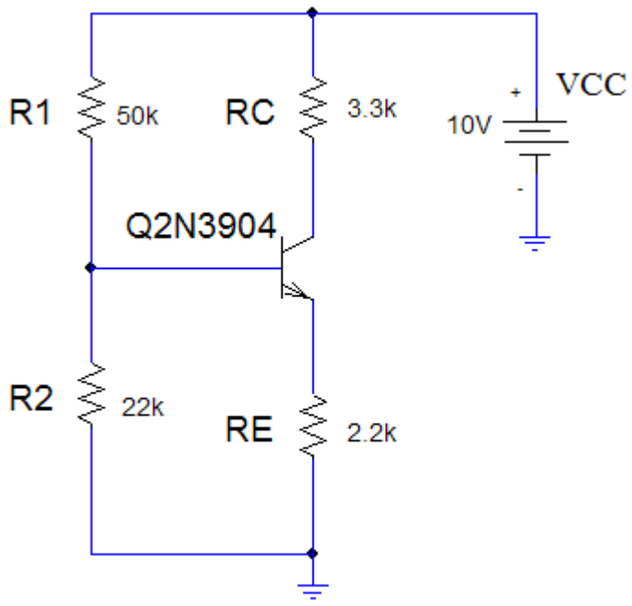


Fig.3. Biasing of BJT

2.1. Draw the circuit of Fig. 3 (Self Bias Circuit). By choosing **Setup analysis**, mark **Bias Point Detail** and **Temperature**. Set Temperature to 27^0 C.

2.2. Run the simulation and click on the **Enable Bias Voltage Display** and **Enable Bias Current Display** icons.

2.3. Fill up the following table.

V_{CC}	V_B	V_E	V_C	V_{CE}	I_B	I_E	I_C	β

2.4. Change R1 to around 57KΩ, so that $V_{CE} = 0.5\ V_{CC}$.

2.5. Change temperature to 50^0 C and note the change in V_{CE}.

2.6. Change transistor model (replace Q2N3904 with Q2N2222) and set temperature back to 27^0 C. Again, note the change in V_{CE}.

2.7. Now, for circuit in Fig. 3, remove RE and short Emitter to ground (Fixed Bias Circuit). Repeat steps 2 to 6. R1 will needed to be set around 228KΩ to achieve $V_{CE} = 0.5\ V_{CC}$.

2.8. Comment on the stability of the biasing circuits (fixed and self) with change in temperature and device model (current gain, etc.).

Small Signal Analysis of BJT

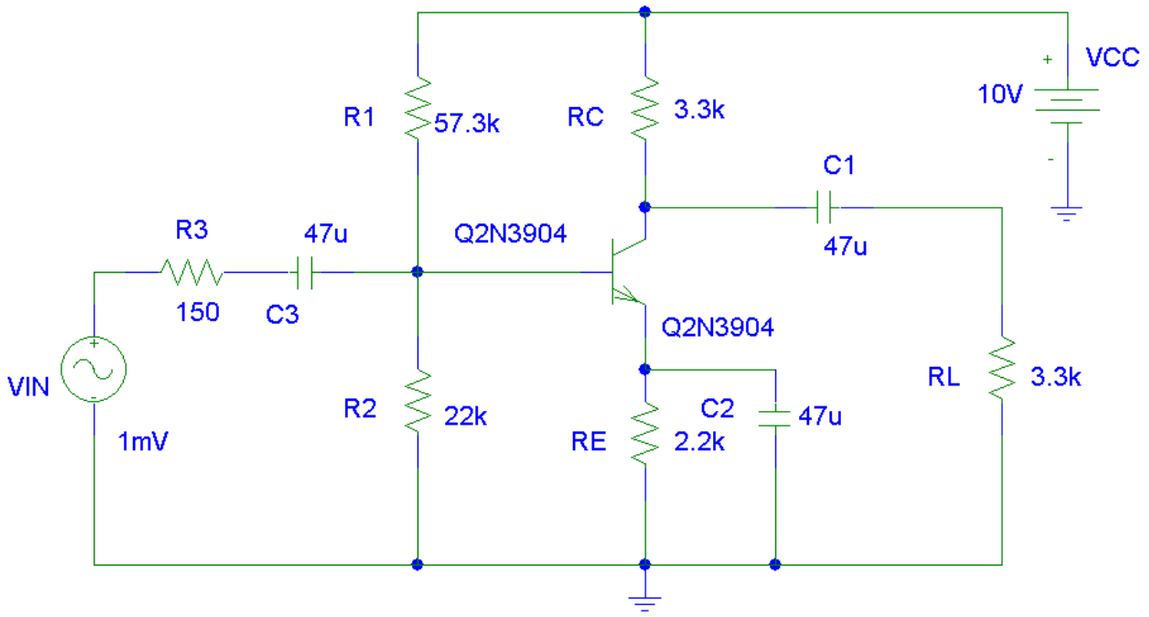


Fig.4. Circuit for Small signal analysis using BJT

3.1. Draw the circuit shown in Fig. 4 in PSpice schematics.

3.2. Here, VIN is variable frequency AC source (Having **Part Name** of **VAC**). Set its amplitude to 1 mV, keeping other parameters (e.g. Vdc) to zero value.

3.3. Select AC Sweep from **Setup Analysis**. Select sweep from 10 Hz to 10 MHz (or higher or lower, ensure that you observe both the cut-off frequencies) in Decade mode, with 20 Pts/decade.

3.4. Run the simulation.

3.5. Observe the voltage gain ($A_V=v_o/v_{in}$) and phase shift between v_o and v_i at different frequencies. [For obtaining phase difference click on the **Add trace** icon, obtain the plotting of **P**(v_o)-**P**(v_{in})].

3.6. Normalize the voltage gain $A_{VN}=A_V/A_{Vmax}$

3.7. Plot the voltage gain (in dB) vs. frequency (f) [$A_{VdB}=20\log_{10}(A_{VN})$]

3.8. Determine the -3dB (cut-off) frequencies from the plot. Also note the phase difference between v_o and v_i at –3dB frequencies.

3.9. [Home work] At mid-band frequency, note the voltage gain (A_V), current gain (A_I), input resistance (R_i) and output resistance (R_o) of the configuration. For output resistance use the knowledge obtained from thevenin's equivalence. *Preserve these values for further use in later experiments.*

3.10. [Homework] Find the h- parameters of the given CE configuration using the data taken in step 9. Consult references for proper equations.