

Department of Electrical and Electronic Engineering  
Shahjalal University of Science and Technology

**EEE 222: Electronic Circuit Simulation Laboratory**  
**EXPERIMENT NO: 09**

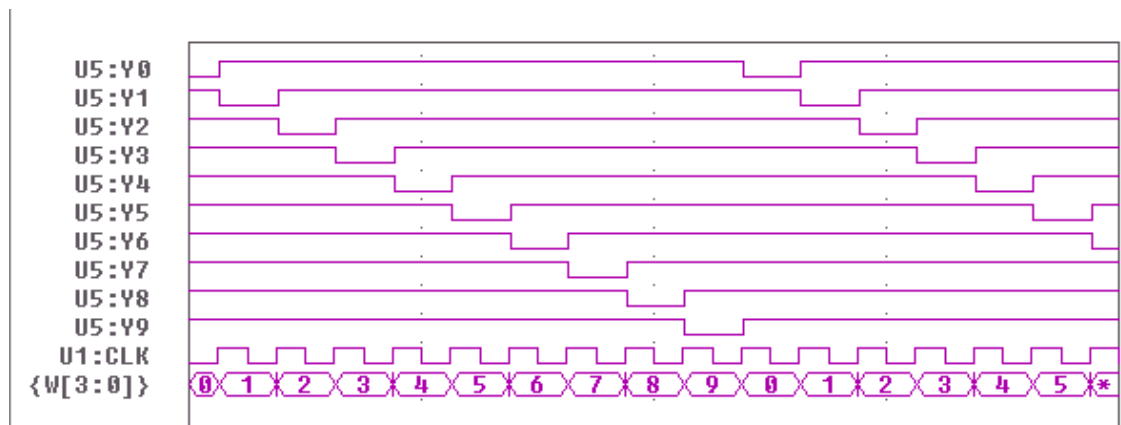
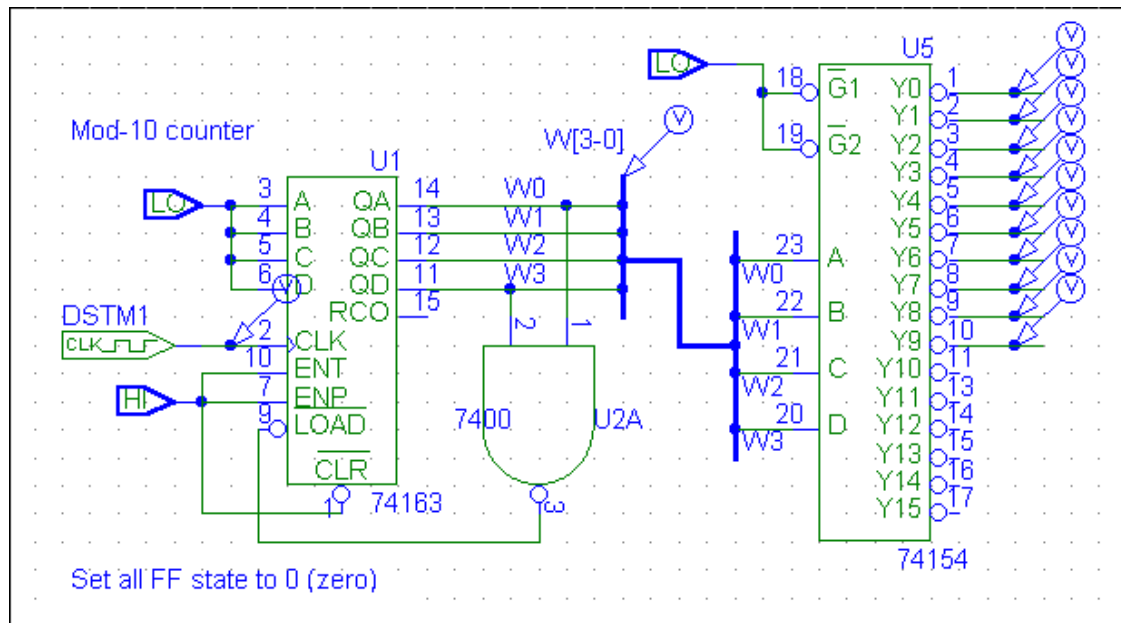
**Name of the Experiment: DIGITAL SIMULATION OF DECODERS**

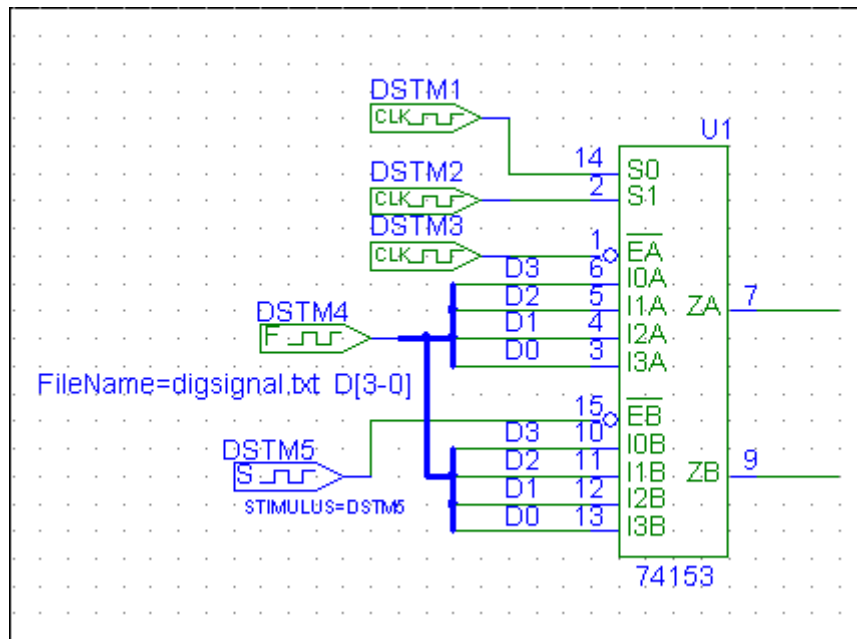
**OBJECTIVES:**

The objectives of this experiment are to

- Simulate the output of a 4-to-16 line decoder
- Simulate the output of a 4-to-10 line (Mod-10) decoder

**THEORY:**





1

**DSTM4 PartName: FileStim**

Name	Value
PKGREF	= DSTM4
FileName=digsignal.txt SigName=D3 D2 D1 D0 IO_MODEL=IO_STM IO_LEVEL=0 ipin(PWR)=\$G_DPWR ipin(GND)=\$G_DGND * REFDES=DSTM4	

☒ Include Non-changeable Attributes  
☒ Include System-defined Attributes

Save Attr  
 Change Display  
 Delete  
 OK  
 Cancel

**\*Header File; This line must be a comment line**  
**D3 D2 D1 D0**

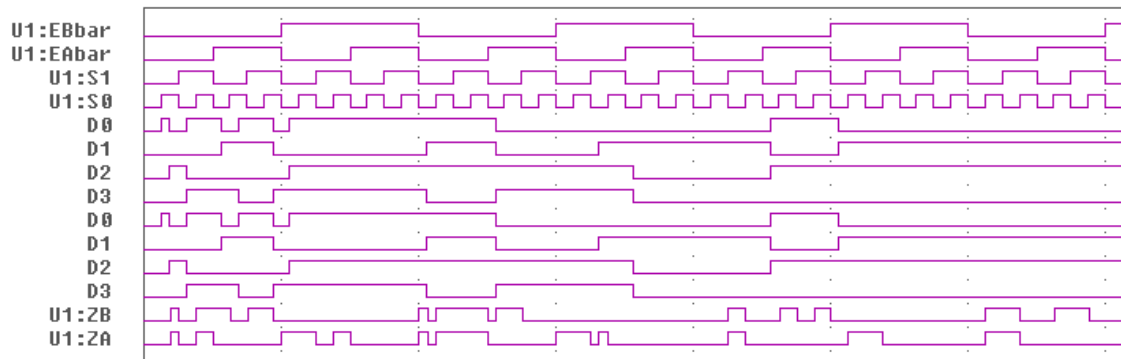
**\*Signal Attribute**

0us 0000  
 +.5us 0001  
 +.25us 0100  
 +.5us 1001  
 +1us 1010  
 +.5us 0011  
 +1us 1000  
 +.5us 1101

**\*Header File; This line must be a comment line**  
**D3 D2 D1 D0**

**\*Signaql Attribute**

**0us 0000**  
**+ .5us 0001**  
**+ .25us 0100**  
**+ .5us 1001**  
**+ 1us 1010**  
**+ .5us 0011**  
**+ 1us 1000**  
**+ .5us 1101**



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**D3 D2 D1 D0**

**\*Signaql Attribute**

**0us 0000**  
**+ .5us 0001**  
**+ .25us 0100**  
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**\*Signaql Attribute**

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