8086 Hardware Specifications

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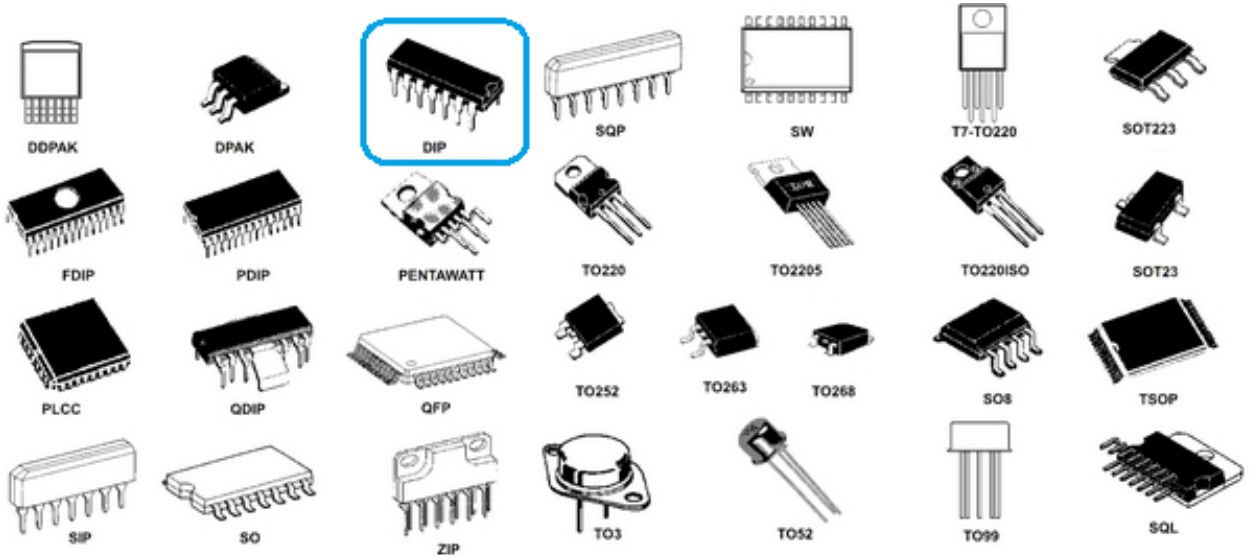
Course ID: CSE 237
Course Title: Microprocessor and Interfacing

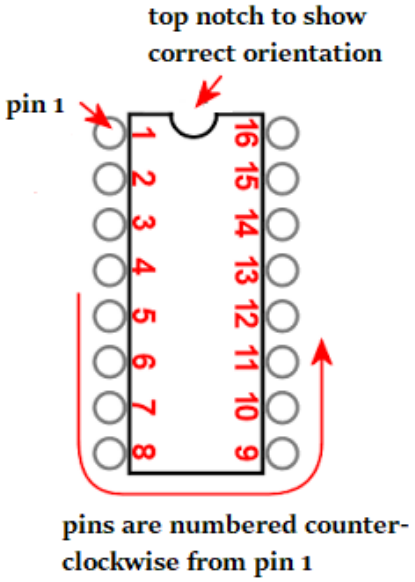
Lecture References:

- **Book:**
  - *Microprocessors and Interfacing: Programming and Hardware,* **Author:** Douglas V. Hall
  - *The 8086/8088 Family: Design, Programming, And Interfacing,* **Author:** John Uffenbeck.

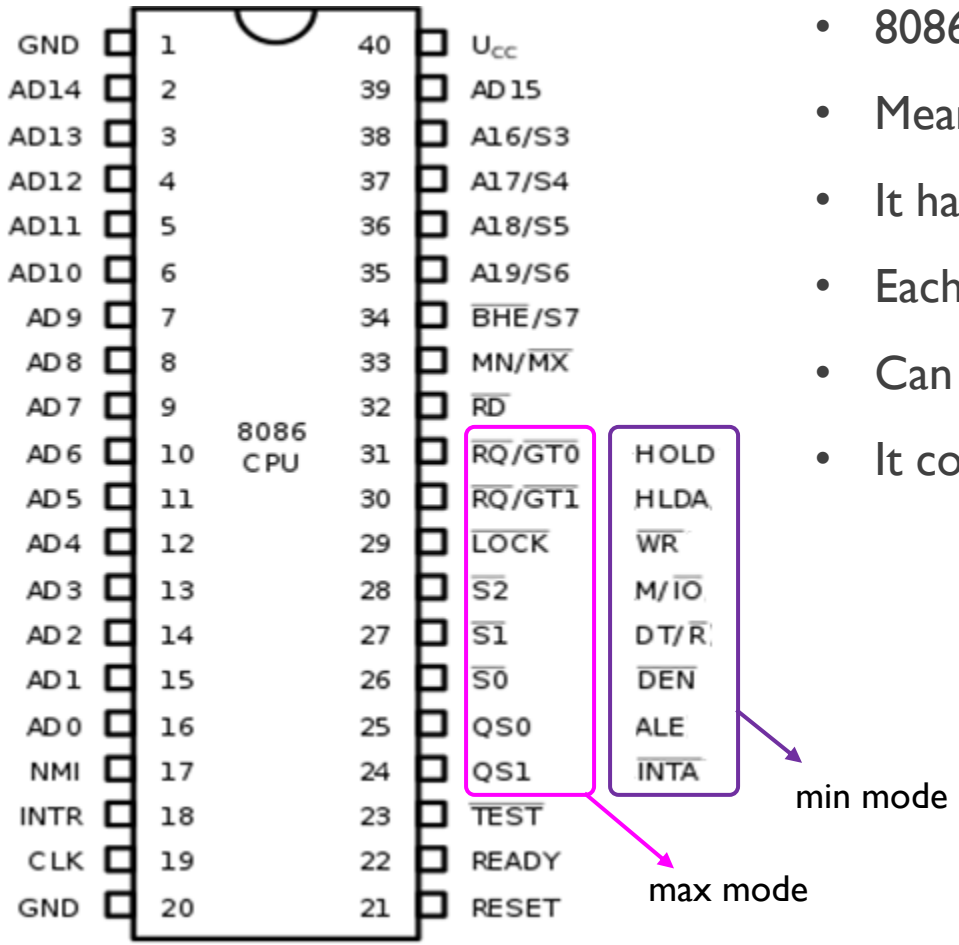
8086 Pin Specification

- is a 40-pin DIPs; **Dual in-line package**
- DIP refers to a rectangular housing with two parallel rows of electrical connection pins.
- DIPs have a notch on one end to show its correct orientation.
- The pins are then numbered as shown in the figure below.





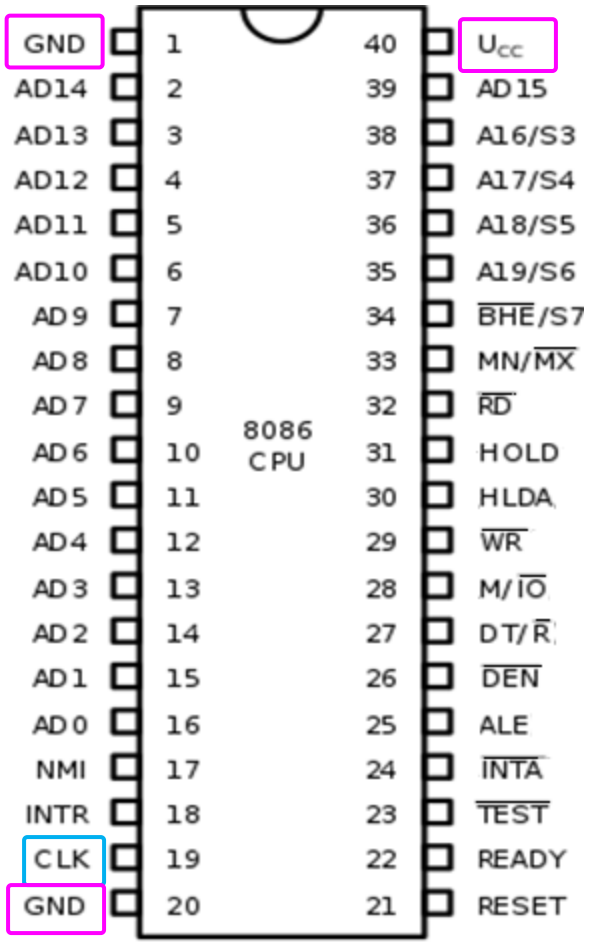
8086 Pin Diagram



Recap

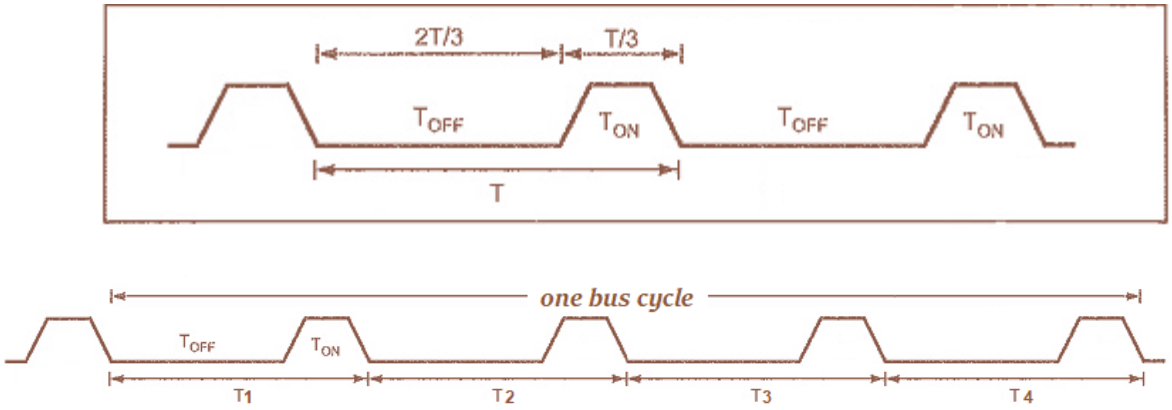
- 8086 is a 16-bit microprocessor.
- Meaning it has 16 data lines/bus.
- It has 20 address lines/bus.
- Each memory location holds only 1 byte
- Can address 2^{20} different memory locations
- It could address up to 1MB of memory.

8086 Pin Specification

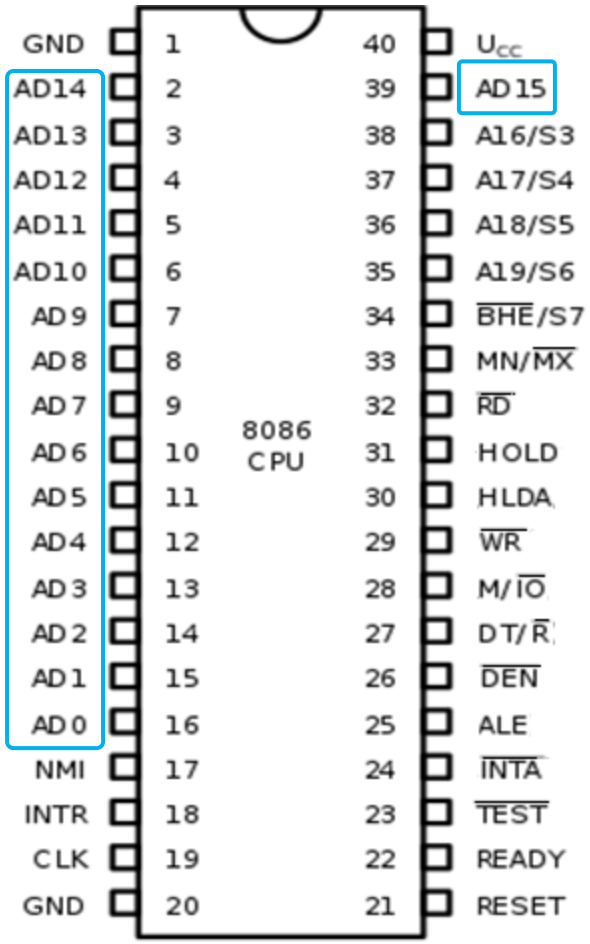


CLK, ***input***

- provides basic timing to control processor operation
- frequencies of different versions are 5, 8 or10 MHz
- asymmetric with a 33% duty cycle



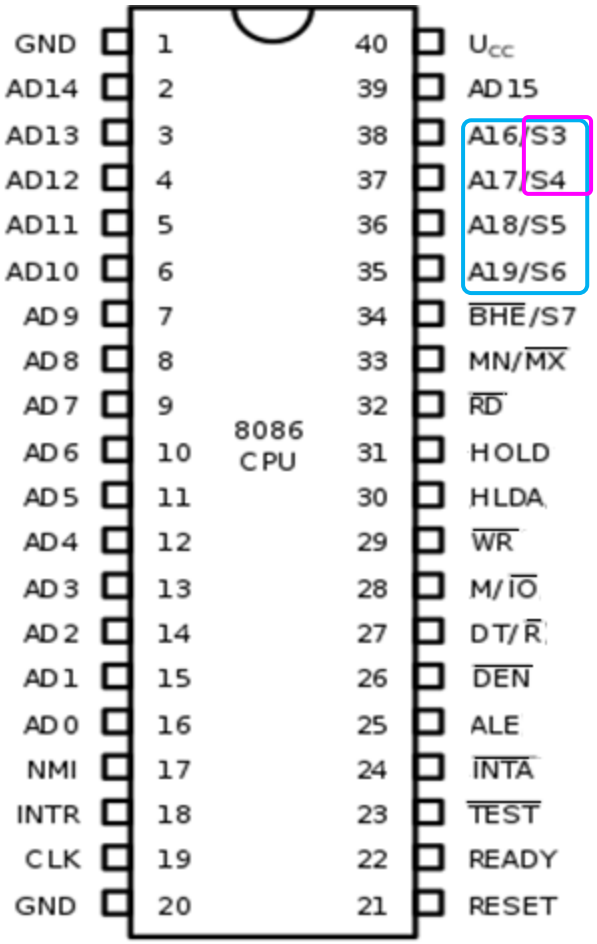
8086 Pin Specification



$$AD_0 - AD_{15}, \boldsymbol{bi - directional}$$

- lines are multiplexed bidirectional address/data bus.
- During T_1, they carry 16-bit address.
- In remaining clock cycles $T_2, T_3\ and\ T_4$, 16-bit data.
- $AD_0 - AD_7$ carry lower order data byte
- $AD_8 - AD_{15}$ carry higher order data byte

8086 Pin Specification

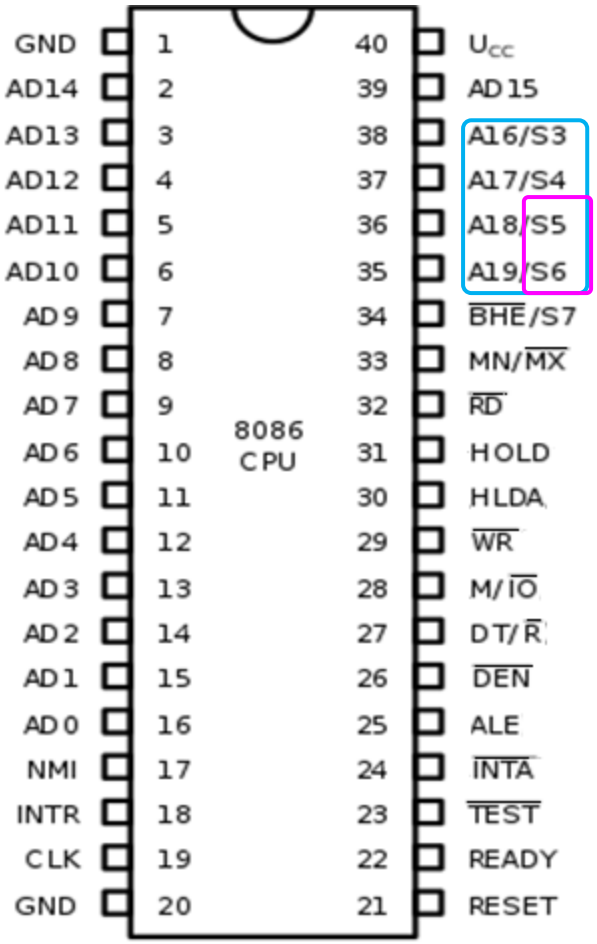


$A_{19}/S_6, A_{18}/S_5, A_{17}/S_4, A_{16}/S_3$, ***output***

- lines are multiplexed address and status bus.
- During T_1, they carry the highest order 4-bit address.
- During T_2, T_3 *and* T_4, status signals.
- S_3 *and* S_4, segment identifiers as in table below

S4	*S3*	*Function*
0	*0*	*Extra segment access*
0	*1*	*Stack segment access*
1	*0*	*Code segment access*
1	*1*	*Data segment access*

8086 Pin Specification



$A_{19}/\boldsymbol{S_6}, A_{18}/\boldsymbol{S_5}, A_{17}/S_4, A_{16}/S_3, \boldsymbol{output}$

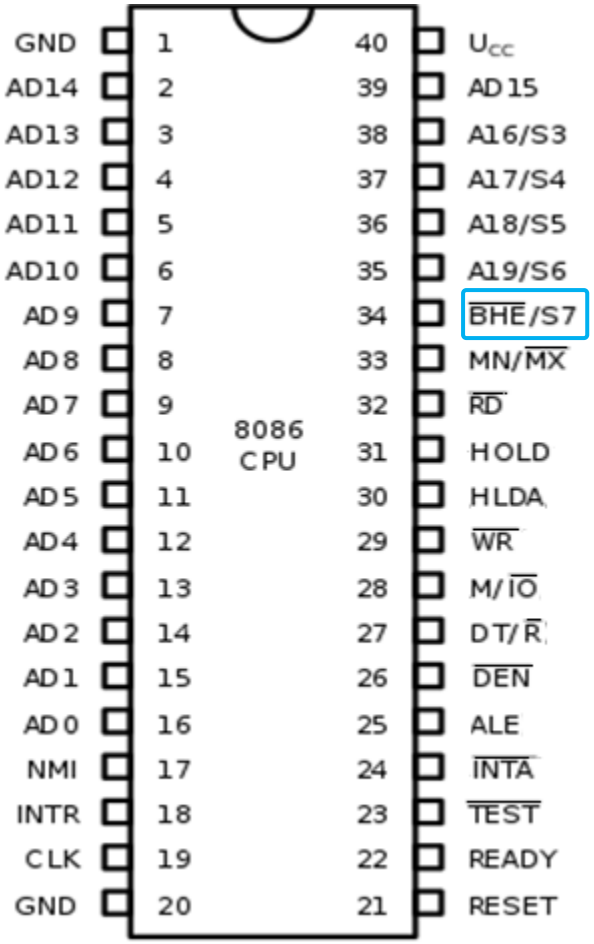
S_5 : Indicates if interrupt is enabled or disabled.

- If S_5 =1 , then the IF = 1, so the interrupt is enabled.
- If S_5 =0 , then the IF = 0, so the interrupt is disabled.

S_6 : Indicates if 8086 is the bus master or not

- If S_6 = 0 , 8086 is the bus master
- If S_6 = 1 , 8086 is not the bus master

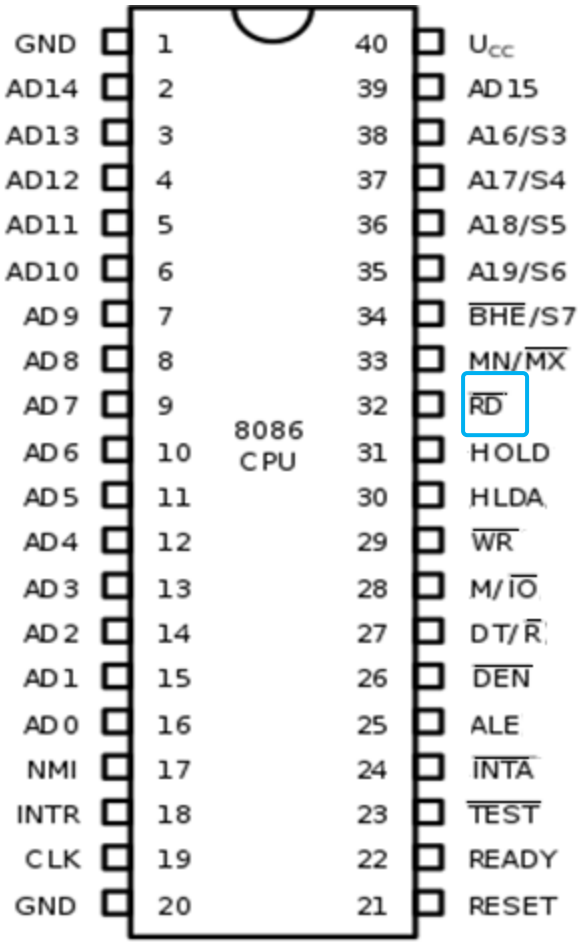
8086 Pin Specification



$\overline{BHE}/S_7$, ***output***

- Bus High Enable
- $\overline{BHE}$ is active low
- To indicate the transfer of data over $AD_8 - AD_{15}$
- Related to memory bank
- Selects odd/high memory bank when $\overline{BHE}$ is 0
- S_7 : Reserved for further development

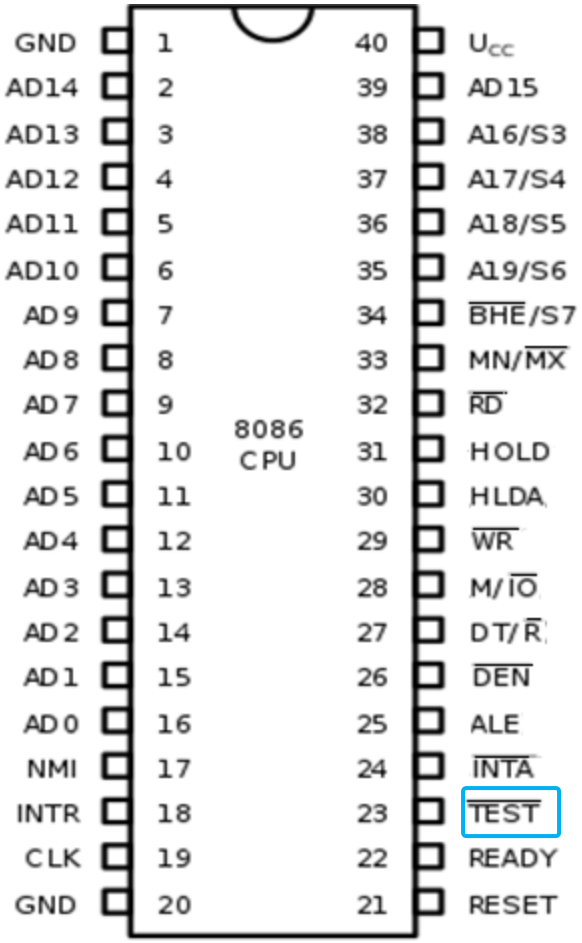
8086 Pin Specification



$\overline{RD}$, ***output***

- is active low
- Indicates read operation when low
- Processor reading from memory or I/O device
- Is low during T_2, T_3 *and* T_w states of the read cycle

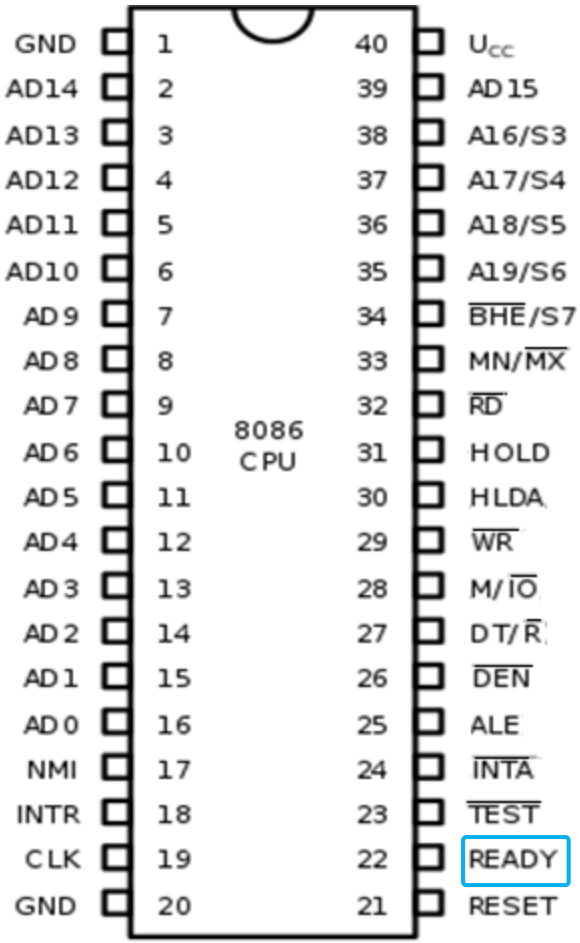
8086 Pin Specification



$\overline{TEST}$, ***input***

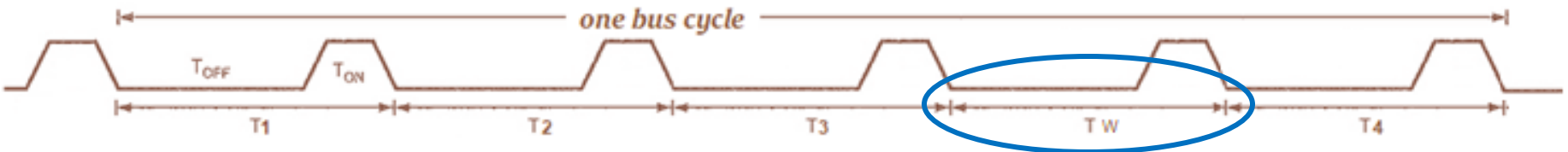
- Is examined by the WAIT instruction.
- If this pin is Low, execution continues.
- Else the processor waits in an idle state.

8086 Pin Specification

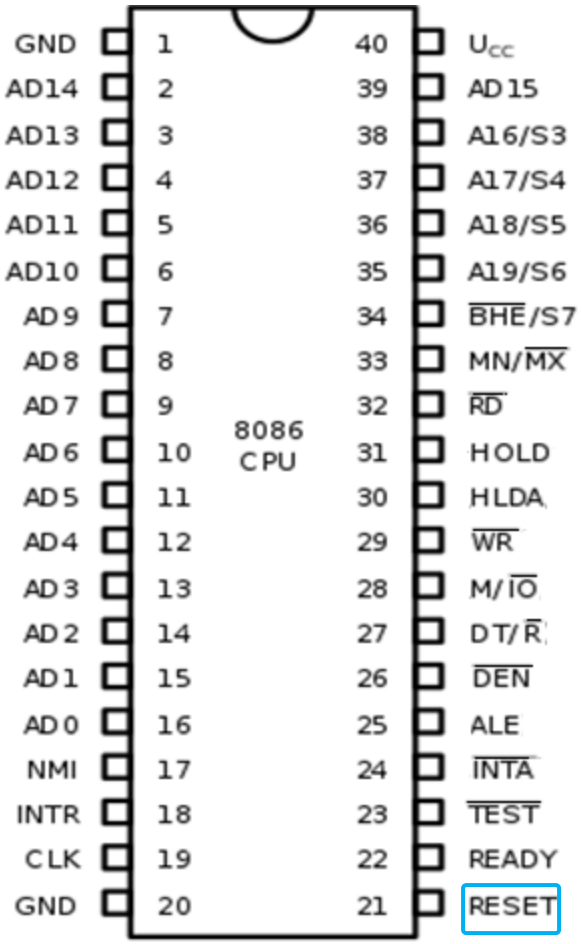


READY, ***input***

- acknowledgement from a slow I/O device or memory
- To indicate ready/completion of data transfer
- When low, microprocessor enters wait state, T_w.



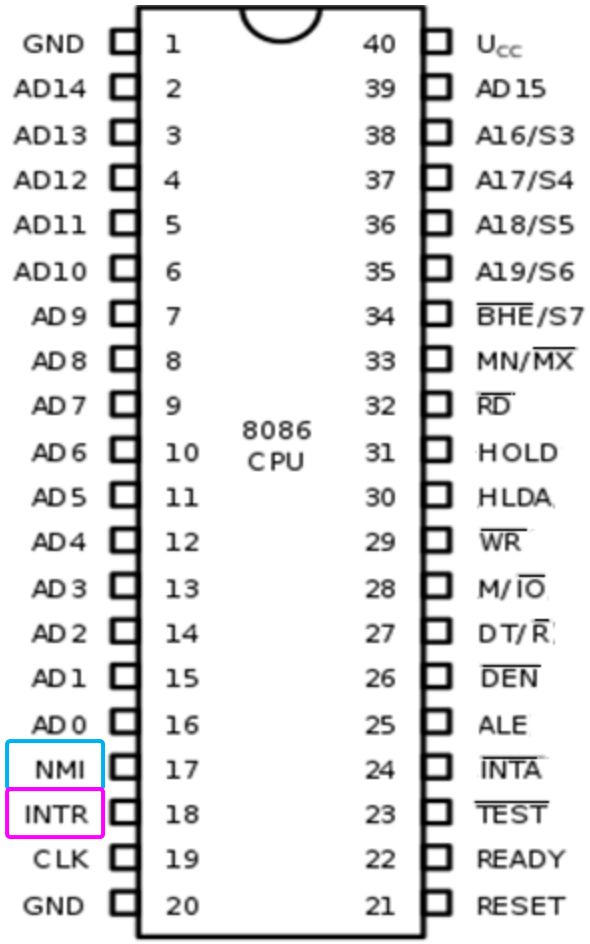
8086 Pin Specification



RESET, ***input***

- To reset the system reset.
- And terminates the current activity.
- Must be active for at least four clock cycles

8086 Pin Specification



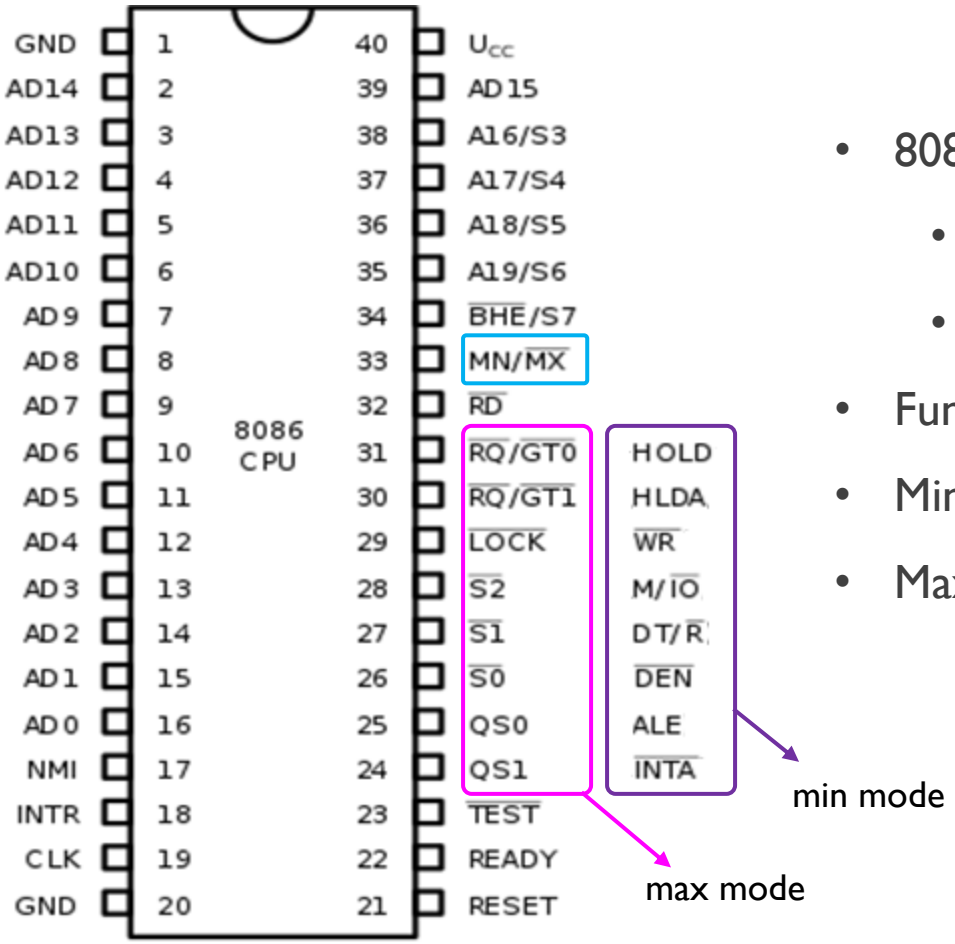
INTR, ***input***

- Interrupt request
- Used to request a hardware interrupt.
- Can be masked.

NMI, ***input***

- Non-maskable interrupt signal.
- Causes a type-2 interrupt.
- Initiates the interrupt at the end of the current instruction.

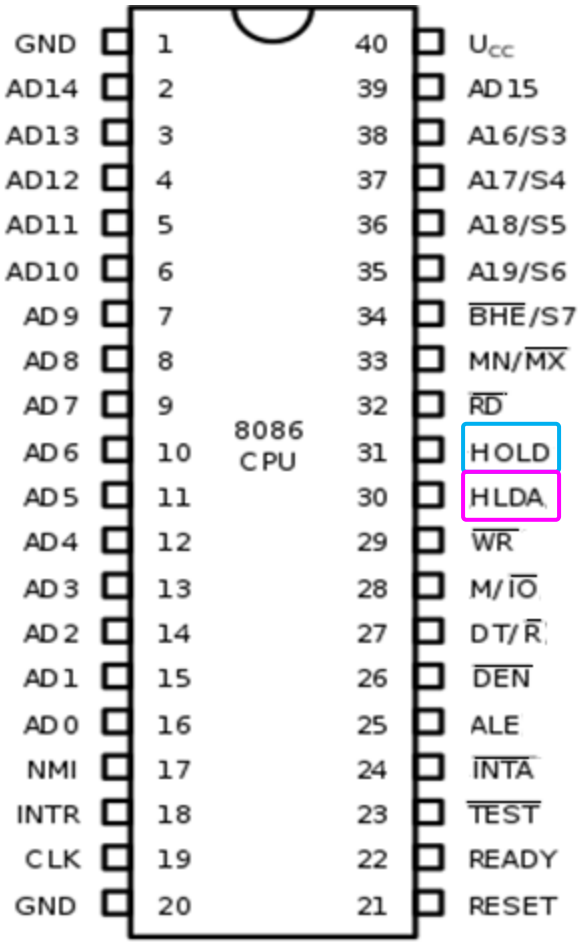
8086 Pin Specification



$MN/\overline{MX}$, ***input***

- 8086 works in two modes:
  - Minimum Mode if high
  - Maximum Mode if low
- Functions of pins 24-31 depend on the mode
- Minimum Mode - single processor
- Maximum Mode - multi processor

Minimum Mode Pin Specification



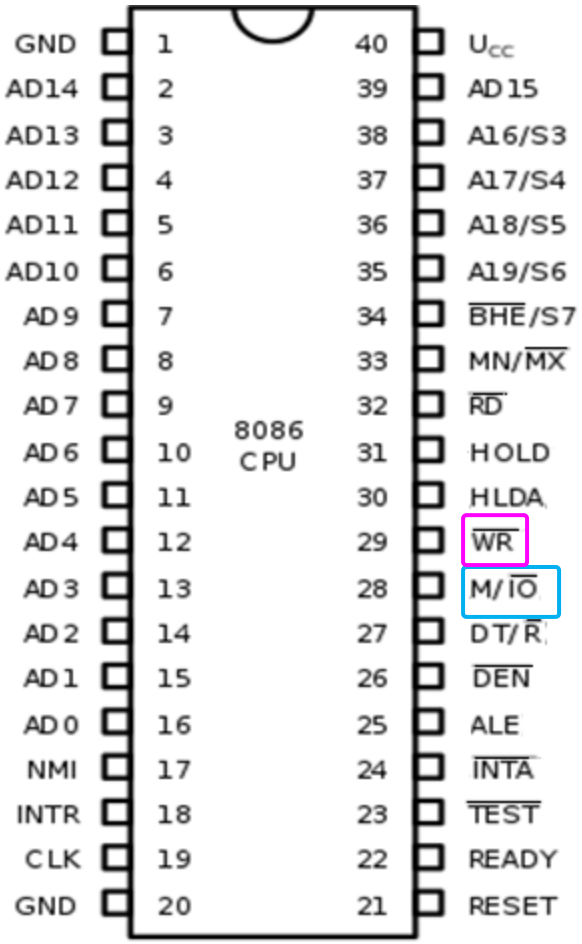
HOLD, ***input***

- To request for bus by another device.
- It is an active HIGH signal.

HLDA, ***output***

- Hold Acknowledgment.
- When acknowledged, it relinquish the bus to the requesting device

Minimum Mode Pin Specification



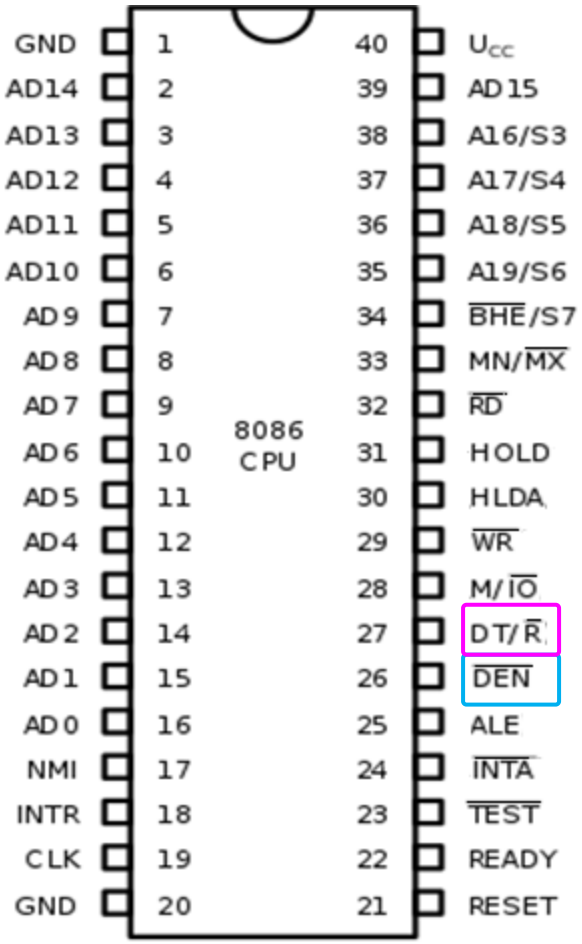
$\overline{WR}$, ***output***

- Active low write signal.
- Writes data to memory or output device depending on $M/\overline{IO}$ signal.

$M/\overline{IO}$, ***output***

- Differentiates memory access from I/O access.
- When high, memory is accessed.
- When low, I/O devices are accessed.

Minimum Mode Pin Specification



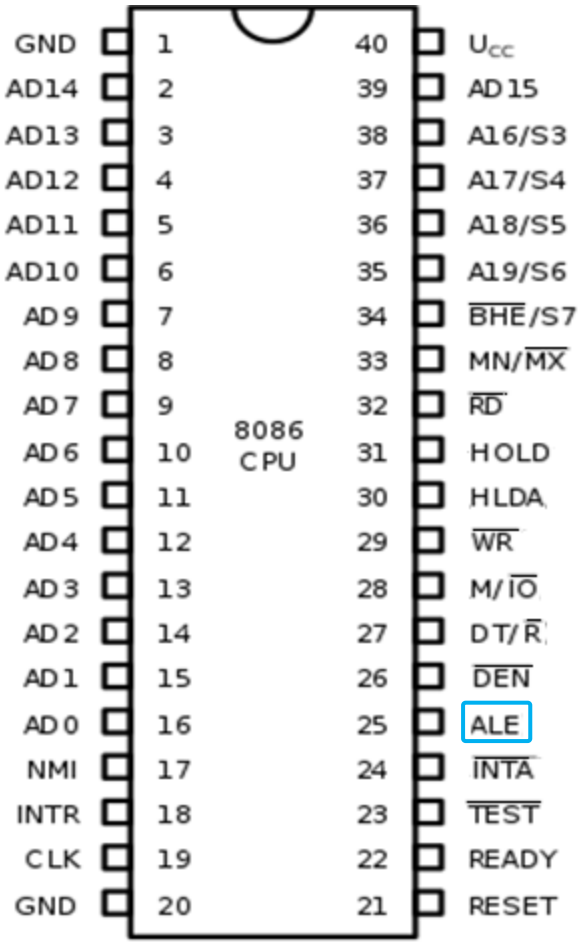
$DT/\bar{R}$, ***output***

- Data Transmit/Receive signal.
- indicates the direction of flow *through the transceiver*.
- When high, data is transmitted out i.e. written to.
- When low, data is received in i.e. read in.

$\overline{DEN}$, ***output***

- Data Enable signal.
- Used to enable a transceiver connected to the µP

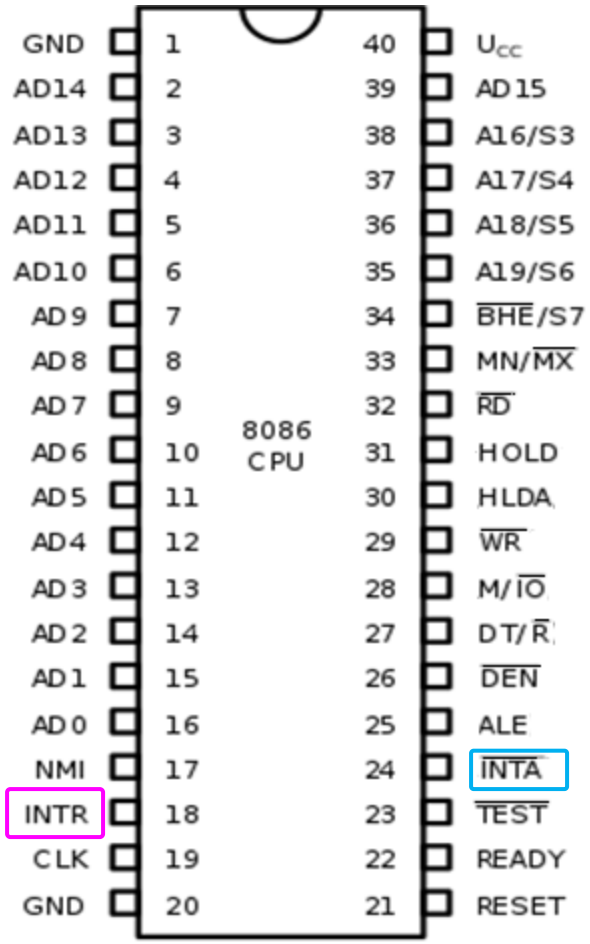
Minimum Mode Pin Specification



ALE, ***output***

- Address Latch Enable
- indicates an address is available on bus $AD_0 - AD_{15}$.
- active high during T_1 state

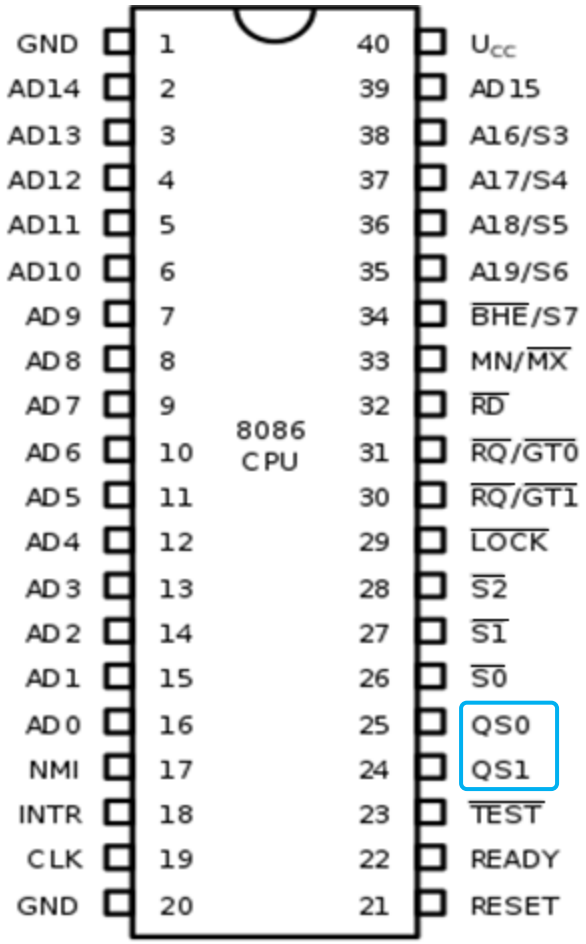
Minimum Mode Pin Specification



$\overline{INTA}$, ***output***

- An active low signal.
- An interrupt acknowledge signal.
- When microprocessor receives an INTR signal, it acknowledges the interrupt by generating this signal
- When low it indicates an interrupt is being serviced.

Maximum Mode Pin Specification

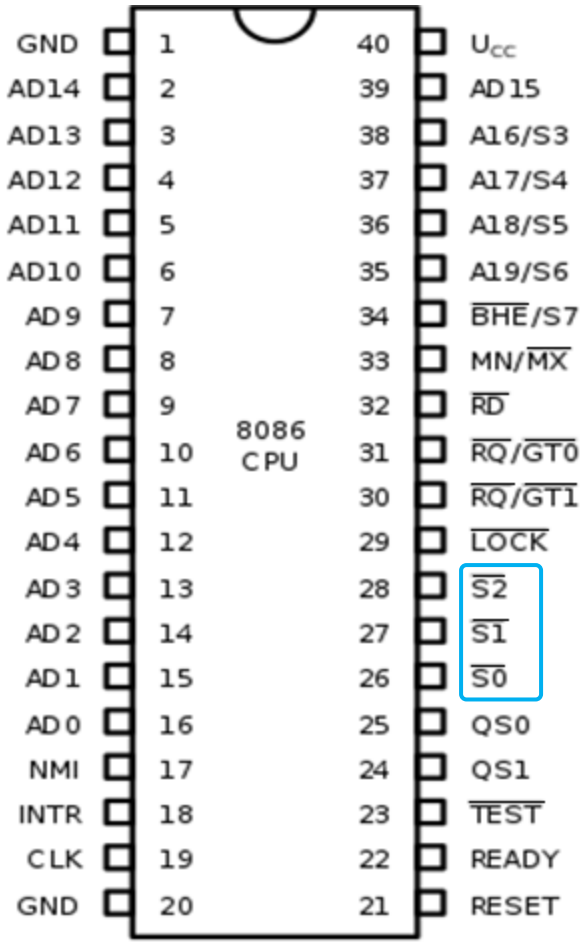


QS_0 *and* QS_1, ***output***

- Instruction queue status.
- Instruction queue is 6 bytes long

QS_1	QS_0	***Function***
0	*0*	*No Operation. During the last clock cycle, nothing was taken from the queue.*
0	*1*	*First Byte. The byte taken from the queue was the first byte of the instruction.*
1	*0*	*Queue Empty. The queue has been reinitialized as a result of the execution of a transfer instruction.*
1	*1*	*Fetch subsequent byteSubsequent Byte. The byte taken from the queue was a subsequent byte of the instruction.*

Maximum Mode Pin Specification

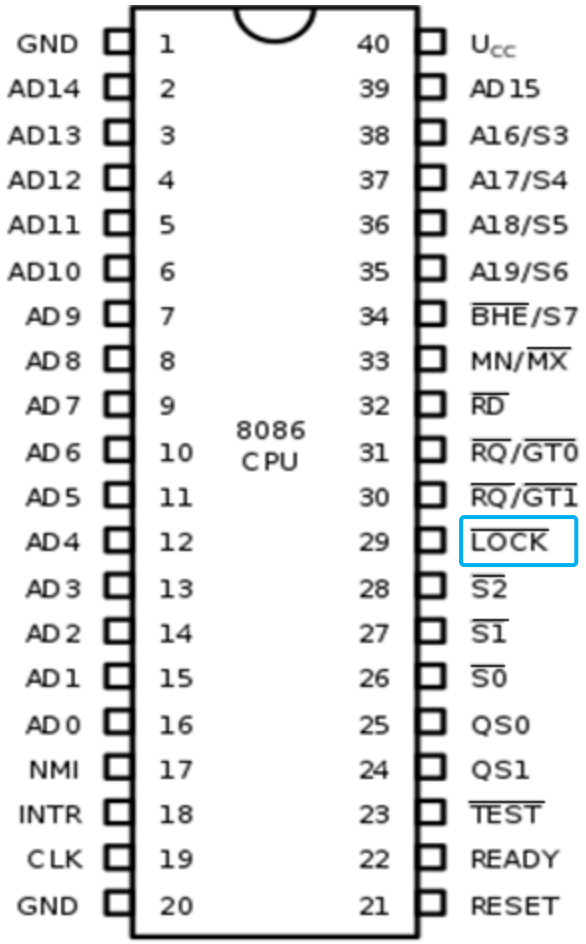


$\overline{S_0}, \overline{S_1}, \overline{S_2}, \boldsymbol{output}$

- Status Signals.
- indicate operation done by the microprocessor
- Related to memory and I/O access control signals.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	**Function**
0	0	0	Interrupt acknowledgement
0	0	1	Read data from I/O port
0	1	0	Write data from I/O port
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive state

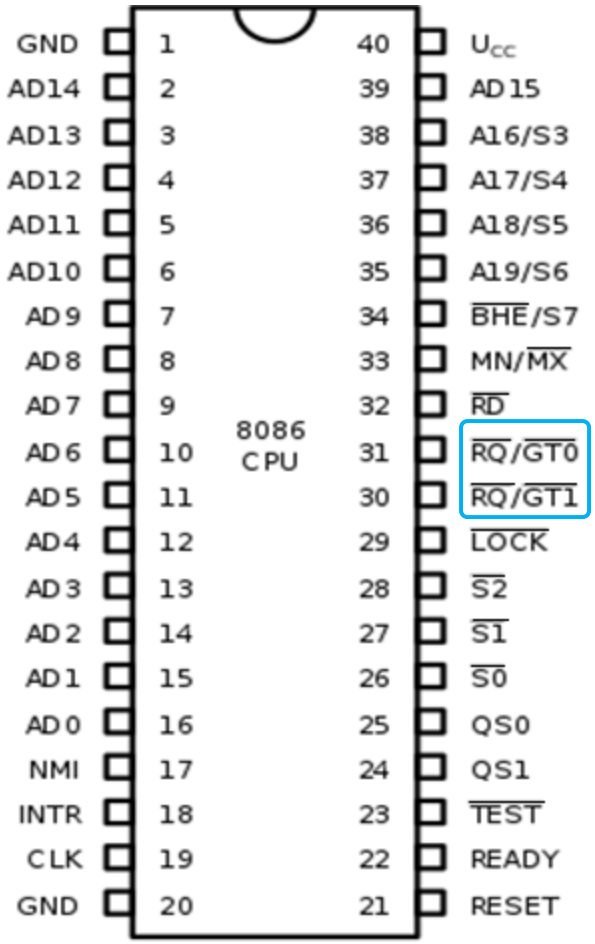
Maximum Mode Pin Specification



$\overline{LOCK}$, ***output***

- When low, all interrupts are masked
- Indicates to other processors to not request for system bus.
- No HOLD request is granted.
- No bus is relinquished to the other processors

Maximum Mode Pin Specification



$\overline{RQ/GT_0}$ **and** $\overline{RQ/GT_1}$, ***bi − directional***

- Request/Grant pins.
- Other processors request the CPU through these for system bus.
- CPU sends acknowledge signal on the same lines.
- $\overline{RQ/GT_0}$ has higher priority than $\overline{RQ/GT_1}$.

QUIZ

1) Assuming you want to type a secret message using a keypad connected to an 8086 microprocessor, deduce the values of the following pins during that time. Justify your answers too.
   a) $\overline{RD}$ e.g. mention if low (0) / high (1) and why.
   b) $\overline{WR}$
   c) $\mathrm{M}/\overline{IO}$
2) Do you think there may be other pins involved? If so, justify your answer.

Thank You !!