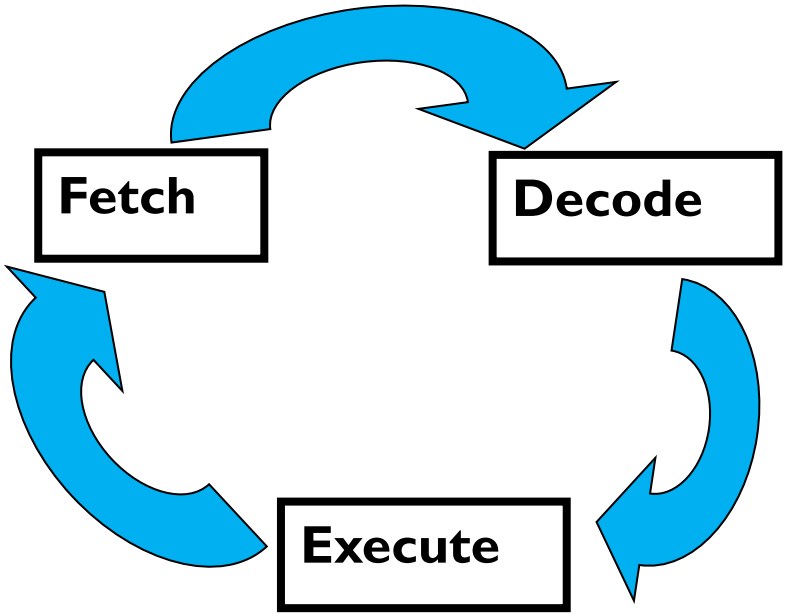
8086 Clocks & Timing Diagrams

Course Teacher:

Md. Fahmidur Rahman Sakib
Lecturer, Department of Computer Science & Engineering
Metropolitan University

Course ID: CSE 237
Course Title: Microprocessor and Interfacing

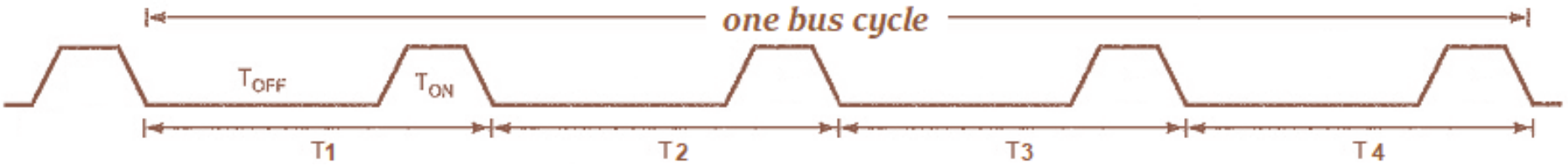
Microprocessor Operation

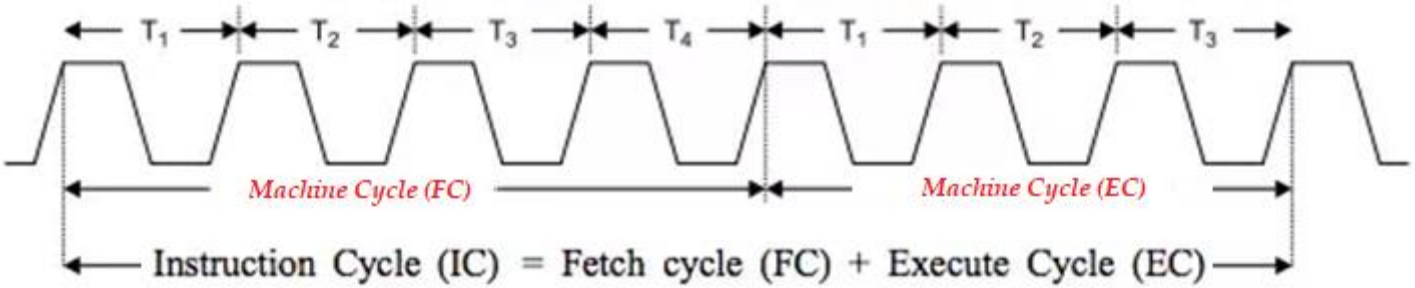


- An instruction e.g. MOV [7531h], AX ; SUB CH, [0ABCh] etc
- The time a µP requires to complete **fetch-(decode)-execute** operation of a single instruction is known as ***Instruction Cycle***

Microprocessor Operation

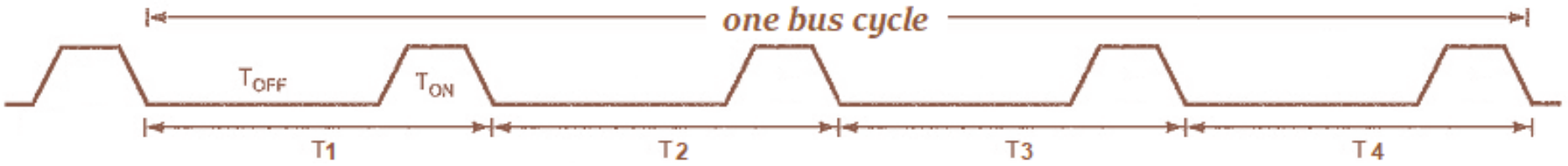
- ***Instruction Cycle*** consists of one or more ***Machine Cycles***
- A basic µP operation such as reading/writing a byte from or to memory or I/O port is called a ***Machine/Bus cycle***





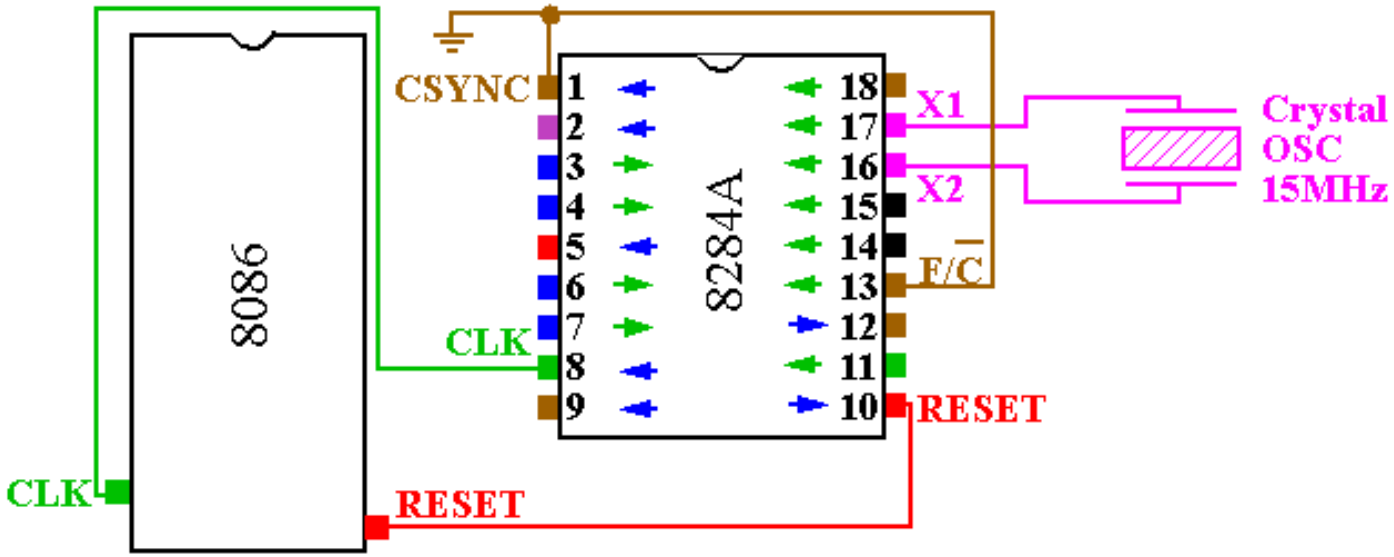
Microprocessor Operation

- A ***Machine (bus) cycle*** consists of at least **four** clock cycles, called **T** states.
- One cycle of a clock is called a **State**
- Each read or write operation takes 1 bus cycle.



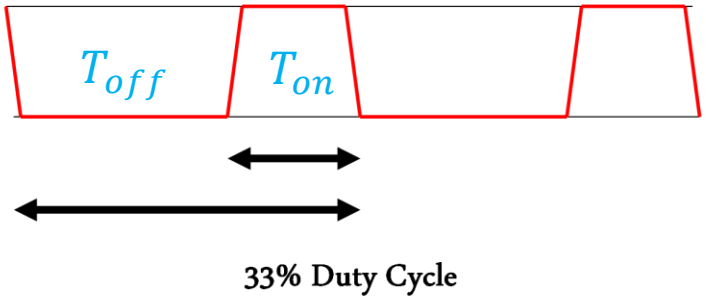
Clock Generation

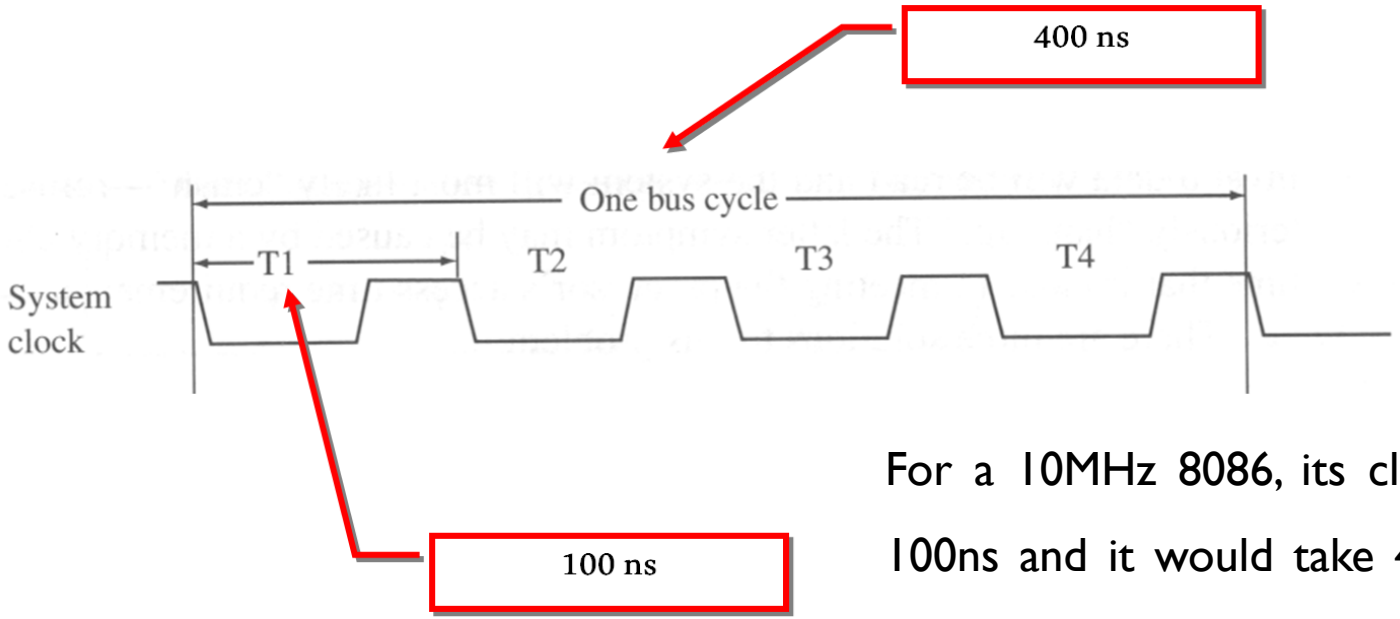
- Clock generator circuit is 8284A and connected to **pin 19** (**CLK**) of 8086.



System Clock Concept

- 8086 is found to operate in between 5 to 10 Mhz.
- An 8086 running at 5MHz, its clock pulses will be of 200ns and it would take 800ns for a complete bus cycle.





For a 10MHz 8086, its clock pulses will be of 100ns and it would take 400ns for a complete bus cycle.

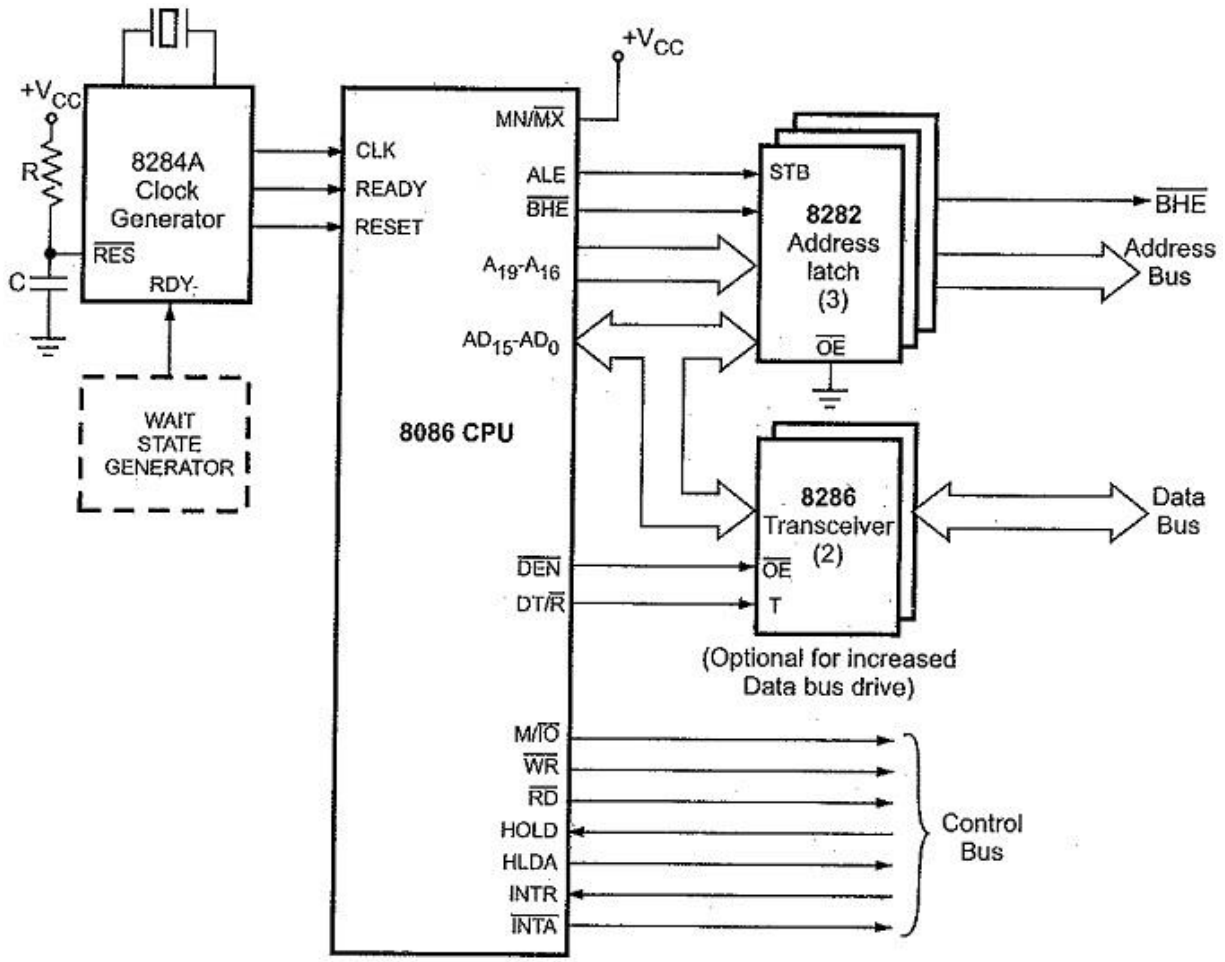


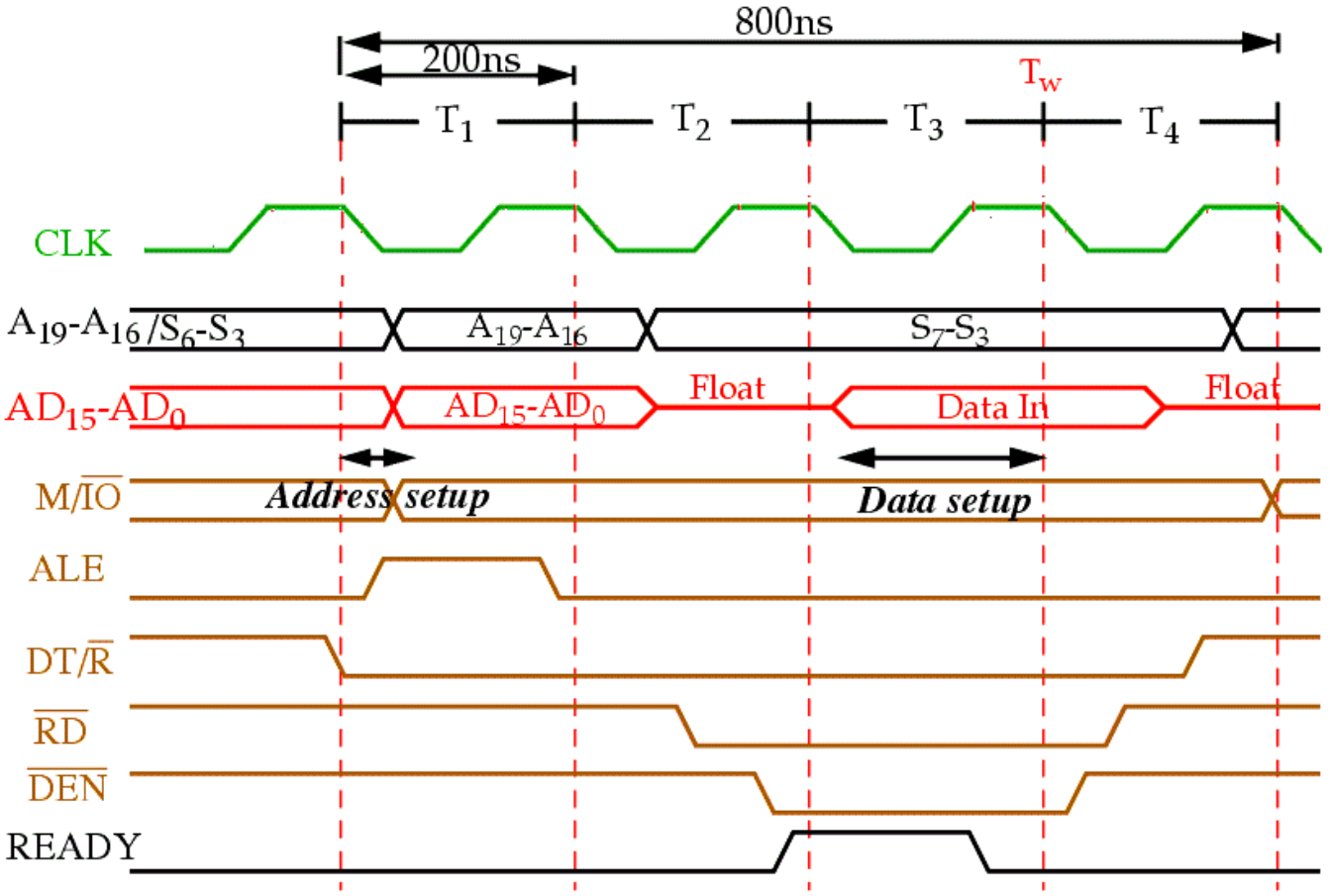
Fig. 10.2 Typical minimum mode configuration

Clock States - Why are there T states?

- In 8086, address and data lines are multiplexed to reduce number of pins e.g. AD_{0-15} else 32 pins would have been needed instead of 16
- The µp needs time to change the signals during each bus cycle.
- Memory devices need time to interpret the address value and then **read/write** the data (*access time*)
- A specific defined action occurs during each T state (***T*** $_1$ - ***T*** $_4$)
  - ***T*** $_1$: Address is output
  - ***T*** $_2$: Bus cycle type (Mem/IO, read/write)
  - ***T*** $_3$: Data is supplied / Data is received
  - ***T*** $_4$: Data latched by CPU, control signals removed

READ BUS Timing (Complete BUS Cycle)

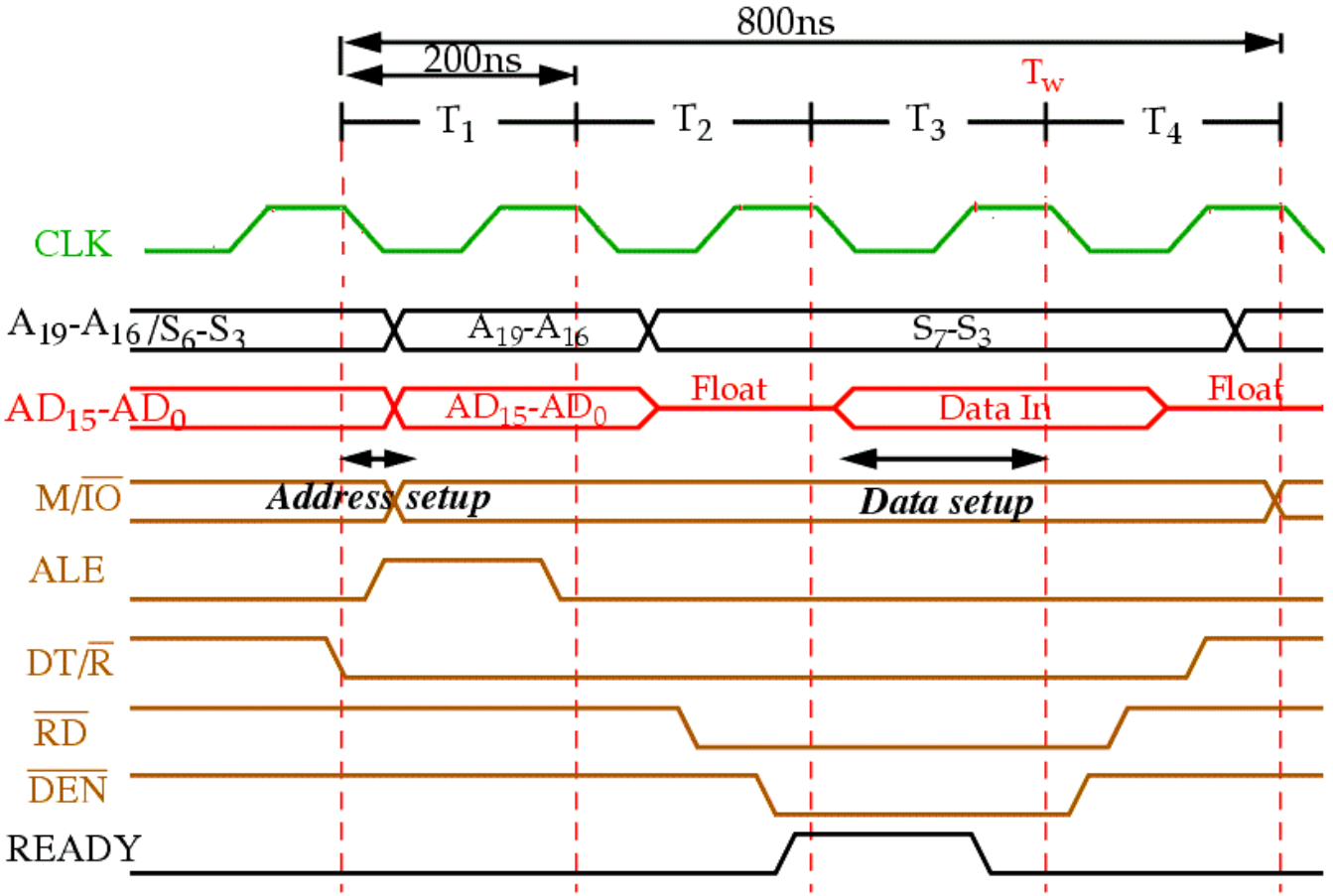
T_1: Address is output



Address of memory is sent out by 8086 via address bus
Used Control signals: ALE, DT/R', M/IO' shows some output

READ BUS Timing (Complete BUS Cycle)

T_2: Bus cycle type (MEMORY/IO, READ/WRITE)

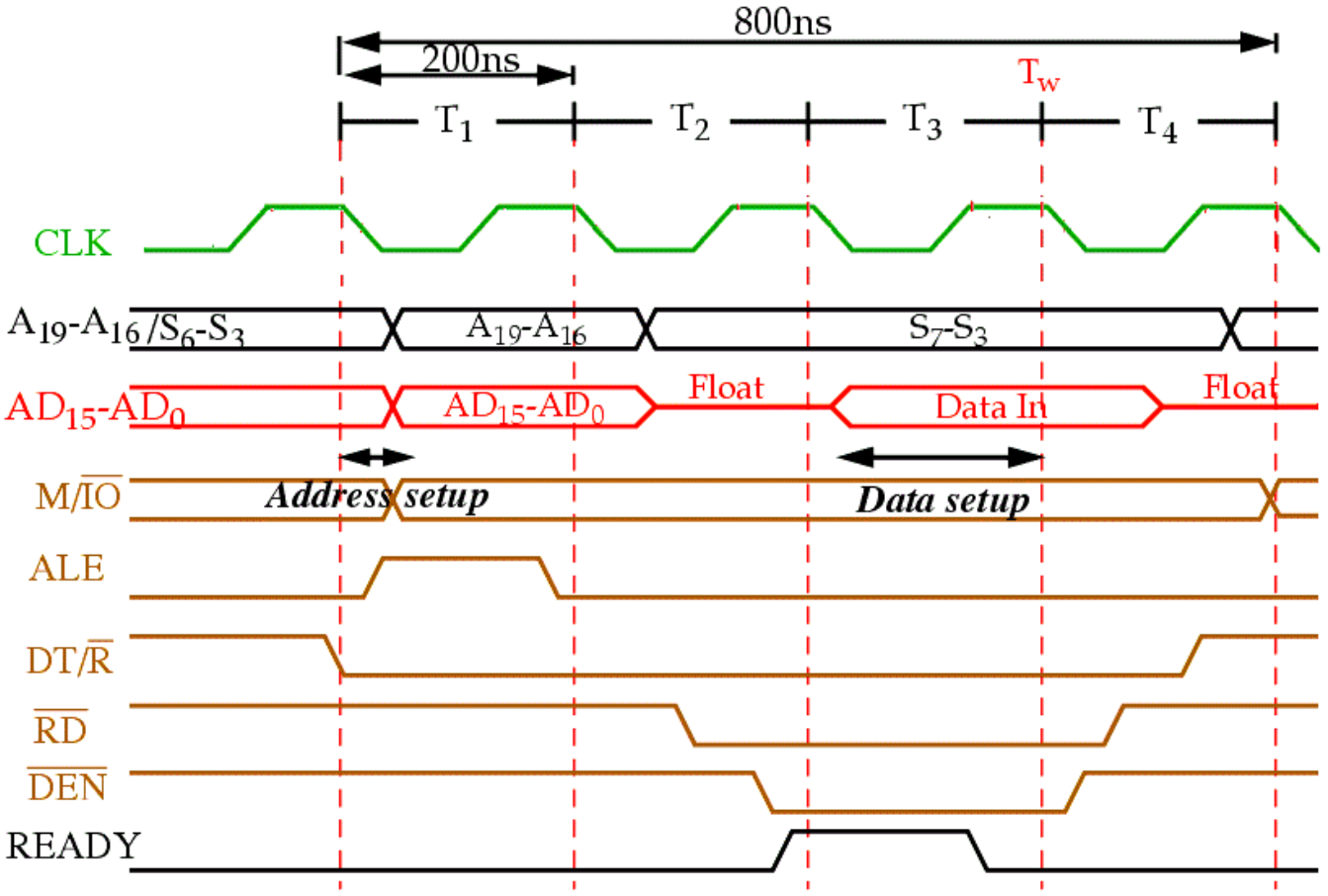


8086 issues either RD' or WR' and DEN'

In case of WRITE (WR) operation, data to be written appear on data bus

READ BUS Timing (Complete BUS Cycle)

T_3: Data is supplied



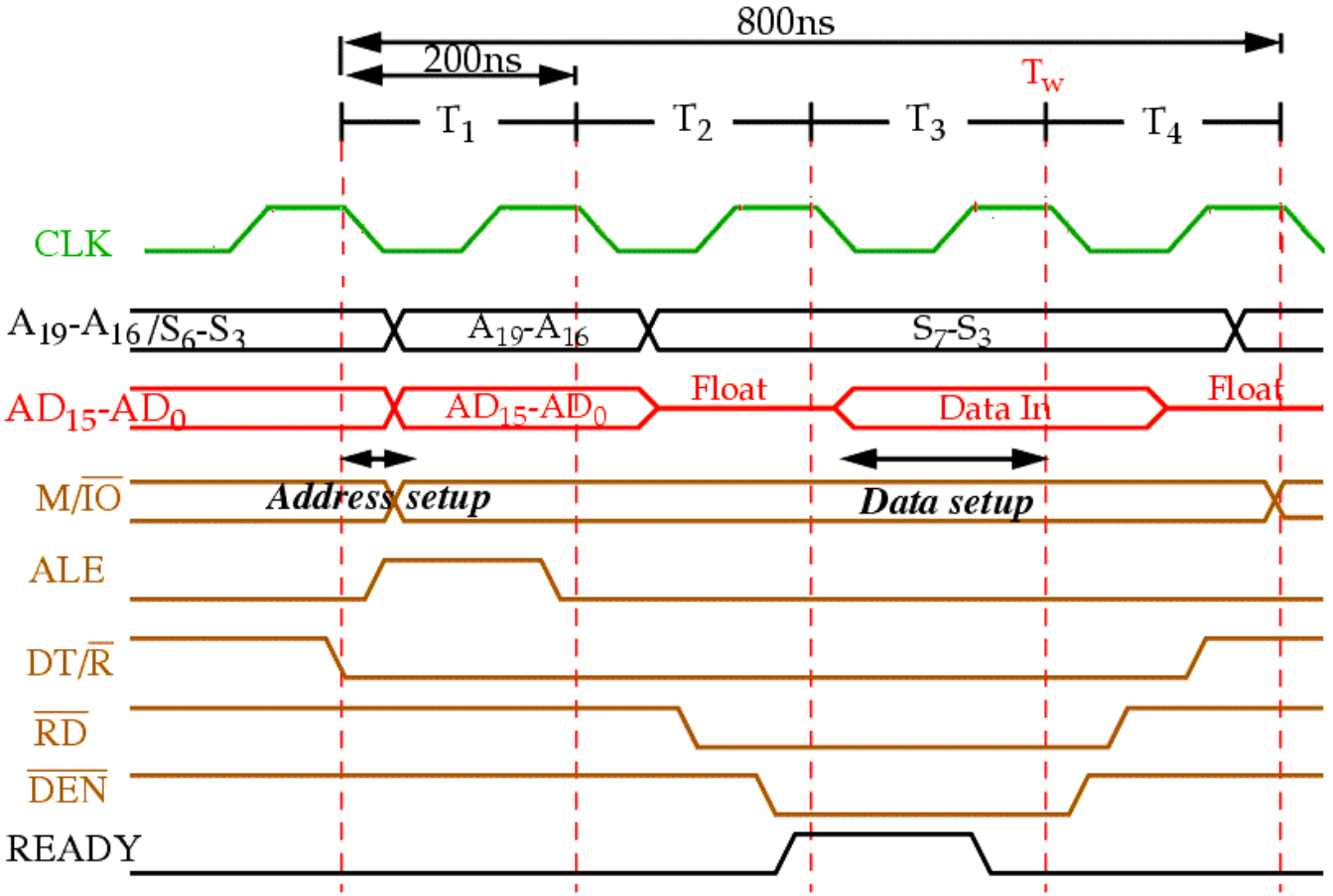
READY is sampled at the end of T2

If READY is low, T3 becomes a wait state (Tw), means no operation (NOP).

In READ bus cycle data bus is sampled at end of T3

READ BUS Timing (Complete BUS Cycle)

T_4: Data latched by µP, control signals removed



All bus signals deactivated in preparation for next bus cycle
µP sampled data bus for data that read from M or I/O

Clock States

- A specific, defined action occurs during each T states ($T_1 - T_4$)
- **T_1**: Address is output
  - Address of memory is sent out by 8086 via address bus
  - Used Control signals: ALE, DT/R', M/IO' shows some output
- **T_2**: Bus cycle type (MEMORY/IO, READ/WRITE)
  - 8086 issues either RD' or WR' and DEN'
  - In case of **WRITE (WR)** operation, data to be written appear on data bus

Clock States

- **T_3**: Data is supplied
  - READY is sampled at the end of T_2
    - If READY is low, T_3 becomes a wait state (T_w), means no operation (NOP).
    - In **READ** bus cycle data bus is sampled at end of T_3
- **T_4**: Data latched by µP, control signals removed
  - All bus signals deactivated in preparation for next bus cycle
  - µP sampled data bus for data that read from M or I/O
  - At trailing edge of WR', transfer data to M or I/O

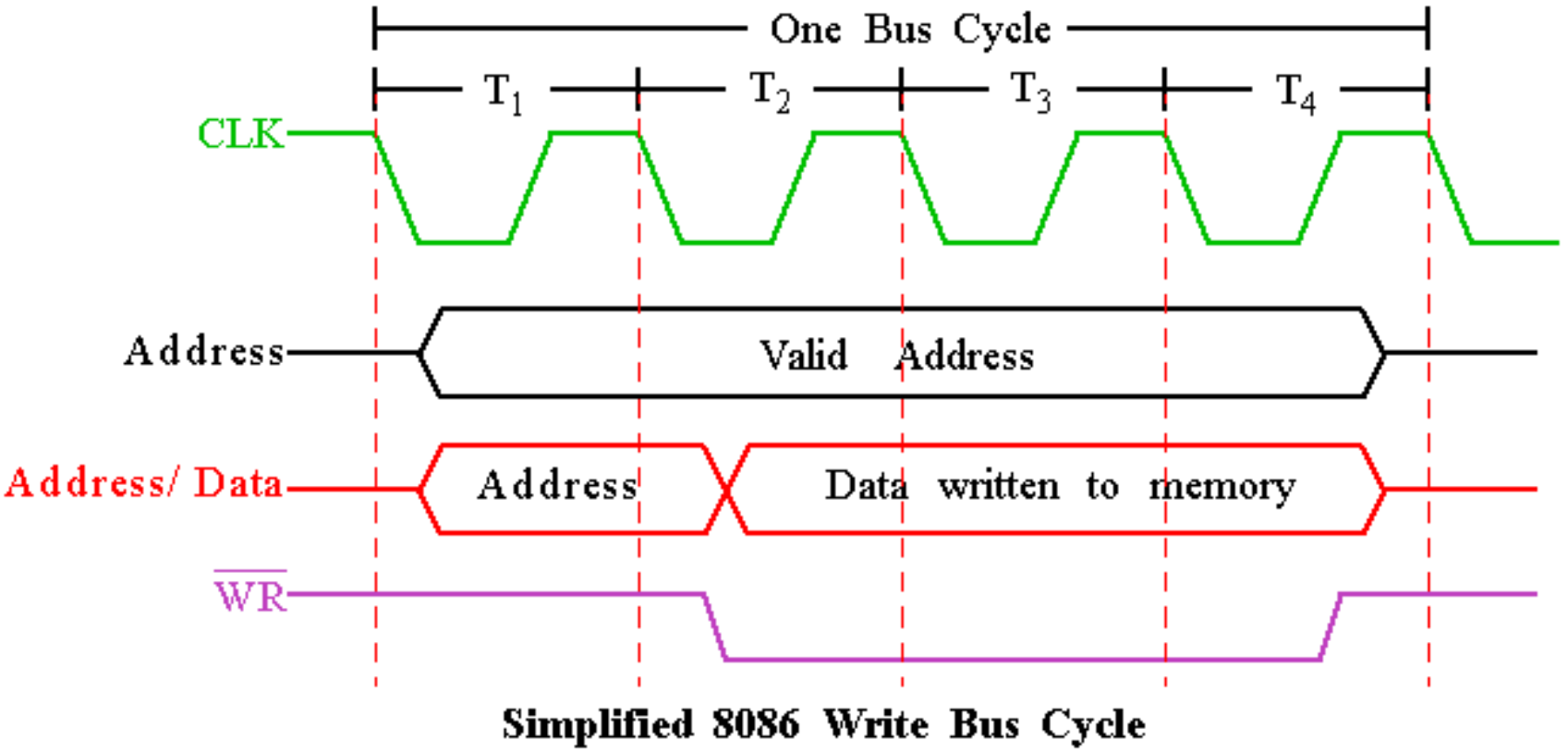
8086 Ready pin

- The READY input is controlled to insert "Wait states" into the timing of the microprocessor for slower memory and I/O components..
- If the READY pin is at a logic 0 level, the micro-processor enters into wait states and remains idle.
- When it is high (logic 1), it indicates that the device is ready to transfer data.
- A wait state is a situation in which a computer processor is waiting for the completion of some event before resuming activity.
- A program or process in a wait state is inactive for the duration of the wait state.

Ready pin and Wait state

- When a computer processor works at a faster clock speed than the random access memory (RAM) that sends it instructions, it is set to go into a wait state for one or more clock cycles so that it is synchronized with RAM speed. In general, the more time a processor spends in wait states, the slower the performance of that processor.
- Wait states are a pure waste for a processor's performance. Modern designs try to eliminate or hide them using a variety of techniques: CPU caches, instruction pipelines, instruction prefetch, simultaneous multithreading and others.

WRITE BUS Timing



Simplified 8086 Write Bus Cycle

- What are the functions of each pin in different **T states** during **WRITE** operation ??

Thank You !!