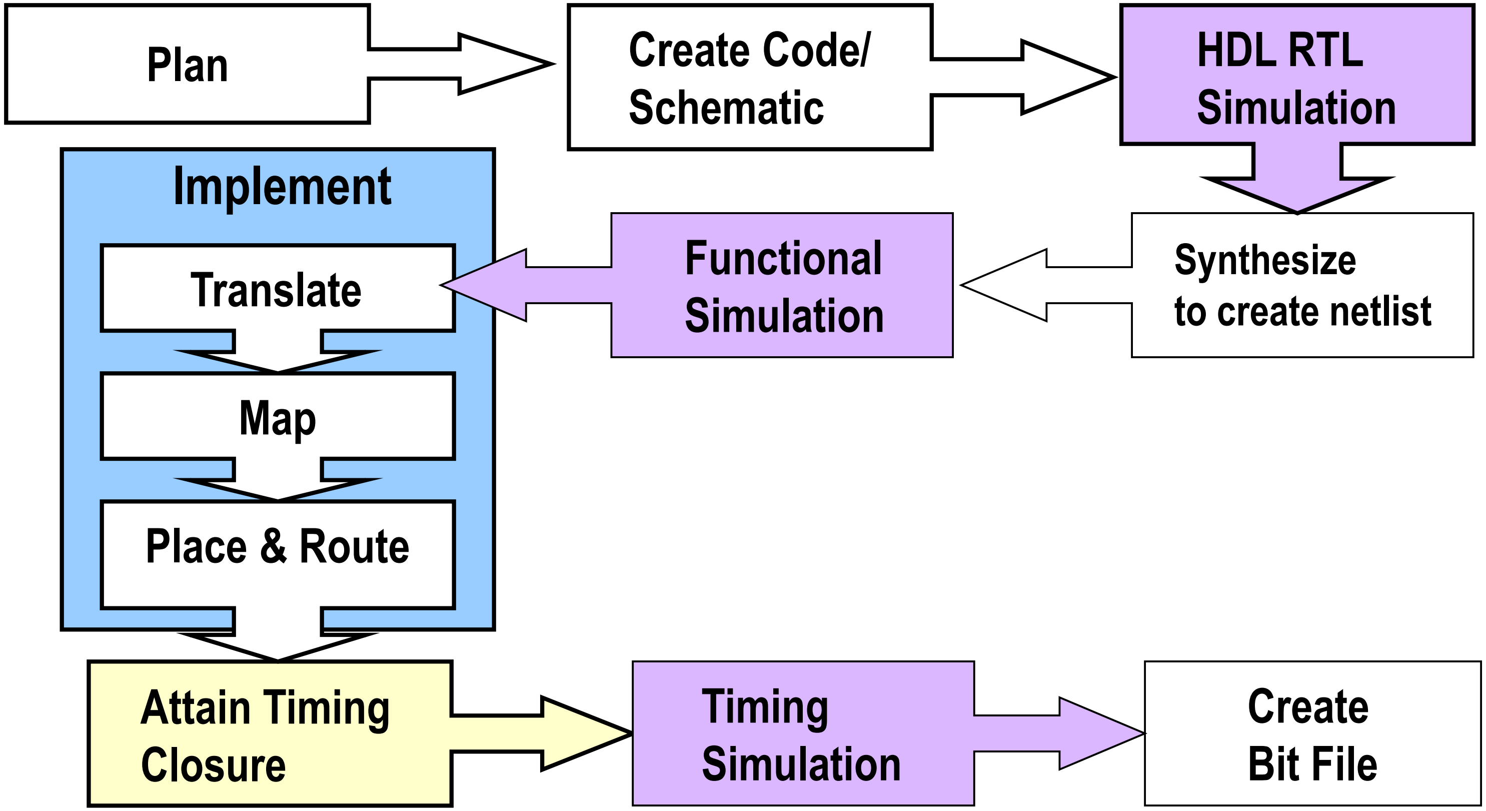
Implementation Process

Ehsan Yazdian

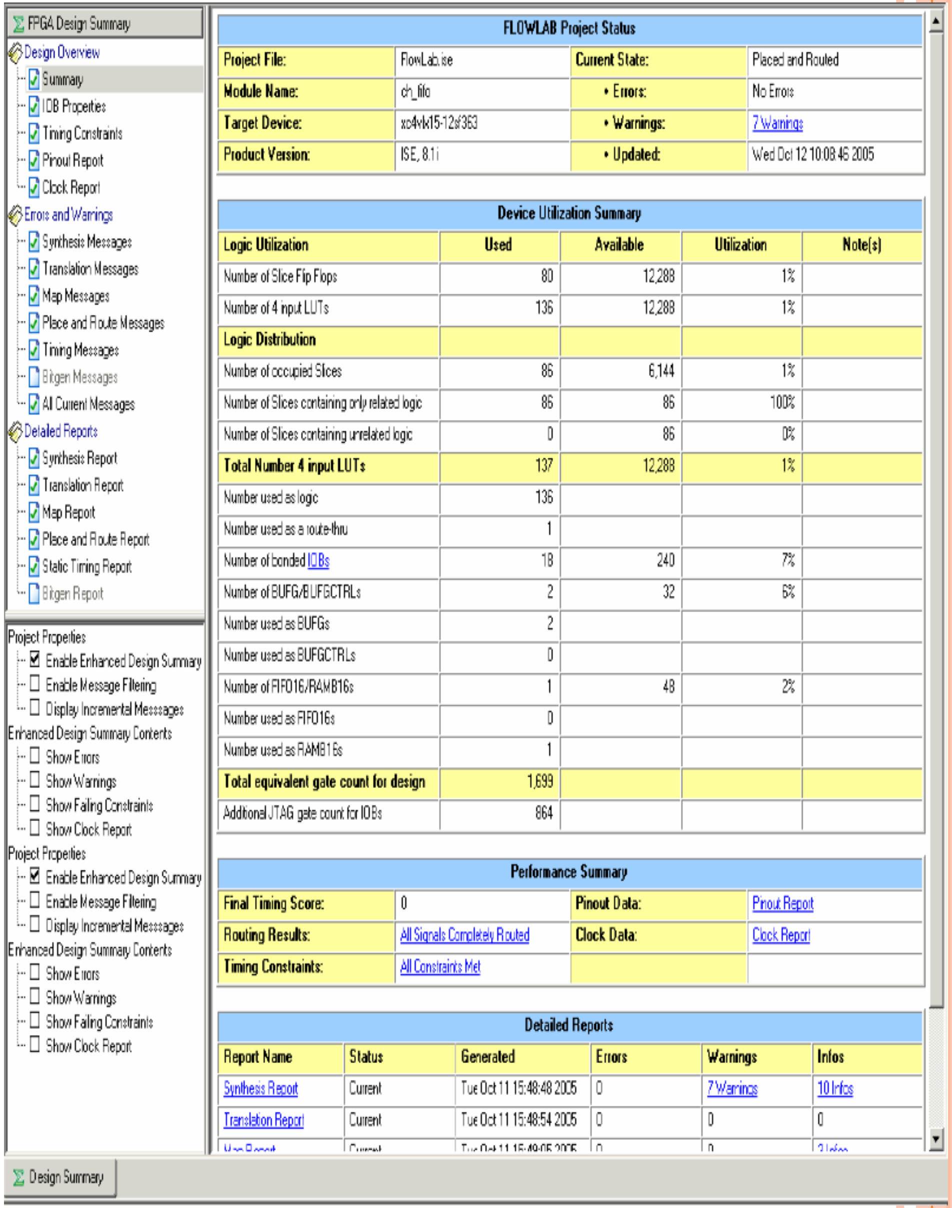
Design Flow

- Xilinx Design Flow



The Design Summary Displays Design Data

- Quick View of Reports
- Constraints
- Project Status
- Device Utilization
- Design Summary Options
- Performance
- Constraints Reports



FPGA Design Summary

- Design Overview
  - Summary
  - IOB Properties
  - Timing Constraints
  - Pinout Report
  - Clock Report
- Errors and Warnings
  - Synthesis Messages
  - Translation Messages
  - Map Messages
  - Place and Route Messages
  - Timing Messages
  - Bitgen Messages
  - All Current Messages
- Detailed Reports
  - Synthesis Report
  - Translation Report
  - Map Report
  - Place and Route Report
  - Static Timing Report
  - Bitgen Report

Project Properties
- ☑ Enable Enhanced Design Summary
- □ Enable Message Filtering
- □ Display Incremental Messsages

Enhanced Design Summary Contents
- □ Show Errors
- □ Show Warnings
- □ Show Failing Constraints
- □ Show Clock Report

Project Properties
- ☑ Enable Enhanced Design Summary
- □ Enable Message Filtering
- □ Display Incremental Messsages

Enhanced Design Summary Contents
- □ Show Errors
- □ Show Warnings
- □ Show Failing Constraints
- □ Show Clock Report

FLOWLAB Project Status			
Project File:	FlowLab.ise	**Current State:**	Placed and Routed
Module Name:	ch_fifo	**• Errors:**	No Errors
Target Device:	xc4vlx15-12sf363	**• Warnings:**	7 Warnings
Product Version:	ISE, 8.1i	**• Updated:**	Wed Oct 12 10:08:46 2005

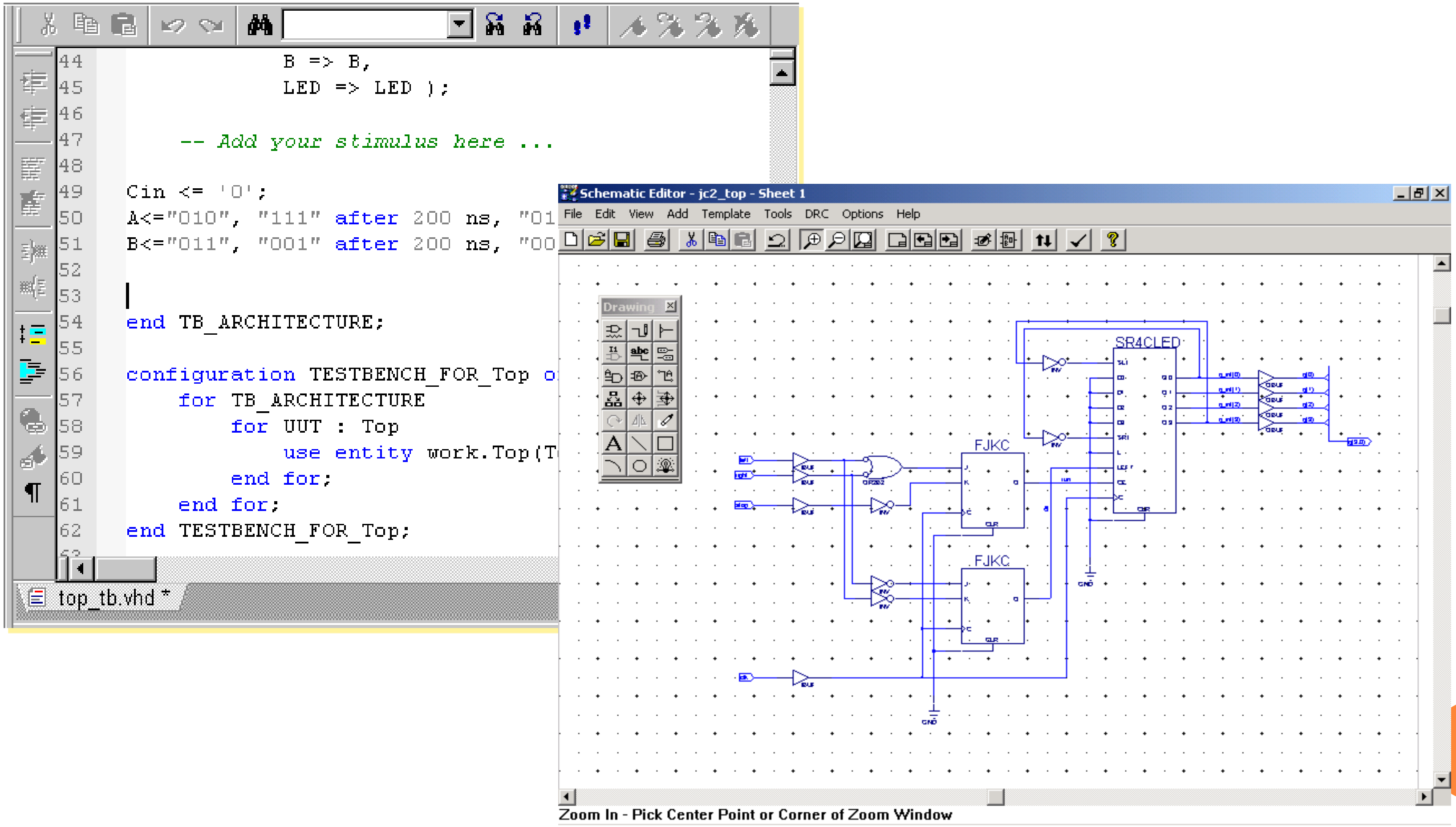
Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	80	12,288	1%	
Number of 4 input LUTs	136	12,288	1%	
Logic Distribution				
Number of occupied Slices	86	6,144	1%	
Number of Slices containing only related logic	86	86	100%	
Number of Slices containing unrelated logic	0	86	0%	
Total Number 4 input LUTs	137	12,288	1%	
Number used as logic	136			
Number used as a route-thru	1			
Number of bonded IOBs	18	240	7%	
Number of BUFG/BUFGCTRLs	2	32	6%	
Number used as BUFGs	2			
Number used as BUFGCTRLs	0			
Number of FIFO16/RAMB16s	1	48	2%	
Number used as FIFO16s	0			
Number used as RAMB16s	1			
Total equivalent gate count for design	1,699			
Additional JTAG gate count for IOBs	864			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Tue Oct 11 15:48:48 2005	0	7 Warnings	10 Infos
Translation Report	Current	Tue Oct 11 15:48:54 2005	0	0	0
Map Report	Current	Tue Oct 11 15:49:05 2005	0	0	2 Infos

Design Summary

Design Entry: HDL Coding, Schematic or State Machine



```
      B => B,
      LED => LED );

  -- Add your stimulus here ...

Cin <= '0';
A<="010", "111" after 200 ns, "01
B<="011", "001" after 200 ns, "00


end TB_ARCHITECTURE;

configuration TESTBENCH_FOR_Top o
  for TB_ARCHITECTURE
    for UUT : Top
      use entity work.Top(T
    end for;
  end for;
end TESTBENCH_FOR_Top;
```

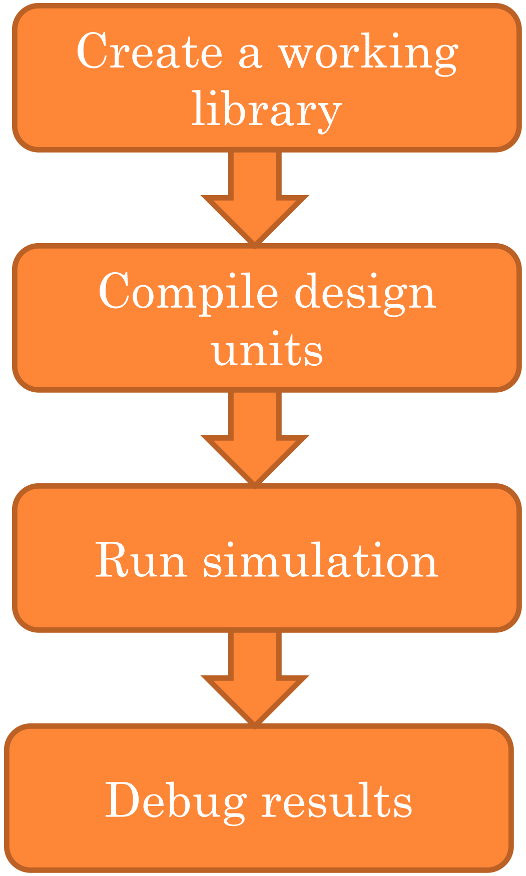
Zoom In - Pick Center Point or Corner of Zoom Window

SIMULATION BY TESTBENES

- After HDL coding, the code has to be tested using "tesbench".
- Simulation tools:
  - Active-HDL
  - Modelsim (Mentor Graphics)
  - Synopsys VCS (Synopsys)
  - ISIM (Xilinx)
  - NCVerilog (Cadence)tbenches" (Verification).

Working With ModelSim

- Basic Simulation Flow

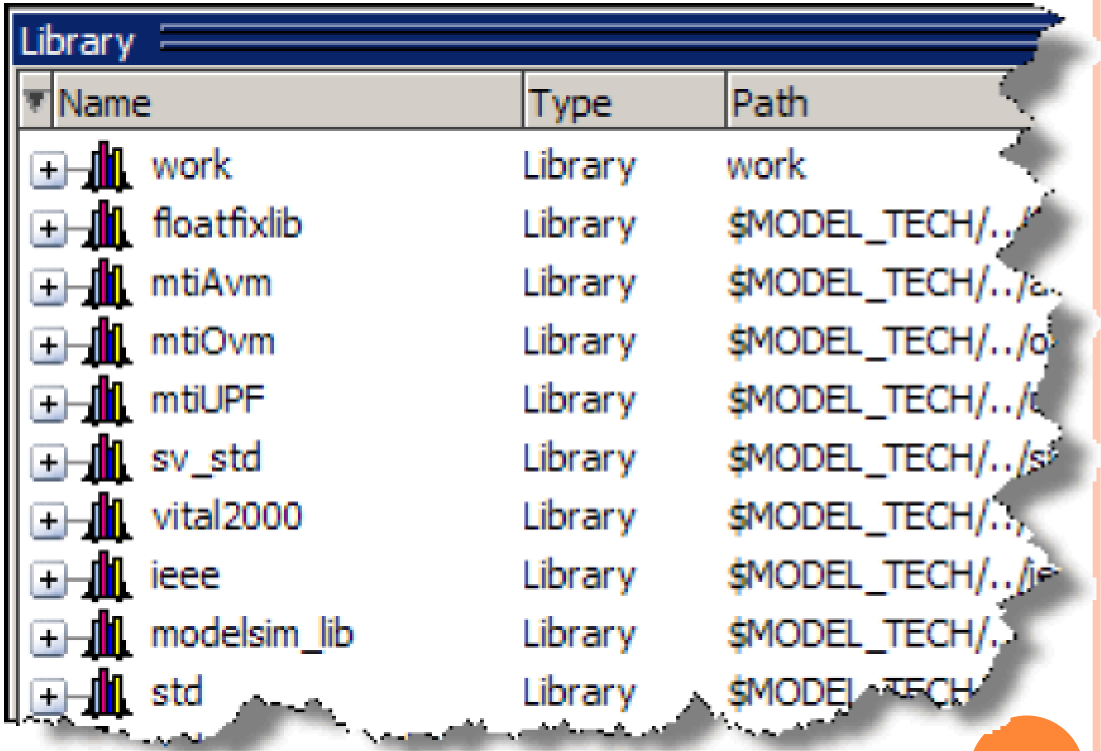


Create a working library

Compile design units

Run simulation

Debug results



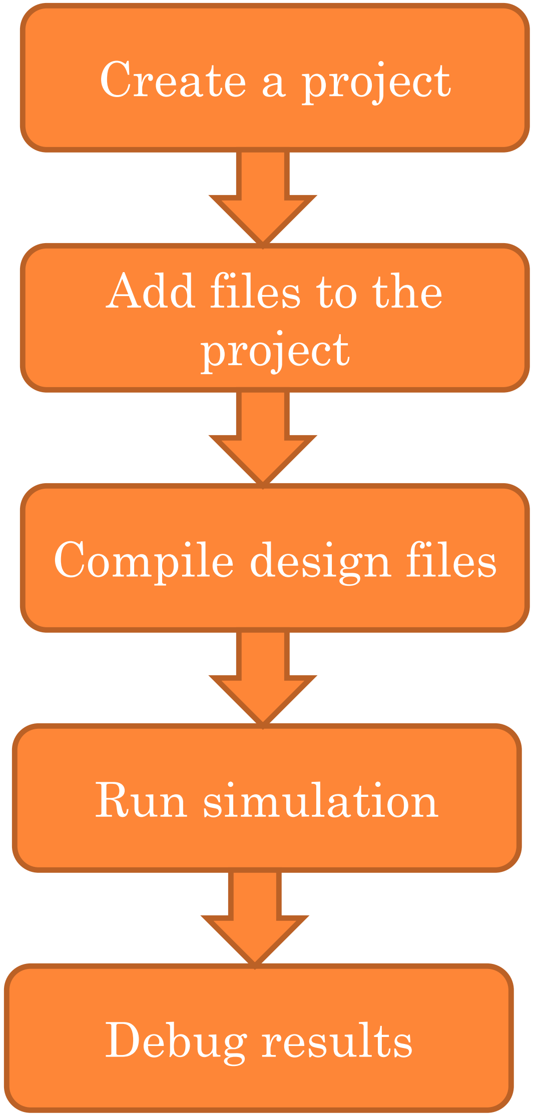
Library

Name	Type	Path
work	Library	work
floatfixlib	Library	$MODEL_TECH/../
mtiAvm	Library	$MODEL_TECH/../a..
mtiOvm	Library	$MODEL_TECH/../o
mtiUPF	Library	$MODEL_TECH/../
sv_std	Library	$MODEL_TECH/../s
vital2000	Library	$MODEL_TECH/../
ieee	Library	$MODEL_TECH/../ie
modelsim_lib	Library	$MODEL_TECH/..
std	Library	$MODEL_TECH

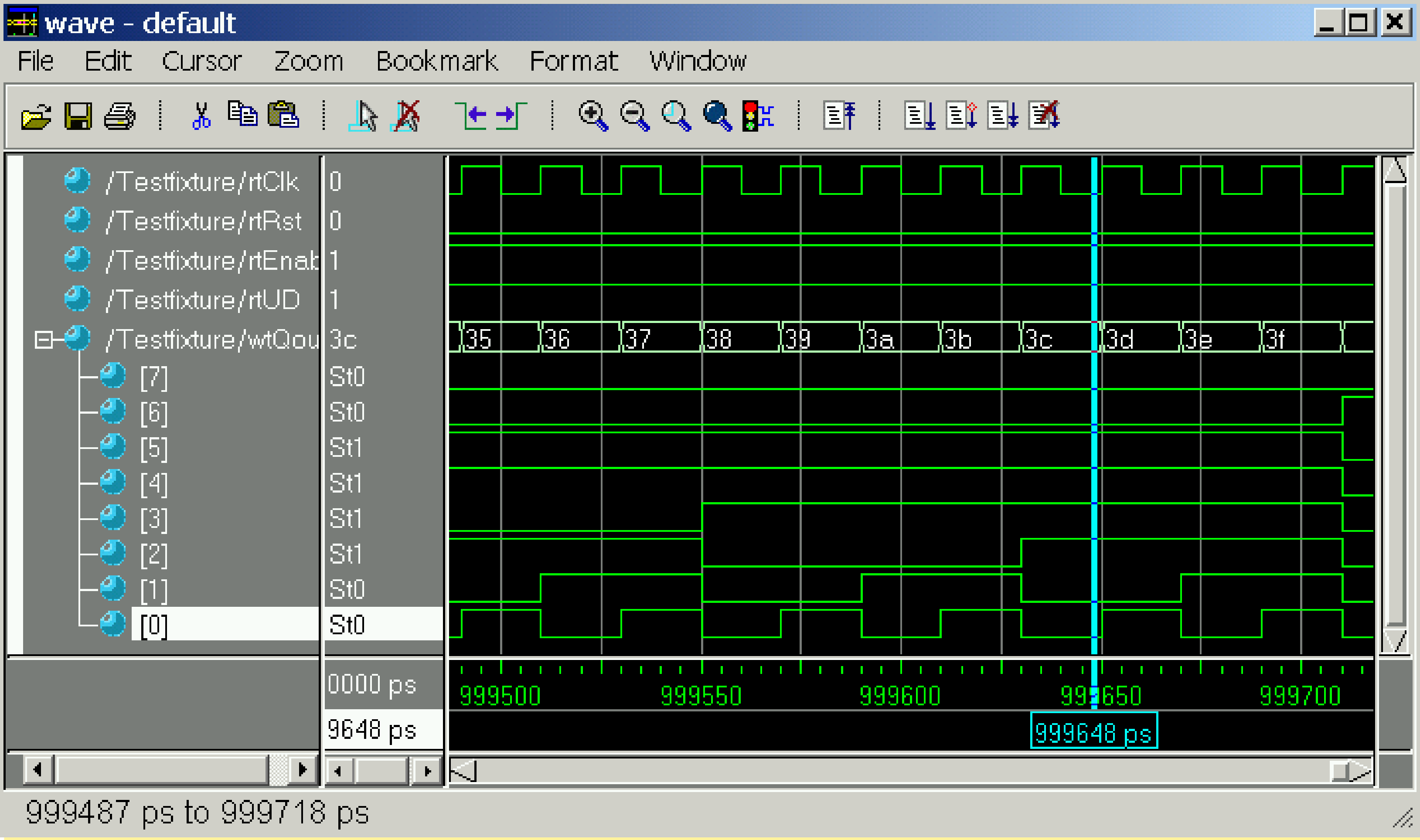
ModelSim

- Project Flow
- Similar to the basic simulation flow.

- Differences:
  - Working library is created automatically.
  - Projects are persistent and will open every time you invoke ModelSim.



ModelSim



/Testfixture/rtClk	0
/Testfixture/rtRst	0
/Testfixture/rtEnab	1
/Testfixture/rtUD	1
/Testfixture/wtQou	3c
[7]	St0
[6]	St0
[5]	St1
[4]	St1
[3]	St1
[2]	St1
[1]	St0
[0]	St0

0000 ps

9648 ps

999487 ps to 999718 ps

Simulating The Design

- When you instantiate a device-specific component in your design, the simulator must reference a library that describes the functionality of the component to ensure proper simulation.
- Xilinx simulation libraries:
  - UNISIM library for functional simulation of Xilinx primitives
  - UniMacro library for functional simulation of Xilinx macros
  - XilinxCoreLib library for functional simulation of Xilinx cores
  - Xilinx EDK library for behavioral simulation of Xilinx Embedded Development Kit (EDK) IP components
  - SIMPRIM library for timing simulation of Xilinx primitives

Modelsim do file

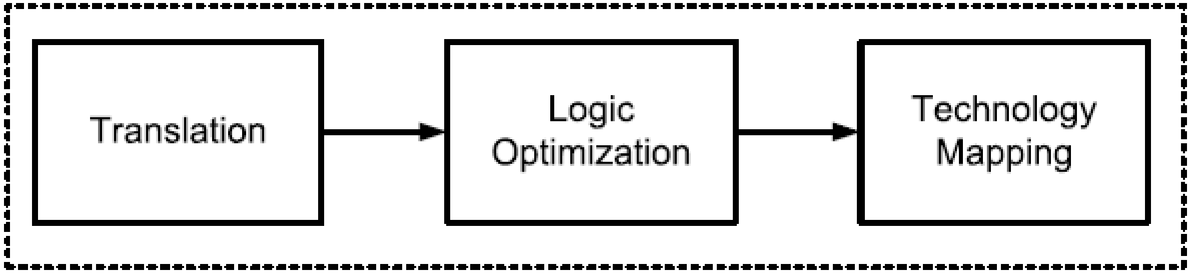
- Generating a do file for project.
  - Using the automatic do file generated by Xilinx ISE.
- Example

```
vlib work

vlog  "adder.v"
vlog  "top.v"
vlog  "testbench.v"
vlog  "C:/Xilinx/13.4/ISE_DS/ISE//verilog/src/glbl.v‶
vsim -voptargs="+acc" -t 1ps -lib work work.testbench glbl
do {wave.do}
view wave
view structure
view signals
do {testbench.udo}

run 1000ns
```

Synthesis

Synthesis Definition

- **Synthesis =** Translation + Logic optimization + Technology Mapping
  - **Translation: going from RTL to B**oolean function
  - **Logic Optimization : Optimizing** and minimizing Boolean function
  - **Technology Mapping (TM): Map** the Boolean function to the target library



Synthesis

SYNTHESIS

- **Input:**
  - HDL Code
  - “Technology library” file Standard cells
    - Basic gates (AND, OR, NOR, …)
    - Macro cells (Adders, Muxes, Memory, Flip-flops, …)
  - Constraint file (Timing, area, power, loading requirement, optimization Alg.)

- **Output:**
  - A gate-level “Netlist” of the des
  - Timing files (.sdf)

- This process is done using various optimization algorithms

An Example

```
always @ (a, b)
    case ({a,b})
         2'b00: out = 1;
         2'b01: out = 1;
         2'b11: out = 1;
         default: out = 0;
endcase
```

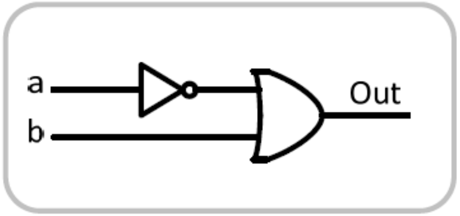
Translation

$$out = \bar{a}b + ab + \bar{a}\bar{b}$$

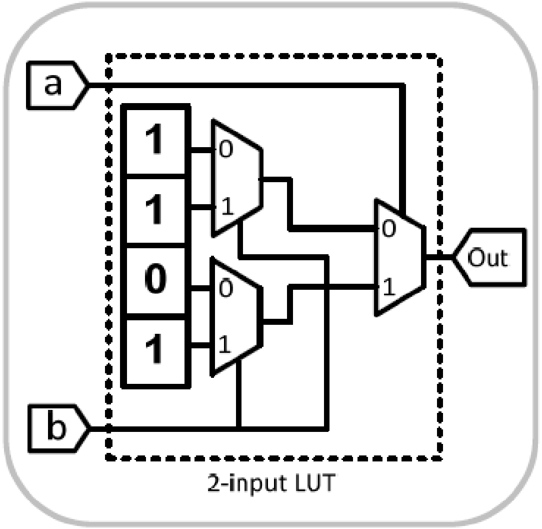
Optimization

$$out = \bar{a} + b$$

Technology Mapping



ASIC

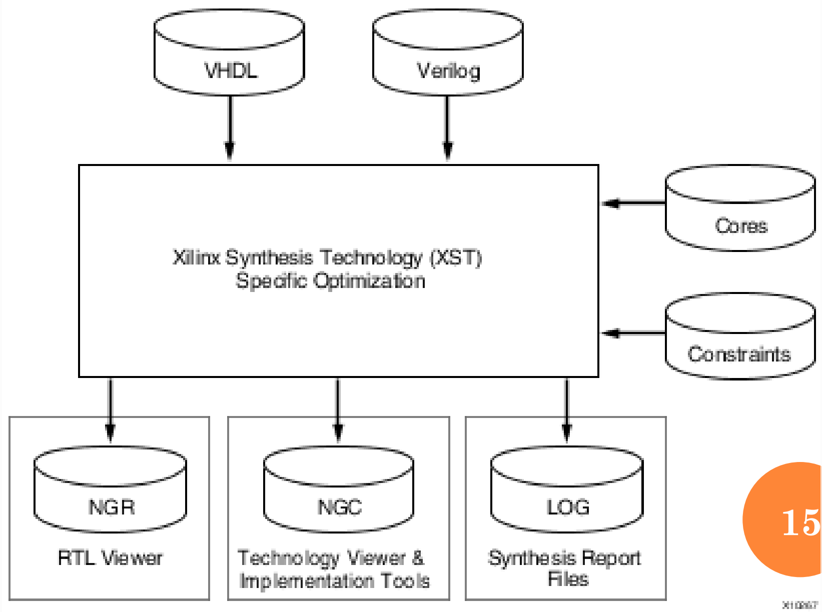


FPGA

SYNTHESIS OPERATION

- Generating an EDIF or NGC netlist to bring into the Xilinx implementation tools
  - The NGC file is a netlist that contains both logical design data and constraints that takes the place of both EDIF and NCF files.
- Popular synthesis tools

Vendor	Product	Platform
Xilinx	ISE-XST	FPGA
Mentor Graphics	Precision/ LeonardoSpectrum	FPGA/ASIC
Synplicity	Synplify Pro	ASIC
Cadence	Encounter RTL Compiler	ASIC
Altera	Quarrtus II	FPGA



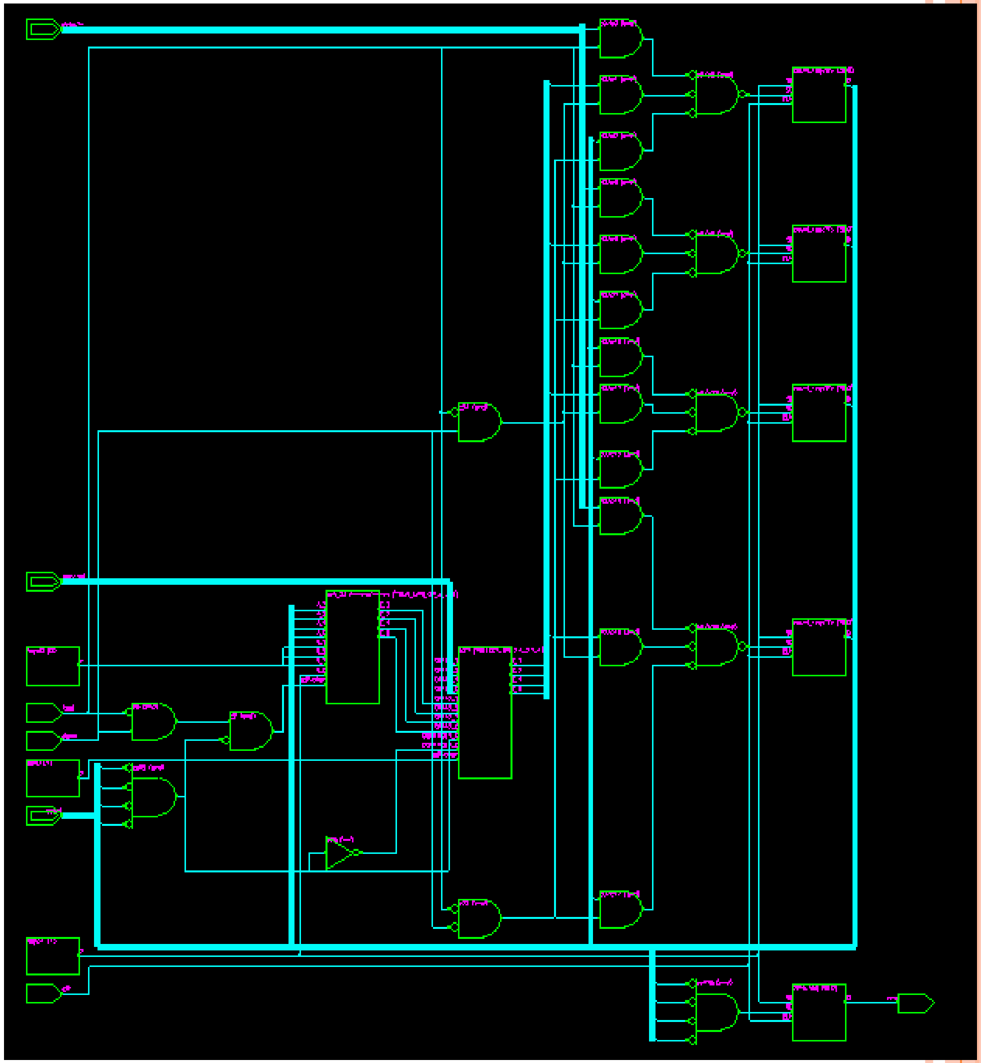
FEATURES OF SYNTHESIS TOOLS

- Interpret RTL code (Register-transfer level: Describing the code as registers and the combinational logics between them)
- Produce synthesized circuit netlist in standard EDIF (Electronic Design Interchange Format).
- Give preliminary performance estimates.
- Some can display circuit schematics corresponding to EDIF netlist.

SYNTHESIS

- HDL Code to Netlist conversion

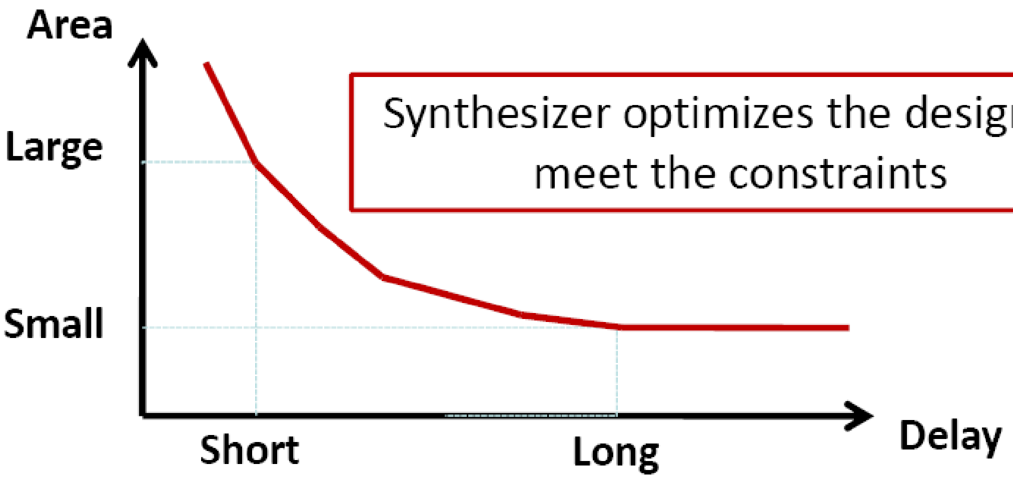
Synthesis



```
Example
module
   Counter(Clk,Rst,Enable,UD,Qout);
//--------( I/O )----------
input     Clk,Rst,Enable,UD;
Output reg [7:0]   Qout;

always @( posedge Clk ) begin
  if( Enable ) begin
    if( Rst )      Qout = 8'h00;
    else if( UD )  Qout = Qout + 1;
    else if( !UD ) Qout = Qout - 1;
 end
end

endmodule
```

SYNTHESIS IS CONSTRAINT-DRIVEN

- Synthesis Constraints:
  - Speed: Maximum expected clock frequency
  - Area: Minimum Area on Chip
  - Power Consumption

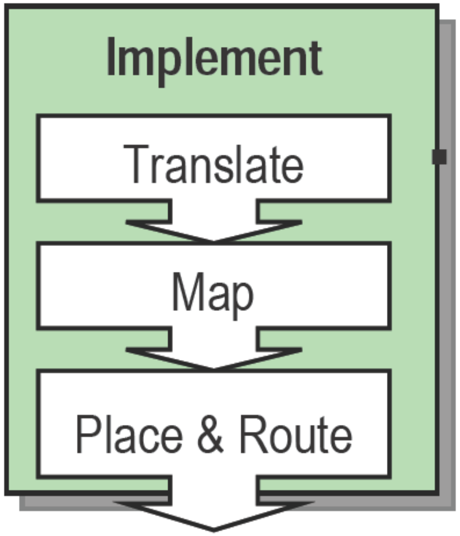


Synthesizer optimizes the design to meet the constraints

Implementation

IMPLEMENTATION

- After synthesis the entire implementation process is performed by FPGA vendor tools.



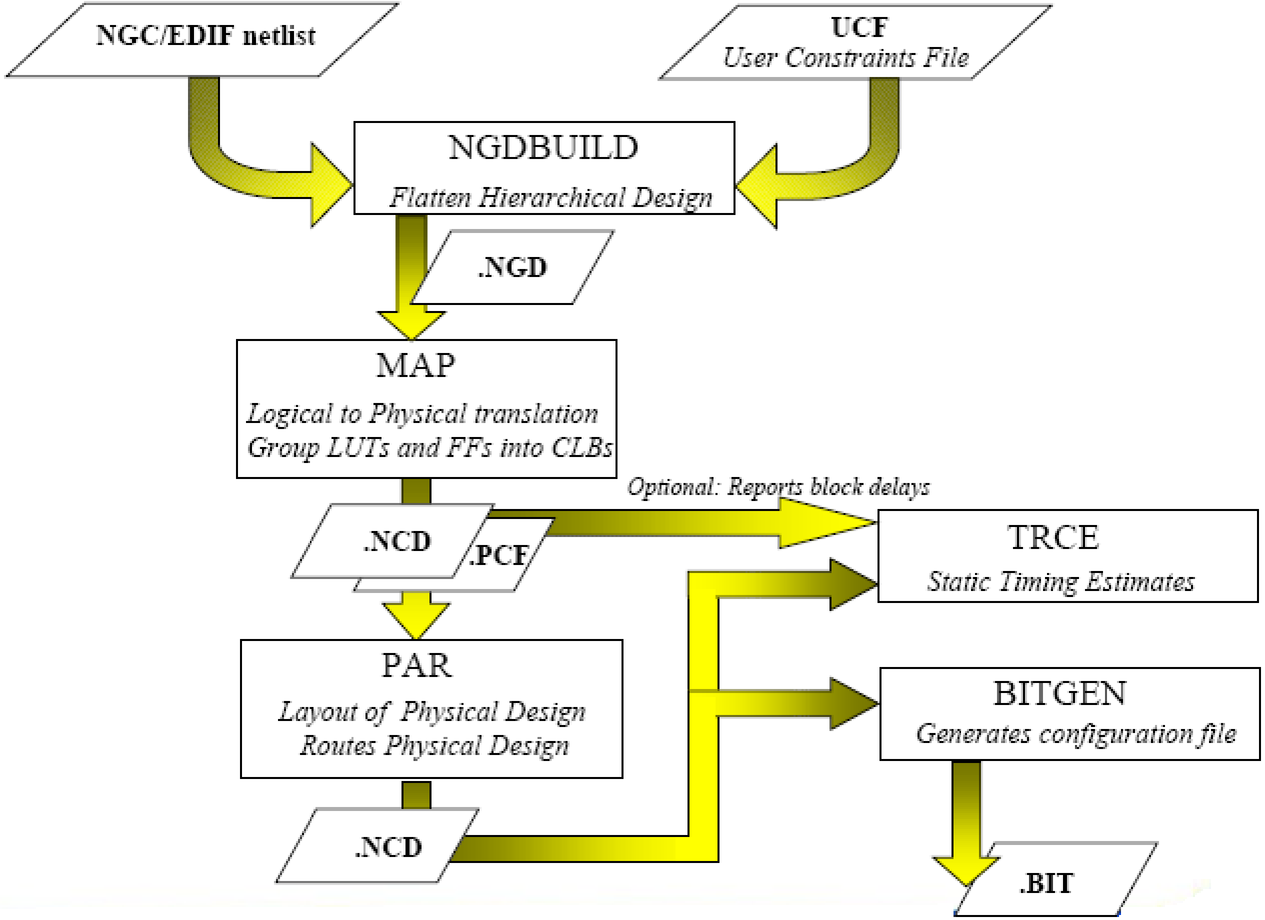
- Implementation includes many phases
  - **Translate**
  - **Map**
  - **Place & Route**

IMPLEMENTATION

- **Translate:**
  - Merge multiple design files into a single netlist.
- **Map:**
  - Group logical symbols from the netlist (gates) into physical components (slices and IOBs).
- **Place & Route:**
  - Place components onto the chip, connect the components, and extract timing data into reports.

- Each phase generates files that allow you to use other Xilinx tools.
  - Floorplanner, FPGA Editor, XPower

ISE Implementation Flow


NGC/EDIF netlist
UCF
User Constraints File
NGDBUILD
Flatten Hierarchical Design
.NGD
MAP
Logical to Physical translation
Group LUTs and FFs into CLBs
Optional: Reports block delays
.NCD
.PCF
TRCE
Static Timing Estimates
PAR
Layout of Physical Design
Routes Physical Design
BITGEN
Generates configuration file
.NCD
.BIT

Translate: Ngdbuild

- Putting all thing together, so that we need all parts of project
- Inputs:
  - Project synthesized EDIF file
  - UCF constraints file
  - Core's .edn file

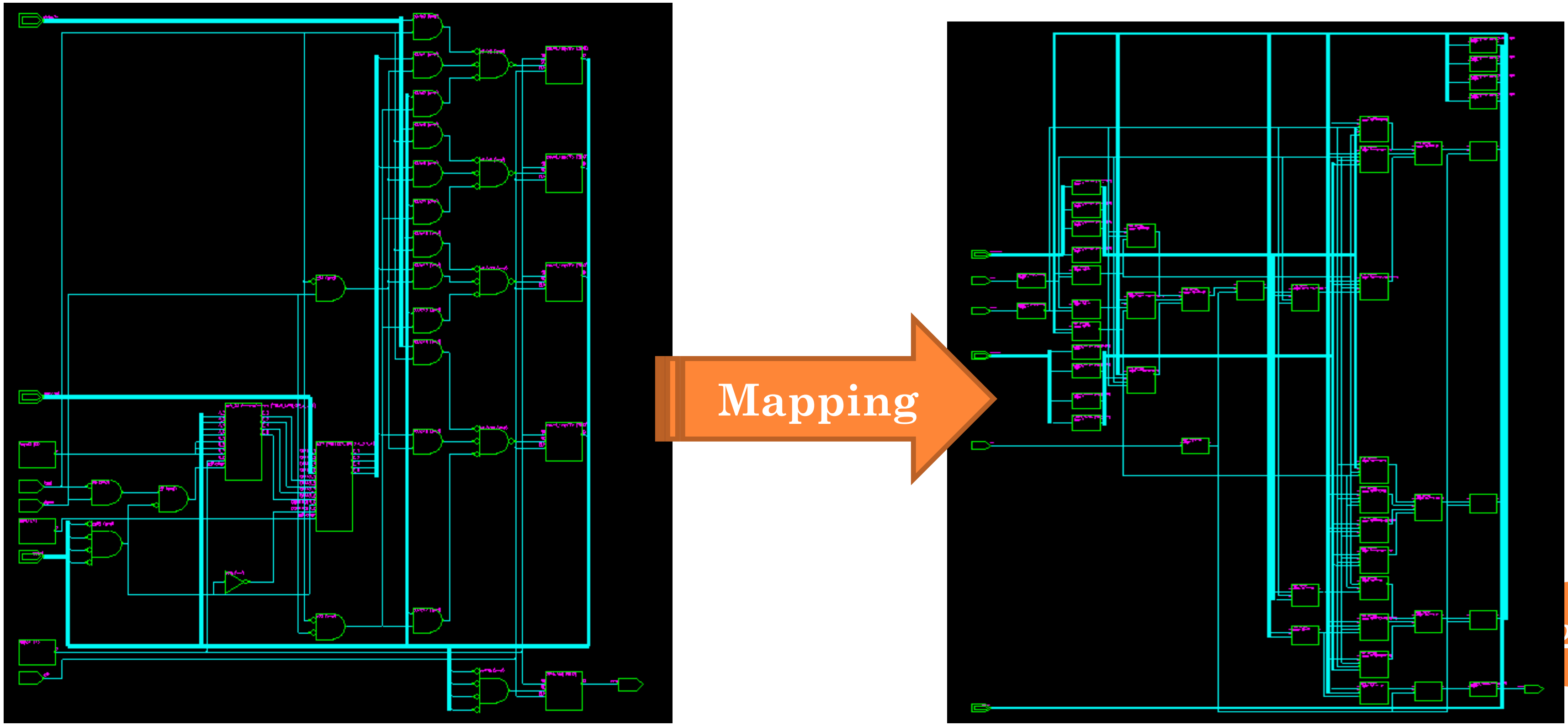
- Output: **N**ative **G**eneric **D**atabase (NGD)

MAP

- Map the generic form to device.
- Make necessary optimization, eliminate unnecessary logic.
- Estimate resource usage, just % (110%!)
- Input: NGD file
- Output: NCD, PCF, MRP (report)
    - NCD: Native Circuit Description.
    - A physical description of the design in terms of the components in the target Xilinx device.
    - PCF : Physical Constraints File

Map

- Digital Circuit Element to Technology Element Mapping



MAP REPORT

Command Line : map -ise test_implementation.ise -intstyle ise –p xc3sd1800a-fg676-5 -cm area -ir off -pr off -c 100 -o top_map.ncd top.ngd top.pcf

Target Device : xc3sd1800a

Target Package : fg676

Target Speed : -5

Mapper Version : spartan3adsp -- $Revision: 1.51 $

Mapped Date : Sat Mar 09 01:16:17 2013

Design Summary

Number of 4 input LUTs: 3 out of 33,280 1%

Number of occupied Slices: 2 out of 16,640 1%

Number of Slices containing only related logic: 2 out of 2 100%

Number of Slices containing unrelated logic: 0 out of 2 0%

Number of bonded IOBs: 8 out of 519 1%

Number of BUFGMUXs: 1 out of 24 4%

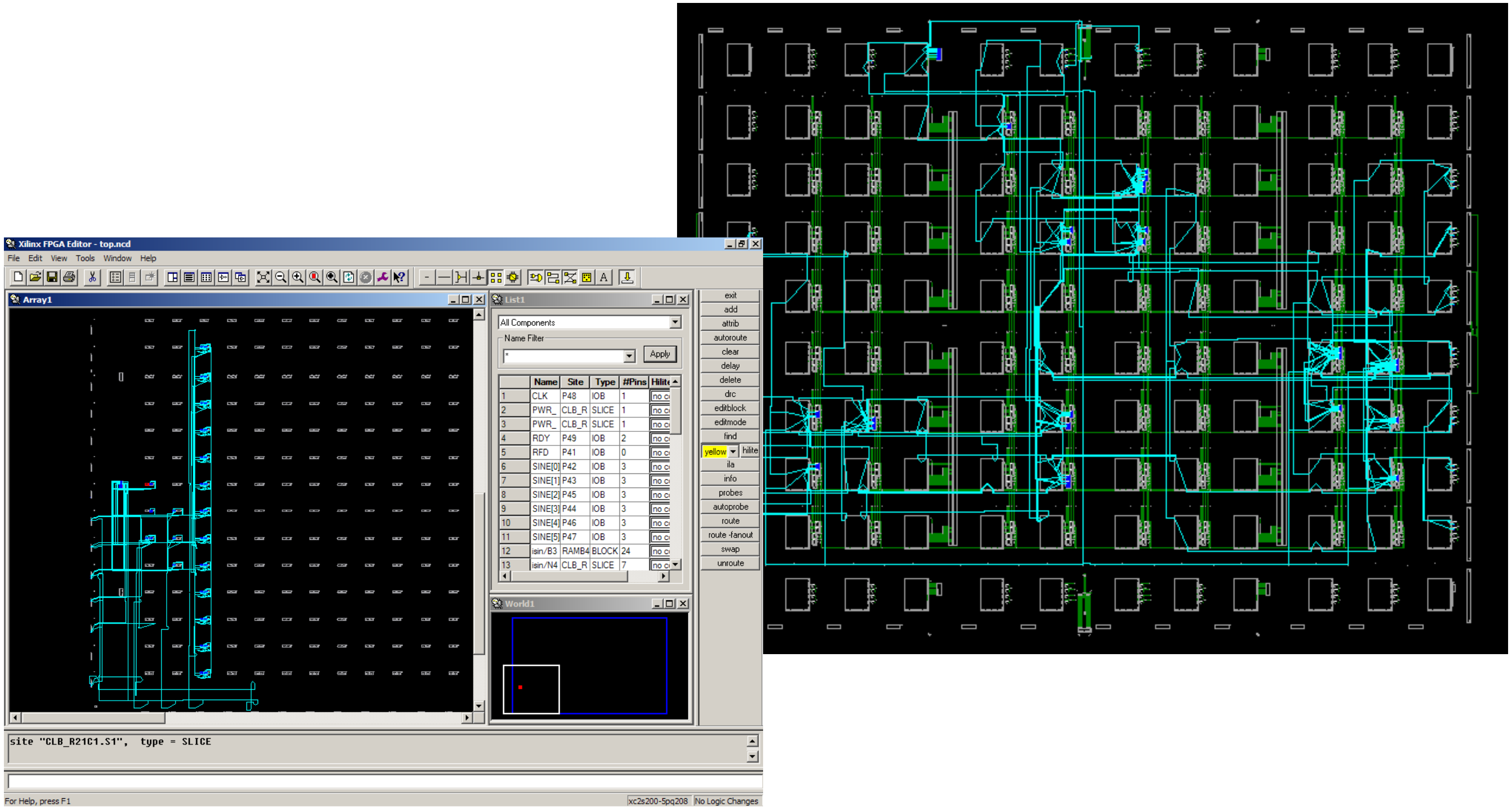
Average Fanout of Non-Clock Nets: 1.67

PAR (Place & Route)

- Place and Route all the logics
- Some of placing process done in previous steps
- Overused area give error in this section
- Input: Unrouted .ncd
- Output: Routed .ncd

PLACE & ROUTE

- Sitting place for each element of circuit



	Name	Site	Type	#Pins	Hilite
1	CLK	P48	IOB	1	no c
2	PWR_	CLB_R	SLICE	1	no c
3	PWR_	CLB_R	SLICE	1	no c
4	RDY	P49	IOB	2	no c
5	RFD	P41	IOB	0	no c
6	SINE[0]	P42	IOB	3	no c
7	SINE[1]	P43	IOB	3	no c
8	SINE[2]	P45	IOB	3	no c
9	SINE[3]	P44	IOB	3	no c
10	SINE[4]	P46	IOB	3	no c
11	SINE[5]	P47	IOB	3	no c
12	isin/B3	RAMB4	BLOCK	24	no c
13	isin/N4	CLB_R	SLICE	7	no c

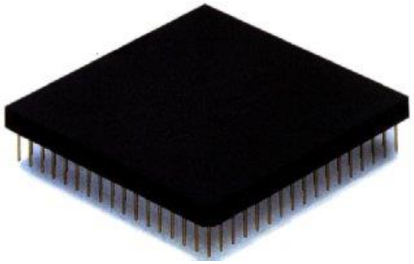
```
site "CLB_R21C1.S1",  type = SLICE
```

Place & route report

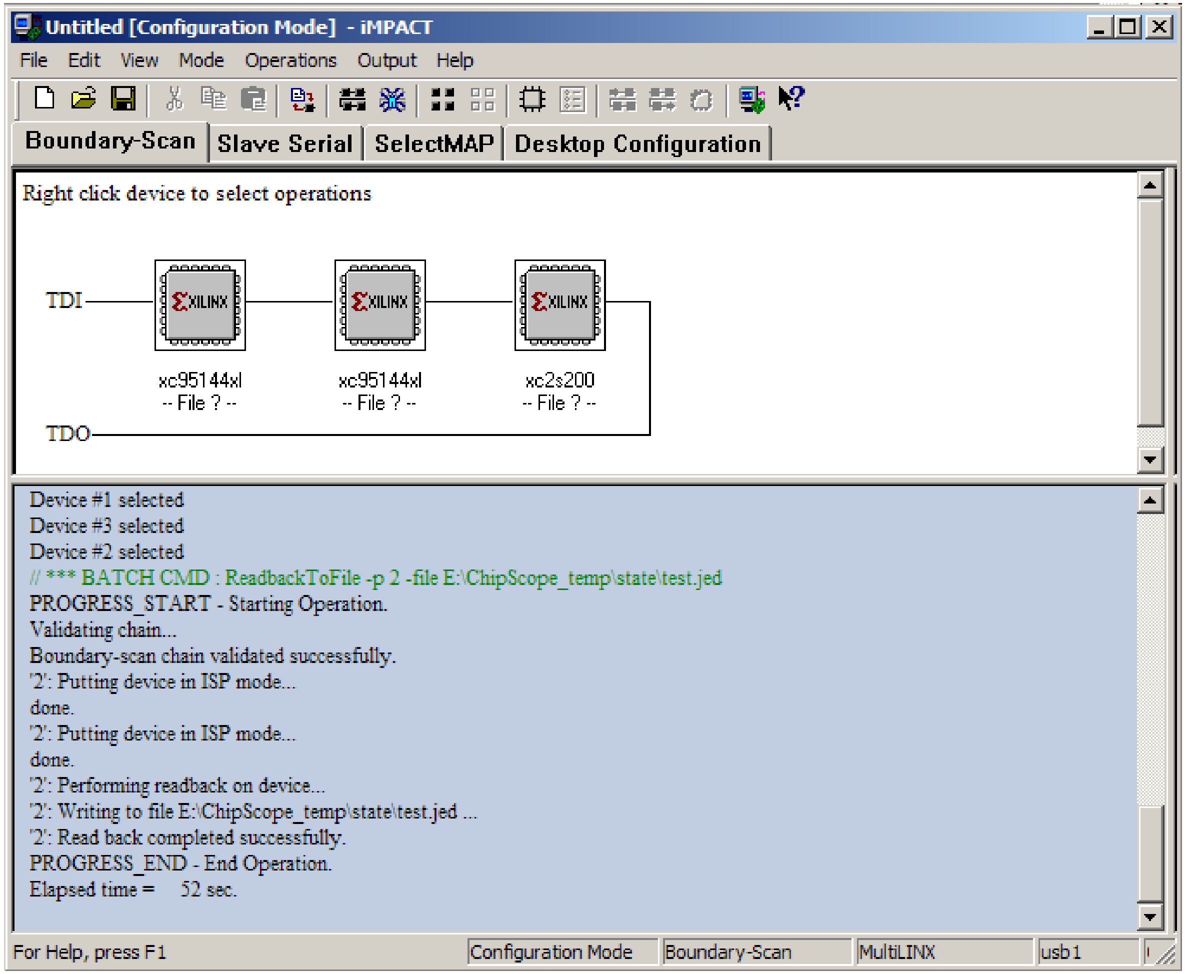
- Place & route report
- Static Timing Report

Configuration

- Once a design is implemented, you must create a file that the FPGA can understand
- This file is called a bitstream: a BIT file (.bit extension)
- The BIT file can be downloaded directly into the FPGA, or the BIT file can be converted into a PROM file, which stores the programming information

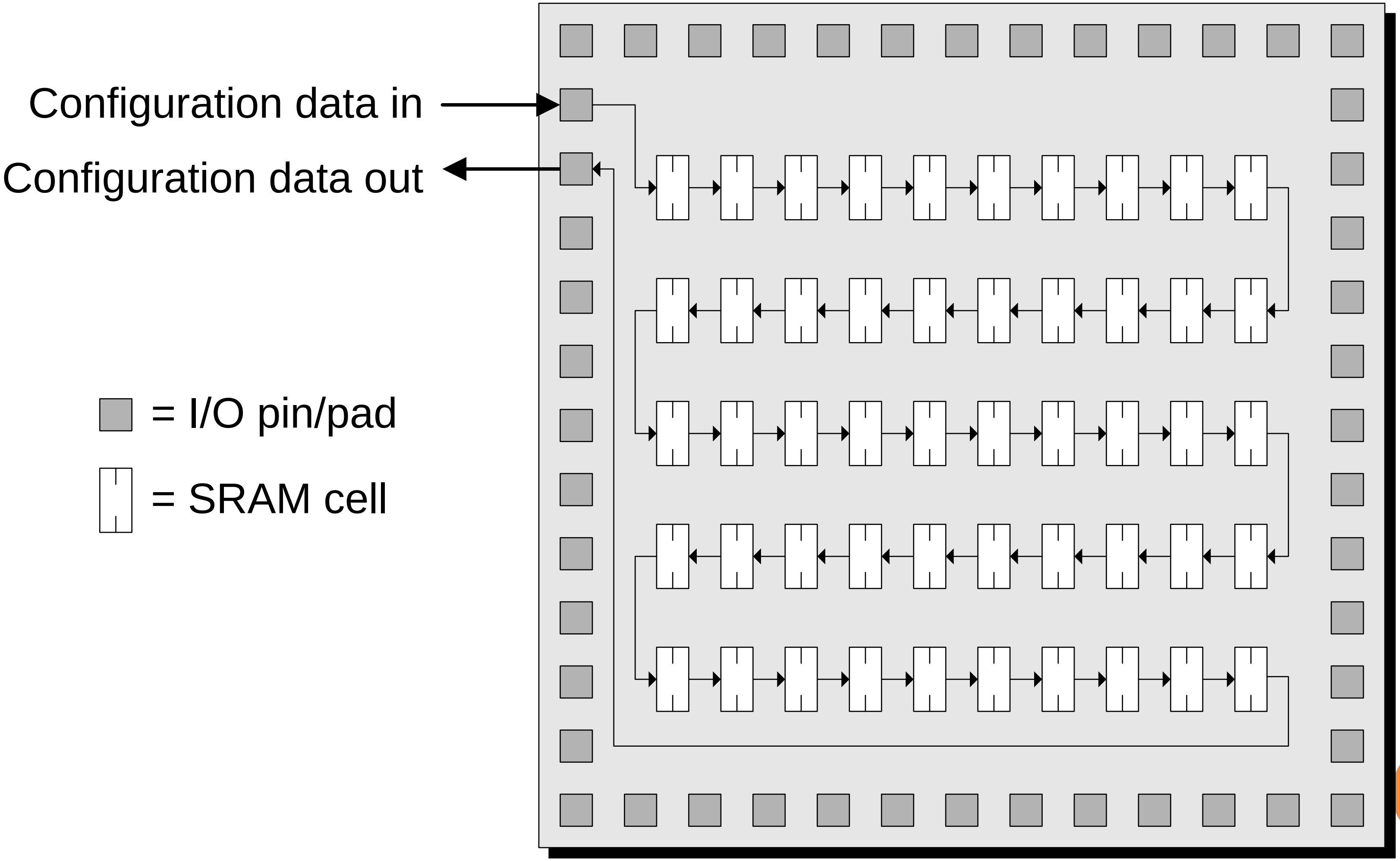


Impact Software



```
Device #1 selected
Device #3 selected
Device #2 selected
// *** BATCH CMD : ReadbackToFile -p 2 -file E:\ChipScope_temp\state\test.jed
PROGRESS_START - Starting Operation.
Validating chain...
Boundary-scan chain validated successfully.
'2': Putting device in ISP mode...
done.
'2': Putting device in ISP mode...
done.
'2': Performing readback on device...
'2': Writing to file E:\ChipScope_temp\state\test.jed ...
'2': Read back completed successfully.
PROGRESS_END - End Operation.
Elapsed time =     52 sec.
```

Configuration of SRAM based FPGAs



Configuration data in

Configuration data out

■ = I/O pin/pad

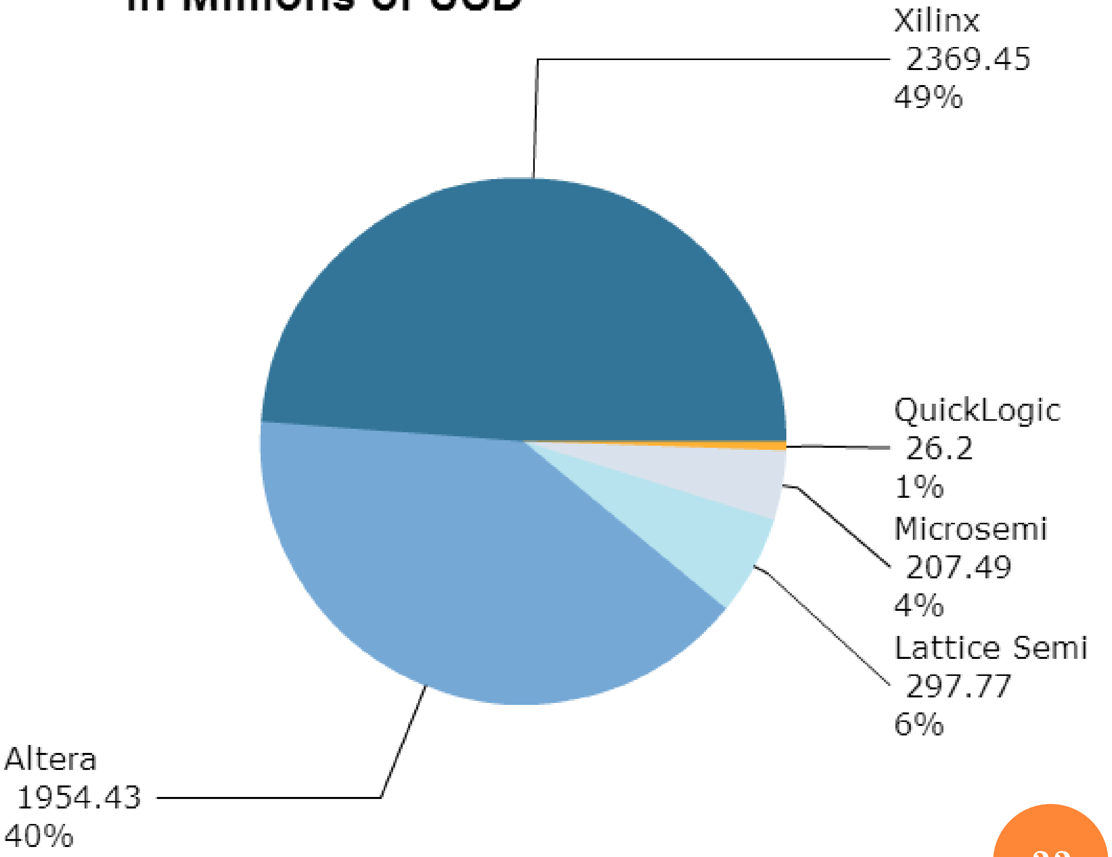
▯ = SRAM cell

Major FPGA Vendors

FPGA Vendors

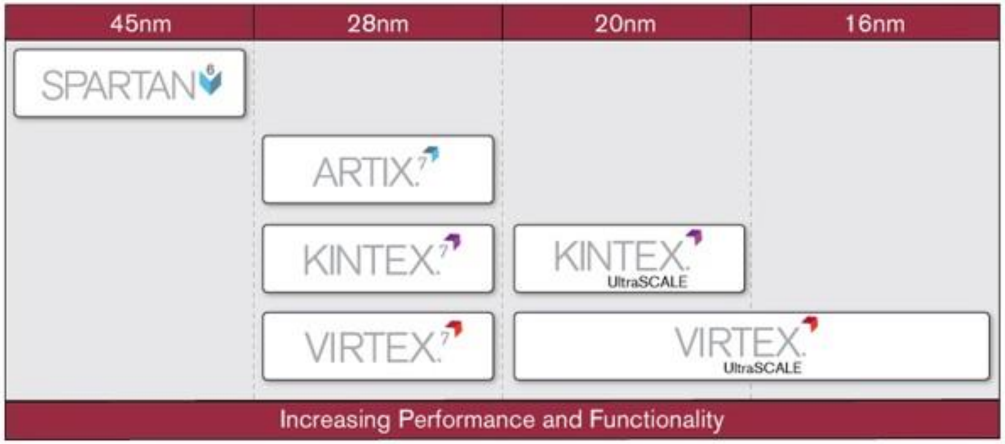
- **Xilinx, Inc.**
- **Altera Corp.**
- Lattice Semiconductor
- Microsemi (Actel)
- Quick Logic Corp.
- Atmel
- Achronix
- Tabula

FPGA Market Share by 2010 revenue in Millions of USD



Xilinx FPGA Families

- **High-performance families**
  - **Virtex (220 nm)**
  - **Virtex-E, Virtex-EM (180 nm)**
  - **Virtex-II , Virtex-II PRO (130 nm)**
  - **Virtex-4 (90 nm)**
  - **Virtex-5 (65 nm)**
  - **Virtex-6 (40 nm)**
  - **Artix-7 (28 nm)**
  - **Kintex-7 (28 nm)**
  - **Virtex-7 (20nm)**



45nm | 28nm | 20nm | 16nm

SPARTAN 6

ARTIX 7

KINTEX 7

KINTEX UltraSCALE

VIRTEX 7

VIRTEX UltraSCALE

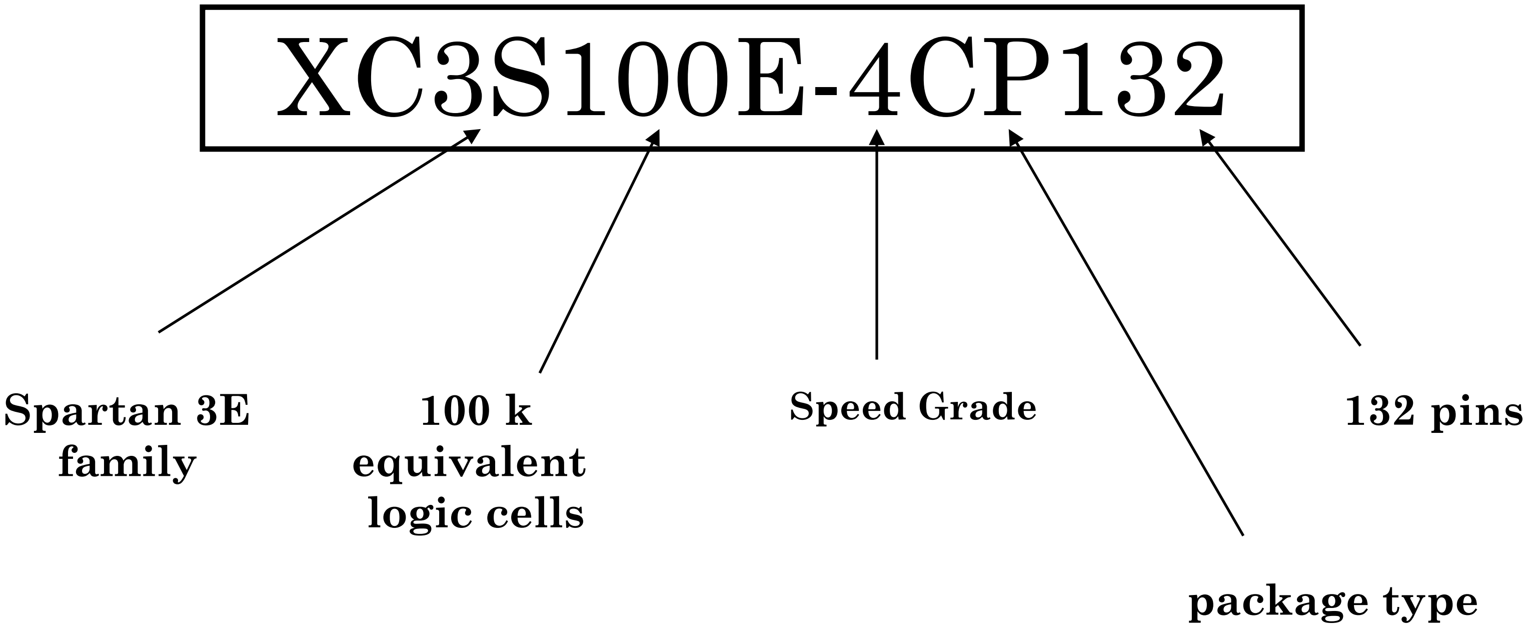
Increasing Performance and Functionality

- **Low Cost Family**
  - **Spartan/XL – derived from XC4000**
  - **Spartan-II**
  - **Spartan-IIE**
  - **Spartan-3 (90 nm)**
    - **Spartan-3E – logic optimized**
    - **Spartan-3A – I/O optimized**
    - **Spartan-3A DSP – DSP optimized**
  - **Spartan-6 (45 nm)**

XILINX FPGA FAMILIES

Features	Artix™-7	Kintex™-7	Virtex®-7	Spartan®-6	Virtex-6
Logic Cells	215,000	480,000	2,000,000	150,000	760,000
BlockRAM	13Mb	34Mb	68Mb	4.8Mb	38Mb
DSP Slices	740	1,920	3,600	180	2,016
DSP Performance (symmetric FIR)	930GMACS	2,845GMACS	5,335GMACS	140GMACS	2,419GMACS
Transceiver Count	16	32	96	8	72
Transceiver Speed	6.6Gb/s	12.5Gb/s	28.05Gb/s	3.2Gb/s	11.18Gb/s
Total Transceiver Bandwidth (full duplex)	211Gb/s	800Gb/s	2,784Gb/s	50Gb/s	536Gb/s
Configuration AES	Yes	Yes	Yes	Yes	Yes
I/O Pins	500	500	1,200	576	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V
EasyPath™ Cost Reduction Solution	-	Yes	Yes	-	Yes

FPGA Nomenclature



XC3S100E-4CP132

Spartan 3E family

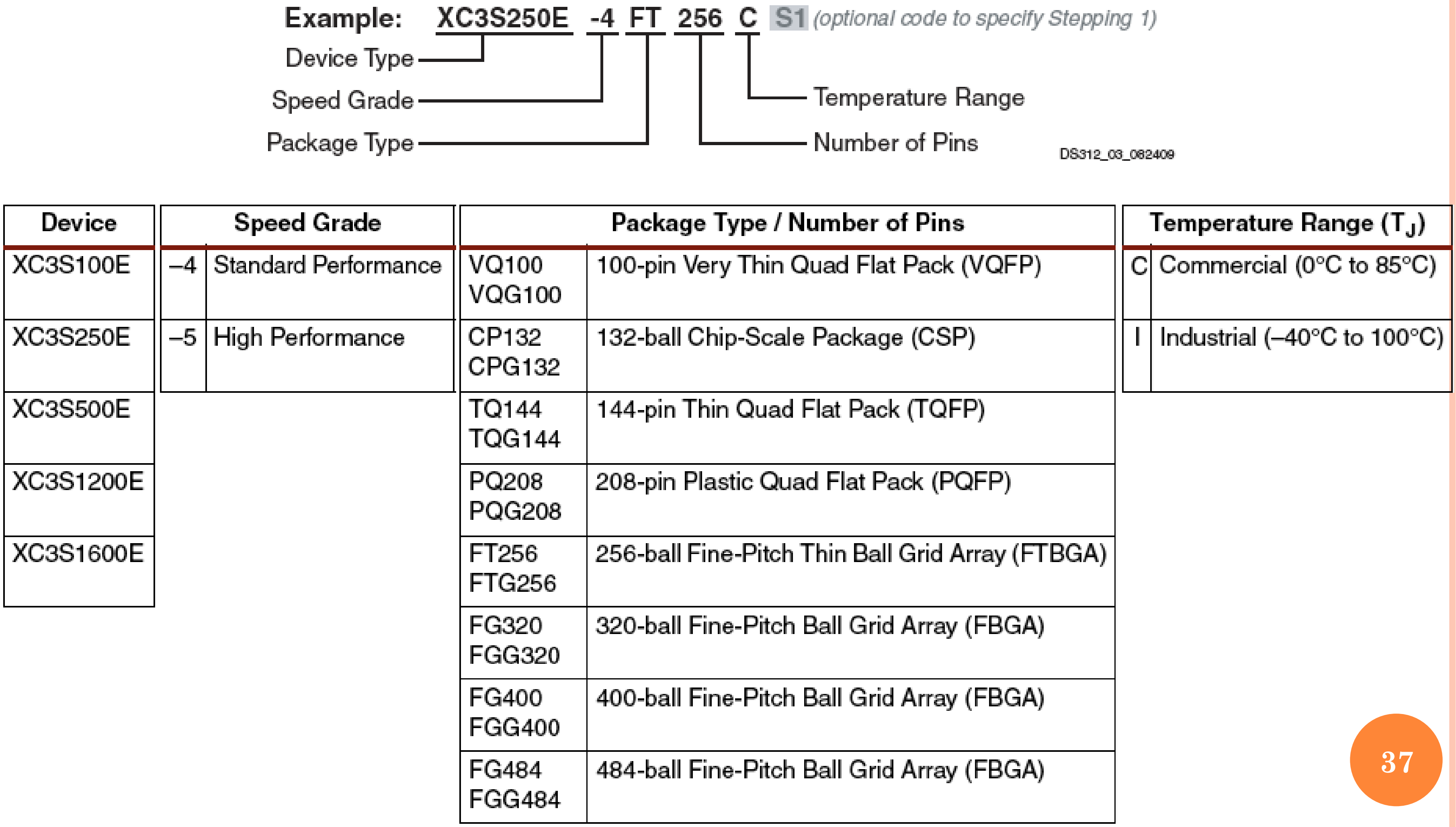
100 k equivalent logic cells

Speed Grade

132 pins

package type

FPGA Nomenclature



Example: XC3S250E -4 FT 256 C S1 *(optional code to specify Stepping 1)*

Device Type
Speed Grade
Package Type
Temperature Range
Number of Pins
DS312_03_082409

Device
XC3S100E
XC3S250E
XC3S500E
XC3S1200E
XC3S1600E

Speed Grade	
–4	Standard Performance
–5	High Performance

Package Type / Number of Pins	
VQ100 VQG100	100-pin Very Thin Quad Flat Pack (VQFP)
CP132 CPG132	132-ball Chip-Scale Package (CSP)
TQ144 TQG144	144-pin Thin Quad Flat Pack (TQFP)
PQ208 PQG208	208-pin Plastic Quad Flat Pack (PQFP)
FT256 FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)
FG320 FGG320	320-ball Fine-Pitch Ball Grid Array (FBGA)
FG400 FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)
FG484 FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)

Temperature Range (T_J)	
C	Commercial (0°C to 85°C)
I	Industrial (–40°C to 100°C)

ALTERA FPGA DEVICES

Technology	Low-cost	Mid-range	High-performance
130 nm	Cyclone		Stratix
90 nm	Cyclone II		Stratix II
65 nm	Cyclone III	Arria I	Stratix III
40 nm	Cyclone IV	Arria II	Stratix IV

How to Select an Appropriate FPGA

1. ***Speed Requirement***
   - *If the Maximum Frequency requirement for the design is not met with a* particular Xilinx device,
     - choose a Xilinx device of higher Speed Grade
     - switch to next generation Xilinx Product Family.
   - In Target Device Name, -x indicates Speed Grade available for the device. (Higher the indicated Speed Grade number, higher is the maximum frequency obtained through that device)

2. ***Logic Density***
   - ***Device utilization summary***
3. ***Package Type and Number of I/O Pins***