

Question Paper

Exam Date & Time: 26-Nov-2018 (08:30 AM - 11:30 AM)



MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

FIRST SEMESTER B.TECH END SEMESTER EXAMINATIONS, NOV 2018

Basic Electronics [ECE 1051 - 2018 -PHY]

Marks: 50

Duration: 180 mins.

A

Answer all the questions.

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed

- 1) For the biasing circuit shown in figure Q1A with silicon (4)
A) transistor, $R_1 = 39k\Omega$, $R_2 = 8.2k\Omega$, $R_C = 3.3k\Omega$, $R_E = 1k\Omega$,
 $V_{CC} = 18V$, $V_{BE} = 0.7V$ and $\beta = 120$. Determine I_B , I_C , V_{CE} ,
 V_E and V_B .

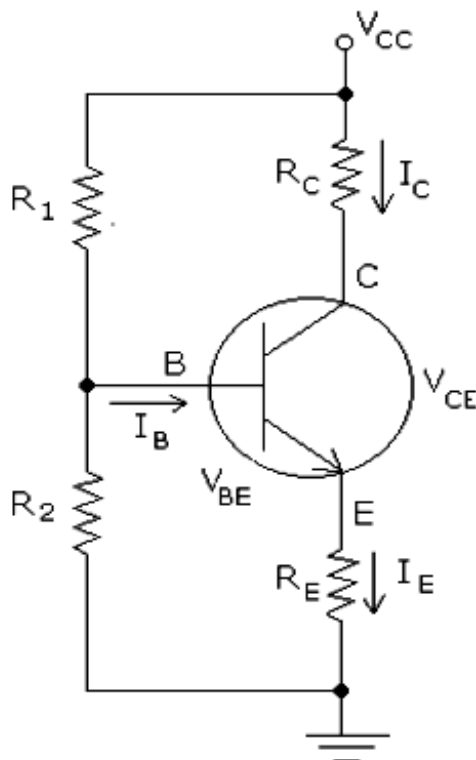


Figure Q1A

- B) Draw the circuit diagram of a full wave bridge rectifier with (3)
capacitor filter. Given $V_m = 24V$, $R_L = 1k\Omega$, $C = 1000\mu F$ and
 $f = 50Hz$, calculate the DC voltage and ripple factor.

- C) Draw the circuit diagram of RC coupled amplifier and discuss the role of coupling capacitor and emitter bypass capacitor. (3)
- 2) (i) Draw the circuit diagram of an OPAMP non inverting amplifier and derive the expression for its output voltage. (4)
- A) (ii) The inputs to the OPAMP are $V_{1(\text{non-inv})} = 3.5\text{mV}$ and $V_{2(\text{inv})} = -1.5\text{mV}$. If the differential gain is 60dB and CMRR is 40dB, calculate the output voltage.
- B) In an OPAMP comparator circuit $V_{\text{ref}} = -2\text{V}$ is applied to the non-inverting terminal and $V_{\text{in}} = 10\sin(\omega t)\text{V}$ is applied to the inverting terminal. Draw the circuit diagram and plot the input and output waveforms. Assume $V_{\text{sat}} = \pm 15\text{V}$. (3)
- C) Subtract $(11.75)_{10}$ from $(5.50)_8$ using 2's complement method. (3)
- 3) In a certain application, four inputs A, B, C, D are fed to a logic circuit, producing an output Z which controls a relay. (4)
- A) $Z = 1$ for the input states (ABCD): 0000, 0010, 0101, 0110, 1101 and 1110. The states 1000 and 1001 do not occur and $Z = 0$ for the remaining input states.
- i) Obtain truth table for Z.
- ii) Use Karnaugh map to find a minimal SOP and implement the same using NAND gates only.
- B) Draw the logic circuit of 3 bit up counter using negative edge triggered JK flip-flops. Also sketch the timing diagram. (3)
- C) With a neat logic diagram and table explain the shifting of data 111011 in a Serial-In Serial-Out 4-bit shift register. Also mention how many clock cycles are required to shift the MSB of above mentioned data to the output. (3)
- 4) Define frequency modulation. Sketch frequency modulated signal in time domain for a sinusoidal modulating signal. A carrier of peak amplitude 5V and frequency 90MHz is frequency modulated by a sinusoidal voltage of peak amplitude 5V and frequency 10 KHz. If the frequency sensitivity is 10Hz/V, calculate the frequency deviation and modulation index. Write the equation for the resulting FM wave. (4)
- A)

- B) The output current of a 60% modulated AM signal generator is 1.5A. To what value will this current rise if the generator is modulated additionally by another audio wave, whose modulation index is 0.7? (3)
- C) Highlight three important reasons why modulation is required in wireless communication. (3)
- 5) List the different types of analog pulse modulation schemes. Describe each with relevant waveforms. (4)
- A)
- B) Sketch the modulated signal waveforms for ASK, FSK and PSK if the modulating data stream is 10101. (3)
- C) Explain the following terms with reference to electronic communication systems (3)
- i) TDMA ii) MAN iii) EIR

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Question Paper

Exam Date & Time: 28-Dec-2018 (08:30 AM - 11:30 AM)



MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

FIRST SEMESTER B.TECH END SEMESTER MAKEUP EXAMINATIONS, DEC 2018

Basic Electronics [ECE 1051 - 2018 -PHY]

Marks: 50

Duration: 180 mins.

A

Answer all the questions.

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed

- 1) For the biasing circuit shown in Figure Q1A with silicon (4)
A) transistor, $R_B = 470k\Omega$, $R_C = 2.7k\Omega$, $V_{BE}=0.7V$, $V_{CC} = 16V$
and $\beta = 90$. Determine I_B , I_C , V_{CE} , V_E and V_B .

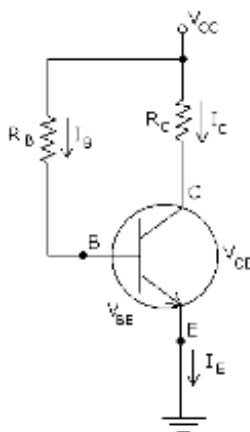


Figure Q1A

- B) Draw the input and output V-I characteristics of an npn (3)
transistor in CE Configuration. If $V_{CE} = 0.2V$ and $V_{BE}=0.7V$,
identify the region of operation of the transistor.
- C) Draw the circuit of Zener voltage regulator. Given $V_i =$ (3)
 $20V$, $R_S = 220\Omega$, $V_Z = 10V$, $P_{Zmax} = 400mW$, determine V_L ,
 I_L , I_Z , and I_R for the Zener voltage regulator if $R_L = 470\Omega$.
- 2) (i) Define the terms Differential gain, CMRR, Slew Rate and (4)
Input resistance with respect to OPAMP.
A) (ii) Design a circuit using OPAMP to obtain output $V_o = -$
 $(0.1V_a + V_b + 10V_c)$ where, V_a , V_b and V_c are the input
signals. Draw the circuit diagram. (Select $R_F = 1k\Omega$)

- B) Draw the circuit diagrams of Integrator and Differentiator using OPAMP. Derive the expressions for the output voltage of these circuits. (3)
- C) Perform $(75)_8 - (67)_{10}$ using 1's complement method. (3)
- 3) A logical function is defined by $f(A,B,C,D) = \sum m(0,2,4,6,8,13) + \sum d(5,7,10,11,12)$. Simplify the expression using K-Map and implement using NAND gates only. (4)
- A)
- B) Test the received code word 1011101 for error if data stream 1101 was encoded using (7,4) Hamming code over noisy channel. (3)
- C) Realize a 3-bit down counter using positive edge triggered JK flip flops. Draw the timing diagram for the same. (3)
- 4) Define Amplitude modulation. Sketch AM signal in time domain for a sinusoidal modulating signal. An AM wave is expressed by the following equation: (4)
- A)
- $$V_{AM}(t) = 6.5 (1 + 0.5 \sin 5027t) \cos (10053 \times 10^3 t)$$
- Sketch the spectrum of this AM Signal.
- B) Write the equation for Frequency Modulated signal in time domain for a sinusoidal modulating signal. Determine the bandwidth of FM signal required to transmit 10 kHz, 2V peak amplitude signal with frequency sensitivity 3 kHz/V using Carson's rule. (3)
- C) When the modulation percentage is 75, an AM transmitter produces 10kW of power. Determine the carrier power. What would be the percentage power saving if the carrier and one of the sidebands were suppressed before transmitting the signal? (3)
- 5) Draw the block diagram of Digital Communication system and explain the function of each block. (4)
- A)
- B) Highlight the various functions involved in the data communication system. (3)
- C) Explain the following terms with reference to electronic communication systems. (3)
- i) CDMA ii) FSK iii) VLR

MOSFET

2.1 INTRODUCTION

Today's field of microelectronics is dominated by a type of device called the metal oxide-semiconductor field-effect transistor (MOSFET). MOSFETs (also called as MOS devices) considered in the 1930s but first realized in the 1960s. In this chapter, we analyse the structure and operation of MOSFETs, small signal models for circuit design.

2.1 STRUCTURE OF MOSFET

A simple geometry of MOSFET consisting of a conductive (e.g., metal) plate, an insulator ("dielectric"), and a doped piece of silicon as illustrated in Fig. 2.1(a), operates as a capacitor. When a potential difference is applied as shown in Fig. 2.1(b), positive charge placed on the top plate attracts minority carriers i.e., electrons (negative charge) from the piece of silicon. We therefore observe that a "channel" of free electrons may be created at the interface between the insulator and the piece of silicon, potentially serving as a good conductive path if the electron density is sufficiently high. The key point here is that the density of electrons in the channel varies with V_1 , as evident from $Q = CV$, where C denotes the capacitance between the two plates. The dependence of the electron density upon V_1 leads to an interesting property: if, as depicted in Fig. 2.1(c), we allow a current to flow from left to right through the silicon material, V_1 can control the current by adjusting the resistivity of the channel thus building a voltage-controlled current source.

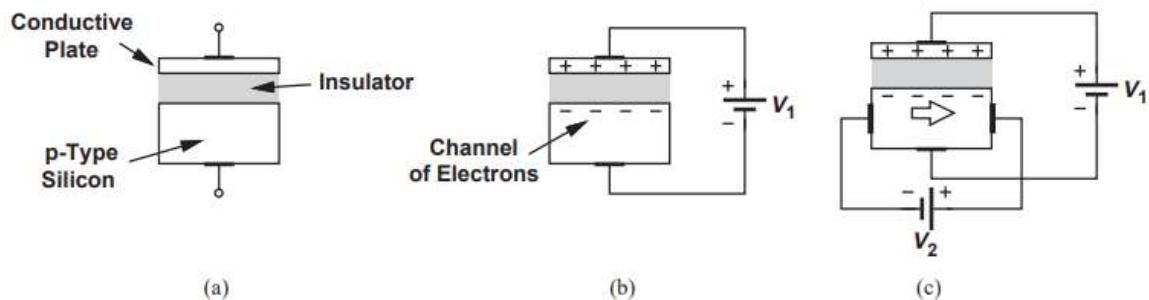


Figure 2.1 (a) Hypothetical semiconductor device, (b) operation as a capacitor, (c) current flow as a result of potential difference.

The ability of silicon fabrication technology to produce extremely thin but uniform dielectric layers lead to the MOSFET structure shown in Fig. 2.2(a) as an amplifying device. The top conductive plate Called the "gate" (G) resides on a thin dielectric (insulator) layer, which itself is deposited on the underlying p-type silicon "substrate." To allow current flow through the silicon material, two contacts are attached to the substrate through two heavily-doped n-type regions because direct connection of metal to the substrate would not produce a good "ohmic" contact.² These two terminals are called "source" (S) and "drain" (D) to indicate that the former can provide charge carriers and the latter can absorb them. Figure 2.2(a) reveals that the device is symmetric with respect to S and D; i.e., depending on the voltages applied to the device, either of these two terminals can drain the charge carriers from the other. As explained in Section 2.2, with n-type source/drain and p-type substrate, this transistor operates with electrons rather than holes and is therefore called an n-type MOS (NMOS) device. We draw the device as shown in Fig. 2.2(b) for

simplicity. Figure 2.2(c) depicts the circuit symbol for an NMOS transistor, wherein the arrow signifies the source terminal.

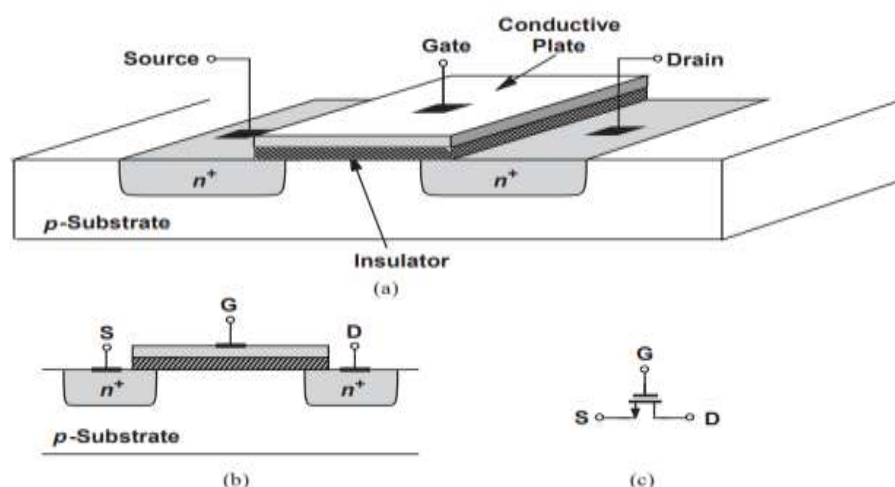


Figure 2.2 (a) Structure of MOSFET, (b) side view, (c) circuit symbol

The gate plate must serve as a good conductor and was in fact realized by metal (aluminum) in the early generations of MOS technology. However, it was discovered that noncrystalline silicon (“polysilicon” or simply “poly”) with heavy doping (for low resistivity) exhibits better fabrication and physical properties. Thus, today’s MOSFETs employ polysilicon gates. The dielectric layer sandwiched between the gate and the substrate plays a critical role in the performance of transistors and is created by growing silicon dioxide (or simply “oxide”) on top of the silicon area. The n^+ regions are sometimes called source/drain “diffusion,” referring to a fabrication method used in early days of microelectronics.

2.2 OPERATION OF MOSFET

The simple structures shown in Figs. 2.1 and 2.2 suggests that the MOSFET may conduct current between the source and drain if a channel of electrons is created by making the gate voltage sufficiently positive. Moreover, we expect that the magnitude of the current can be controlled by the gate voltage. Note that the gate terminal draws no (low-frequency) current as it is insulated from the channel by the oxide.

Let us first consider the arrangement shown in Fig. 2.3(a), where the source and drain are grounded and the gate voltage is varied. Recall from Fig. 2.1(b) that, as V_G rises, the positive charge on the gate must be mirrored by negative charge in the substrate. While we stated in Section 2.1 that electrons are attracted to the interface, in reality, another phenomenon precedes the formation of the channel. As V_G increases from zero, the positive charge on the gate repels the holes in the substrate, thereby exposing negative ions and creating a depletion region as illustrated in Fig. 2.3(b). Note that the device still acts as a capacitor- positive charge on the gate is mirrored by negative charge in the substrate- but no channel of mobile charge is created yet. Thus, no current can flow from the source to the drain. We say the MOSFET is off. As V_G increases, the charge on the gate, more negative ions are exposed and the depletion region under the oxide becomes deeper. if V_G becomes sufficiently positive, free electrons are attracted to the oxide-silicon interface, forming a conductive channel as shown in Fig. 2.3(c). We say the MOSFET is on. The gate

potential at which the channel begins to appear is called the “threshold voltage,” V_{TH} , and falls in the range of 300 mV to 500 mV. Note that the electrons are readily provided by the n^+ source and drain regions, and need not be supplied by the substrate. It is interesting to recognize that the gate terminal of the MOSFET draws no (low frequency) current. Resting on top of the oxide, the gate remains insulated from other terminals and simply operates as a plate of a capacitor.

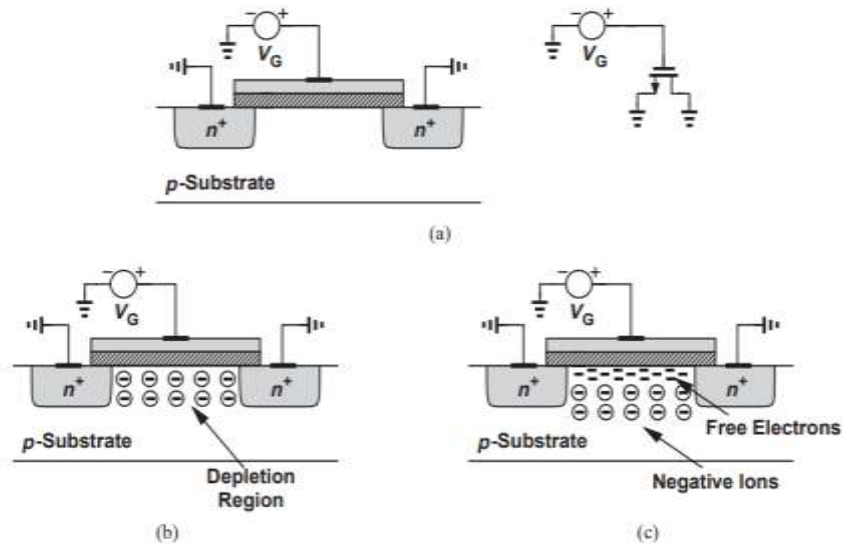


Figure 2.3 (a) MOSFET with gate voltage, (b) formation of depletion region, (c) formation of channel

2.3 Channel Pinch-Off

If the drain voltage is high enough to produce $V_G - V_D \leq V_{TH}$, then the channel ceases to exist near the drain. We say the gate-substrate potential difference is not sufficient at $x = L$ to attract electrons and the channel is “pinched off” [Fig. 2.4 (a)].

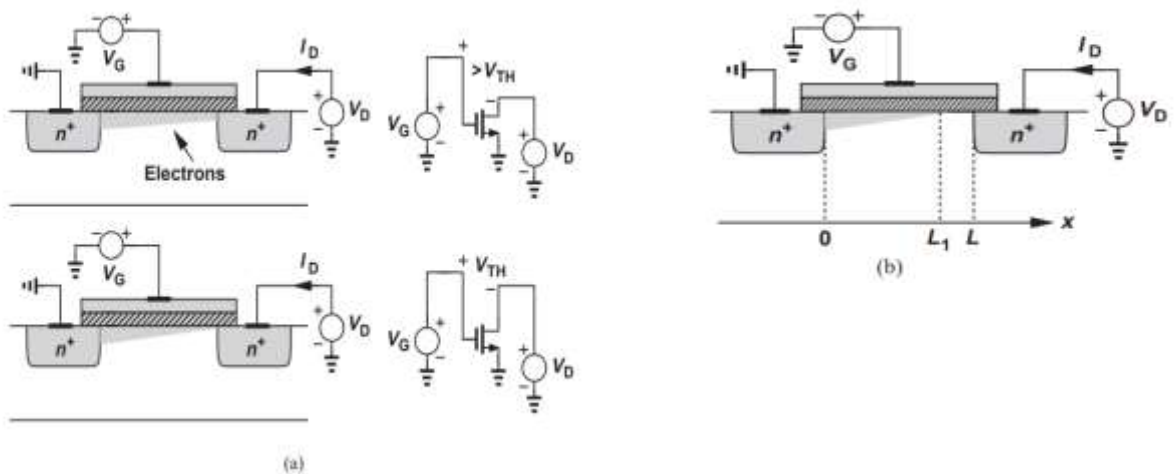


Figure 2.4 (a) Pinchoff, (b) variation of length with drain voltage

If V_D rises even higher than $V_G - V_{TH}$, $V(x)$ now goes from 0 at $x = 0$ to $V_D > V_G - V_{TH}$ at $x = L$. The voltage difference between the gate and the substrate falls to V_{TH} at some point $L_1 < L$ [Fig. 2.4(b)]. The device therefore contains no channel between L_1 and L . However, the device still conducts once the electrons reach the end of the channel. They

experience the high electric field in the depletion region surrounding the drain junction and are rapidly swept to the drain terminal.

2.4 Derivation of I-V Characteristics

We now formulate the behaviour of MOSFETs in terms of their terminal voltages.

2.4.1 Channel Charge Density

Our derivations require an expression for the channel charge (i.e., free electrons) per unit length, also called the “charge density.” From $Q = CV$, we note that if C is the gate capacitance per unit length and V the voltage difference between the gate and the channel, then Q is the desired charge density. Denoting the gate capacitance per unit area by C_{ox} (expressed in F/m^2 or $fF/\mu m^2$), we write $C = WC_{ox}$ to account for the width of the transistor (Fig. 2.5). Moreover, we have $V = V_{GS} - V_{TH}$ because no mobile charge exists for $V_{GS} < V_{TH}$. (Hereafter, we denote both the gate and drain voltages with respect to the source.) It follows that

$$Q = WC_{ox}(V_{GS} - V_{TH}) \quad (2.1)$$

Where Q is expressed in coulomb/meter.

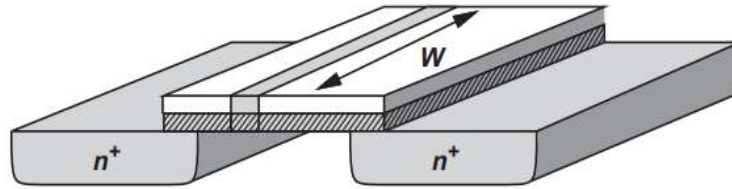


Figure 2.5 Illustration of capacitance per unit length

As we know that the channel voltage varies along the length of the transistor, and the charge density falls as we go from the source to the drain. Thus, Eq. (2.1) is valid only near the source terminal, where the channel potential remains close to zero. As shown in Fig. 2.6, we denote the channel potential at x by $V(x)$ and write

$$Q = WC_{ox}(V_{GS} - V(x) - V_{TH}) \quad (2.2)$$

noting that $V(x)$ goes from zero to V_D if the channel is not pinched off.

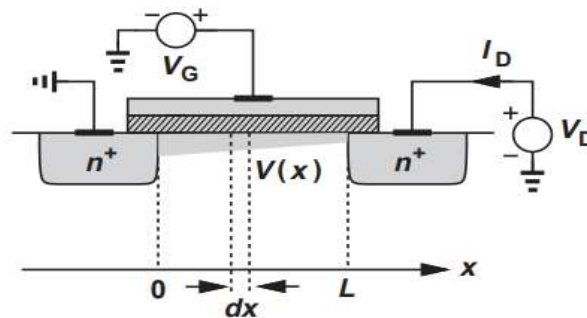


Figure 2.6 Device illustration for calculation of drain current

2.4.2 Drain Current

Consider a bar of semiconductor having a uniform charge density (per unit length) equal to Q and carrying a current I (Fig. 2.7). We know that, (i) Current ‘ I ’ is given by the total charge that passes through the cross section of the bar in one second, and (ii) if the carriers

move with a velocity of v m/s, then the charge enclosed in v meters along the bar passes through the cross section in one second. Since the charge enclosed in v meters is equal to $Q \cdot v$, we have

$$I = Q \cdot v \quad (2.3)$$

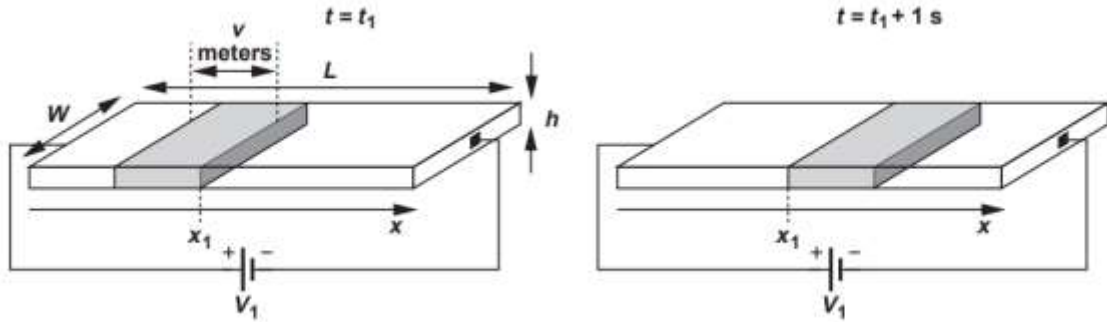


Figure 2.7 Relationship between charge velocity and current

We know that,

$$v = -\mu_n E \quad (2.4)$$

$$= +\mu_n \frac{dV}{dx} \quad (2.5)$$

where dV/dx denotes the derivative of the voltage at a given point. Combining Eqs. (2.2), (2.3), and (2.5), we obtain

$$I_D = WCox(V_{GS} - V(x) - V_{TH})\mu_n \frac{dV(x)}{dx} \quad (2.6)$$

our immediate need is to find an expression for I_D in terms of the terminal voltages. To this end, we write

$$\int_{x=0}^{x=L} I_D dx = \int_{V(x)=0}^{V(x)=V_{DS}} \mu_n Cox W [V_{GS} - V(x) - V_{TH}] dV. \quad (2.7)$$

That is,

$$I_D = \frac{1}{2} \mu_n Cox \frac{W}{L} [2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \quad (2.8)$$

From the Eq (2.8), the linear dependence of I_D upon μ_n , C_{ox} , and W/L is to be expected: a higher mobility yields a greater current for a given drain-source voltage; a higher gate oxide capacitance leads to a larger electron density in the channel for a given gate-source voltage; and a larger W/L (called the device “aspect ratio”) is equivalent to placing more transistors in parallel. Also, for a constant V_{GS} , I_D varies parabolically with V_{DS} (Fig. 2.8), reaching a maximum of

$$I_{D,max} = \frac{1}{2} \mu_n Cox \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (2.9)$$

at $V_{DS} = V_{GS} - V_{TH}$.

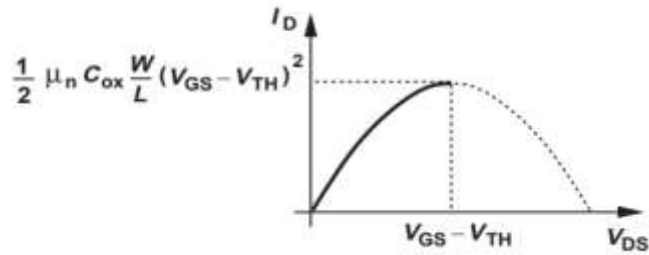


Figure 2.8 Parabolic ID-VDS characteristic

2.4.3 Triode and Saturation Regions

Equation (2.8) expresses the drain current in terms of the device terminal voltages, implying that the current begins to fall for $V_{DS} > V_{GS} - V_{TH}$. We say the device operates in the “triode region” (also called the “linear region”) if $V_{DS} < V_{GS} - V_{TH}$ (the rising section of the parabola). We also use the term “deep triode region” for $V_{DS} \ll 2(V_{GS} - V_{TH})$, where the transistor operates as a resistor. In reality, the drain current reaches “saturation,” that is, becomes constant for $V_{DS} > V_{GS} - V_{TH}$ (Fig. 2.9) as the channel experiences pinch-off if $V_{DS} = V_{GS} - V_{TH}$. Thus, further increase in V_{DS} simply shifts the pinch-off point slightly toward the drain.

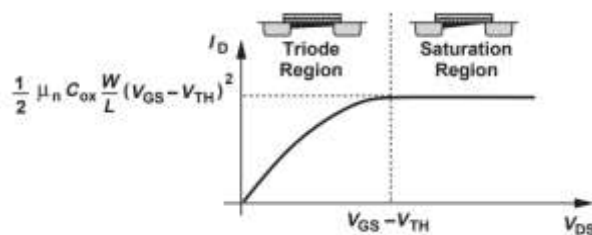


Figure 2.9 Overall MOS characteristic

Problems:

2.1 Calculate the bias current of M_1 in Fig. 2.10. Assume $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$ and $V_{TH} = 0.4 \text{ V}$. If the gate voltage increases by 10 mV, what is the change in the drain voltage?

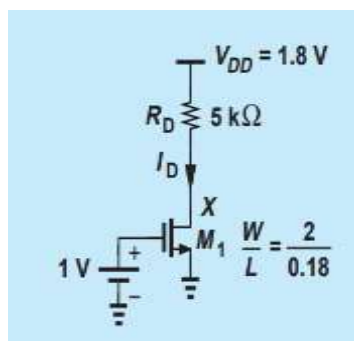


Figure 2.10 Simple MOS circuit

Solution

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$= 200 \mu\text{A}$$

We must check our assumption by calculating the drain potential:

$$\begin{aligned} V_X &= V_{DD} - R_D I_D \\ &= 0.8 \text{ V} \end{aligned}$$

The drain voltage is lower than the gate voltage, but by less than V_{TH}

The illustration in Fig. 2.8 therefore indicates that M_1 indeed operates in saturation. If the gate voltage increases to 1.01 V, then

$$I_D = 206.7 \mu\text{A}$$

lowering V_X to

$$V_X = 0.766 \text{ V}$$

Fortunately, M_1 is still saturated. The 34mV change in V_X reveals that the circuit can amplify the input.

**2.2 Determine the value of W/L in Fig. 2.10 that places M_1 at the edge of saturation and calculate the drain voltage change for a 1mV change at the gate. Assume $V_{TH} = 0.4 \text{ V}$.
Solution**

With $V_{GS} = +1 \text{ V}$, the drain voltage must fall to $V_{GS} - V_{TH} = 0.6 \text{ V}$ for M_1 to enter the triode region. That is,

$$\begin{aligned} I_D &= \frac{V_{DD} - V_{DS}}{R_D} \\ &= 240 \mu\text{A} \end{aligned}$$

Since I_D scales linearly with W/L ,

$$\begin{aligned} \left. \frac{W}{L} \right|_{\max} &= \frac{240 \mu\text{A}}{200 \mu\text{A}} \cdot \frac{2}{0.18} \\ &= \frac{2.4}{0.18} \end{aligned}$$

If V_{GS} increases by 1 mV,

$$\begin{aligned} I_D &= 248.04 \mu\text{A}, \\ \Delta V_X &= \Delta I_D \cdot R_D \\ &= 4.02 \text{ mV} \end{aligned}$$

The voltage gain is thus equal to 4.02 in this case.

2.5 MOS TRANSCONDUCTANCE

As a voltage-controlled current source, a MOS transistor can be characterized by its transconductance:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (2.10)$$

This quantity serves as a measure of the “strength” of the device: a higher value corresponds to a greater change in the drain current for a given change in V_{GS} . Using Equation 2.9 for the saturation region, we have

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \quad (2.11)$$

Also, substituting for $V_{GS} - V_{TH}$ from Eq. (2.9), we obtain

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

2.6 SMALL SIGNAL MODEL OF MOSFET

We now develop small signal model that can be used in circuit analysis and design.

Viewing the transistor as a voltage controlled current source, we draw the basic model as in Fig. 2.11(a), where $i_D = g_m v_{GS}$ and the gate remains open. To represent channel-length modulation, i.e., variation of i_D with v_{DS} , we add a resistor as in Fig. 2.11(b):

$$r_o = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} \quad (2.12)$$

$$= \frac{1}{I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \lambda} \quad (2.13)$$

Since channel-length modulation is relatively small, the denominator of Eq. (2.13) can be approximated as $I_D \cdot \lambda$, yielding

$$r_o \approx \frac{1}{\lambda I_D}$$

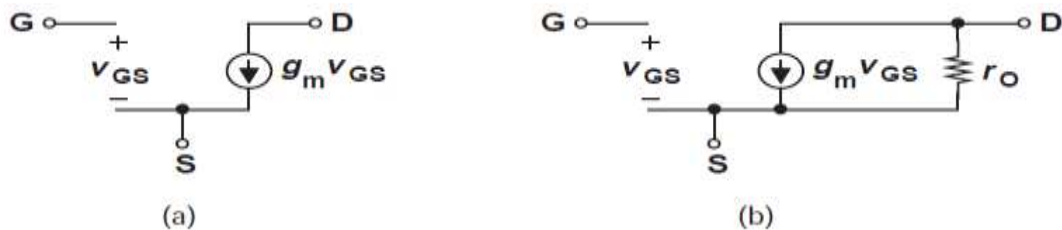


Figure 2.11: (a) Small-signal model of MOSFET, (b) inclusion of channel-length modulation

EXAMPLE

2.3 A MOSFET is biased at a drain current of 0.5 mA. If $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$, $W/L = 10$, and $\lambda = 0.1 \text{ V}^{-1}$, calculate its small-signal parameters.

Solution

We have

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

$$= 1 / 1 \text{ k}\Omega$$

$$r_o \approx \frac{1}{\lambda I_D}$$

$$= 20 \text{ k}\Omega$$