

## Features

- High Performance, Low Power AVR<sup>®</sup> 8-Bit Microcontroller
- Advanced RISC Architecture
  - 123 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20 MHz
- High Endurance Non-volatile Memory Segments
  - 2/4/8K Bytes of In-System Self-Programmable Flash Program Memory
    - Endurance: 10,000 Write/Erase Cycles
  - 128/256/512 Bytes of In-System Programmable EEPROM
    - Endurance: 100,000 Write/Erase Cycles
  - 128/256/512 Bytes of Internal SRAM
  - Data retention: 20 Years at 85°C / 100 Years at 25°C
  - In-System Programmable via SPI Port
  - Programming Lock for Software Security
- Peripheral Features
  - One 8/16-bit Timer/Counter with Prescaler
  - One 8/10-bit High Speed Timer/Counter with Prescaler
    - 3 High Frequency PWM Outputs with Separate Output Compare Registers
    - Programmable Dead Time Generator
  - 10-bit ADC
    - 11 Single-Ended Channels
    - 16 Differential ADC Channel Pairs
    - 15 Differential ADC Channel Pairs with Programmable Gain (1x, 8x, 20x, 32x)
  - On-chip Analog Comparator
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - Universal Serial Interface with Start Condition Detector
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - debugWIRE On-chip Debug System
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Four Sleep Modes: Low Power Idle, ADC Noise Reduction, Standby and Power-Down
  - On-Chip Temperature Sensor
- I/O and Packages
  - 16 Programmable I/O Lines
  - 20-pin PDIP, 20-pin SOIC, 20-pin TSSOP and 32-pad MLF
- Operating Voltage
  - 1.8 – 5.5V
- Speed Grades
  - 0 – 4 MHz @ 1.8 – 5.5V
  - 0 – 10 MHz @ 2.7 – 5.5V
  - 0 – 20 MHz @ 4.5 – 5.5V
- Power Consumption at 1MHz, 1.8V, 25°C
  - Active: 200 µA
  - Power-Down Mode: 0.1 µA



**8-bit AVR<sup>®</sup>  
Microcontroller  
with 2/4/8K  
Bytes In-System  
Programmable  
Flash**

**ATtiny261A  
ATtiny461A  
ATtiny861A**

**Preliminary**

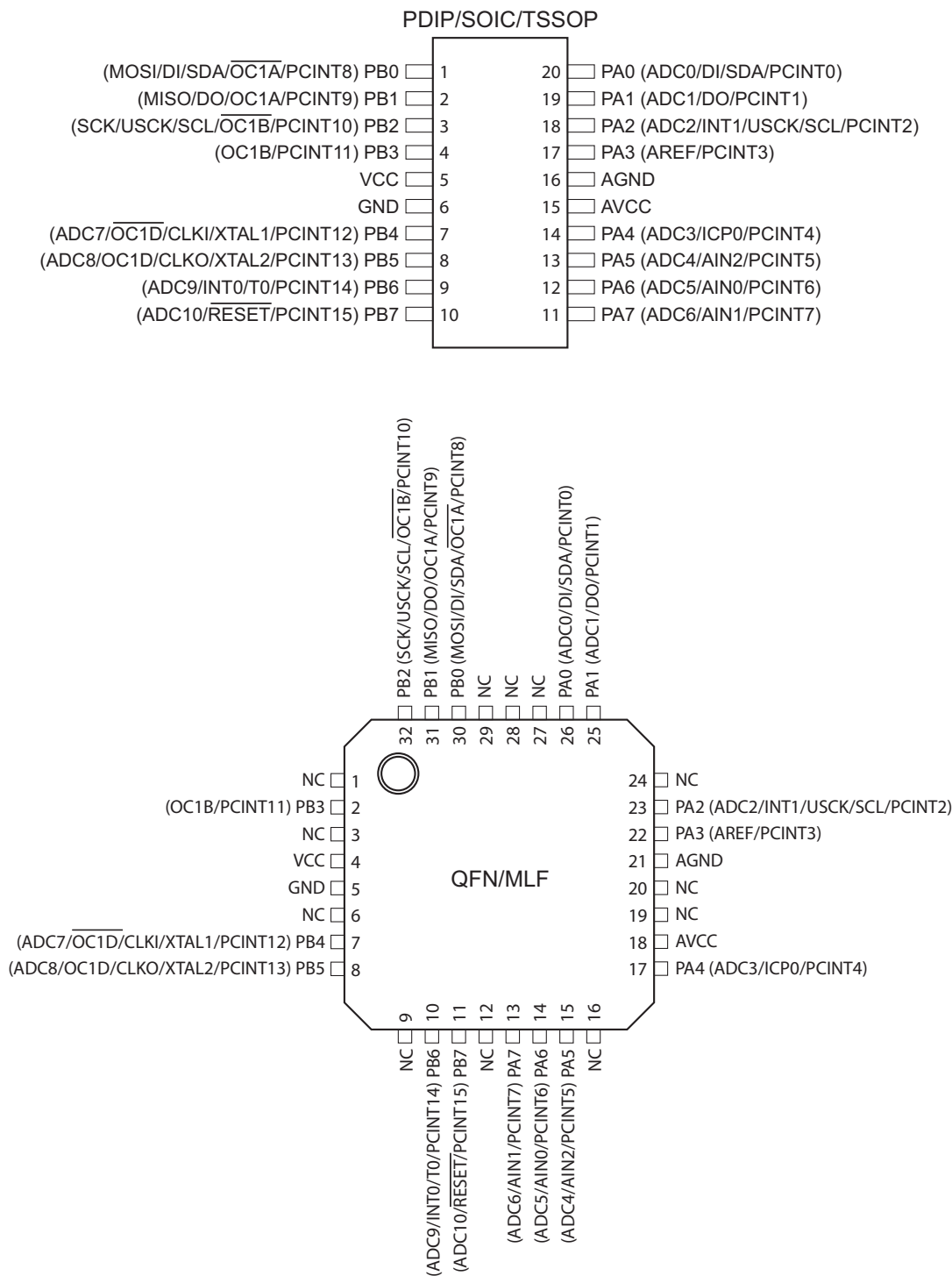
**Summary**

8197AS-AVR-10/09



## 1. Pin Configurations

Figure 1-1. Pinout ATtiny261A/461A/861A



Note: To ensure mechanical stability the center pad underneath the QFN/MLF package should be soldered to ground on the board.

## **1.1 Pin Descriptions**

### **1.1.1 VCC**

Supply voltage.

### **1.1.2 GND**

Ground.

### **1.1.3 AVCC**

Analog supply voltage. This is the supply voltage pin for the Analog-to-digital Converter (ADC), the analog comparator, the Brown-Out Detector (BOD), the internal voltage reference and Port A. It should be externally connected to VCC, even if some peripherals such as the ADC are not used. If the ADC is used AVCC should be connected to VCC through a low-pass filter.

### **1.1.4 AGND**

Analog ground.

### **1.1.5 Port A (PA7:PA0)**

An 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. Output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, port pins that are externally pulled low will source current if pull-up resistors have been activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the device, as listed on [page 61](#).

### **1.1.6 Port B (PB7:PB0)**

An 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. Output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, port pins that are externally pulled low will source current if pull-up resistors have been activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the device, as listed on [page 64](#).

### **1.1.7 RESET**

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in [Table 19-4 on page 187](#). Shorter pulses are not guaranteed to generate a reset.

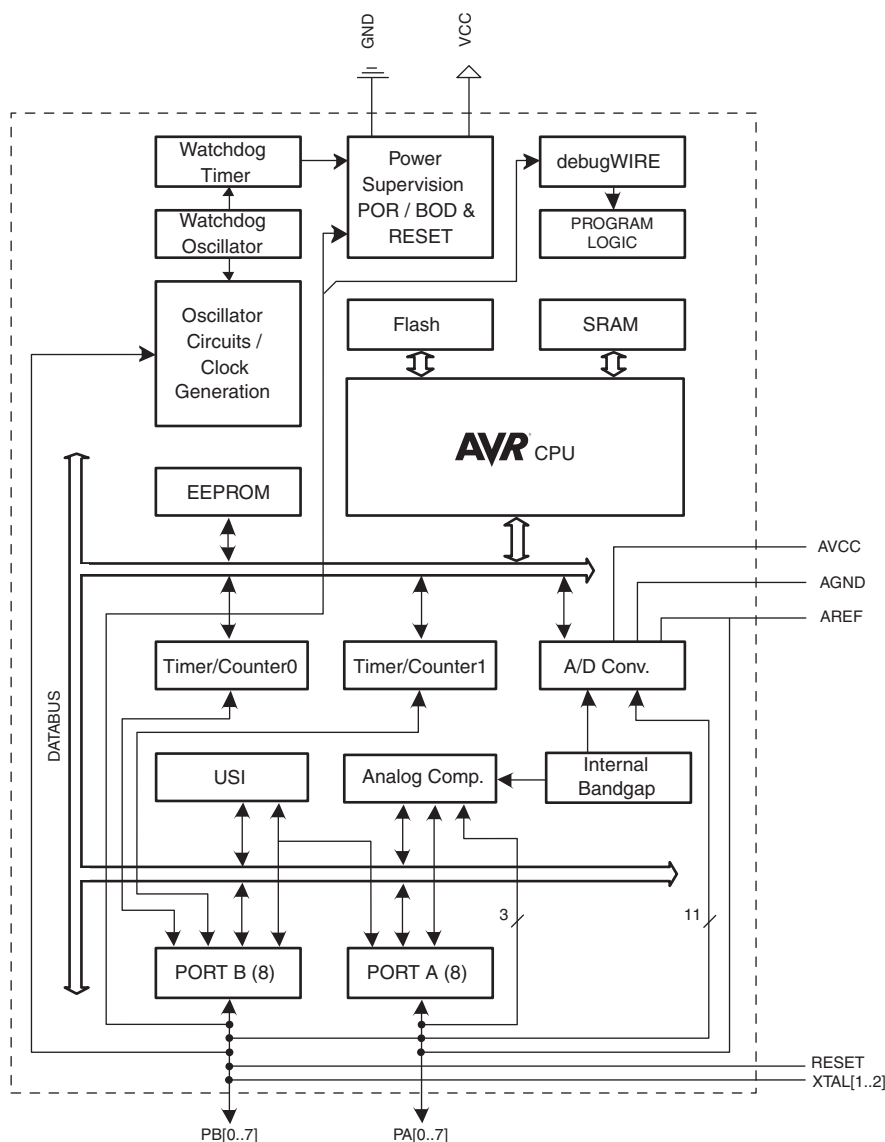
The reset pin can also be used as a (weak) I/O pin.

## 2. Overview

ATtiny261A/461A/861A are low-power CMOS 8-bit microcontrollers based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the devices achieve throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

### 2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATTiny261A/461A/861A provides the following features: 2/4/8K byte of In-System Programmable Flash, 128/256/512 bytes EEPROM, 128/256/512 bytes SRAM, 16 general purpose I/O lines, 32 general purpose working registers, an 8-bit Timer/Counter with compare modes, an 8-bit high speed Timer/Counter, a Universal Serial Interface, Internal and External Interrupts, an 11-channel, 10-bit ADC, a programmable Watchdog Timer with internal oscillator, and four software selectable power saving modes. Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping, allowing very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core.

The ATTiny261A/461A/861A AVR is supported by a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, and Evaluation kits.

## 3. General Information

### 3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at <http://www.atmel.com/avr>.

### 3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in the extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically, this means "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR". Note that not all AVR devices include an extended I/O map.

### 3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

## 4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	<a href="#">page 8</a>
0x3E (0x5E)	SPH	–	–	–	–	–	SP10	SP9	SP8	<a href="#">page 11</a>
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	<a href="#">page 11</a>
0x3C (0x5C)	Reserved	–								
0x3B (0x5B)	GIMSK	INT1	INT0	PCIE1	PCIE0	–	–	–	–	<a href="#">page 50</a>
0x3A (0x5A)	GIFR	INTF1	INTF0	PCIF	–	–	–	–	–	<a href="#">page 51</a>
0x39 (0x59)	TIMSK	OCIE1D	OCIE1A	OCIE1B	OCIE0A	OCIE0B	TOIE1	TOIE0	TICIE0	<a href="#">page 84, page 121</a>
0x38 (0x58)	TIFR	OCF1D	OCF1A	OCF1B	OCF0A	OCF0B	TOV1	TOV0	ICF0	<a href="#">page 85, page 121</a>
0x37 (0x57)	SPMCSR	–	–	–	CTPB	RFLB	PGWRT	PGERS	SPMEN	<a href="#">page 166</a>
0x36 (0x56)	PRR	–	–	–	–	PRTIM1	PRTIM0	PRUSI	PRADC	<a href="#">page 35</a>
0x35 (0x55)	MCUCR	BODS	PUD	SE	SM1	SM0	BODSE	ISC01	ISC00	<a href="#">page 37, page 67, page 50</a>
0x34 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	<a href="#">page 45,</a>
0x33 (0x53)	TCCR0B	–	–	–	TSM	PSR0	CS02	CS01	CS00	<a href="#">page 83</a>
0x32 (0x52)	TCNT0L	Timer/Counter0 Counter Register Low Byte								<a href="#">page 83</a>
0x31 (0x51)	OSCCAL	Oscillator Calibration Register								<a href="#">page 32</a>
0x30 (0x50)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	PWM1A	PWM1B	<a href="#">page 110</a>
0x2F (0x4F)	TCCR1B	PWM1X	PSR1	DTPS11	DTPS10	CS13	CS12	CS11	CS10	<a href="#">page 166</a>
0x2E (0x4E)	TCNT1	Timer/Counter1 Counter Register								<a href="#">page 119</a>
0x2D (0x4D)	OCR1A	Timer/Counter1 Output Compare Register A								<a href="#">page 119</a>
0x2C (0x4C)	OCR1B	Timer/Counter1 Output Compare Register B								<a href="#">page 120</a>
0x2B (0x4B)	OCR1C	Timer/Counter1 Output Compare Register C								<a href="#">page 120</a>
0x2A (0x4A)	OCR1D	Timer/Counter1 Output Compare Register D								<a href="#">page 120</a>
0x29 (0x49)	PLLCSR	LSM	–	–	–	–	–	PCKE	PLLE	<a href="#">page 118</a>
0x28 (0x48)	CLKPR	CLKPCE	–	–	–	–	CLKPS3	CLKPS2	CLKPS1	<a href="#">page 32</a>
0x27 (0x47)	TCCR1C	COM1A1S	COM1A0S	COM1B1S	COM1B0S	COM1D1	COM1D0	FOC1D	PWM1D	<a href="#">page 115</a>
0x26 (0x46)	TCCR1D	FP1E1	FPEN1	FPNC1	FPES1	FPAC1	FPF1	WGM11	WGM10	<a href="#">page 116</a>
0x25 (0x45)	TC1H	–	–	–	–	–	–	TC19	TC18	<a href="#">page 119</a>
0x24 (0x44)	DT1	DT1H3	DT1H2	DT1H1	DT1H0	DT1L3	DT1L2	DT1L1	DT1L0	<a href="#">page 122</a>
0x23 (0x43)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	<a href="#">page 52</a>
0x22 (0x42)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	<a href="#">page 52</a>
0x21 (0x41)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	<a href="#">page 45</a>
0x20 (0x40)	DWDR	DWDR[7:0]								<a href="#">page 35</a>
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	<a href="#">page 20</a>
0x1E (0x3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	<a href="#">page 21</a>
0x1D (0x3D)	EEDR	EEPROM Data Register								<a href="#">page 21</a>
0x1C (0x3C)	EECR	–	–	EEDM1	EEDM0	EERIE	EEMPE	EEPE	EERE	<a href="#">page 21</a>
0x1B (0x3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	<a href="#">page 67</a>
0x1A (0x3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	<a href="#">page 67</a>
0x19 (0x39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	<a href="#">page 68</a>
0x18 (0x38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	<a href="#">page 68</a>
0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	<a href="#">page 68</a>
0x16 (0x36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	<a href="#">page 68</a>
0x15 (0x35)	TCCR0A	TCW0	ICEN0	ICNC0	ICES0	ACIC0	–	–	CTC0	<a href="#">page 82</a>
0x14 (0x34)	TCNT0H	Timer/Counter0 Counter Register High Byte								<a href="#">page 84</a>
0x13 (0x33)	OCR0A	Timer/Counter0 Output Compare Register A								<a href="#">page 84</a>
0x12 (0x32)	OCR0B	Timer/Counter0 Output Compare Register B								<a href="#">page 84</a>
0x11 (0x31)	USIPP	–	–	–	–	–	–	–	USIPOS	<a href="#">page 134</a>
0x10 (0x30)	USIBR	USI Buffer Register								<a href="#">page 131</a>
0x0F (0x2F)	USIDR	USI Data Register								<a href="#">page 130</a>
0x0E (0x2E)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	<a href="#">page 131</a>
0x0D (0x2D)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICKL	USITC	<a href="#">page 132</a>
0x0C (0x2C)	GPOR2	General Purpose I/O Register 2								<a href="#">page 22</a>
0x0B (0x2B)	GPOR1	General Purpose I/O Register 1								<a href="#">page 23</a>
0x0A (0x2A)	GPOR0	General Purpose I/O Register 0								<a href="#">page 23</a>
0x09 (0x29)	ACSRB	HSEL	HLEV	–	–	–	ACM2	ACM1	ACM0	<a href="#">page 138</a>
0x08 (0x28)	ACSRA	ACD	ACBG	ACO	ACI	ACIE	ACME	ACIS1	ACIS0	<a href="#">page 137</a>
0x07 (0x27)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	<a href="#">page 154</a>
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	<a href="#">page 153</a>
0x05 (0x25)	ADCH	ADC Data Register High Byte								<a href="#">page 154</a>
0x04 (0x24)	ADCL	ADC Data Register Low Byte								<a href="#">page 154</a>
0x03 (0x23)	ADCSRB	BIN	GSEL	–	REFS2	MUX5	ADTS2	ADTS1	ADTS0	<a href="#">page 158</a>
0x02 (0x22)	DIDR1	ADC10D	ADC9D	ADC8D	ADC7D	–	–	–	–	<a href="#">page 159</a>
0x01 (0x21)	DIDR0	ADC6D	ADC5D	ADC4D	ADC3D	AREFD	ADC2D	ADC1D	ADC0D	<a href="#">page 159</a>
0x00 (0x20)	TCCR1E	–	–	OC1OE5	OC1OE4	OC1OE3	OC1OE2	OC1OE1	OC1OE0	<a href="#">page 117</a>

- Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
  2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
  3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVR's, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.



## 5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
<b>ARITHMETIC AND LOGIC INSTRUCTIONS</b>					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	RdI,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	RdI,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
<b>BRANCH INSTRUCTIONS</b>					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N $\oplus$ V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N $\oplus$ V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then $PC \leftarrow PC + k + 1$	None	1/2
<b>BIT AND BIT-TEST INSTRUCTIONS</b>					
SBI	P,b	Set Bit in I/O Register	$I/O(P,b) \leftarrow 1$	None	2
CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Twos Complement Overflow.	$V \leftarrow 1$	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1
<b>DATA TRANSFER INSTRUCTIONS</b>					
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow Rr, X \leftarrow X + 1$	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q, Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	3
SPM		Store Program Memory	$(z) \leftarrow R1:R0$	None	
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
<b>MCU CONTROL INSTRUCTIONS</b>					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/Timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

## 6. Ordering Information

### 6.1 ATtiny261A

Speed (MHz)	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operational Range
20 <sup>(3)</sup>	1.8 – 5.5V	ATtiny261A-MU ATtiny261A-PU ATtiny261A-SU ATtiny261A-XU	32M1-A 20P3 20S2 20X	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$ , see [Figure 19.3 on page 185](#).

Package Type	
<b>32M1-A</b>	32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF)
<b>20P3</b>	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>20S2</b>	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC)
<b>20X</b>	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline Package (TSSOP)

## 6.2 ATtiny461A

Speed (MHz)	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operational Range
20 <sup>(3)</sup>	1.8 – 5.5V	ATtiny461A-MU ATtiny461A-PU ATtiny461A-SU ATtiny461A-XU	32M1-A 20P3 20S2 20X	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$ , see [Figure 19.3 on page 185](#).

Package Type	
<b>32M1-A</b>	32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF)
<b>20P3</b>	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>20S2</b>	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC)
<b>20X</b>	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline Package (TSSOP)

## 6.3 ATtiny861A

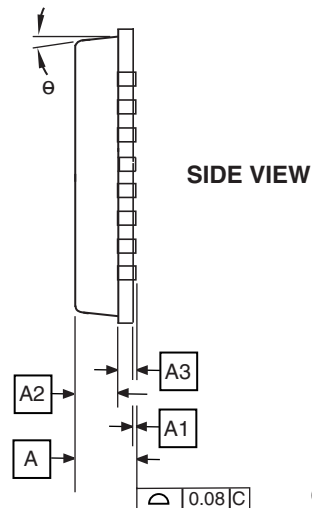
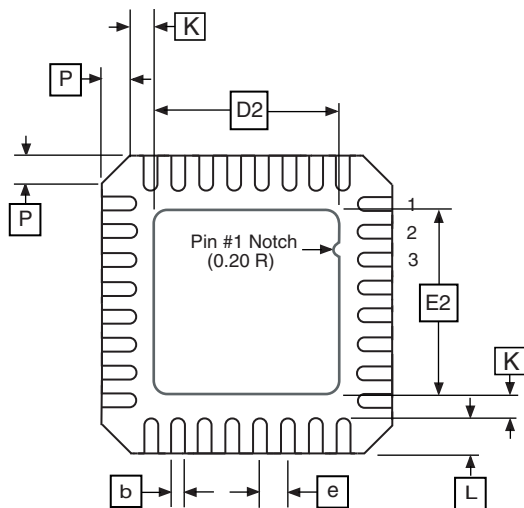
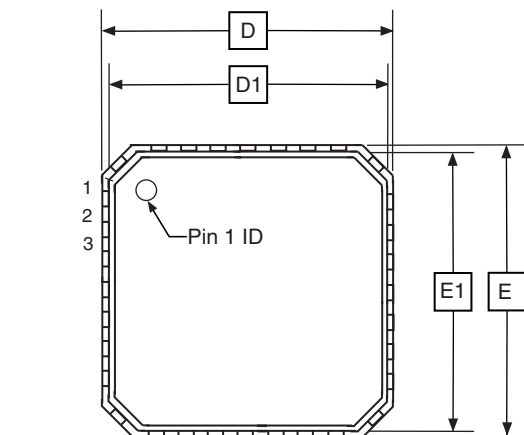
Speed (MHz)	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operational Range
20 <sup>(3)</sup>	1.8 – 5.5V	ATtiny861A-MU ATtiny861A-PU ATtiny861A-SU ATtiny861A-XU	32M1-A 20P3 20S2 20X	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$ , see [Figure 19.3 on page 185](#).

Package Type	
<b>32M1-A</b>	32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF)
<b>20P3</b>	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>20S2</b>	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC)
<b>20X</b>	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline Package (TSSOP)

## 7. Packaging Information

### 7.1 32M1-A



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A2	–	0.65	1.00	
A3	0.20 REF			
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e	0.50 BSC			
L	0.30	0.40	0.50	
P	–	–	0.60	
Θ	–	–	12°	
K	0.20	–	–	

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

5/25/06



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#### TITLE

**32M1-A**, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm,  
3.10 mm Exposed Pad, Micro Lead Frame Package (MLF)

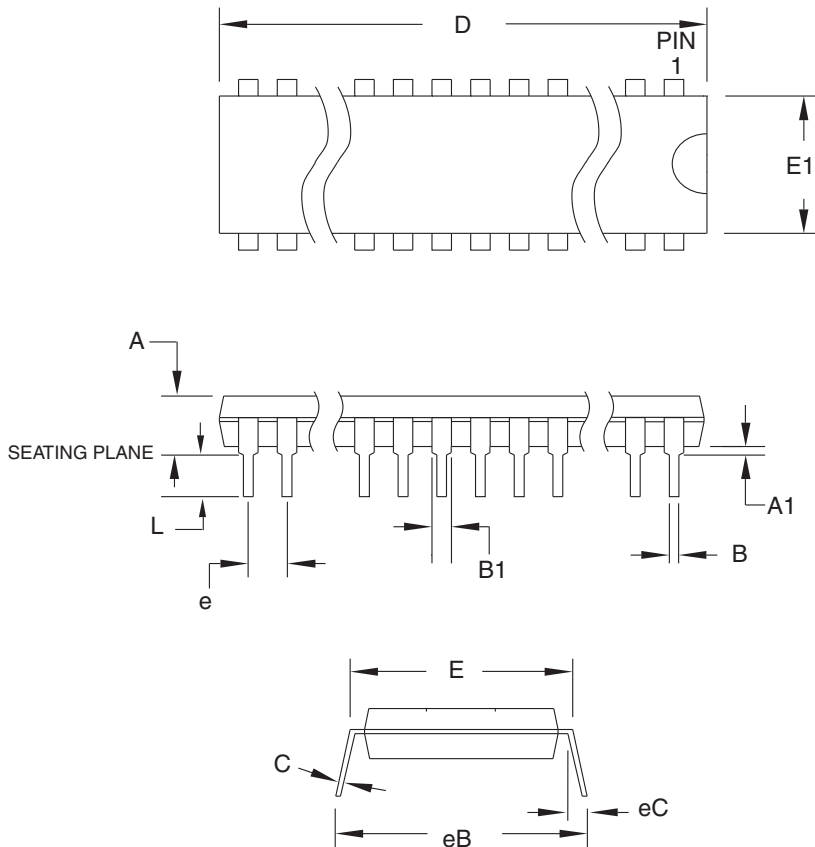
#### DRAWING NO.

32M1-A

#### REV.

E

## 7.2 20P3



- Notes:
1. This package conforms to JEDEC reference MS-001, Variation AD.
  2. Dimensions D and E1 do not include mold Flash or Protrusion.  
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	25.493	–	25.984	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

1/12/04



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### TITLE

**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual  
Inline Package (PDIP)

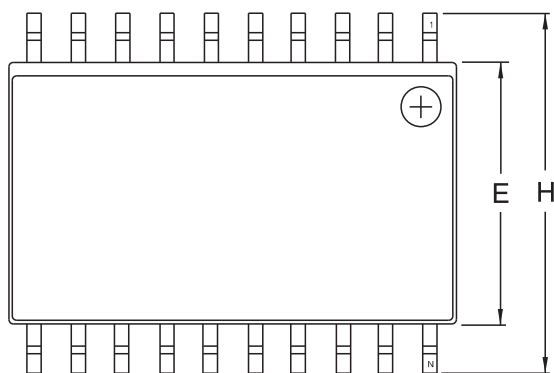
### DRAWING NO.

20P3

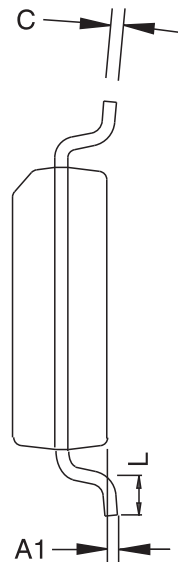
### REV.

C

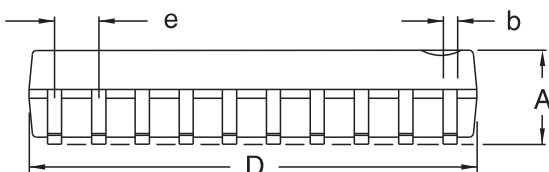
## 7.3 20S2



Top View



End View



Side View

**COMMON DIMENSIONS**  
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

- Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
  2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006") per side.
  3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010") per side.
  4. 'L' is the length of the terminal for soldering to a substrate.
  5. The lead width 'b', as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side.



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**TITLE**

**20S2**, 20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)

**DRAWING NO.**

20S2

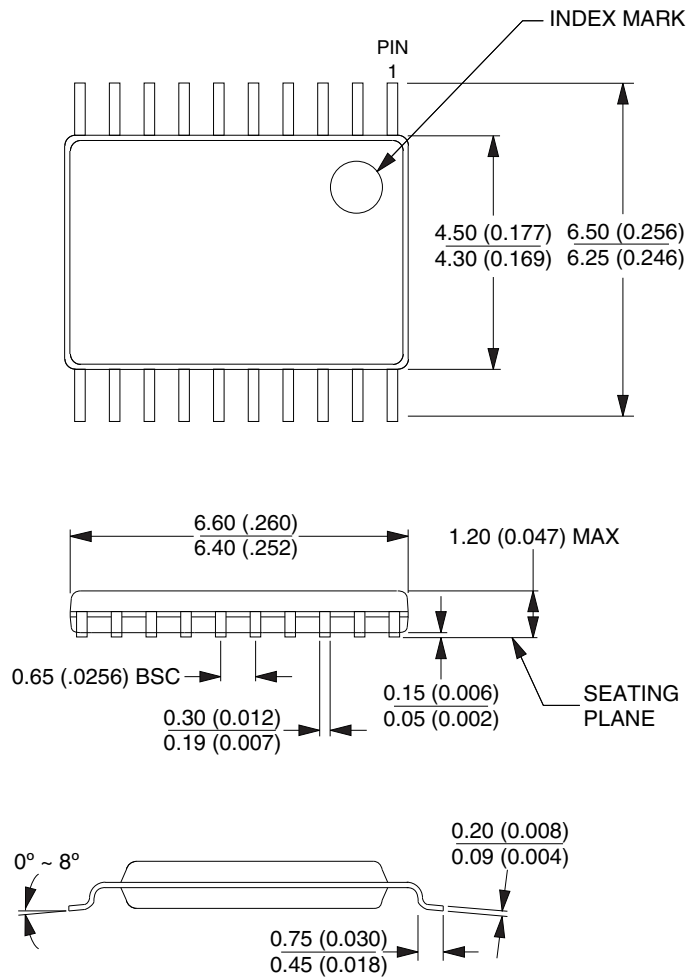
**REV.**

B



## 7.4 20X

Dimensions in Millimeters and (Inches).  
Controlling dimension: Millimeters.  
JEDEC Standard MO-153 AC



10/23/03



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### TITLE

**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width,  
Plastic Thin Shrink Small Outline Package (TSSOP)

### DRAWING NO.

20X

### REV.

C



## 8. Errata

### 8.1 Errata ATtiny261A

The revision letter in this section refers to the revision of the ATtiny261A device.

#### 8.1.1 Rev D

No known errata.

#### 8.1.2 Rev C

Not sampled.

### 8.2 Errata ATtiny461A

The revision letter in this section refers to the revision of the ATtiny461A device.

#### 8.2.1 Rev C

No known errata.

### 8.3 Errata ATtiny861A

The revision letter in this section refers to the revision of the ATtiny861A device.

#### 8.3.1 Rev D

No known errata.

#### 8.3.2 Rev C

Not sampled.

## **9. Datasheet Revision History**

### **9.1 Rev. 8197A – 10/09**

1. Initial revision created from document 2588C (ATtiny261/461/861)
2. Updated "Ordering Information" on [page 11](#), [page 12](#) and [page 13](#). Pb-plated packages are no longer offered and there are no separate ordering codes for commercial operation range, the only available option now is industrial. Also, added new package options
3. Added sections:
  - “Software BOD Disable” on [page 35](#)
  - “ATtiny461A” on [page 221](#)
  - “ATtiny861A” on [page 247](#)
4. Updated sections:
  - “Stack Pointer” on [page 11](#)
  - “OSCCAL – Oscillator Calibration Register” on [page 32](#)
  - “MCUCR – MCU Control Register” on [page 37](#)
  - “MCUCR – MCU Control Register” on [page 50](#)
  - “MCUCR – MCU Control Register” on [page 67](#)
  - “Speed Grades” on [page 185](#)
  - “Enhanced Power-On Reset” on [page 187](#)
  - “ATtiny261A” on [page 195](#)
  - “Register Summary” on [page 7](#)
5. Updated tables:
  - “DC Characteristics.  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 1.8\text{V}$  to  $5.5\text{V}$  (unless otherwise noted).” on [page 184](#)
  - “Additional Current Consumption for the different I/O modules (absolute values).” on [page 193](#)
  - “Additional Current Consumption (percentage) in Active and Idle mode.” on [page 194](#)



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