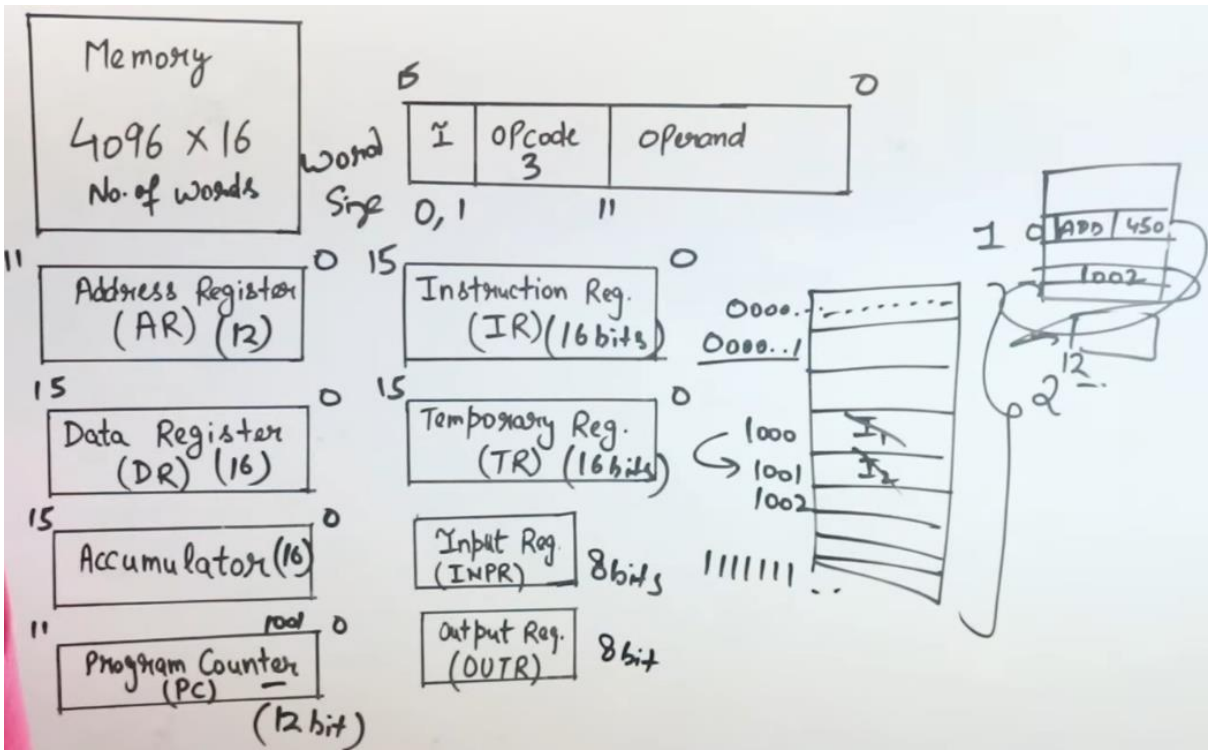
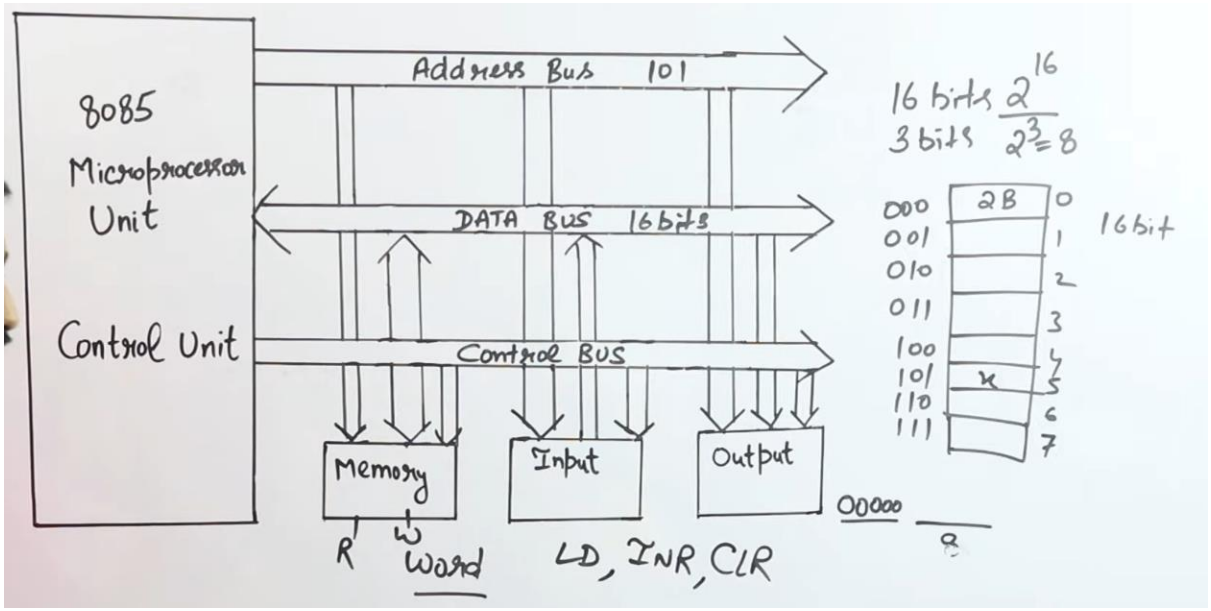
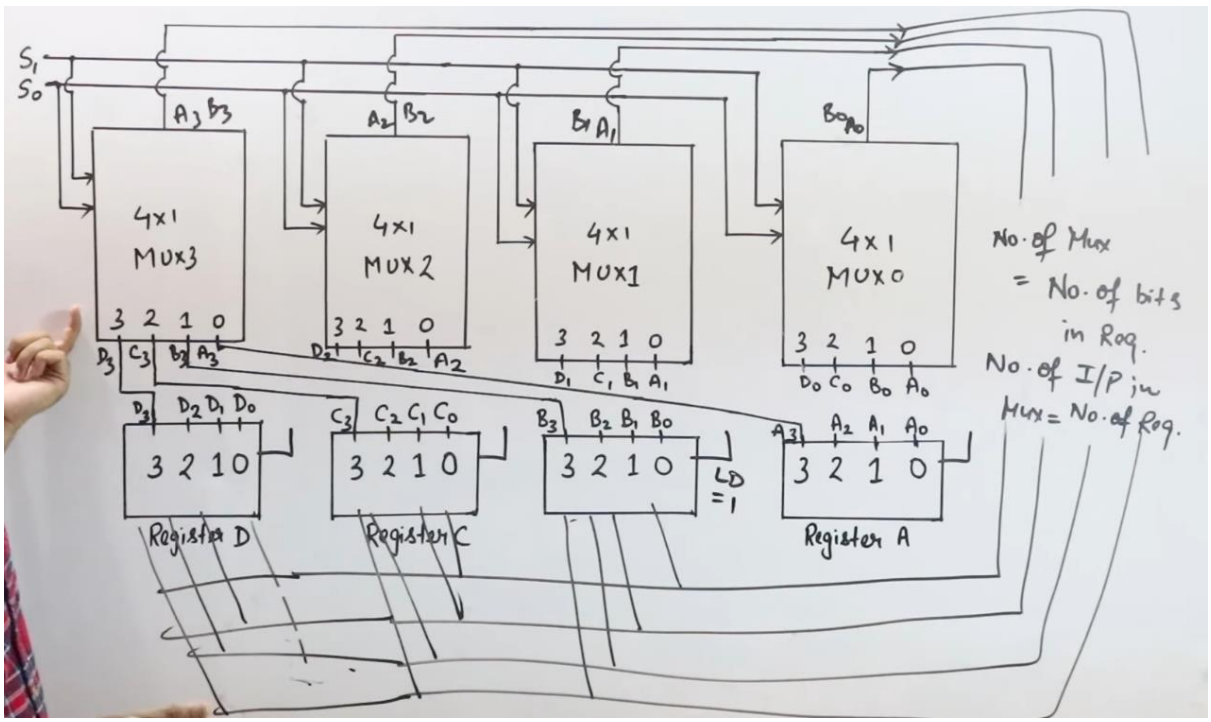
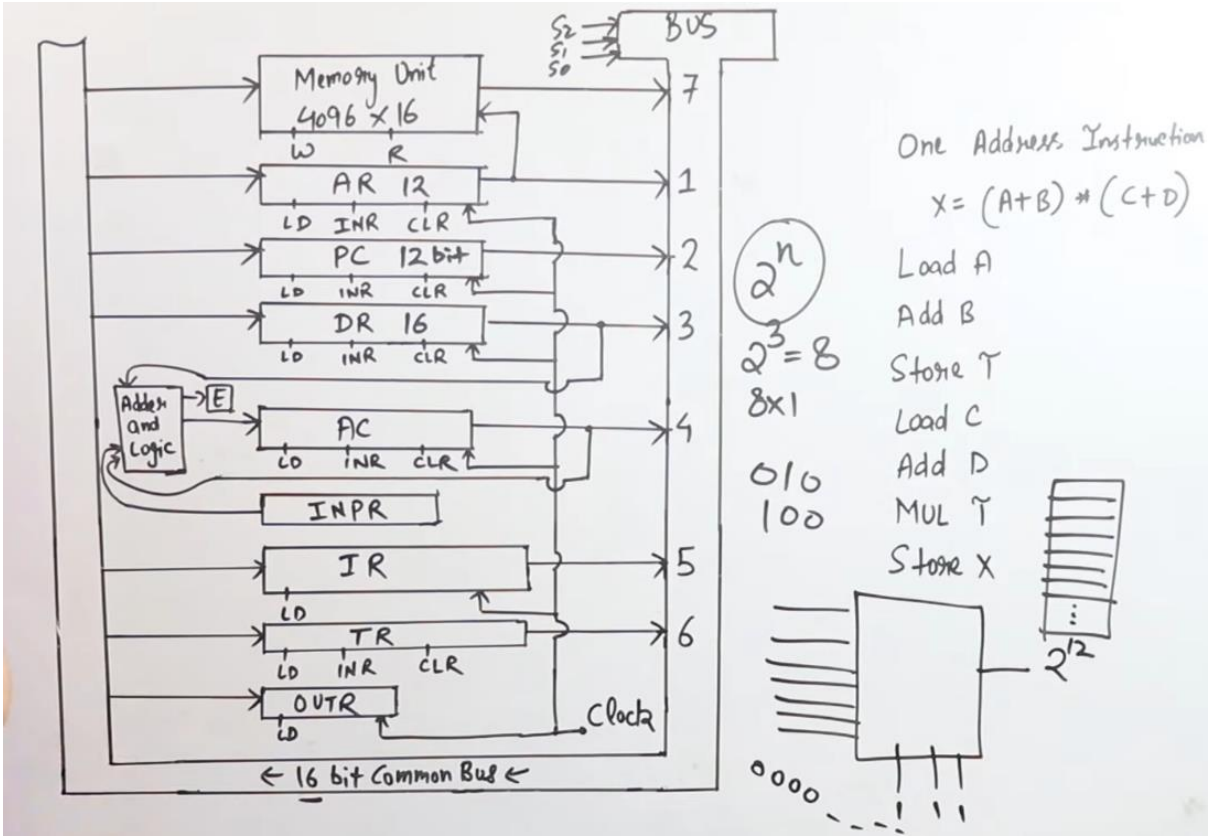
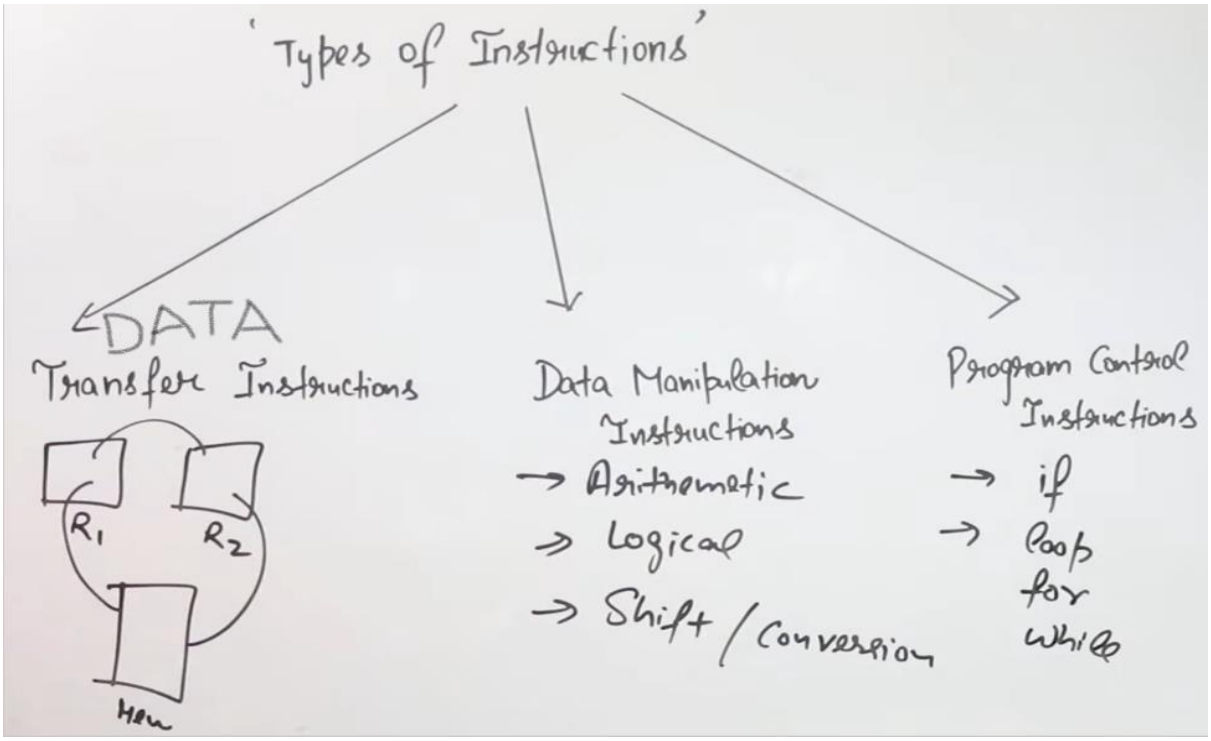
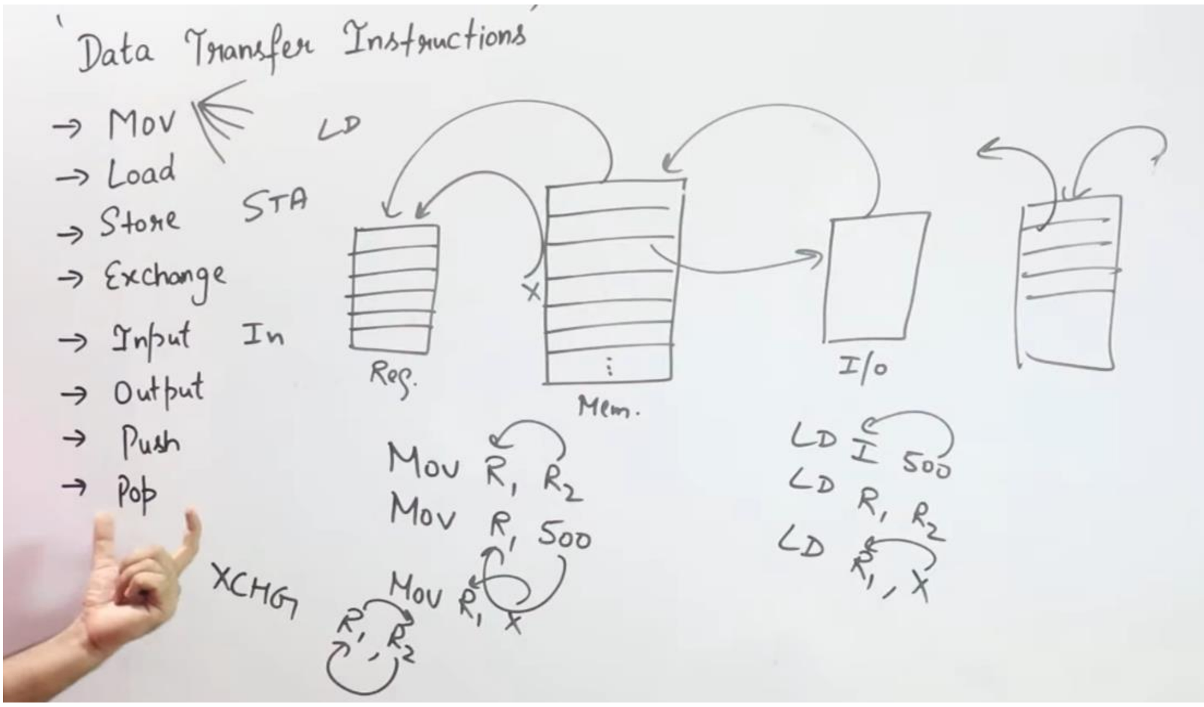

Memory
4096 x 16
No. of words
Word Size
15 0
I
OPcode
3
Operand
0, 1
11
Address Register (AR) (12)
Instruction Reg. (IR) (16 bits)
Data Register (DR) (16)
Temporary Reg. (TR) (16 bits)
Accumulator (16)
Input Reg. (INPR) 8bits
Output Reg. (OUTR) 8bit
Program Counter (PC)
(12 bit)
ADD 450
1002
12
2
0000..0
0000..1
1000
1001
1002
1111111

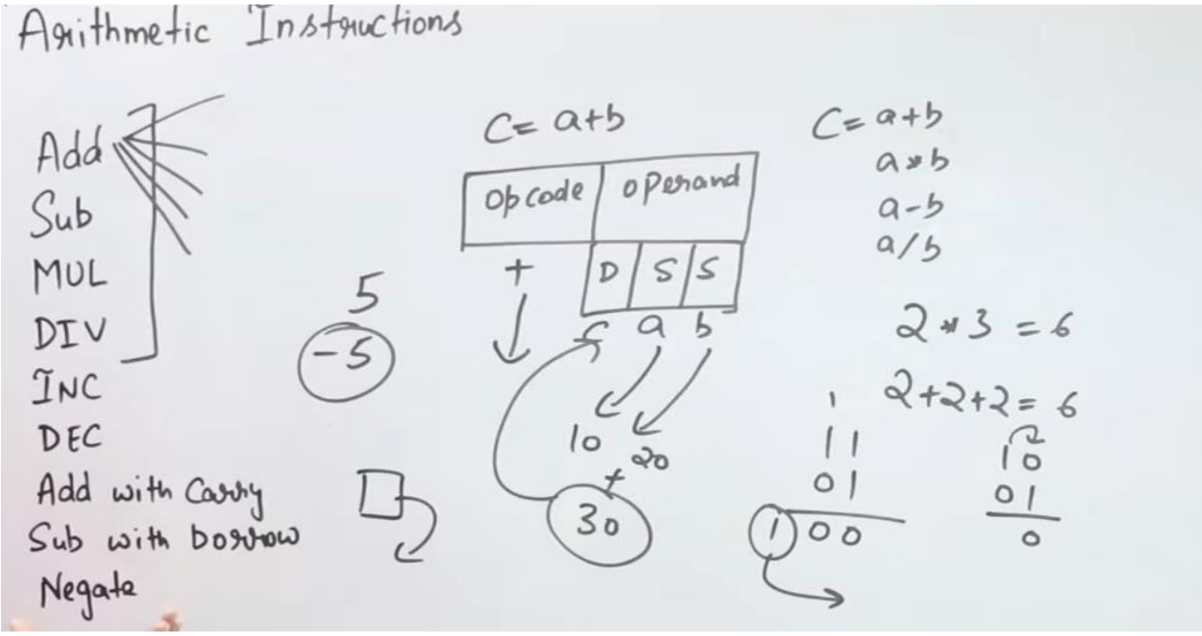

8085
Microprocessor Unit
Control Unit
Address Bus 101
DATA BUS 16 bits
Control BUS
Memory
Input
Output
R
W
Word
LD, INR, CLR
16 bits 2^16
3 bits 2^3 = 8
000
001
010
011
100
101
110
111
2B
16 bit
00000

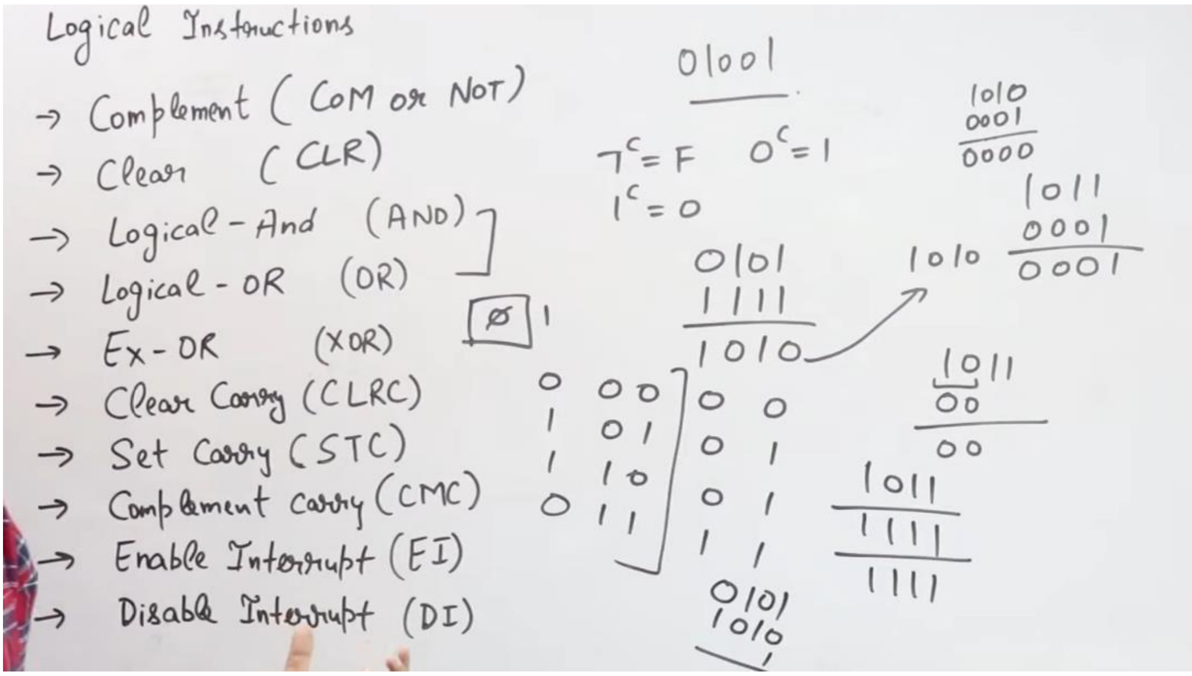

S1
S0
4x1 MUX3
4x1 MUX2
4x1 MUX1
4x1 MUX0
3 2 1 0
Register D
Register C
Register B
Register A
LD = 1
No. of Mux = No. of bits in Reg.
No. of I/P in Mux = No. of Reg.


S2
S1
S0
BUS
Memory Unit
4096 x 16
W
R
AR 12
LD INR CLR
PC 12 bit
LD INR CLR
DR 16
LD INR CLR
Adder and Logic
E
AC
LD INR CLR
INPR
IR
LD
TR
LD INR CLR
OUTR
LD
Clock
16 bit Common Bus
7
1
2
3
4
5
6
One Address Instruction
X = (A+B) * (C+D)
Load A
Add B
Store T
Load C
Add D
MUL T
Store X
2^n
$2^3 = 8$
8x1
010
100
2^{12}
0000


'Types of Instructions'
DATA
Transfer Instructions
R1
R2
Mem
Data Manipulation
Instructions
→ Arithmetic
→ Logical
→ Shift / Conversion
Program Control
Instructions
→ if
→ Loop
for
while

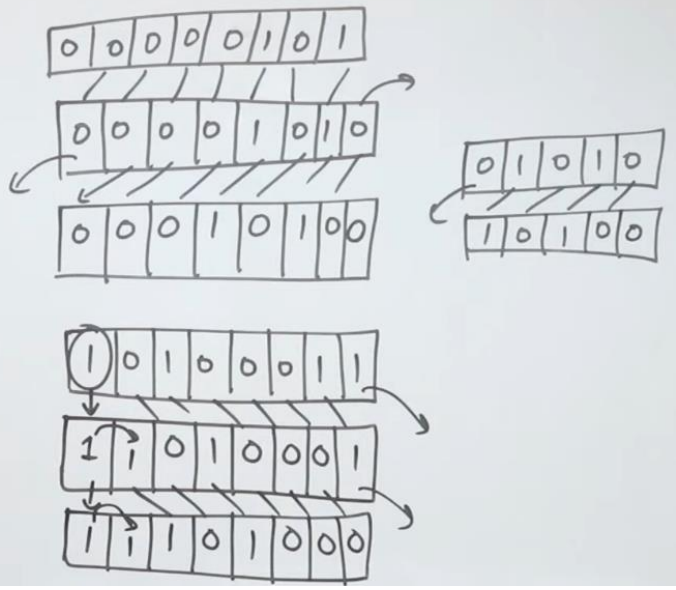

Data Transfer Instructions
→ Mov
→ Load
→ Store
→ Exchange
→ Input
→ Output
→ Push
→ Pop
LD
STA
In
XCHG
Reg.
Mem.
I/O
Mov R1, R2
Mov R1, 500
Mov R1, X
LD I 500
LD R1, R2
LD R1, X


Arithmetic Instructions
Add
Sub
MUL
DIV
INC
DEC
Add with Carry
Sub with Borrow
Negate
5
-5
C = a+b
Op code
operand
+
D
S
S
c a b
10
20
30
C = a+b
a*b
a-b
a/b
2*3 = 6
2+2+2 = 6
11
01
100
10
01
0

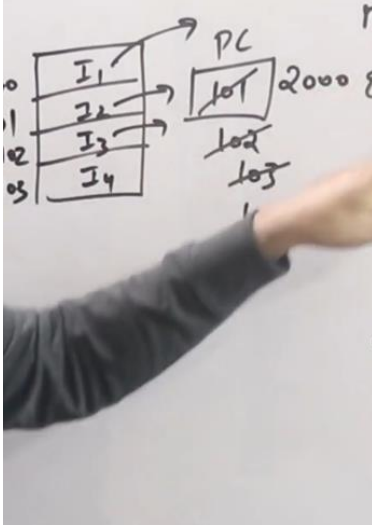

Logical Instructions
→ Complement (COM or NOT)
→ Clear (CLR)
→ Logical - And (AND)
→ Logical - OR (OR)
→ Ex-OR (XOR)
→ Clear Carry (CLRC)
→ Set Carry (STC)
→ Complement carry (CMC)
→ Enable Interrupt (EI)
→ Disable Interrupt (DI)
01001
7^c = F
0^c = 1
1^c = 0
1010
0001
0000
1011
0001
0001
0101
1111
1010
1010
1011
00
00
1011
1111
1111
0101
1010

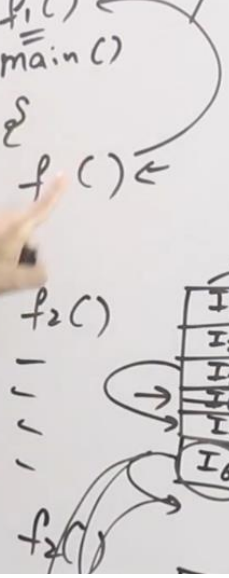
Shift Instructions

- Logical shift left
- Logical shift right
- → Arithmetic shift right
- → Arithmetic shift left
- → Rotate right
- → Rotate Left
- → Rotate right through carry
- → Rotate Left through Carry



Program Control Instructions





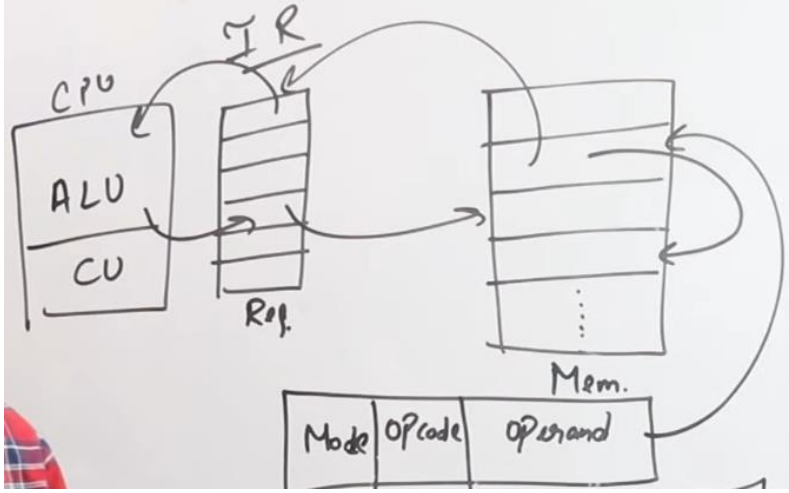
Transfer of Control Instructions

Branch. → Uncond
→ Cond

- Jmp 2000
- B 3000
- Skip Skp
- Call 3000
- Return

BE R1, R2 2000
R1 = R2
R1 ≠ R2
BNZ R1, 2000
R1 = 0

Instruction Format



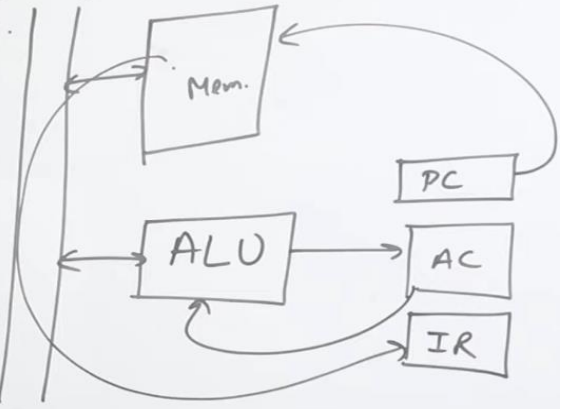

```
main()
{
int a=10;   Data
int b=20;
int c;
c=a+b;      instr.
Pf(c)       instr
}
```

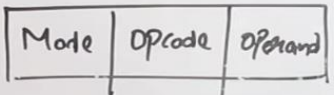
Types of CPU organisations

1) Single Accumulator org.
2) General Register org.
3) Stack organisation

$X = A + B$

Single Address inst.



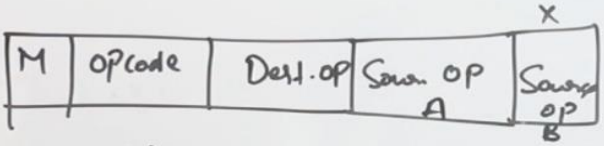


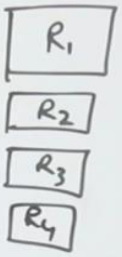
LD A (A)
ADD (B)
Store X ← AC

AC ← AC + B

Types of CPU organisations

1) Single Accumulator org. — 1 Add.
2) General Register org. — 2 add, 3 add
3) Stack organisation





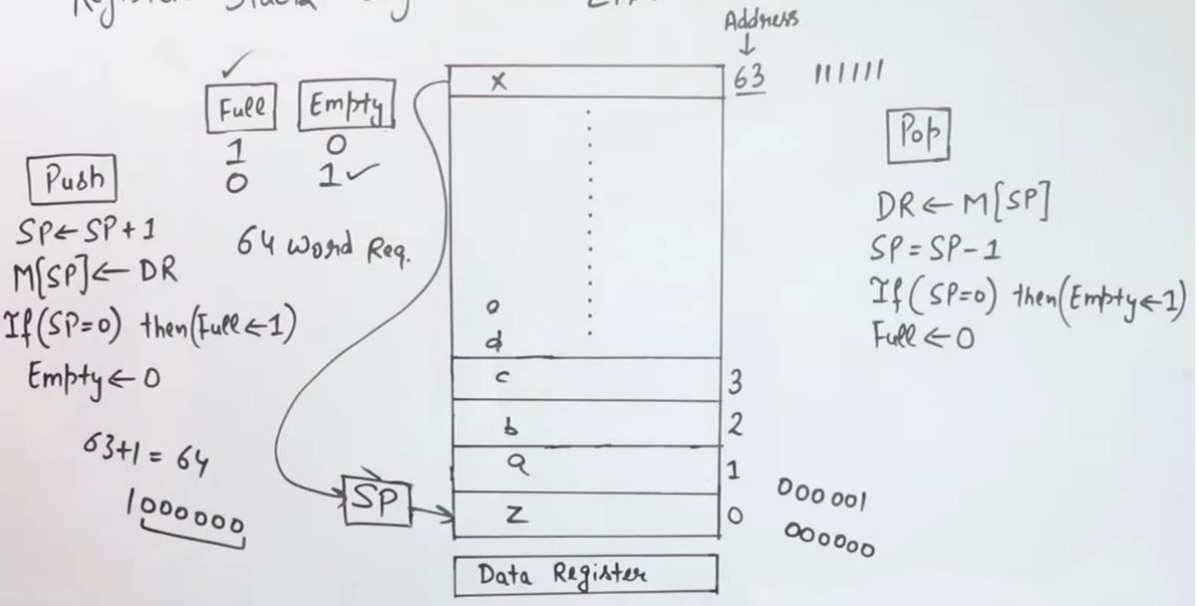
$X = (A+B) * (C+D)$

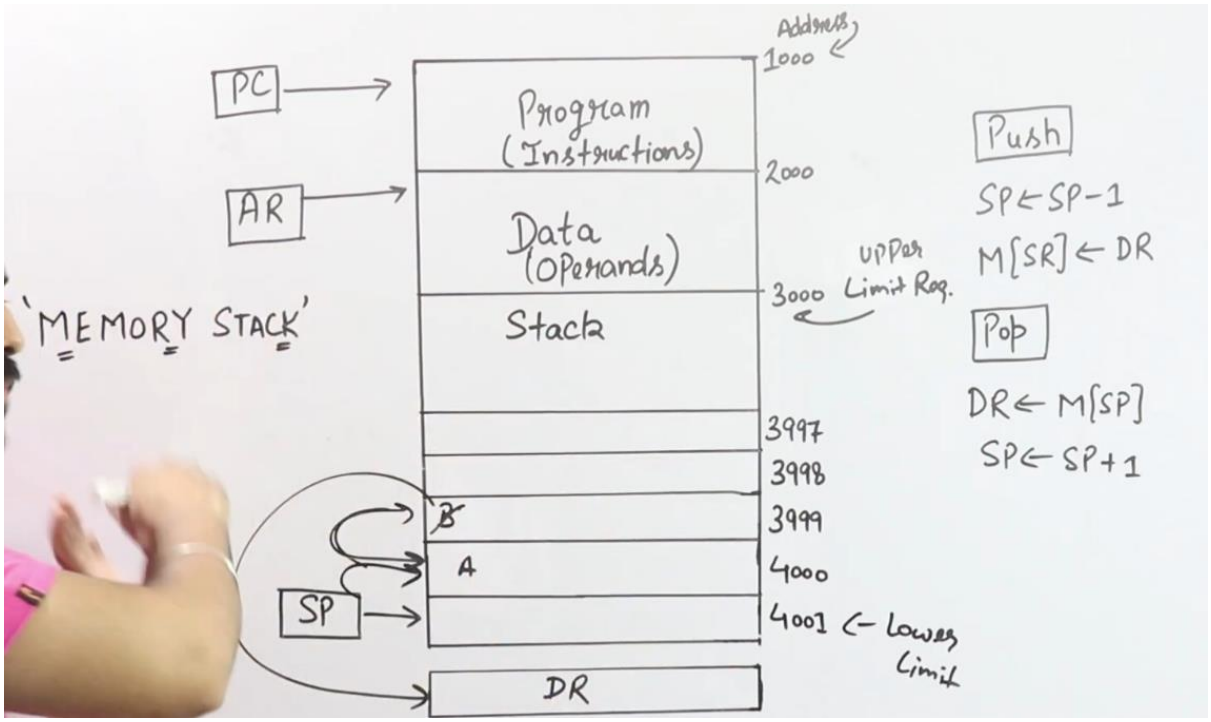
Mov R_1 A
Add R_1 B — $R_1 \leftarrow R_1 + B$
Mov R_2 C
Add R_2 D — $R_2 \leftarrow R_2 + D$
MUL R_1 R_2 — $R_1 \leftarrow R_1 * R_2$

Add R_1 A,B
Add R_2 , C,D
MUL X, R_1, R_2

$R_1 \leftarrow (A)+(B)$
$R_2 \leftarrow (C+D)$
$M[X] \leftarrow R_1 * R_2$

Register Stack organisation LIFO





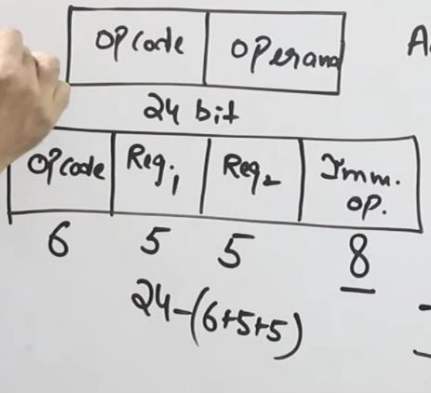
A machine has 24 bit instruction format. It has 32 registers and each of which is 32 bit long. It needs to support 49 instructions. Each instruction has two register operands and one immediate operand. If the immediate operand is signed integer the minimum value of immediate operand is ____.

A) -64

B) -128

C) -256

d) -32



Add R_1 R_2 50

$2^5 = 32$

$2^6 = 64$

0-255

256

-128 to 127