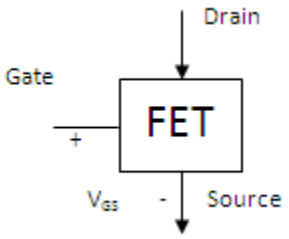
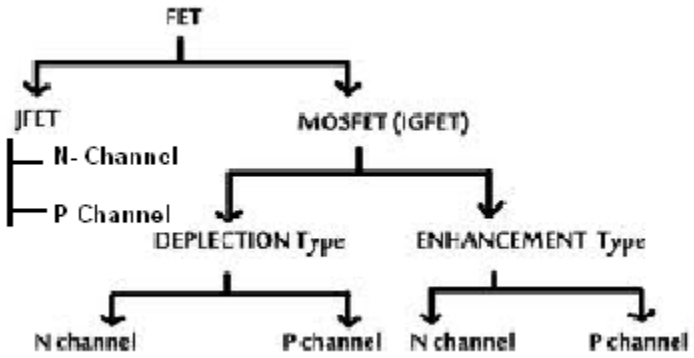
Field Effect Transistor: Construction and Characteristic of JFETs. Transfer Characteristic. CS,CD,CG amplifier and analysis of CS amplifier
MOSFET (Depletion and Enhancement) Type, Transfer Characteristic,

FET(Field Effect Transistor)

Field Effect Transistor (FET) is a **voltage controlled device**. i.e. the output characteristics of this device are controlled by the input voltage and not by the input current.

FET is **unipolar** device. i.e. the operation of FET depends upon the flow of majority carriers only. For the FET, an electric field is established by the charges present that will control the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.





JFET (Junction Field Effect Transistor)-JFET is a three terminal device with one terminal capable of controlling the current between the other two.

There are two types of JFET

1- N-channel JFET 2- P-Channel JFET

N-channel JFET- It consists of an N-type semiconductor substrate with P-type heavily doped regions diffused on opposite sides of its middle part. The space between the junctions is called a channel. The top of the N-type channel is connected through an ohmic contact to a terminal referred to as the Drain(D), while lower end of the same material is connected through an ohmic contact to a terminal referred to as the source(S). The Two P-type materials are connected together and to the gate (G) terminal. In the absence of any applied potentials the JFET has two P-N junctions under No-Bias Conditions.

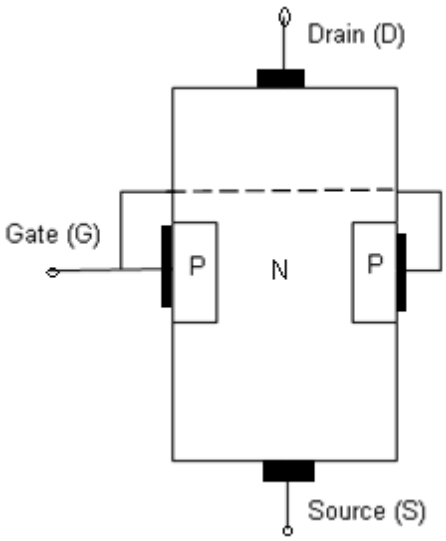


Fig:**N-Channel**

JFET Volt-Ampere (V-I) Characteristics

There are two types of JFET Characteristics

1- Drain Characteristics 2- Transfer Characteristics

Drain Characteristics-

- **Case-1 -** When V_{GS}**= 0 V** and V_{DS}**= 0 V**.In this condition the drain current is zero.
- **Case-2 -** When V_{GS} **=0 V** and V_{DS} **> 0 V**. i.e. some positive value.

The gate and source are connected directly i.e. V_{GS} = 0 V. In this situation $I_D = I_S$ (i.e. $V_{DS} = V_{DD}$).

Under this condition the flow of charge is relatively uninhabited and limited only by resistance of the N-Channel between drain and source.

Depletion region is wider near the drain side as compared to source side because when current lows in silicon bar, there occurs a voltage drop across the channel along whole length due to this bias voltage.

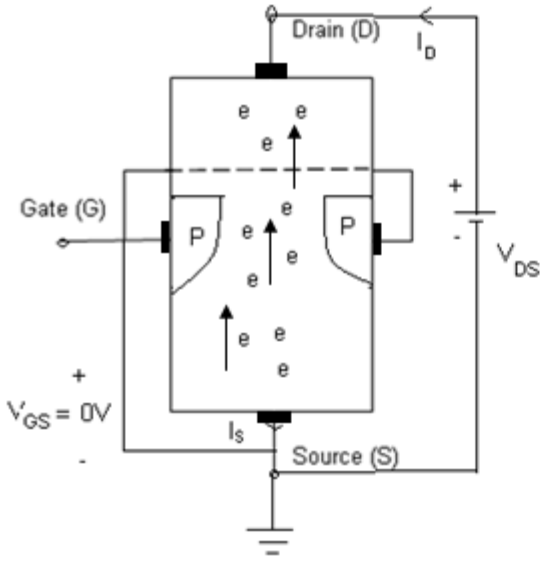


Fig: **Working of N-channel**

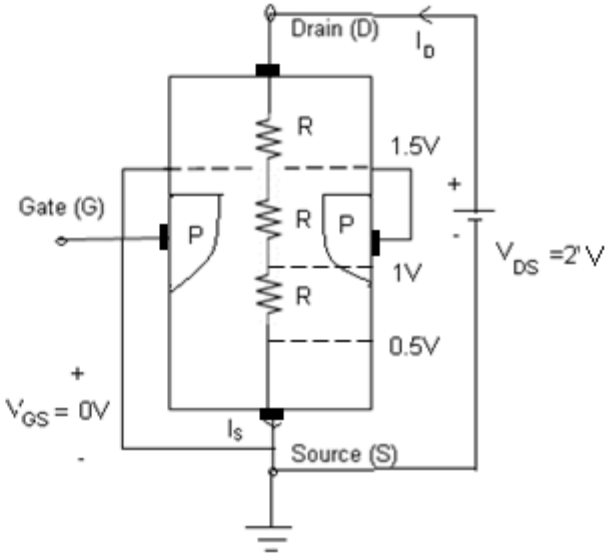


Fig: **Non-Uniform Distribution of Depletion Layer**

Pinch-Off- If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" , this condition referred to as " **pinch-off** " will result. The drain to source voltage (V_{DS}) at which the channel pinch off occurs, is known as **pinch-off voltage (V_P).**

I_{DSS}- I_{DSS} is the maximum drain current for a JFET and is defined by the conditions **V_{GS}=0 V and V_{DS}> |V_P|.**

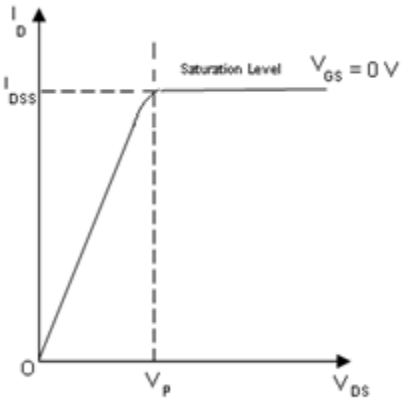
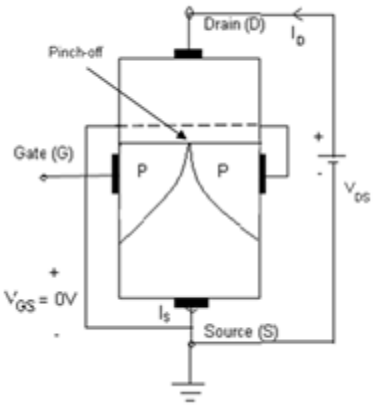
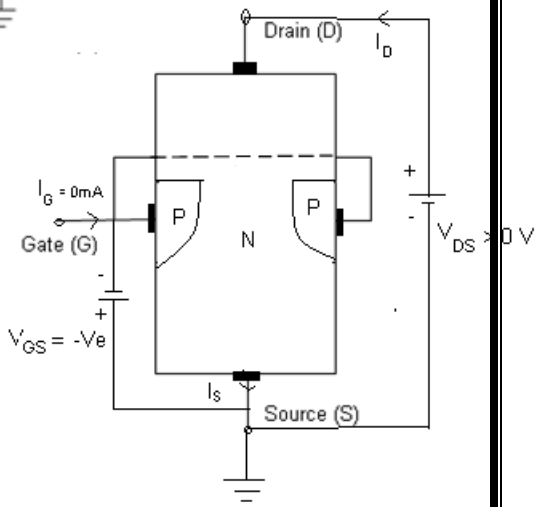


Fig: **Drain Characteristics when V_{GS} = 0V**

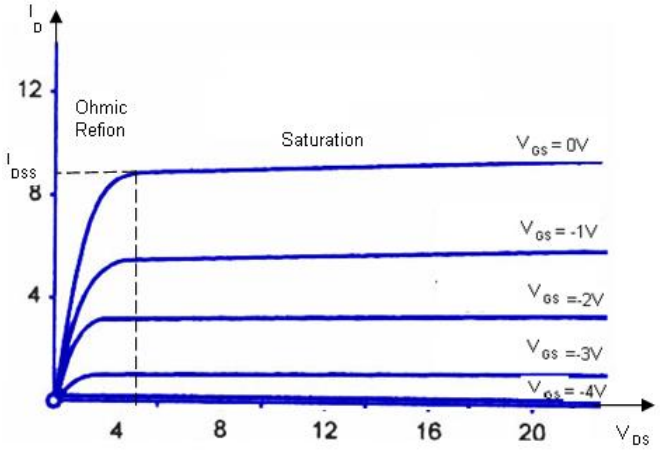


- **Case -3 –** When **V_{GS}< 0 V** and **V_{DS}>0.**

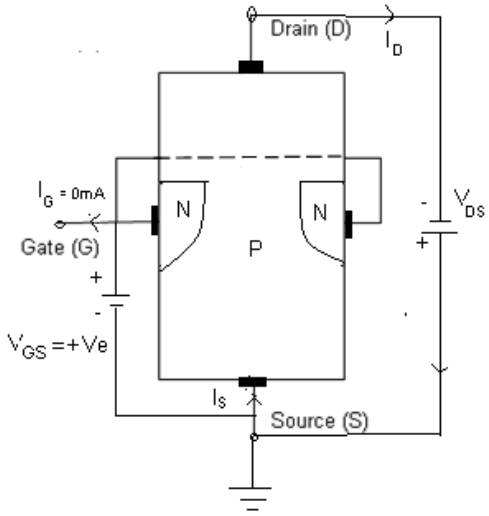
Under this condition P-N Junction being reverse biased and increase the width of the depletion layer. Now, If V_{GS} is increased more negatively then the situation of pinch-off occurs. At this instant, I_{Dmax} also decreases because channel becomes narrower due to reverse bias.

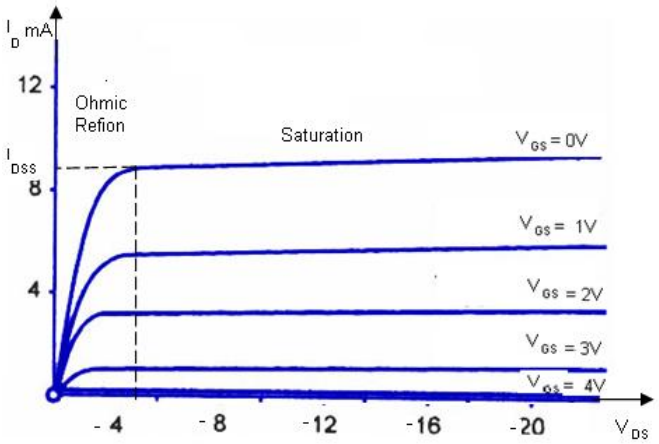


When **V_{GS}= -V_P then I_D= 0 mA.** → Device is turned-off.
The Level of V_{GS} that results in I_D= 0mA is defined by V_{GS}=V_P with V_P being a negative voltage for N-channel devices and a positive voltage for P-Channel JFETs.

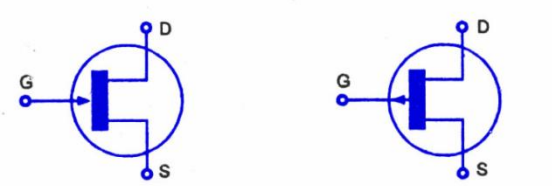


P-Channel Drain & Transfer Charcteristics





Symbols



N-Channel JFET *P-Channel JFET*

Schematic Symbols For JFETs

Note:

I_G= 0 is the important characteristics of JFET .The drain current I_D depends upon following factors-

- No. of majority carriers.
- Length of the channel.
- Cross- sectional area of the channel.

Transfer Characteristics- Following equation governs the transfer characteristics of JFET

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{VP}\right]^2$$

I_D= Drain current

I_{DSS}= saturation (max value) of drain current at V_{GS}= 0 V

V_{GS}= Gate to Source Voltage

V_P= Pinch-off voltage

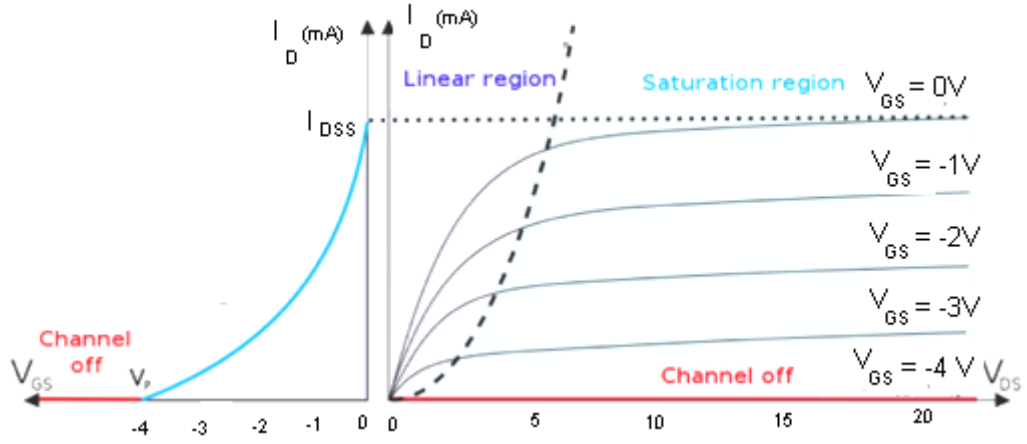


Fig: **Transfer Characteristics of N-channel JFET**

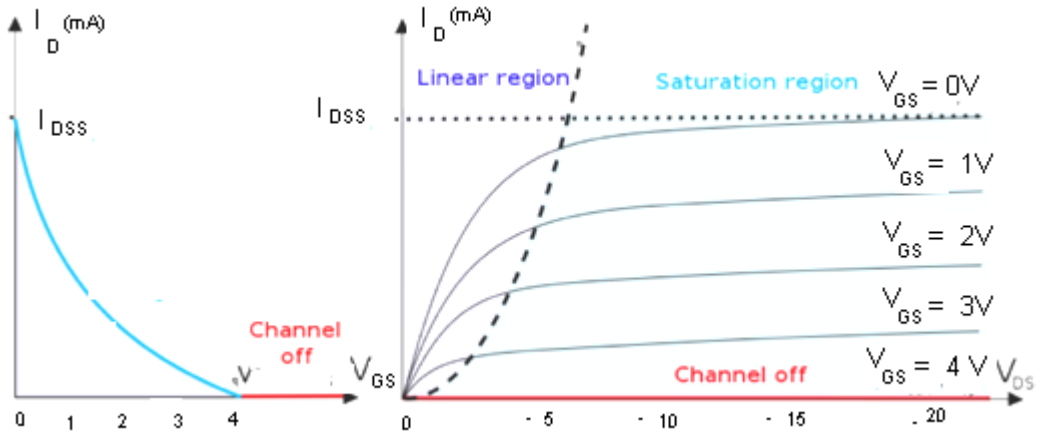


Fig: **Transfer Characteristics of P-channel JFET**

Important points regarding drain characteristics of N-channel JFET.

- Drain current is maximum when V_{GS} = 0 V i.e. $I_D = I_{DSS}$ and $V_{DS} \geq |V_P|$.
- In FET, generally avalanche breakdown occurs.
- V_P is a particular value of V_{GS} with either positive or negative sign dependaing upon the type of the FET. i.e. whether it is P-Channel or N-Channel.

  For P-Channel V_P is positive.

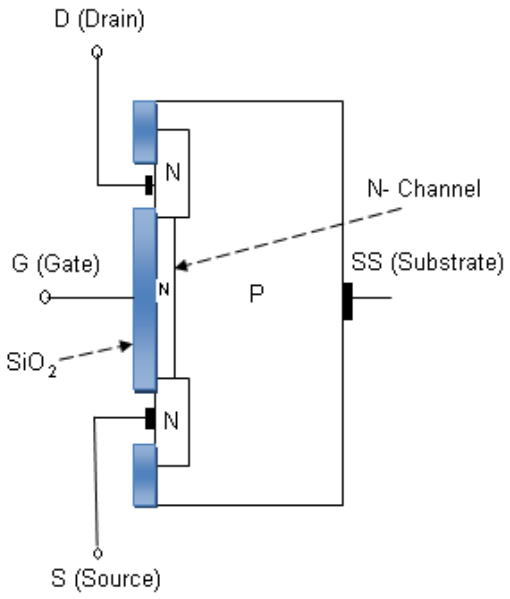
  For N-Channel V_P is negative.

- For gate to source voltages V_{GS} less than (more negative than) the pinch-off level, the drain current is OA (I_D = 0A).

V_{GS}	I_D
0 V	I_{DSS}
0.3 V_P	$I_{DSS}/2$
0.5 V_P	$I_{DSS}/4$
V_P	0 mA

MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

1- Depletion Type MOSFET

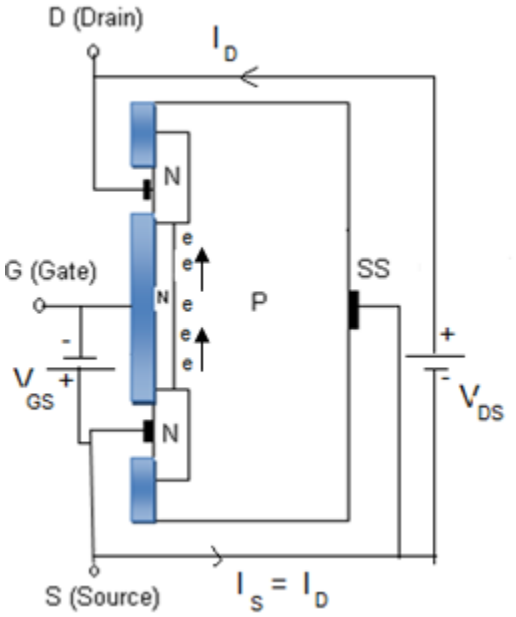


N-Channel- A slab of P-Type material is formed from a silicon base and is referred to as the substrate. The source (S) and drain (D) terminals are connected through metallic contacts to N-doped regions linked by an N-channel. The Gate is also connected to a metal contact surface but remains insulated from the N-Channel by a thin silicon dioxide (SiO_2) layer.

This SiO_2 layer acts as a dielectric that sets up opposing electric fields within the dielectric when exposed to an externally applied field.

"There is no direct electrical connection between the gate terminal & the channel of a MOSFET"
" It is the insulating layer of SiO_2 in the MOSFET concentration that accounts for very desirable high input impedance of the device".

Working



- **Case-1- V_{GS} = 0 V** and **V_{DS} > 0** → the result is an attraction for the positive potential at the drain by the free electrons of the N-channel and a current similar to that established through the channel of the JFET.
- **Case-2- V_{GS} = -ve** and **V_{DS} > 0** → In this case, electrons move towards P-type substrate & attracts holes from P-type substrate.

Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the N-channel available for conduction. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}.

- **Case-3- V_{GS} = +ve** and **V_{DS} > 0** → For +ve value of V_{GS} , the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and established new carriers through the collisions resulting between accelerating particles.

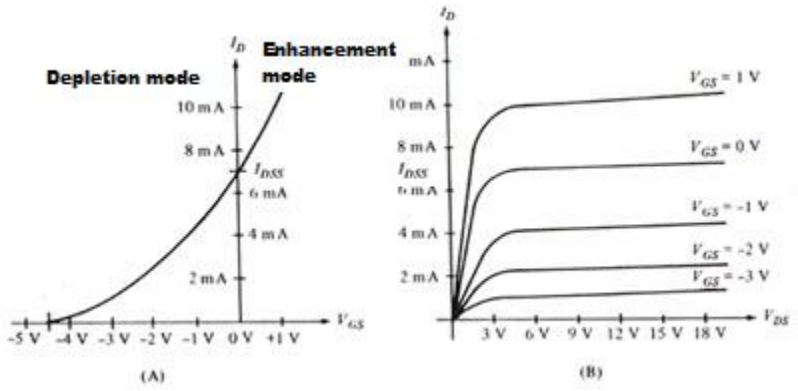
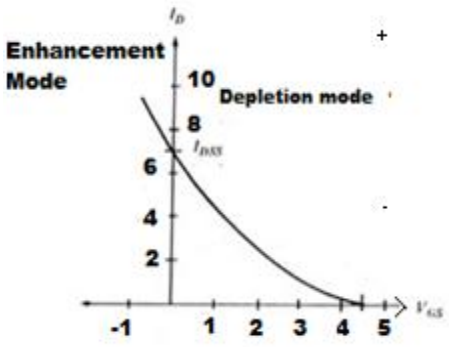


Fig: **Drain & Transfer Characteristics of N-Channel Depletion type MOSFT**

P-Channel Depletion Type MOSFET



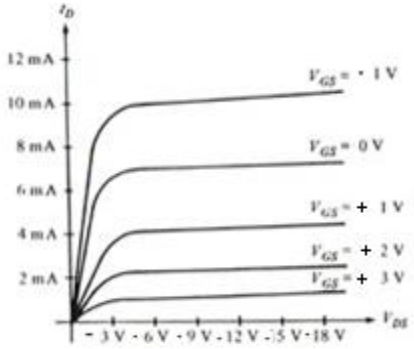


Fig: Drain & Transfer Characteristics of P-Channel Depletion type MOSFT

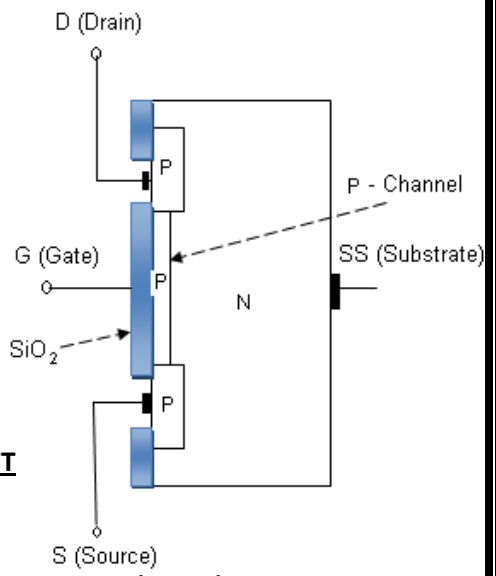
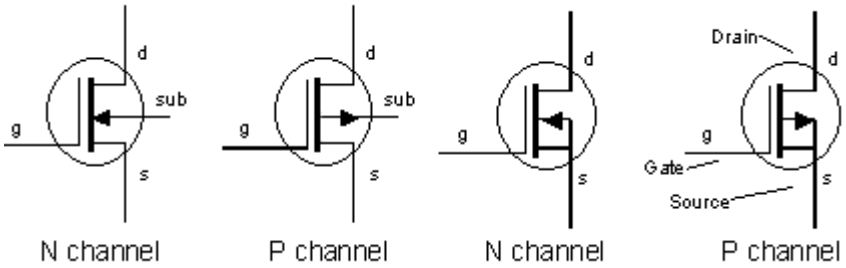
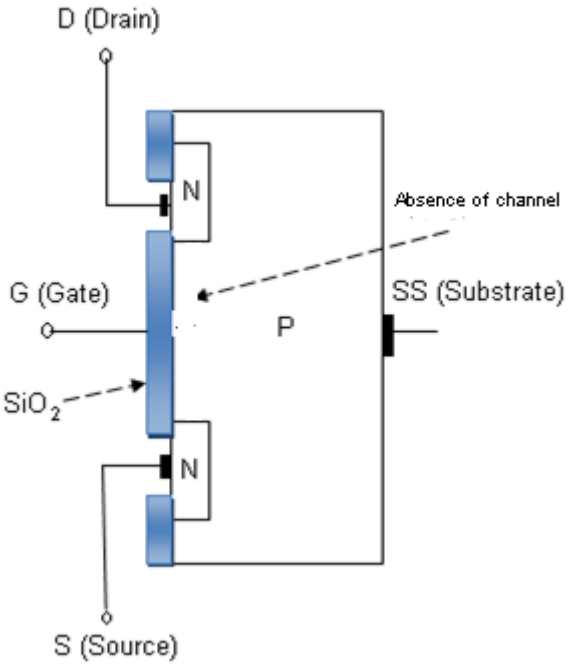


Fig: **P-Channel D- MOSFET**

Symbol: Depletion (D) Type MOSFET



2- Enhancement type MOSFET



N-Channel- the N-channel enhancement type MOSFET consists of a lightly doped P-type substrate into which two highly doped N-regions are diffused. The absence of a channel between the two N-doped region.

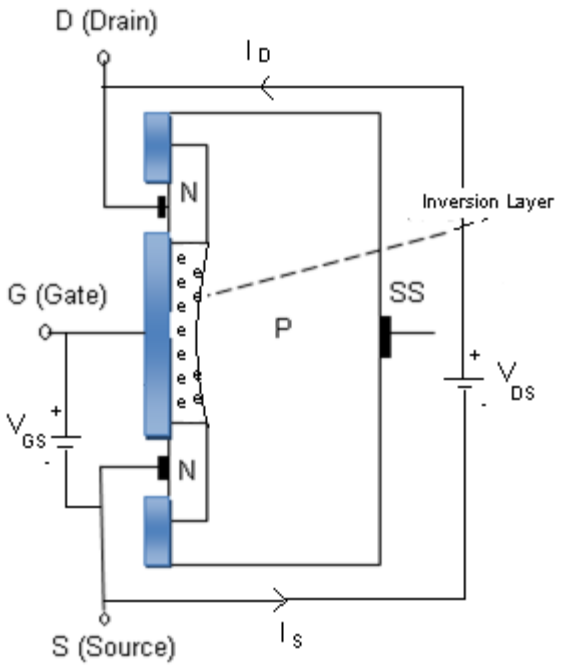
Case-1- V_{GS}= 0 V → If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device, the absence of an N-channel will result in a current (I_D) effectively 0 A.

Case-2- When both V_{GS} > 0 V and V_{DS}> 0 V → when both V_{GS} and V_{DS} have been set at positive voltage greater than 0V., establishing the drain and gate at a positive potential with respect to the source.

As the positive potential is applied between gate & source due to the presence of SiO_2 layer which acts as a dielectric, is attracts the charge carriers (electrons) from substrate.

As V_{GS} increases in magnitude the concentration of electrons near the SiO_2 surface increases until eventually the induced N-type region can support a measurable flow between drain & source, resulting the formation of inversion layer, this inversion layer. This inversion layer is formed when a certain gate to source voltage (V_{GS}) is applied. Thus, the minimum value of gate voltage at which inversion of semiconductor surface takes place is known as threshold voltage (V_T).

Since the channel is no-existent with V_{GS}= 0V and "enhanced" by the application of a positive gate to source voltage. This type of MOSFET is called Enhancement type MOSFET.



Drain and Transfer characteristics of N-Channel Enhancement type MOSFET.

r levels of $V_{GS} > V_T$ the drain current is related to the applied gate to source voltage by the following non-relationship.

$$I_D = K (V_{GS} - V_T)^2$$

Where V_{GS} =applied gate to source voltage
V_T = Threshold Voltage
I_D = Drain Current
K = Constant

The values of K can be determined from the following equation. I_D(on) & V_{GS} (on) are the values for each at a particular part on the characteristics of the device.

$$K = \frac{ID(on)}{(VGS(on) - VT)^2}$$

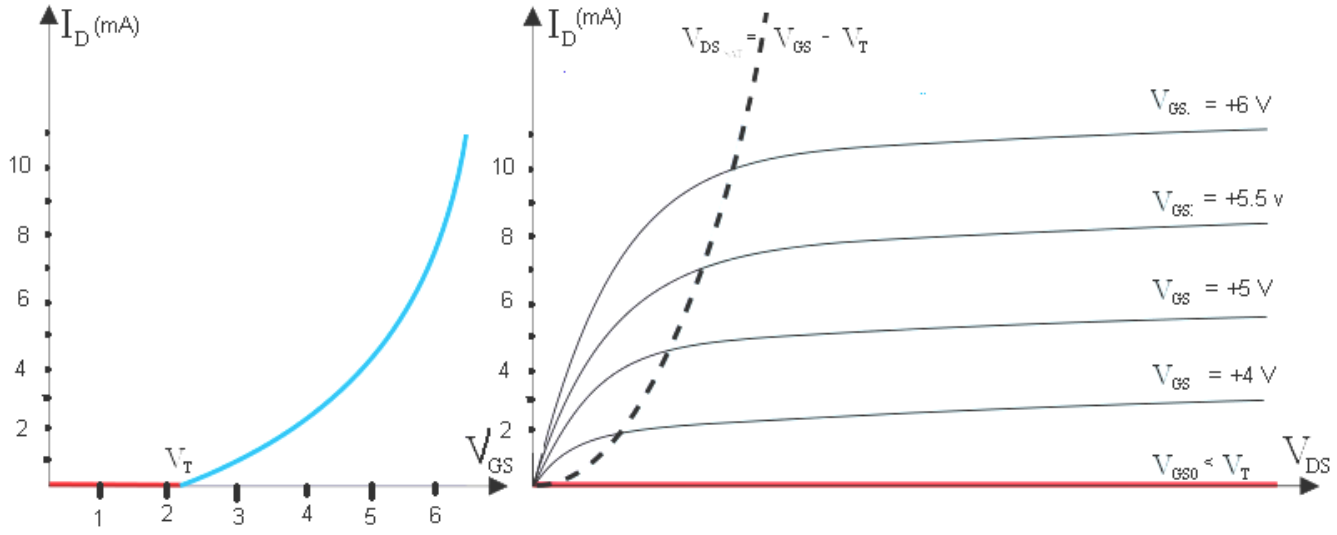
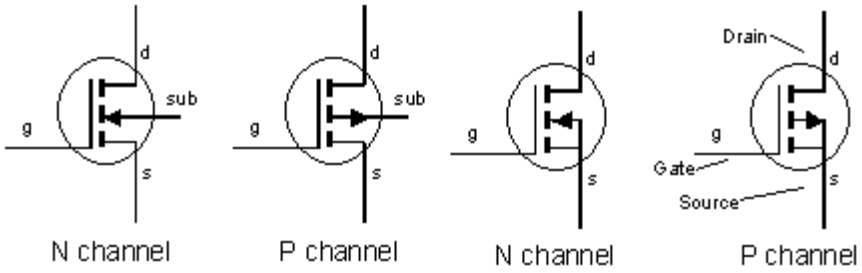


Fig: **Drain and Transfer characteristics of N-Channel Enhancement type MOSFET**

Symbols: Enhancement Type MOSFET



Important Points for FET Biasing

- $I_G \approx 0$ mA.
- $I_D = I_S$
- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{VP}\right]^2$ **For JFETs and Depletion Type MOSFET**
- $I_D = K (V_{GS} - V_T)^2$ **For Enhancement Type MOSFET**