Design and Automation Methodology of a Wideband, High-PSRR LDO using Device Look-up Tables

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***Abstract*—This work presents a Look-up Table (LuT)-based methodology for designing wideband, high Power Supply Rejection Ratio (PSRR) Low Dropout Regulators (LDOs). The proposed methodology has been automated using a Python script to produce optimal sizes for all LDO transistors. A high-PSRR LDO has been designed in 180-nm CMOS technology utilizing this methodology and its automation script. The LDO achieves a DC-PSRR of -60 dB, with a worst-case PSRR of -36 dB across frequencies and load currents. Across the stability performance metrics, an error percentage of less than 2.5% is achieved between calculated and simulated values. Therefore, this approach addresses the limitations of the traditional MOSFET square-law model while retaining analytical insights and design intuition, reducing design iterations and shortening the overall design cycle.**

***Index Terms*—Look-up Table (LuT) methodology, LDO, Linear Regulators, wideband power supply rejection, CMOS design, Python script, PSRR, analog-design automation, gm/Id**

I. Introduction

Using MOSFET square law for designing analog circuits can lead to significant differences between theoretical design calculations and simulated circuit behavior. This difference is more pronounced at sub-90-nm nodes and for low overdrive voltages. The gm/Id methodology [1], also known as the look-up table (LuT)-based design approach, offers a robust solution to size transistors for the given MOS Figures of merit, namely gm/Id, Id/W, ft and gmro, as it relies on the actual device characterization data [2]. However, different analog circuit blocks with various performance metrics require different LuT-based design flows [3]. Furthermore, the vast data set available with technology characterization can add complexity to LuT-based methods and demand automation incorporated into the overall design flow.

This work demonstrates a design and automation methodology for wideband high PSRR LDOs using technology LuTs. The proposed workflow follows two steps: In step 1, algorithms 1 and 2 take the design specification and derive the MOS FOMs. In step 2, these FOM values and technology LuTs are fed to the automation script, which automates the entire design flow to obtain optimum sizes for all transistors. Following this performance-specific design and automation flow, a strong correlation between circuit-design calculations and simulation results is achieved.

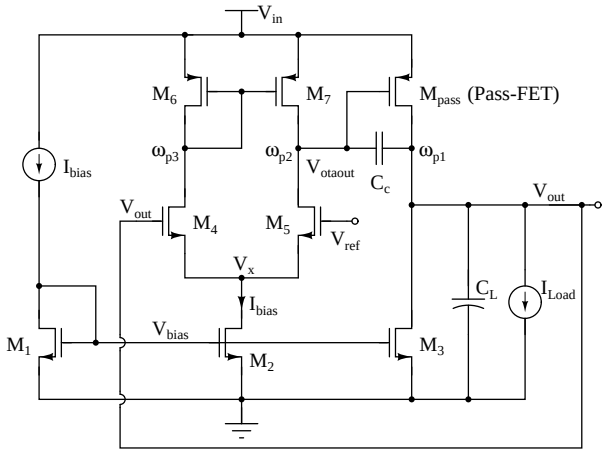


Fig. 1. Externally-compensated PMOS-based LDO

The presented methodology enables creating and sharing standardized design flows, promoting collaboration among designers and, as a result, contributing to open-source design effort [4] [5]. This work uses automation scripts to streamline device sizing and reduce design time while preserving the analytical insights necessary for design accuracy [6].

Section II-A/B/C describes Algorithms 1 and 2, which are used to derive transistor FOMs from given performance specifications. Section II-D presents Algorithms 3 and 4, which take as input the above-derived FOMs and technology LuTs to produce optimum device sizes. Section III presents the correlation between the calculated and simulated performance of a wideband high PSRR LDO designed using the presented methodology. Section IV summarizes and concludes the work.

II. Design-flow of a high-PSRR externally-compensated LDO using device LuTs

Figure 1 shows an externally-compensated LDO with a PMOS Pass FET (also called PMOS-based LDO). The following sections discuss the step-by-step description of the proposed design methodology:

A. Sizing the pass transistor, M_{pass}

The LDO pass-FET is sized to support maximum load current and $(gm/I_d = 10)$, which is a proxy for $V_{ov} = 200mV$

from conventional square-law paradigm. Minimum channel length, $L_{min} = 180nm$ is used to minimize the device area. Algorithm 1 shows the detailed steps to compute the width of the pass-FET, W_{pass}, and also to calculate its small-signal parameters: g_{mpass}, $(r_{Opass} = r_{out,p1})$, and C_{ggpass}. In this step, the pass-FET intrinsic gain and output-pole frequency, ω_{p1}, are also calculated.

B. Worst-case load condition

Determining the dependence of LDO small-signal performance metrics on load conditions is critical to this design flow and is summarized via the equations below.

The loop gain, A_{LG}, is expressed as the product of the gain of the pass transistor, A_{pass} and the error-amplifier gain, A_{diff} and is given by:

$$A_{LG}\big|_{DC} = (g_{mpass} r_{Opass}) \cdot [g_{m4}(r_{O5} \parallel r_{O7})] \tag{1}$$

where $g_{mpass} \cdot r_{Opass}$ is the intrinsic gain of the pass FET, g_{m4} and $(r_{O5} \parallel r_{O7})$ are the transconductance and output resistance of the error-amplifier, respectively. The dominant pole, set by the output stage of the LDO, is given by:

$$\omega_{p1} \approx \left(\frac{1}{r_{Opass} C_L}\right) \propto I_{Load} \tag{2}$$

The non-dominant pole, ω_{p2}, is set by the error-amplifier output and is given by:

$$\omega_{p2} = \left[\frac{1}{(r_{O5} \parallel r_{O7}) \cdot C_{ggpass}}\right] \tag{3}$$

The unity-gain bandwidth, ω_{ugb}, is proportional to the g_m of the pass transistor and error-amplifier gain, A_{diff}:

$$\omega_{ugb} \propto \left(\frac{g_{mpass} \cdot A_{diff}}{C_L}\right) \propto \sqrt{I_{Load}} \tag{4}$$

As the load current, I_{Load}, increases, the dominant pole, ω_{p1}, and the unity-gain bandwidth, ω_{ugb}, increase and move closer to the second pole at the error-amplifier output, ω_{p2}. Therefore, the worst-case phase-margin of an externally-compensated LDO is at heavy or maximum load current.

C. Sizing of error-amplifier transistors

The DC-PSRR of PMOS LDO can be approximated [7] as,

$$\text{PSRR}_{DC} = -20\log_{10}(A_{LG,dc}) \tag{6}$$

where $A_{LG,dc}$ is the DC loop gain. From the given DC-PSRR specification, $A_{LG,dc}$ can be evaluated from equation (6) which is then used to calculate A_{diff} and the other stability metrics as shown in Algorithm 2. As an example, to achieve a phase-margin of $\geq 45°$:

$$\omega_{p2} = \left(\frac{A_{LG,dc}}{\omega_{p1|Heavy}}\right) = \frac{A_{LG,dc}}{\left(\frac{1}{r_{Opass|Heavy} \cdot C_L}\right)} \tag{8}$$

Algorithm 2 illustrates the design flow for the NMOS input pair $(M_{4,5})$, where gm/I_d is set by the I_{bias} specification,

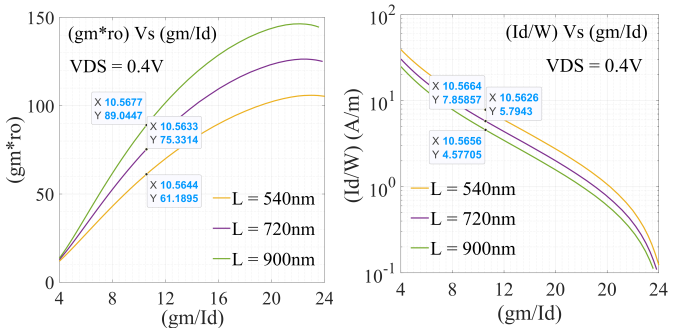
Algorithm 1 Sizing the Pass FET (M_{pass})

Given the load circuit parameters C_L and $I_{load,max}$,

1: Set (gm/I_d) and L_{pass} to the following values,
- Set $\left(\frac{g_m}{I_d}\right)$ = 10
- Set $L_{pass} = L_{min} = 180\text{-}nm$

2: Lookup Tables (LuTs):
- Extract transistor FoM's at $\left(\frac{g_m}{I_d}\right)$ = 10 from the following LuT's,
  - Intrinsic gain LuT $\rightarrow (g_m \cdot r_o)$ versus $\left(\frac{g_m}{I_d}\right)$
  - Transit frequency LuT $\rightarrow f_T$ versus $\left(\frac{g_m}{I_d}\right)$
  - Current density LuT $\rightarrow \left(\frac{I_d}{W}\right)$ versus $\left(\frac{g_m}{I_d}\right)$

3: Computation block:
- Calculate pass-FET small signal parameters from the extracted FoM values,
  - $g_{mpass} = \left(\frac{g_m}{I_d}\right) \cdot I_{load,max}$
  - $r_{Opass} = \left[\frac{(g_m \cdot r_o)}{g_{mpass}}\right]$ and $C_{ggpass} = \left(\frac{g_{mpass}}{f_T}\right)$
  - $\omega_{p1} = \left(\frac{1}{r_{Opass} \cdot C_L}\right)$
  - $W_{pass} = \left[\frac{I_{load,max}}{\left(\frac{I_d}{W}\right)}\right]$



(a) (b)

Fig. 2. Device Lookup Table (LuT) plots generated for an NMOS transistor in 180-nm CMOS process technology.

and $g_{m4,5}$, which is derived from the pass-FET intrinsic gain and the error-amplifier output resistance.

For the PMOS-transistor load, $M_{6,7}$, the flow follows a similar approach to that of the pass-FET. $I_{d,6,7}$ current is set to $(I_{bias}/2)$ and (g_m/I_d) ratio matched to that of pass-FET. However, in the case of the PMOS load, we utilize technology plots where the drain-source voltage (V_{ds}) is approximated as $(V_{th} + V_{ov}) \simeq 0.6V$ in the design example.

In this design, for the bias transistors, $M_{1,2,3}$, the lengths and g_m/I_d are chosen to be same as that of $M_{4,5}$. Transistor widths, $W_{1,2,3}$ are computed using the steps outlined in Algorithm 1.

D. Automation script for MOSFET sizing

Figure 3 shows the block level description of the 'LDO-(gm/Id)' design flow script. The script takes design speci-

Algorithm 2 Sizing the error-amplifier transistors $(M_{4,5})$

1: Input parameters:
- $g_{mpass} \cdot r_{Opass}$
- $C_{gggpass}$
- Output pole frequency, ω_{p1}
- I_{bias} or I_Q

2: Computation block:
- Calculate the error-amplifier transistors' small signal parameters from the given input parameters,
  - $A_{diff}\big|_{DC} = \left[\frac{A_{LG}\big|_{DC}}{(g_{mpass} \cdot r_{Opass})}\right]$
  - $\omega_{ugb} = \left(A_{LG}\big|_{DC} \cdot \omega_{p1}\right)$
  - $(r_{o5}||r_{o7}) = \left(\frac{1}{C_{gggpass} \cdot \omega_{ugb}}\right)$
  - $\omega_{p2} = \left[\frac{1}{(r_{o5}||r_{o7}) \cdot C_{gggpass}}\right]$
  - $g_{m4} = g_{m5} = \left[\frac{A_{diff}}{(r_{o5}||r_{o7})}\right]$
  - $(g_m \cdot r_O) = \left[g_{m4} \cdot 2 \cdot (r_{O5}||r_{O7})\right]$
  - $\left(\frac{g_m}{I_d}\right) = \left[\frac{g_{m4}}{(I_{bias}/2)}\right]$

3: Lookup Tables (LuTs):
- Find the channel length of transistors $M_{4,5}$ to meet the calculated $(g_m \cdot r_O)$ requirement.
- Extract transistor FoM's at the calculated $\left(\frac{g_m}{I_d}\right)$ from the following LuT's,
  - Transit frequency LuT $\rightarrow f_T$ versus $\left(\frac{g_m}{I_d}\right)$
  - Current density LuT $\rightarrow \left(\frac{I_d}{W}\right)$ versus $\left(\frac{g_m}{I_d}\right)$

4: Transistor Width $(M_{4,5})$:
- Calculate $W_{4,5} \rightarrow W_{4,5} = \left[\frac{(I_{bias}/2)}{\frac{I_d}{W}}\right]$

fications and technology LuTs as inputs, and gives out the optimum dimensions for all LDO transistors. The LuTs are in the form of a 'CSV' file with the following MOSFET FOMs: intrinsic gain, $(g_m \cdot r_o)$, current density (I_d/W), and transit frequency (f_T), characterized against the trans-conductance efficiency (gm/I_d).

Algorithm 1 & 2 are included as computational blocks in this design-automation script.

As a next step, device aspect ratios need to be computed for a derived gmro or ft FOM. To perform this, we need to access technology plots (shown in Fig.2), which can be either limited or too vast to handle. In order to address these concerns, this script uses two functions:

- The "linear interpolation" function is useful to estimate an intermediate value from a given set of discrete data points. In the 'LDO-gm/Id' design flow, this function interpolates the FOM values for a given gm/Id in a limited channel-length techplot set. For example, in Fig.2 the function will find gmro values for multiple finer length steps at a $gm/Id = 10.56$.
- The "distance between a point and a curve" function calculates the Euclidean distance between a target FOM point and a set of data points on a curve. For example, the function will find the optimum channel length for the derived gmro.

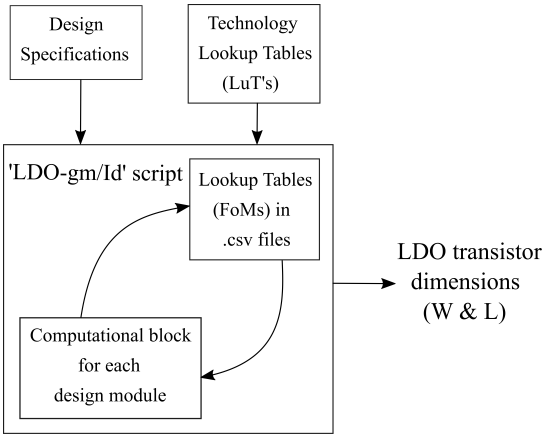


Fig. 3. Block-level description of the 'LDO-(gm/Id)' design flow script.

In summary, to find transistor channel length for desired intrinsic gain $(gm \cdot ro)$, the script does the following: Using the LuT data of 'gmro vs. gm/id' the interpolation function estimates $g_m \cdot r_o$ for a given (gm/Id) at all channel lengths. The distance-to-curve function then calculates the distance between the target and all the $g_m \cdot r_o$ points and then selects the channel length with the smallest distance to target $g_m \cdot r_o$ curve. 'LDO-(gm/Id)' design flow script is implemented using Python which is shared here: Github link [8].

Algorithm 3 Linear Interpolation

1: Input parameters:
- input point, $x \rightarrow \left(\frac{g_m}{I_d}\right)$
- x-coordinates, $x_{data} \rightarrow$ array of $\left(\frac{g_m}{I_d}\right)$ values
- output point, $y \rightarrow$ interpolated $(g_m \cdot r_O)$
- y-coordinates, $y_{data} \rightarrow$ array of $(g_m \cdot r_O)$ values

2: Process:
3: **for** each i from 1 to $\left[len(x_{data}) - 1\right]$ **do**
4: **if** $x \geq x_{data}[i]$ **then**
5: Set $x_0 = x_{data}[i]$, $x_1 = x_{data}[i+1]$
6: Set $y_0 = y_{data}[i]$, $y_1 = y_{data}[i+1]$
7: Perform linear interpolation,
8: $y = y_0 + \left[\frac{(y_1 - y_0)}{(x_1 - x_0)} \cdot (x - x_0)\right]$
9: Return y
10: **end if**
11: **end for**
12: Output:
- $y \rightarrow$ (interpolated y-coordinate for the given x)

III. Simulation results and discussion

In order to validate the proposed LDO design automation methodology using LuTs, an example design with specifica-

Algorithm 4 Distance Between a Point and a Curve

Input parameters:
- x-coordinate of the input point, $x \rightarrow \left(\frac{g_m}{I_d}\right)$
- y-coordinate of the input point, $y \rightarrow (g_m \cdot r_O)$
- $x\_curve \rightarrow$ array of x-coordinates of the curve
- $y\_curve \rightarrow$ array of y-coordinates of the curve

Process:
Initialize $min\_distance = \infty$
for each i from 1 to $len(x\_curve)$ **do**
  Calculate distance between point (x, y) and curve point $(x\_curve[i], y\_curve[i])$:
$distance = \sqrt{(x\_curve[i] - x)^2 + (y\_curve[i] - y)^2}$
  if $distance < min\_distance$ **then**
    Update $min\_distance = distance$
  end if
end for
Output:
- $min\_distance$ (minimum distance between the point and the curve)

TABLE I
TECHNOLOGY LOOKUP TABLE PARAMETERS AND DIMENSIONS OF LDO TRANSISTORS (M_{1-7}) & M_{pass}.

Transistor	g_m/I_d $(1/V)$	$g_m r_O$	I_d/W (A/m)	f_T (GHz)	L (μm)	W (μm)
M_{pass}	10	32.361	8.834	5.76	0.18	1132
$M_{4,5}$	10.56	75.33	5.799	1.49	0.72	4.31
$M_{6,7}$	10	60	9.04	5.96	0.18	2.7
$M_{1,2,3}$	10.56	75.33	5.799	1.49	0.72	8.62

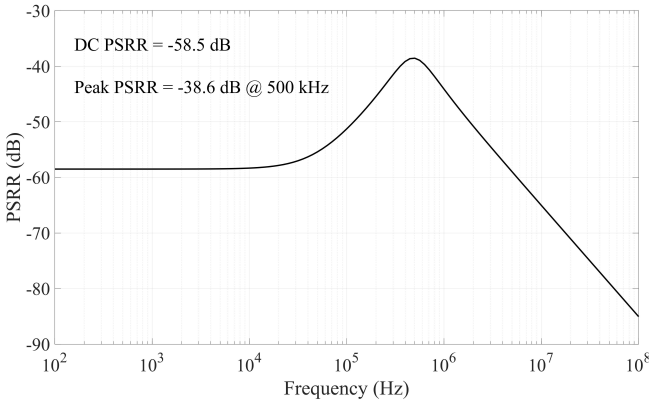


Fig. 4. Simulated PSRR performance, V_{in} = 1.4 V, V_{out} = 1.0 V, I_{Load} = 10 mA, I_{bias} = 50 μA, and C_L = 1 μF.

tions V_{in} = 1.4 V, V_{out} = 1 V, I_{Load} = 10 mA, and a wideband PSRR of $< -30dB$, is designed and simulated in a 180-nm CMOS process technology. Figure 1 shows the schematic of the PMOS-based LDO. The pass-FET (M_{pass}) is sized to support a maximum load current of 10 mA. Error amplifier transistors (M_{4-7}) and C_L are designed to meet the wide-band PSRR specifications, as discussed in section II. Bias transistors (M_{1-3}) are sized for a drain-to-source current of 50 μA, with its length and $\left(g_m/I_d\right)$ kept same as that of $M_{4,5}$. Table I

TABLE II
COMPARISON OF CALCULATED AND SIMULATED STABILITY METRICS WITH ERROR PERCENTAGE

	Calculated	Simulated	Error (%)
DC loop gain $= \left(A_{diff} \cdot A_{pass}\right)$	1000, 60 dB	1000, 60 dB	0%
$f_{p1} \approx \left(\frac{1}{2\pi r_{Opass} C_L}\right)$	489 Hz	485 Hz	0.82%
$f_{p2} \approx \left[\frac{1}{2\pi(r_{O5} \| r_{O7}) C_{ggpass}}\right]$	489 kHz	478 kHz	2.3%
$f_{ugb} \simeq \left(0.787 \cdot f_{p2}\right)$	384 kHz	379.6 kHz	1.16%
Phase margin	51.8^o	51.5^o	0.58%

shows the technology LuT parameters and the dimensions for LDO transistors, obtained from the 'LDO-(gm/Id)' design flow script. Pass-FET and the LDO circuit are estimated to occupy an on-chip area of 400 μm^2 and $\simeq 490 \mu m^2$ respectively.

Table II shows the calculated and simulated stability metrics. Figure 4 shows the simulated PSRR performance of the LDO, with a high DC-PSRR of -58.5 dB, and with a peak PSRR of -38.6 dB at 500 kHz. The LDO supports a maximum load of 10 mA with an output capacitor of 1 µF, maintaining stability across load conditions. Table II validates the correlation between calculated and simulated performance of the proposed 'LDO-(gm/Id)' design methodology. The comparison is tabulated for DC loop gain, pole frequencies, unity-gain frequency and phase margin. Across these metrics, the predicted stability performance has an error of $< 2.5\%$.

IV. CONCLUSION

The 'LDO-gm/Id design methodology' presented in this work achieves a strong correlation of performance between design calculations and simulation results. The demonstrated design and automation flow is adaptable to advanced technology nodes and reduces number of analog design iterations. With the emerging usage of open-source PDKs, methodology-driven designs like this work, can be shared more widely, benefiting the broader analog IC-design community [8].

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[8] An example wideband PSRR LDO circuit designed using the proposed methods in this work and the Python scripts can be found in the following Github, link.