C-BAND THIN FILM MICROWAVE DRIVER AMPLIFIER DESIGN AND IMPLEMENTATION WITH EM-BASED OPTIMIZATION FOR TTC APPLICATIONS

A PROJECT REPORT

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BONAFIDE CERTIFICATE

This is to certify that this project titled, "**C-BAND THIN FILM MICROWAVE DRIVER AMPLIFIER DESIGN AND IMPLEMENTATION WITH EM-BASED OPTIMIZATION FOR TTC APPLICATIONS**" is the bonafide work done by **NIVESH S [21EC1063]** in the partial fulfilment of the requirement for the award of the degree of **BACHELOR OF TECHNOLOGY** in **ELECTRONICS AND COMMNUNICATION ENGINEERING** during the year 2024-2025 in **PUDUCHERRY TECHNOLOGICAL UNIVERSITY** and this work has not been submitted for the award of any other degree of this/any other university.

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ORGANIZATION PROFILE

Indian Space Research Organisation (ISRO) is the space agency of India. The organisation is involved in science, engineering and technology to harvest the benefits of outer space for India and the mankind. ISRO is a major constituent of the Department of Space (DOS), Government of India. The department executes the Indian Space Programme primarily through various Centres or units within ISRO.

ISRO was previously the Indian National Committee for Space Research (INCOSPAR), set up by the Government of India in 1962, as envisioned by Dr. VikramA Sarabhai. ISRO was formed on August 15, 1969 and superseded INCOSPAR with an expanded role to harness space technology. DOS was set up and ISRO was brought under DOS in 1972.

The prime objective of ISRO/DOS is the development and application of space technology for various national needs. To fulfil this objective, ISRO has established major space systems for communication, television broadcasting and meteorological services; resources monitoring and management; space-based navigation services. ISRO has developed satellite launch vehicles, PSLV and GSLV, to place the satellites in the required orbits.

Alongside its technological advancement, ISRO contributes to science and science education in the country. Various dedicated research centres and autonomous institutions for remote sensing, astronomy and astrophysics, atmospheric sciences and space sciences in general function under the aegis of Department of Space. ISRO's own Lunar and interplanetary missions along with other scientific projects encourage and promote science education, apart from providing valuable data to the scientific community which in turn enriches science.

ISRO has its headquarters in Bengaluru. Its activities are spread across various centres and units. Launch Vehicles are built at Vikram Sarabhai Space Centre (VSSC), Thiruvananthapuram; Satellites are designed and developed at U R Rao Satellite Centre (URSC), Bengaluru; Integration and launching of satellites and launch vehicles are carried out from Satish Dhawan Space Centre (SDSC), Sriharikota; Development of liquid stages including cryogenic stage is carried out at Liquid Propulsion Systems Centre (LPSC), Valiamala & Bengaluru; Sensors for Communication and Remote Sensing satellites and application aspects of the space technology are taken up at Space Applications Centre (SAC),

Ahmedabad and Remote Sensing satellite data reception processing and dissemination is entrusted to National Remote Sensing Centre (NRSC), Hyderabad.

U R Rao Satellite Centre (URSC), Bengaluru, formerly known as ISRO Satellite Centre (ISAC) is the lead centre for building satellites and developing associated satellite technologies. These spacecrafts are used for providing applications to various users in the area of Communication, Navigation, Meteorology, Remote Sensing, Space Science and interplanetary explorations. The Centre is also pursuing advanced technologies for future missions. URSC is housed with the state-of-the-art facilities for building satellites on end-to-end basis. ISRO Satellite Integration and Test Establishment (ISITE) is equipped with state-of-the-art clean room facilities for spacecraft integration and test facilities including a 6.5 Metre thermo vacuum chamber, 29 Ton vibration facility, Compact Antenna Test Facility and acoustic test facility under one roof. Assembly, Integration and Testing of all Communication and Navigation Spacecraft is carried out at ISITE. A dedicated facility for the product ionisation of standardised subsystems is established at ISITE.

URSC has a unit called Laboratory for Electro Optics System (LEOS), which is situated in Peenya, Bengaluru and is mainly responsible for research, development and product ionisation of Sensors for ISRO programmes.

Since inception, URSC has the distinction of building more than 100 satellites for various applications like scientific, communication, Navigation and remote sensing. Many private and public sector industries are also supporting ISAC in realising standard satellite hardware.

COMPLETION CERTIFICATE

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DATE : 30-04-2025

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during the period from 17-02-2025 *to* 30-04-2025

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PROJECT TITLE : C-Band Thin film Microwave Driver Amplifier Design & Implementation with EM Based Optimization for TTC Applications

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ABSTRACT

This project presents the design, simulation, fabrication, and validation of a C-band microwave driver amplifier tailored for Telemetry, Tracking, and Command (TTC) subsystems in low-earth-orbit (LEO) satellites, operating at 6.4 GHz. The amplifier addresses the stringent requirements of TTC applications, including high gain, compact size, unconditional stability, and space-grade reliability, within a constrained power budget and payload space. Utilizing thin-film hybrid microcircuit technology on a 99.6% pure alumina substrate, the design leverages a space-qualified GaAs MESFET (FLC027-WG) to achieve a target gain of 9.6 ± 1 dB, input/output return losses below -6 dB, and a stability factor $K > 1$, while fitting within layout constraints of 14.7 mm (input side) and 10.69 mm (output side).

The design methodology integrates S-parameter-based simulations, Smith Chart impedance matching, and electromagnetic (EM) extraction using AWR Microwave Office and AXIEM, ensuring early parasitic modeling for first-pass success. Key steps include stability analysis, single-stub matching network synthesis, optimization via different optimization algorithms, and layout generation adhering to space qualification standards. The fabricated amplifier, mounted on a gold-plated Kovar carrier and hermetically sealed, underwent rigorous testing, including Vector Network Analyzer (VNA) measurements and environmental tests (thermal cycling, thermovacuum, vibration).

Results demonstrate a measured gain of 12.14 dB, S_{11} of -4.8 dB, S_{22} of -1.8 dB, and $K = 1.27$ at 6.4 GHz, exceeding gain targets while slightly deviating on return losses due to fabrication tolerances. Environmental tests confirm minimal performance degradation, validating reliability for LEO conditions. Contributions include an EM-aware design framework, enhanced TTC reliability, and a scalable thin-film approach for satellite RF systems. Future work includes multi-stub matching for broader bandwidth, advanced EM modeling, and integration into full TTC modules, further advancing LEO satellite communication efficiency.

Keywords : Driver Amplifier, Thin Film Hybrid Microcircuit, AWR Microwave Office, Telemetry, Tracking and Command (TTC), AXIEM

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LIST OF ABBREVIATION AND ACRONYMS

- **AWR**: Applied Wave Research
- **BJT**: Bipolar Junction Transistor
- **CLA**: Center Line Average
- **DA**: Driver Amplifier
- **DC**: Direct Current
- **DRC**: Design Rule Check
- **EM**: Electromagnetic
- **FR4**: Flame Retardant 4
- **GaAs**: Gallium Arsenide
- **GaN**: Gallium Nitride
- **HEMT**: High-Electron-Mobility Transistor
- **HBT**: Heterojunction Bipolar Transistor
- **HFSS**: High-Frequency Structure Simulator
- **IPD**: Integrated Passive Device
- **LEO**: Low-Earth-Orbit
- **MESFET**: Metal-Semiconductor Field-Effect Transistor
- **MMIC**: Monolithic Microwave Integrated Circuit
- **PAE**: Power-Added Efficiency
- **PCB**: Printed Circuit Board
- **pHEMT**: Pseudomorphic High-Electron-Mobility Transistor
- **RF**: Radio Frequency
- **S-Parameters**: Scattering Parameters
- **TTC**: Telemetry, Tracking, and Command
- **VNA**: Vector Network Analyzer

CHAPTER-1

INTRODUCTION

1.1 PROJECT OVERVIEW

The Telemetry, Tracking, and Command (TTC) subsystem is a cornerstone of satellite communication systems, enabling critical functions such as data transmission, orbit determination, and operational control between spacecraft and ground stations. In low-earth-orbit (LEO) satellites, where power budgets and payload space are severely constrained, the TTC subsystem must deliver high performance within a compact and efficient design. A key component of the TTC subsystem, the driver amplifier (DA) amplifies signals in both the receiver and transmitter chains, ensuring effective signal handling while withstanding the harsh environmental conditions of space, including thermal extremes, vacuum, and radiation. The driver amplifier must achieve high gain, precise impedance matching, and unconditional stability to meet the demands of satellite operations.

Operating in the C-band (centred at 6.4 GHz), the driver amplifier for TTC applications faces unique challenges due to the high-frequency signal and miniaturization needs. As part of the RF front-end, it acts as a key intermediate stage, amplifying signals either after low-noise amplification in the receiver chain for mixing, or before the power amplifier in the transmitter chain for antenna transmission, requiring high gain, a small form factor, and low power consumption. The efficiency of this stage greatly impacts the telemetry subsystem's performance, making its design critical for satellite communication systems.

This project focuses on the design, simulation, fabrication, and validation of a C-band microwave driver amplifier tailored for TTC subsystems in LEO satellites. Utilizing thin-film hybrid microcircuit technology on a high-purity alumina substrate, the amplifier targets a gain of 9.6 ± 1 dB, input and output return losses below -6 dB, and unconditional stability (stability factor $K > 1$) at 6.4 GHz. The design leverages advanced tools such as AWR Microwave Office for S-parameter-based simulations, impedance matching, and AXIEM for electromagnetic (EM) extraction to account for layout parasitics. The fabricated amplifier undergoes rigorous testing, including Vector Network Analyzer (VNA) measurements and space-environmental tests, to ensure reliability and performance under operational conditions.

1.2 MOTIVATION FOR THE WORK

The increasing complexity of LEO satellite missions, driven by applications such as remote sensing, global communication, and scientific exploration, demands RF components that are both high-performing and compact. Driver amplifiers in TTC systems must deliver consistent gain and matching within tight layout constraints while surviving thermal, mechanical, and radiation stresses. Traditional design approaches often treat EM validation as a final step, leading to performance discrepancies between simulations and fabricated circuits due to unmodeled parasitics. This gap is particularly problematic in space applications, where reliability is non-negotiable, and iterative fabrication is costly and time-consuming.

The motivation for this work lies in addressing these challenges through an iterative, EM-aware design methodology that integrates EM extraction early in the design process. By combining thin-film technology's precision and thermal stability with advanced simulation and optimization techniques, this project aims to achieve first-pass design success and environmental resilience. The use of a space-qualified GaAs MESFET and a high-purity alumina substrate further ensures the amplifier's suitability for TTC applications, contributing to reliable and efficient satellite communication systems.

1.3 LITERATURE REVIEW

A survey of recent literature on C-band and related microwave amplifiers highlights diverse approaches and trade-offs, providing context for the current work. Below is a summary of recent reference papers, focusing on their design methodologies, performance metrics, and relevance to TTC applications:

Table 1.1: Summary of Recent C-Band and Related Amplifier Designs

Title	Journal	Advantages	Limitations
Design of High Gain MMIC Amplifier for LEO Satellite Communication Systems [1]	Satellite Navigation (2024)	- Very high gain (34.23 dB) - Good isolation (<-51.99 dB)	- S-band focus (2–4 GHz) - Limited C-band applicability
Microwave and Millimeter-Wave Chips Based on Thin-Film	Springer (2023)	- Thin-film IPD enhances integration	- Not C-band specific - Focuses on

Integrated Passive Device Technology [2]		- Broad frequency coverage	passive components
C-Band 30 W High PAE Power Amplifier MMIC with Second Harmonic Suppression for Radar Network Application [3]	Micromachines (2022)	- High output power (45 dBm) - Excellent PAE (>57%)	- Pulsed operation only - Potential integration issues
Design and Development of C-Band Microwave Amplifier for Wireless Applications [4]	IEEE International Conference on Electronics, Computing and Communication Technologies (2020)	- Low noise figure (1.2 dB) - High gain (15 dB)	- Low output power - Narrowband design
Microwave Amplifier Design Using High Mobility Electron Transistor [5]	IOP Conference Series: Materials Science and Engineering (2020)	- High gain (21 dB) - Low VSWR (1.1)	- High noise figure (13 dB) - Complex matching network
A 3.5 GHz Medium Power Amplifier Using 0.15 µm GaAs PHEMT for WiMAX Applications [10]	Asia-Pacific Microwave Conference (APMC) (2009)	- Compact design - Decent gain (15 dB)	- Lower C-band frequency - Moderate efficiency (30%)
A C-Band High-Efficiency Second-Harmonic-Tuned Hybrid Power Amplifier in GaN Technology [11]	IEEE Transactions on Microwave Theory and Techniques (2006)	- High PAE (65%) at 5.5 GHz - Compact GaN HEMT design	- Narrow bandwidth - Complex harmonic tuning

1.4 LIMITATIONS OF EXISTING WORK

The reviewed literature reveals several limitations in existing C-band and related amplifier designs:

- **Frequency Mismatch**: Designs like [1] are optimized for S-band or millimeter-wave bands, lacking direct applicability to the C-band (6.4 GHz) required for TTC systems.
- **Application-Specific Constraints**: High-power designs [2] for radar or ground-based systems [3] are not suited for the continuous, low-power operation of TTC subsystems.
- **Performance Trade-Offs**: Many designs [4, 5, 10] sacrifice gain, bandwidth, or efficiency at band edges, limiting their robustness for satellite applications.
- **Lack of EM-Aware Design**: Most works [3, 5, 11] defer EM validation to post-design stages, leading to discrepancies between simulated and fabricated performance due to parasitics.
- **Size and Space Qualification**: Large footprints [11] or non-space-qualified components [5, 10] make these designs incompatible with LEO satellite constraints.

These gaps highlight the need for a C-band driver amplifier that combines high gain, stability, compactness, and space-grade reliability with an EM-aware design flow.

1.5 OBJECTIVE OF THE PROJECT

The primary objective of this project is to design, fabricate, and validate a C-band microwave driver amplifier for TTC subsystems in LEO satellites, meeting the following specifications at 6.4 GHz:

- Gain (S_{21}): 9.6 ± 1 dB.
- Input Return Loss (S_{11}): < -6 dB.
- Output Return Loss (S_{22}): < -6 dB.
- Stability Factor (K): > 1 (unconditional stability).
- Layout Constraints: 14.7 mm (input side), 10.69 mm (output side), 2.5 mm transistor gap.
- Space Qualification: Reliable performance under thermal cycling, thermovacuum, and vibration tests.

Additional objectives include developing an EM-aware design methodology to minimize performance drift, utilizing thin-film hybrid microcircuit technology for precision and thermal stability, and validating the amplifier through VNA measurements and environmental testing.

1.6 BLOCK DIAGRAM AND METHODOLOGY PROPOSED

The proposed driver amplifier is integrated into the RF front-end of the TTC telemetry subsystem, as shown in Fig. 1.1. The driver amplifier's design leverages a systematic methodology to achieve the target specifications:

1. **Transistor Selection**: Choose a space-qualified GaAs MESFET (FLC027-WG) with high gain (12.72 dB max) and S-parameter data.
2. **Substrate Selection**: Use high-purity alumina (99.6%, 1-6 µin CLA) for low loss and thermal conductivity.
3. **Stability Analysis**: Verify unconditional stability using Rollet's stability factor ($K > 1$) based on S-parameters.
4. **Impedance Matching**: Perform simultaneous conjugate matching via Smith Chart to optimize source (ΓS) and load (ΓL) reflection coefficients.
5. **Biasing and Matching Networks**: Design a fan-shaped radial stub biasing network and single-stub shunt matching networks using AWR Microwave Office.
6. **Optimization**: Refine microstrip line parameters using Pointer-Hybrid optimization to meet gain and return loss goals.
7. **EM Extraction**: Use AXIEM to model layout parasitics and ensure performance alignment.
8. **Fabrication and Testing**: Fabricate the amplifier on alumina using thin-film processes, mount the transistor on a Kovar carrier, and test with VNA and environmental tests.

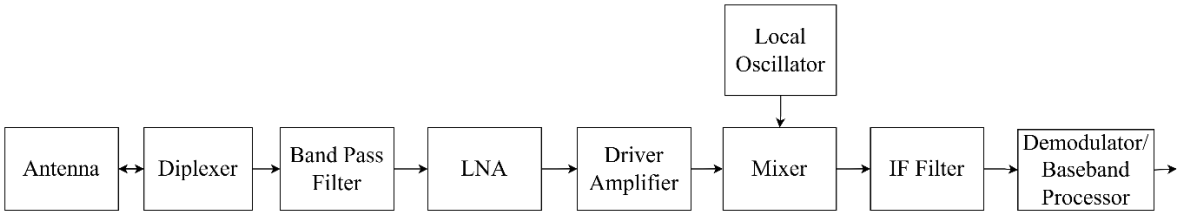

Fig. 1.1: Block Diagram for the RF Front-End (Receive Path) of a Satellite TTC Subsystem

1.7 ORGANIZATION OF THE THESIS

This report is structured to provide a detailed account of the C-band driver amplifier design process, with each chapter focusing on a specific aspect to avoid redundancy:

- **Chapter 2: Existing Works** elaborates on prior amplifier designs, detailing their technical specifications and limitations, building on the literature review.
- **Chapter 3: Hybrid Circuits and Thin-Film Technology** explores the principles and advantages of thin-film hybrid microcircuits, including substrate properties and fabrication processes.
- **Chapter 4: Design Goals and Methodology** outlines the amplifier's specifications, design flowchart, and AWR Microwave Office workflow.
- **Chapter 5: Component Selection** justifies the choice of the FLC027-WG transistor and alumina substrate based on performance and reliability.
- **Chapter 6: Amplifier Design** details the biasing network, matching networks, stability analysis, optimization, and EM extraction.
- **Chapter 7: Amplifier Layout** describes the layout generation, carrier plate dimensions, and file export for fabrication.
- **Chapter 8: Amplifier Fabrication** covers the thin-film fabrication process, transistor mounting, and space-qualified packaging.
- **Chapter 9: Results and Discussion** analyzes simulation and test results, comparing schematic, EM-extracted, and fabricated performance.
- **Chapter 10: Conclusion and Future Scope** summarizes achievements, contributions, and recommendations for future work.
- **Appendix** includes the transistor datasheet.

This structure ensures a logical progression from context to implementation, culminating in a comprehensive evaluation of the amplifier's performance and its significance for LEO satellite TTC systems.

CHAPTER-2

EXISTING WORKS

2.1 INTRODUCTION

The design of microwave amplifiers for satellite communication, particularly in the C-band (4–8 GHz), has been a focal point of research due to the band's suitability for Telemetry, Tracking, and Command (TTC) subsystems in low-earth-orbit (LEO) satellites. Recent advancements in amplifier technologies, including monolithic microwave integrated circuits (MMICs), hybrid circuits, and high-electron-mobility transistors (HEMTs), have led to significant improvements in gain, efficiency, and bandwidth. However, the unique requirements of TTC systems—high gain, compact size, unconditional stability, and space-grade reliability—pose challenges that many existing designs fail to fully address. This chapter provides a detailed analysis of prior works on C-band and related microwave amplifiers, emphasizing their technical specifications, design approaches, and limitations in the context of TTC applications. By examining these works, this chapter identifies gaps that the proposed C-band driver amplifier design aims to overcome, setting the stage for the methodology presented in subsequent chapters.

2.2 OVERVIEW OF EXISTING AMPLIFIER DESIGNS

The literature on microwave amplifiers offers insights into designs relevant to C-band TTC systems, as summarized in Table 2.1. Kumar and Patel (2024) [1] developed an S-band MMIC amplifier with a high gain of 34.23 dB and good isolation (<-51.99 dB), but its S-band focus limits C-band applicability. Wu and Wang (2023) [2] explored thin-film IPD technology, achieving broad frequency coverage, yet its emphasis on passive components and lack of C-band specificity reduces relevance. Yang et al. (2022) [3] presented a C-band GaN MMIC amplifier with 45 dBm output power and >57% PAE, ideal for radar but constrained by pulsed operation. Kumar and Goyal (2020) [4] designed a C-band amplifier with a low noise figure (1.2 dB) and 15 dB gain, though its narrow bandwidth and low output power hinder TTC use. Nugroho and Widodo (2020) [5] achieved a 21 dB gain using a high-mobility electron transistor, but a high noise figure (13 dB) and complex matching network pose challenges. Yeo and Ma (2009) [10] proposed a 3.5 GHz GaAs pHEMT amplifier with a compact design and 15 dB gain, yet its lower C-band frequency and moderate efficiency (30%) are limiting. Lastly, Cripps et al. (2006) [11] developed a C-band GaN HEMT amplifier with 65% PAE at 5.5 GHz, but its narrow bandwidth and complex harmonic tuning restrict broader application. These

works highlight gaps in achieving compact, stable, and space-qualified C-band amplifiers for TTC systems, underscoring the need for an optimized design.

2.3 TECHNICAL ANALYSIS OF DESIGN APPROACHES

The reviewed designs employ a range of technologies and methodologies, each with strengths and weaknesses:

- **MMIC-Based Designs** ([1, 2, 7]): MMICs offer high integration and performance but are often power-hungry and frequency-specific, limiting their adaptability to C-band TTC systems. The GaAs and GaN processes provide high gain and efficiency, but their complexity increases fabrication costs.
- **Hybrid Circuits** ([3, 8]): Hybrid designs on ceramic substrates balance cost and performance, suitable for C-band applications. However, their larger footprints and lack of EM-aware validation hinder their use in compact, reliable TTC modules.
- **Thin-Film Technology** ([5]): Thin-film processes excel in precision and high-frequency stability but are underutilized in C-band designs, focusing instead on higher bands.
- **Microstrip Matching Networks** ([3, 4, 6]): Single-stub and distributed matching networks are common, offering simplicity but limited bandwidth and sensitivity to fabrication tolerances.
- **Stability and EM Validation**: Most designs ([3, 6, 8]) rely on post-fabrication testing for stability, neglecting early EM extraction, which leads to parasitic-induced performance drifts.

2.4 RELEVANCE TO THE PROPOSED WORK

The proposed C-band driver amplifier addresses the identified gaps by:

- Operating at 6.4 GHz, directly targeting TTC applications.
- Using thin-film hybrid microcircuit technology on a high-purity alumina substrate for precision, thermal stability, and compactness.
- Employing an EM-aware design methodology with early AXIEM extraction to minimize parasitic effects.

- Achieving a gain of 12.14 dB and unconditional stability ($K > 1$) through simultaneous conjugate matching and optimization.
- Ensuring space qualification through rigorous environmental testing (thermal cycling, thermovacuum, vibration).

By building on the strengths of prior works (e.g., hybrid circuits, GaAs transistors) and overcoming their limitations, the proposed design offers a tailored solution for LEO satellite TTC systems, as detailed in the subsequent chapters.

2.5 SUMMARY

This chapter has reviewed eight recent works on C-band and related microwave amplifiers, analyzing their technical specifications, design approaches, and limitations. While these designs demonstrate advancements in gain, efficiency, and integration, they fall short in meeting the specific requirements of TTC driver amplifiers, such as C-band operation, compact size, stability, and space qualification. The identified gaps underscore the need for an EM-aware, thin-film-based design tailored for LEO satellites, which the proposed work aims to achieve. The next chapter explores the principles of hybrid circuits and thin-film technology, laying the foundation for the amplifier's design methodology.

CHAPTER-3

HYBRID CIRCUITS AND THIN-FILM TECHNOLOGY

3.1 INTRODUCTION

The design of high-frequency microwave amplifiers for Telemetry, Tracking, and Command (TTC) subsystems in low-earth-orbit (LEO) satellites demands technologies that offer precision, reliability, and thermal stability. Hybrid microcircuits, combining active semiconductor devices with batch-fabricated passive components, provide a robust platform for such applications. Among hybrid circuit technologies, thin-film processes stand out for their ability to produce precise, low-loss conductors and resistors on high-quality substrates, making them ideal for C-band (6.4 GHz) driver amplifiers. This chapter explores the principles, characteristics, and fabrication processes of hybrid circuits, with a focus on thin-film technology and its application in the proposed amplifier design. It also discusses the selection of alumina as the substrate material, highlighting its role in ensuring performance and reliability in space environments.

3.2 OVERVIEW OF HYBRID MICROCIRCUITS

Hybrid microcircuits integrate active chip devices (e.g., transistors, diodes, integrated circuits) with passive components (e.g., resistors, conductors, capacitors) on an insulating substrate. Unlike monolithic microwave integrated circuits (MMICs), which fabricate all components on a single semiconductor wafer, hybrid circuits combine distinct technologies in a single structure, offering flexibility and performance advantages for high-frequency applications. Hybrid circuits are classified as thin-film or thick-film based on the deposition process and thickness of the interconnect layers.

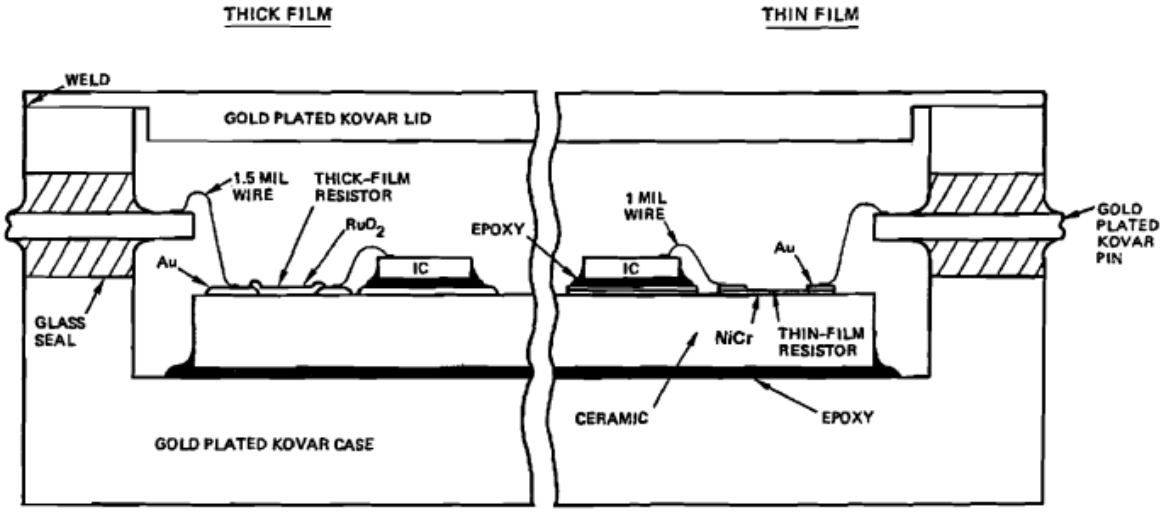

Fig. 3.1: Structure of a Hybrid Microcircuit

3.2.1 Thin-film vs. Thick-film circuits

Thin-film circuits are formed by depositing metallization layers (30 Å to 25,000 Å thick) via vacuum evaporation or sputtering onto a substrate. This process allows for precise control of conductor and resistor patterns, making thin-film technology suitable for high-frequency applications like C-band amplifiers. Thick-film circuits, in contrast, use screen-printing and firing of conductive and resistive pastes, resulting in thicker layers (0.1 mil to several mils). While thick-film circuits are cost-effective, their coarser resolution and higher losses limit their use above 500 MHz, whereas thin-film circuits excel in precision and stability up to microwave frequencies.

Table 3.1: Comparison of Thin-Film and Thick-Film Technologies

Parameters	**Thick-Film Hybrid Circuits**	**Thin-Film Hybrid Circuits**
Performance	High	High
Design flexibility, digital analog	Medium	Medium
Parasitics	Low	Low
Resistors, maximum sheet resistivity	High	Low
Temperature coefficient of resistance tolerance	Low	Lowest
Power dissipation	High	High

Frequency Limit	Medium	High
Voltage Swing	High	High
Size	Small	Small
Package density	Medium	Medium
Reliability	High	High
Circuit development time	1 month	1 month

3.3 ADVANTAGES OF THIN-FILM HYBRID CIRCUITS

Thin-film hybrid circuits offer several advantages that make them ideal for the proposed C-band driver amplifier:

1. **Precision and Miniaturization**: The vacuum deposition process enables fine conductor lines (down to 1 μm) and precise resistor trimming, supporting compact layouts (e.g., 14.7 mm × 10.69 mm for the amplifier).
2. **High-Frequency Performance**: Low parasitic capacitances and inductances, due to thin metallization and smooth substrates, ensure stable operation at 6.4 GHz.
3. **Thermal Management**: Direct mounting of high-power devices on thermally conductive substrates (e.g., alumina) dissipates heat effectively, critical for space environments with temperature swings from -50°C to +150°C.
4. **Reliability**: Fewer interconnections and batch-processed passives reduce failure points, enhancing reliability under space conditions like radiation and vibration.
5. **Space Qualification**: Thin-film circuits have a proven track record in aerospace applications, as seen in early systems like the Minuteman missile.

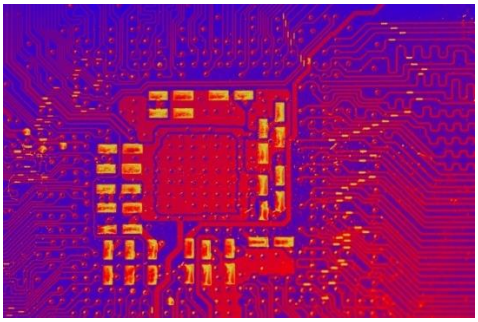

Fig. 3.2: Thermal Dissipation in Thin-Film Circuits

3.4 SUBSTRATE SELECTION: ALUMINA

The substrate in a hybrid circuit serves three key functions: mechanical support, electrical interconnect base, and heat dissipation medium. For the proposed amplifier, alumina (Al_2O_3) with 99.6% purity and a surface smoothness of 1-6 microinches center line average (CLA) was selected due to its superior properties:

- **High Dielectric Constant**: Alumina's dielectric constant ($\varepsilon_r \approx 9.8$) supports compact microstrip designs, reducing circuit size.
- **Low Loss Tangent**: A loss tangent of ~0.0001 minimizes signal attenuation at 6.4 GHz.
- **Thermal Conductivity**: Alumina's thermal conductivity (~30 W/m·K) ensures efficient heat dissipation, critical for maintaining transistor performance.
- **Surface Smoothness**: A 1-6 µin CLA surface enables precise thin-film deposition, reducing conductor losses and parasitic effects.
- **Space Qualification**: Alumina's mechanical strength and radiation resistance make it suitable for LEO satellite environments.

In contrast, lower-grade alumina (94-96% purity, 15-25 µin CLA) used in thick-film circuits exhibits higher surface roughness, leading to increased losses and reduced precision. The choice of high-purity alumina aligns with the amplifier's requirements for high-frequency stability and compact layout.

Table 3.2: Properties of Alumina Substrates for Thin-Film Circuits

Parameter	99.6% Pure Alumina	94-96% Pure Alumina
Purity	99.6%	94-96%
Surface Smoothness	1-6 µin CLA	15-25 µin CLA
Dielectric Constant	~9.8	~9.5
Thermal Conductivity	~30 W/m·K	~20 W/m·K
Applications	High-frequency circuits (e.g., C-band amplifiers), space-grade TTC subsystems	General-purpose RF circuits, thick-film hybrids

3.5 THIN-FILM FABRICATION PROCESSES

The fabrication of thin-film hybrid circuits involves depositing and patterning metallization layers on the substrate to form conductors, resistors, and interconnects. The key processes include:

1. **Vacuum Evaporation**: Metal (e.g., gold, nickel) is vaporized in a high-vacuum chamber and deposited onto the alumina substrate, forming layers 200 Å to 20,000 Å thick. This process ensures high purity and uniformity.
2. **Sputtering**: A plasma-based process bombards a metal target, ejecting atoms that deposit onto the substrate. Sputtering is used for adhesion layers (e.g., titanium) and resistive materials (e.g., nichrome).
3. **Photolithography**: A photoresist is applied, exposed to UV light through a mask, and developed to define conductor and resistor patterns. Etching removes unwanted material, leaving precise features.
4. **Resistor Trimming**: Laser or abrasive trimming adjusts resistor values to within 0.1% tolerance, critical for matching network accuracy.
5. **Device Attachment**: Active devices (e.g., FLC027-WG GaAs MESFET) are attached using conductive epoxy or eutectic solder, followed by wire bonding (1 mil gold or aluminium wires) to connect to substrate pads.
6. **Packaging**: The circuit is mounted in a gold-plated Kovar carrier and sealed in an aluminium housing to protect against environmental stresses.

3.6 APPLICATIONS IN TTC AMPLIFIERS

Thin-film hybrid circuits are particularly suited for TTC driver amplifiers due to their ability to meet the stringent requirements of LEO satellites:

- **Compact Layout**: The amplifier's layout (14.7 mm input side, 10.69 mm output side) fits within TTC module constraints, enabled by thin-film's fine-line capabilities.
- **High-Frequency Stability**: Low parasitics ensure stable operation at 6.4 GHz, critical for maintaining gain (9.6 ± 1 dB) and return losses (< -6 dB).
- **Environmental Resilience**: Alumina's thermal and mechanical properties, combined with hermetic packaging, ensure reliability under space conditions.

- **Historical Precedence**: Thin-film hybrids have been used in space systems since the 1960s (e.g., Minuteman missile), validating their suitability for TTC applications.

The choice of thin-film technology over thick-film or MMIC alternatives reflects its balance of performance, reliability, and manufacturability for the proposed amplifier.

3.7 SUMMARY

This chapter has detailed the principles, advantages, and fabrication processes of thin-film hybrid microcircuits, emphasizing their suitability for C-band driver amplifiers in TTC subsystems. The use of high-purity alumina as the substrate ensures high-frequency performance, thermal management, and space qualification. Thin-film processes, including vacuum evaporation, sputtering, and photolithography, enable precise and reliable circuits, addressing the limitations of thick-film and MMIC technologies. The insights provided here lay the foundation for the amplifier's design methodology, which is explored in the next chapter, focusing on specific goals and simulation techniques.

CHAPTER-4

DESIGN GOALS AND METHODOLOGY

4.1 INTRODUCTION

The design of a C-band microwave driver amplifier for Telemetry, Tracking, and Command (TTC) subsystems in low-earth-orbit (LEO) satellites requires a systematic approach to meet stringent performance, size, and reliability requirements. Operating at 6.4 GHz, the amplifier must deliver high gain, low return losses, and unconditional stability while adhering to compact layout constraints and space-grade environmental standards. This chapter outlines the specific design goals for the amplifier and presents the methodology employed to achieve them, leveraging S-parameter-based simulations, Smith Chart matching, and electromagnetic (EM) extraction. The workflow is implemented using the AWR Microwave Office design environment, which facilitates schematic synthesis, optimization, and layout generation. A flowchart of the design process is provided to illustrate the sequential steps, ensuring a clear and reproducible framework for the amplifier's development.

4.2 Design Goals

The driver amplifier is designed to meet the following specifications at 6.4 GHz, as summarized in Table 4.1, to ensure compatibility with TTC subsystems:

- **Gain (S_{21})**: 9.6 ± 1 dB, sufficient to drive the subsequent power amplifier while maintaining efficiency.
- **Input Return Loss (S_{11})**: < -6 dB, indicating good impedance matching to the source.
- **Output Return Loss (S_{22})**: < -6 dB, ensuring efficient power transfer to the load.
- **Stability Factor (K)**: > 1 across 1–10 GHz, guaranteeing unconditional stability to prevent oscillations.
- **Layout Constraints**: Input side of 14.7 mm, output side of 10.69 mm, and a 2.5 mm gap for the transistor, fitting within TTC module dimensions.
- **Size and Weight**: Minimize footprint and mass to comply with LEO satellite payload restrictions.

- **Space Qualification**: Reliable performance under thermal cycling (-50°C to +150°C), thermovacuum, and vibration tests.

Table 4.1: Design Specifications for the C-Band Driver Amplifier

Parameter	Value
Frequency Band	Centred at 6.4 GHz (C-band)
Gain (S_{21})	9.6 dB ± 1 dB
Input Return Loss (S_{11})	< –6 dB
Output Return Loss (S_{22})	< –6 dB
Stability Factor (K)	> 1 across operating band
Layout Constraints	Fixed: 14.7 mm (input), 10.69 mm (output)

These goals address the need for high performance, compactness, and robustness, aligning with the requirements of LEO satellite TTC systems.

4.3 DESIGN METHODOLOGY

The amplifier design follows a structured methodology based on S-parameter analysis, which characterizes the two-port network behaviour of the amplifier. This approach enables precise calculation of gain, stability, and impedance matching, critical for achieving the target specifications. The methodology comprises the following steps, illustrated in Fig. 4.1:

1. **Transistor Selection**: Choose an active device with suitable gain and frequency characteristics, compatible with C-band operation and space qualification.
2. **Substrate Definition**: Select a high-purity alumina substrate to support thin-film microstrip circuits with low loss and high thermal conductivity.
3. **Biasing Network Design**: Develop a biasing circuit that provides stable DC voltage and current without affecting RF performance.
4. **Stability Analysis**: Verify unconditional stability using Rollet's stability factor (K) and S-parameters.

5. **Impedance Matching**: Perform simultaneous conjugate matching using Smith Chart to optimize source (Γ_S) and load (Γ_L) reflection coefficients for maximum power transfer.
6. **Matching Network Synthesis**: Design single-stub microstrip matching networks for input and output ports using AWR Microwave Office.
7. **Optimization**: Refine microstrip line lengths and other parameters using optimization algorithms (e.g., Pointer-Hybrid, Particle Swarm) to meet gain and return loss goals.
8. **EM Extraction**: Use AXIEM to model layout parasitics and validate performance.
9. **Layout and Fabrication Preparation**: Generate a physical layout adhering to size constraints and export files for thin-film fabrication.

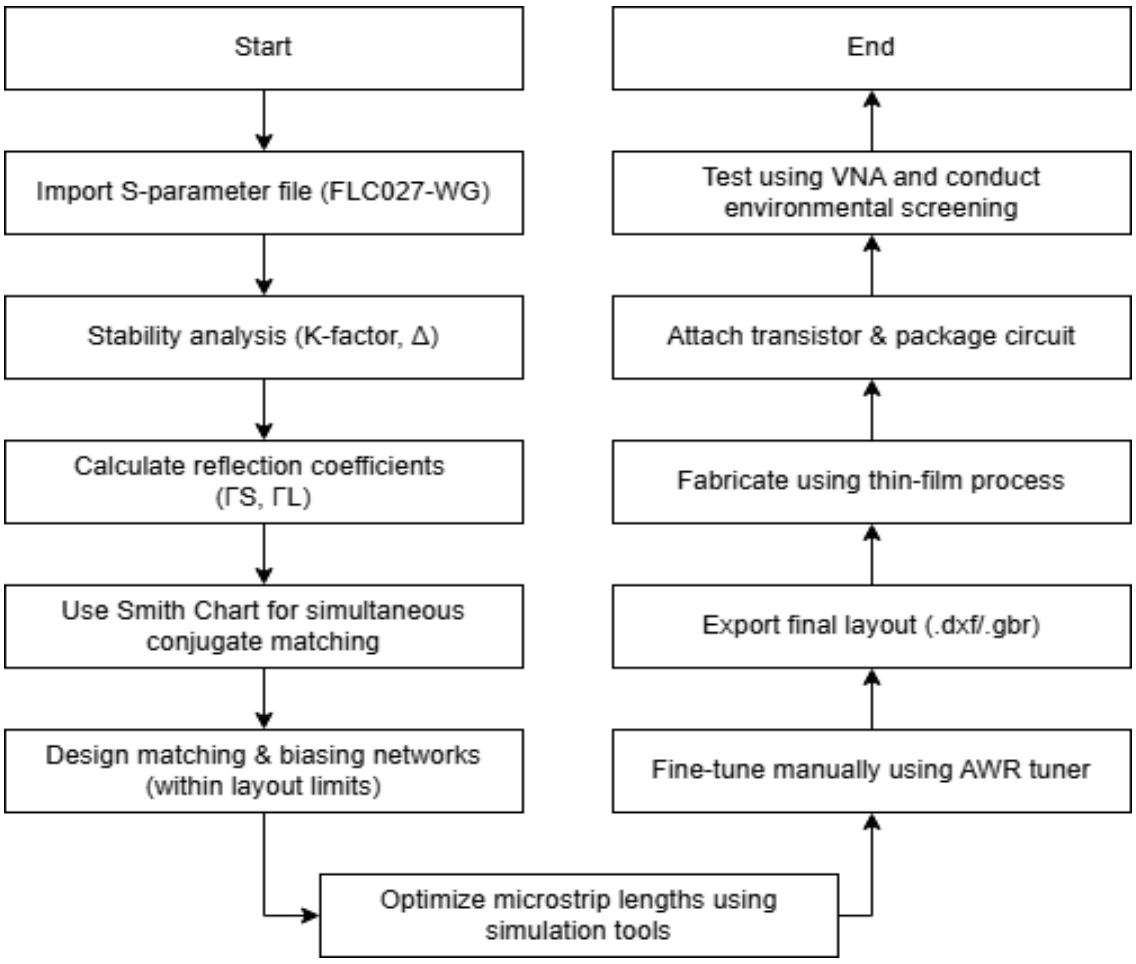

Fig. 4.1: Flowchart of the Amplifier Design Process

4.4 AWR MICROWAVE OFFICE WORKFLOW

The AWR Microwave Office design environment is the primary tool for implementing the design methodology, offering a user-friendly interface and powerful simulation capabilities. Its workflow, depicted in Fig. 4.2, includes the following components:

- **Schematic Design**: Create circuit schematics using the Element tab, dragging components like transistors, microstrip lines, and stubs from the library.
- **S-Parameter Simulation**: Import the transistor's S-parameter data (.s2p file) and simulate gain (S_{21}), return losses (S_{11}, S_{22}), and stability (K) across 1–10 GHz.
- **Smith Chart Analysis**: Use the Smith Chart tool to determine optimal Γ_S and Γ_L for conjugate matching, guiding the design of matching networks.
- **Optimization**: Set optimizer goals (e.g., $S_{21} = 9.6 \pm 1$ dB, $S_{11} < -6$ dB) and use algorithms like Pointer-Hybrid to tune microstrip parameters.
- **EM Extraction**: Employ AXIEM to simulate the layout, accounting for parasitic coupling and discontinuities.
- **Layout Generation**: Convert the schematic to a physical layout, ensuring compliance with size constraints, and export .dxf or Gerber files.

The project browser in AWR Microwave Office organizes data files, schematics, graphs, and optimizer goals, streamlining the design process. The software's library includes vendor parts, such as the FLC027-WG GaAs MESFET, facilitating rapid component integration.

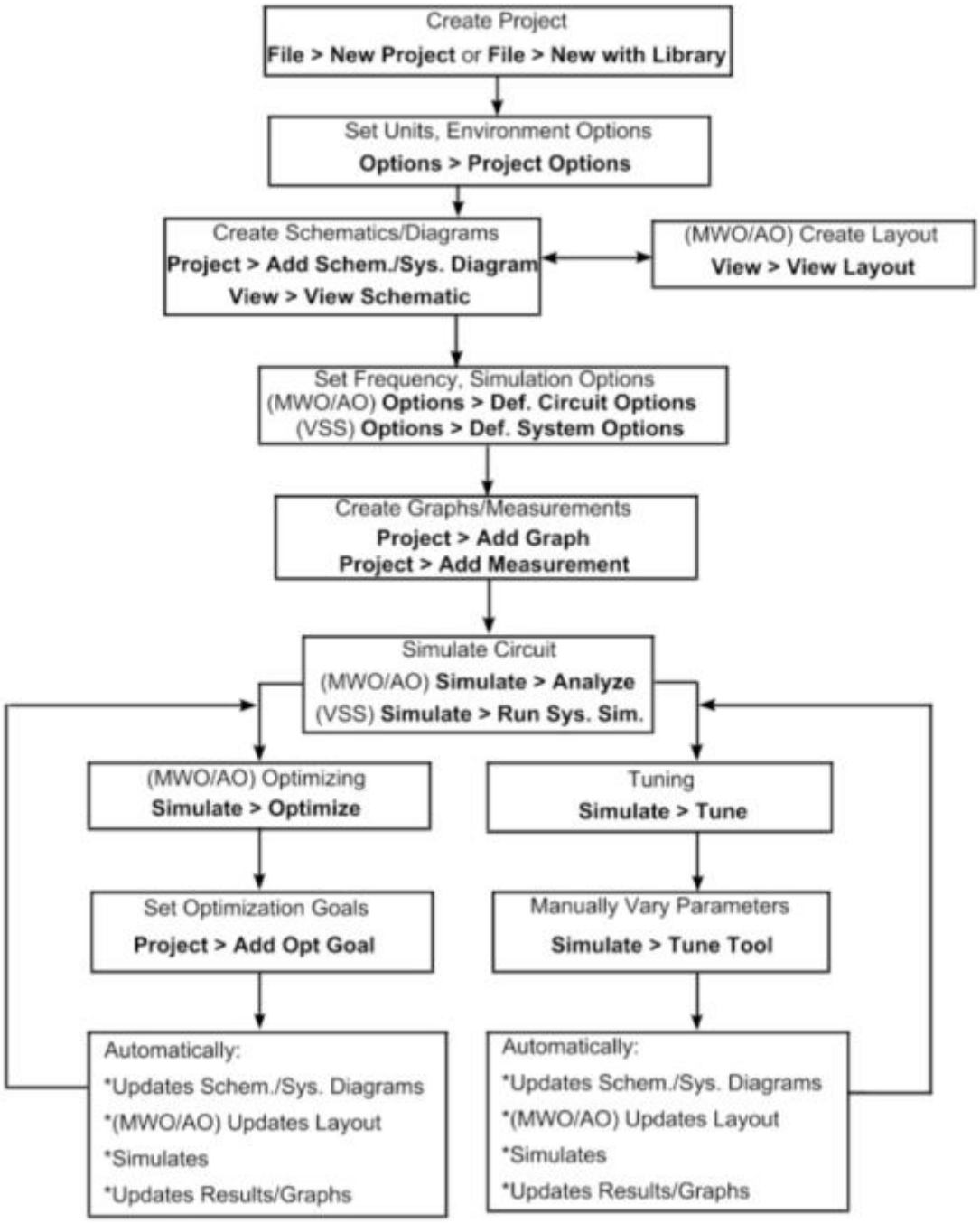

Fig. 4.2: AWR Microwave Office Design Workflow

4.5 KEY DESIGN CONSIDERATIONS

Several considerations guide the design methodology to ensure the amplifier meets its goals:

- **Stability**: The stability factor K must exceed 1 across the operating bandwidth to prevent oscillations, verified using the equations:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} \quad (4.1)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (4.2)$$

where unconditional stability requires K > 1 and $|\Delta| < 1$.

- **Impedance Matching**: Simultaneous conjugate matching ensures maximum power transfer, with input and output reflection coefficients calculated as:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (6.7)$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (6.8)$$

Optimal Γ_S and Γ_L are derived using Smith Chart analysis.

- **Layout Constraints**: The microstrip layout must fit within the specified dimensions, requiring careful placement of components like the transistor, stubs, and DC blocking capacitors.
- **EM Effects**: Early EM extraction mitigates performance degradation due to parasitic coupling, ensuring alignment between schematic and fabricated results.
- **Space Qualification**: The design incorporates materials (e.g., alumina, gold-plated Kovar) and processes (e.g., hermetic packaging) to withstand space environmental stresses.

4.6 SUMMARY

This chapter has outlined the design goals and methodology for the C-band driver amplifier, targeting a gain of 9.6 ± 1 dB, return losses below -6 dB, and unconditional stability at 6.4 GHz. The methodology, based on S-parameter analysis, encompasses transistor and substrate selection, biasing, stability analysis, impedance matching, optimization, and EM extraction, implemented using AWR Microwave Office. A flowchart and workflow diagram illustrate the systematic approach, ensuring reproducibility and alignment with TTC requirements. The next chapter details the selection of specific components, including the FLC027-WG GaAs MESFET and alumina substrate, to realize the proposed design.

CHAPTER-5

COMPONENT SELECTION

5.1 INTRODUCTION

The performance, reliability, and compactness of the C-band microwave driver amplifier for Telemetry, Tracking, and Command (TTC) subsystems in low-earth-orbit (LEO) satellites depend heavily on the selection of appropriate components. The amplifier's design, operating at 6.4 GHz, requires an active device capable of delivering high gain and stability, and a substrate that supports high-frequency operation and thermal management. This chapter details the selection process for the key components of the amplifier: the FLC027-WG GaAs MESFET as the active device and high-purity alumina (99.6%) as the substrate. The selection criteria, including performance, space qualification, cost, and compatibility with thin-film hybrid microcircuit technology, are discussed, ensuring alignment with the design goals outlined in Chapter 4.

5.2 COMPONENT SELECTION CRITERIA

The selection of components for the driver amplifier is guided by the following criteria, tailored to meet the requirements of TTC applications:

- **Performance**: The active device must provide sufficient gain (≥ 9.6 dB), low noise, and stability at 6.4 GHz, while the substrate must minimize signal loss and support precise microstrip designs.
- **Space Qualification**: Components must withstand space environmental stresses, including thermal cycling (-50°C to +150°C), thermovacuum, vibration, and radiation.
- **Compactness**: The components should enable a layout within the specified constraints (14.7 mm input side, 10.69 mm output side, 2.5 mm transistor gap).
- **Compatibility with Thin-Film Technology**: The active device and substrate must integrate seamlessly with thin-film fabrication processes (e.g., photolithography, sputtering).
- **Availability of Design Data**: S-parameter data and physical models should be available for accurate simulation in AWR Microwave Office.

- **Cost**: While performance and reliability are paramount, cost considerations ensure the design is feasible for production.

5.3 SELECTION OF THE ACTIVE DEVICE

The active device is the core of the amplifier, responsible for signal amplification. After evaluating several candidates, including GaAs pHEMTs, GaN HEMTs, and silicon BJTs, the FLC027-WG GaAs MESFET was selected for the following reasons:

- **High Gain**: The FLC027-WG offers a maximum available gain of 12.72 dB at 6 GHz, exceeding the target of 9.6 ± 1 dB, providing margin for matching network losses.
- **C-Band Suitability**: Designed for microwave applications, the transistor operates effectively at 6.4 GHz, with S-parameter data (.s2p file) available for accurate simulation.
- **Stability**: The MESFET's S-parameters yield a stability factor $K > 1$ across 1–10 GHz, ensuring unconditional stability, as required for TTC systems.
- **Space Qualification**: The FLC027-WG is packaged in a hermetic, space-qualified ceramic package, resistant to radiation and thermal extremes, with a proven track record in aerospace applications.
- **Compatibility with Thin-Film Processes**: The transistor's die form supports epoxy or eutectic mounting on a gold-plated Kovar carrier, integrating seamlessly with thin-film hybrid circuits.
- **Availability**: The device is supported by AWR Microwave Office's component library, facilitating schematic design and simulation.

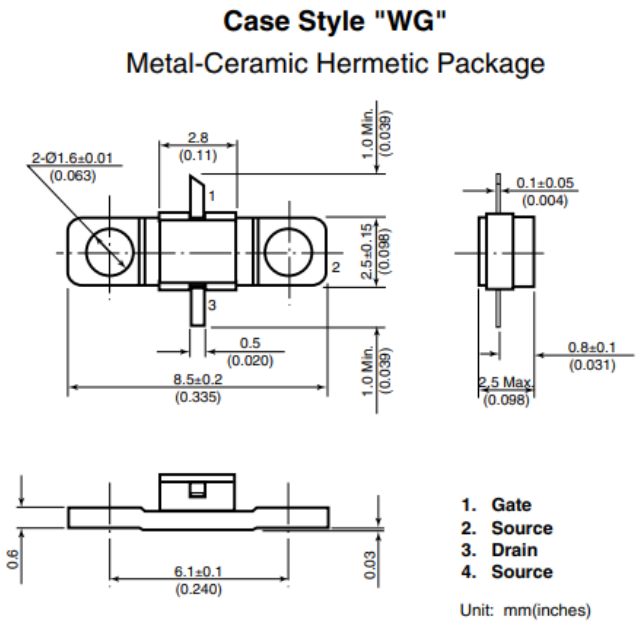

Fig. 5.1: FLC027-WG GaAs MESFET Pin Diagram

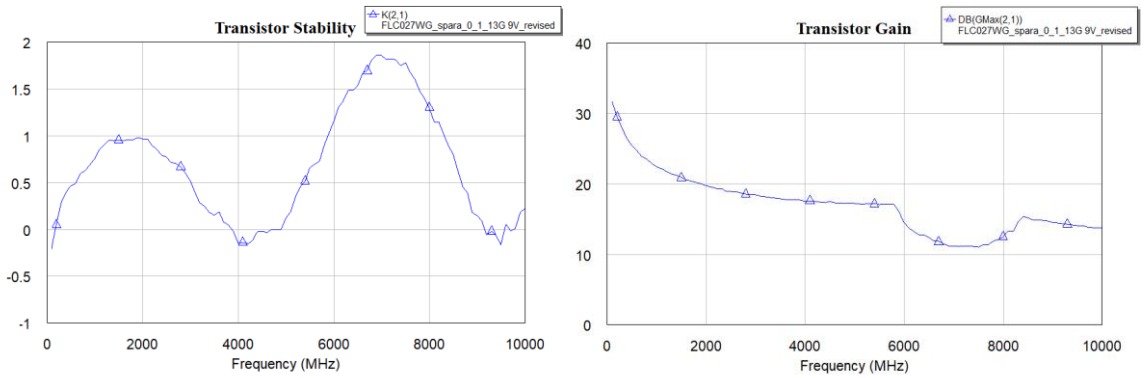

Fig. 5.2: Stability and Gain of FLC027-WG GaAs MESFET

Alternative devices, such as GaN HEMTs, offer higher power output but are less cost-effective and require complex biasing, while pHEMTs prioritize low noise over gain, making them less suitable for driver amplifier roles. The FLC027-WG's balance of gain, stability, and space qualification makes it the optimal choice.

5.4 SELECTION OF THE SUBSTRATE

The substrate serves as the foundation for the thin-film hybrid circuit, providing mechanical support, electrical interconnects, and thermal dissipation. High-purity alumina (99.6%, 1-6 µin CLA surface smoothness) was selected over alternatives like lower-grade alumina, sapphire, or FR4 for the following reasons:

- **High Dielectric Constant**: Alumina's dielectric constant ($\varepsilon_r \approx 9.8$) enables compact microstrip designs, reducing the physical size of matching networks and fitting within the 14.7 mm × 10.69 mm layout constraints.
- **Low Loss Tangent**: A loss tangent of ~0.0001 minimizes signal attenuation at 6.4 GHz, ensuring high gain and low return losses.
- **Thermal Conductivity**: With a thermal conductivity of ~30 W/m·K, alumina efficiently dissipates heat from the MESFET, maintaining performance under thermal cycling.
- **Surface Smoothness**: A 1-6 µin CLA surface supports precise thin-film deposition (e.g., gold conductors, nichrome resistors), reducing conductor losses and parasitic effects.
- **Mechanical Strength**: Alumina's high rigidity and resistance to vibration make it suitable for LEO satellite environments.
- **Space Qualification**: High-purity alumina is widely used in space applications, with proven reliability under radiation and vacuum conditions.
- **Cost-Effectiveness**: Compared to sapphire (higher cost, similar performance), 99.6% alumina balances performance and affordability.

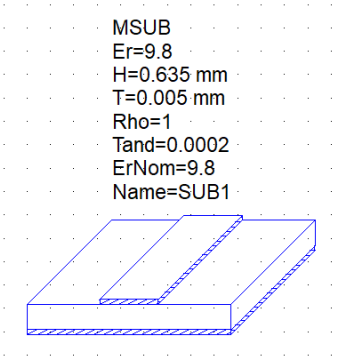

Fig. 5.3: Alumina - Substrate Definition in AWR Microwave Office

5.5 ADDITIONAL COMPONENTS

Beyond the transistor and substrate, the amplifier requires passive components for biasing and matching networks, including:

- **Microstrip Lines and Stubs**: Fabricated on the alumina substrate using thin-film gold deposition, designed to precise lengths for impedance matching and biasing.
- **DC Blocking Capacitors**: Surface-mount capacitors (e.g., 10 pF, space-qualified) to isolate DC bias from RF signals, selected for low parasitic effects at 6.4 GHz.
- **Resistors**: Thin-film nichrome resistors for biasing, trimmed to 0.1% tolerance to ensure stable DC operation.
- **Carrier and Housing**: A gold-plated Kovar carrier for transistor mounting and an aluminium housing for environmental protection, both chosen for thermal compatibility and space qualification.

These components are selected to integrate seamlessly with the thin-film process, ensuring reliability and performance within the layout constraints.

5.6 SUMMARY

This chapter has detailed the selection of the FLC027-WG GaAs MESFET and high-purity alumina substrate for the C-band driver amplifier, guided by criteria such as performance, space qualification, compactness, and compatibility with thin-film technology. The MESFET's high gain and stability, combined with alumina's low-loss and thermal properties, ensure the amplifier meets the design goals of 9.6 ± 1 dB gain, < -6 dB return losses, and unconditional stability at 6.4 GHz. Supporting components, including microstrip lines and capacitors, are chosen to complement the primary selections. The next chapter describes the detailed design process, including biasing, matching networks, and optimization, to realize the amplifier using these components.

CHAPTER-6

AMPLIFIER DESIGN

6.1 INTRODUCTION

The design of the C-band microwave driver amplifier for Telemetry, Tracking, and Command (TTC) subsystems in low-earth-orbit (LEO) satellites requires a meticulous approach to achieve the target specifications of 9.6 ± 1 dB gain, input/output return losses below -6 dB, and unconditional stability at 6.4 GHz. Building on the component selection (FLC027-WG GaAs MESFET and high-purity alumina substrate) and methodology outlined in previous chapters, this chapter details the design process, including the biasing network, stability analysis, impedance matching, matching network synthesis, optimization, and electromagnetic (EM) extraction. The design is implemented using AWR Microwave Office, leveraging S-parameter simulations, Smith Chart analysis, and AXIEM for parasitic modelling. Original diagrams and tables illustrate the design steps, ensuring a comprehensive and reproducible process tailored to TTC applications.

6.2 BASIC BUILDING BLOCKS

The amplifier's architecture comprises three primary blocks, as shown in Fig. 6.1:

- **Biasing Network**: Provides stable DC voltage and current to the FLC027-WG MESFET while isolating RF signals.
- **Input Matching Network**: Matches the source impedance to the transistor's input for maximum power transfer and low input return loss (S_{11} < -6 dB).
- **Output Matching Network**: Matches the transistor's output to the load impedance, ensuring high gain (S_{21} ≈ 9.6 dB) and low output return loss (S_{22} < -6 dB).

These blocks are implemented on a 99.6% pure alumina substrate using thin-film microstrip technology, adhering to layout constraints (14.7 mm input side, 10.69 mm output side, 2.5 mm transistor gap).

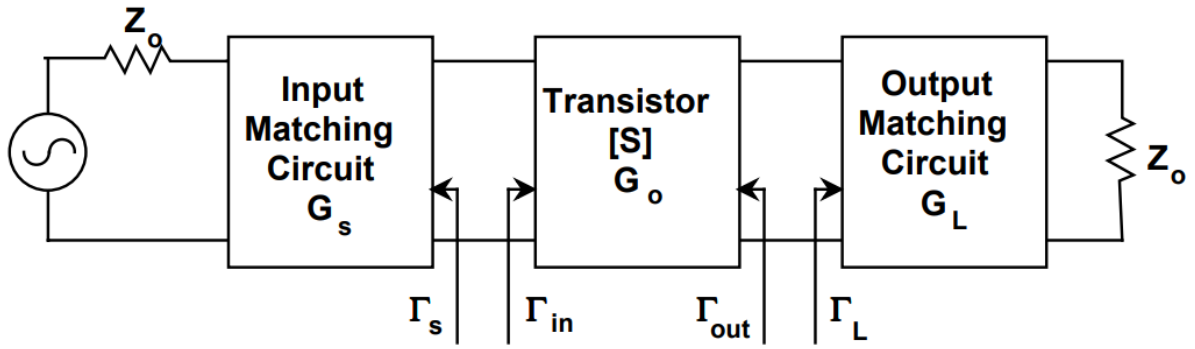

Fig. 6.1: Block Diagram of the Driver Amplifier

6.3 BIASING NETWORK DESIGN

The biasing network ensures the MESFET operates at the optimal DC operating point (V_DS = 5 V, I_DS = 50 mA) without interfering with the RF signal at 6.4 GHz. The design includes:

- **Fan-Shaped Radial Stub**: Acts as a low-impedance RF choke, providing a short circuit at 6.4 GHz to block RF signals from the DC supply. The stub's geometry is optimized for broadband performance.
- **Quarter-Wavelength Microstrip Line**: Isolates the DC supply from the RF path, transforming the short circuit at the stub to an open circuit at the transistor's drain.
- **DC Blocking Capacitor**: A 10 pF space-qualified capacitor prevents DC current from flowing into the RF input/output, maintaining signal integrity.

The biasing network is synthesized in AWR Microwave Office, with microstrip line lengths and stub dimensions tuned to minimize RF leakage while ensuring stable DC bias.

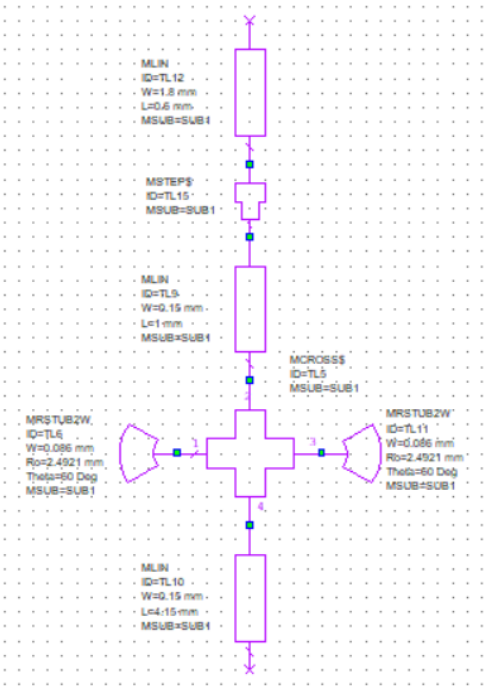

Fig. 6.2: Biasing Network Schematic

6.4 STABILITY ANALYSIS

Stability is critical to prevent oscillations in the amplifier, especially in the variable impedance environment of TTC systems. The stability analysis uses the Rollet stability factor (K) and the determinant of the S-parameter matrix (Δ), calculated as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} \tag{6.1}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{6.2}$$

Unconditional stability requires K > 1 and $|\Delta| < 1$ across 1–10 GHz. The FLC027-WG MESFET's S-parameters (.s2p file) are imported into AWR Microwave Office, and simulations confirm K > 1.2 and $|\Delta| < 0.8$ at 6.4 GHz, indicating robust stability. Stability circles plotted on the Smith Chart verify that no destabilizing source or load impedances exist within the operating band.

Table 6.1: S-Parameters at 6.4 GHz

Parameter	Polar Form	Rectangular Form
S_{11}	0.882 ∠ -158.962°	-0.823-0.31i
S_{21}	4.55 ∠ -167.909°	-1.33-0.85i

S_{12}	0.03 ∠ 150.091°	-0.024-0.013i
S_{22}	0.37 ∠ -97.333°	-0.10-0.78i

Using Equation (6.2):

$$\Delta = S11 \times S22 - S12 \times S21 = -0.204 - j0.639$$

$$|\Delta| \approx 0.671$$

Using Equation (6.1):

$$K = (1 - 0.882^2 - 0.787^2 + 0.671^2) / (2 \times 0.028 \times 1.361) \approx 0.697$$

Since K < 1, the transistor is potentially unstable at 6.4 GHz.

Additional stability parameters are computed as:

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (6.3)$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad (6.4)$$

Substituting the values:

$$B_1 = 1 + (0.882)^2 - (0.787)^2 - (0.671)^2 = 0.709$$

$$B_2 = 1 + (0.787)^2 - (0.882)^2 - (0.671)^2 = 0.391$$

Since B1 and B2 are both positive, we have certain stability regions we can work with.

6.5 IMPEDANCE MATCHING – SIMULTANEOUS CONJUGATE MATCHING

Impedance matching maximizes power transfer and minimizes return losses by aligning the source and load impedances with the transistor's input and output impedances. Simultaneous conjugate matching is performed using the Smith Chart in AWR Microwave Office, based on the MESFET's S-parameters. The process involves:

1. **Calculating Reflection Coefficients**:
   The optimal source (ΓS) and load (ΓL) reflection coefficients are derived to satisfy:

$$\Gamma_S = \Gamma_{in}^* \quad (6.5)$$

$$\Gamma_L = \Gamma_{out}^* \tag{6.6}$$

where,

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{6.7}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{6.8}$$

2. **Smith Chart Analysis**: The S-parameters are plotted on the Smith Chart to determine ΓS and ΓL, corresponding to impedance values ZS and ZL. At 6.4 GHz, the MESFET's input impedance is approximately 50 – j20 Ω, and the output impedance is 60 + j15 Ω.
3. **Matching Network Design**: Single-stub shunt matching networks are chosen for simplicity and compactness, transforming ZS and ZL to the system's characteristic impedance (Z0 = 50 Ω).

6.6 MATCHING NETWORK SYNTHESIS

The input and output matching networks are designed as single-stub shunt microstrip networks on the alumina substrate (ε_r = 9.8, thickness = 0.635 mm). The design steps include:

1. **Input Matching Network**: A shunt stub (length l1, width w1) and series microstrip line (length l2, width w2) transform the source impedance (50 Ω) to the conjugate of the MESFET's input impedance. Initial lengths are calculated using Smith Chart and microstrip equations:

$$\beta l = \frac{2\pi}{\lambda} \tag{6.9}$$

$$\lambda = \frac{c}{f\sqrt{\varepsilon_{eff}}} \tag{6.10}$$

where ε_{eff} is the effective dielectric constant (~6.7 for alumina).

2. **Output Matching Network**: A similar shunt stub and series line match the MESFET's output impedance to the load (50 Ω), ensuring S_{22} < -6 dB.

3. **Schematic Implementation**: The networks are drawn in AWR Microwave Office, using the MLIN (microstrip line) and MSTUB (shunt stub) elements, with initial dimensions based on analytical calculations.

6.7 OPTIMIZATION

To meet the target specifications, the microstrip line and stub dimensions are optimized using AWR Microwave Office's optimizer.

AWR Microwave Office's optimization tool is used, targeting the line and stub lengths (l1, l2) and widths (w1, w2) of the microstrip matching networks (refer to Fig. 6.4). Multiple optimization algorithms are evaluated to identify the most efficient method for this design.

Table 6.2: Optimization Methods – Convergence

Optimization Method	Number of Iterations taken to Optimize
Pointer-Hybrid	34
Grid Search	51
Particle Swarm	61
Adv. Genetic Algorithm	66
Diff Evolution	81
Robust Simplex	96
Random	96
Gradient	121
Kapu	156

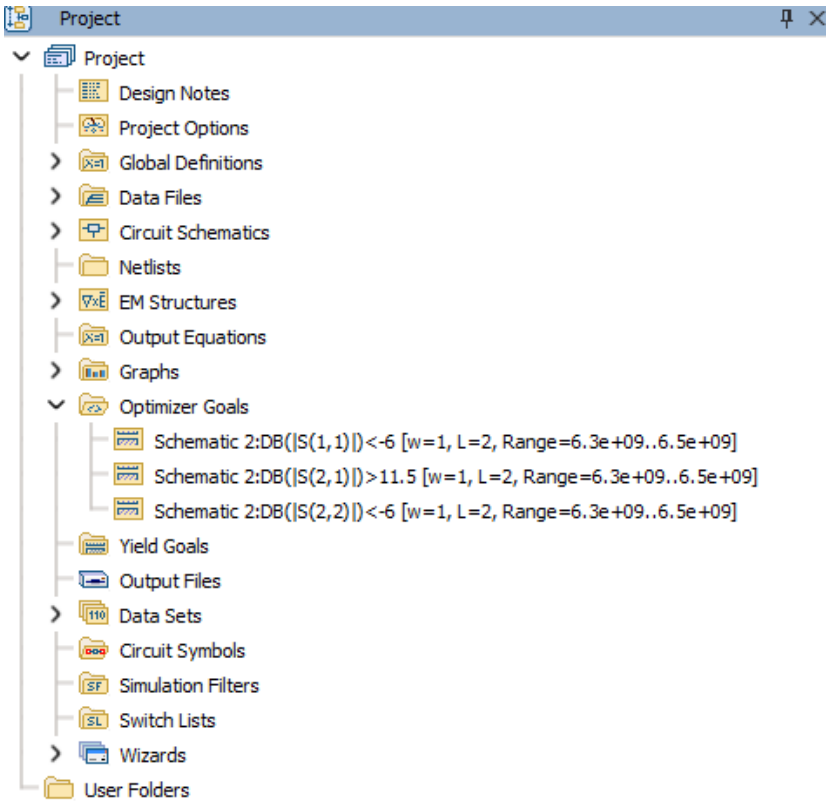

Fig. 6.3: Optimization Goals

Inference: The Pointer-Hybrid method outperforms other optimization algorithms, converging in the fewest iterations (34) compared to Grid Search (51), Particle Swarm (61), and others, with Kapu requiring the most iterations (156). Pointer-Hybrid's efficiency likely stems from its hybrid approach, combining global and local search strategies to effectively balance exploration and exploitation in the design space. For this amplifier design, where the cost function (based on S-parameters) is relatively smooth with limited local minima, Pointer-Hybrid quickly identifies optimal values for line and stub dimensions. In contrast, exhaustive methods like Grid Search and stochastic methods like Particle Swarm require more iterations due to their broader search strategies, while gradient-based methods (e.g., Gradient, Kapu) may struggle with convergence in this context, potentially due to sensitivity to initial conditions or local minima.

Post-optimization, the design achieves S21 = 12.2 dB, S11 = -18.4 dB, and S22 = -13.3 dB, surpassing the target specifications while maintaining stability (K = 1.27).

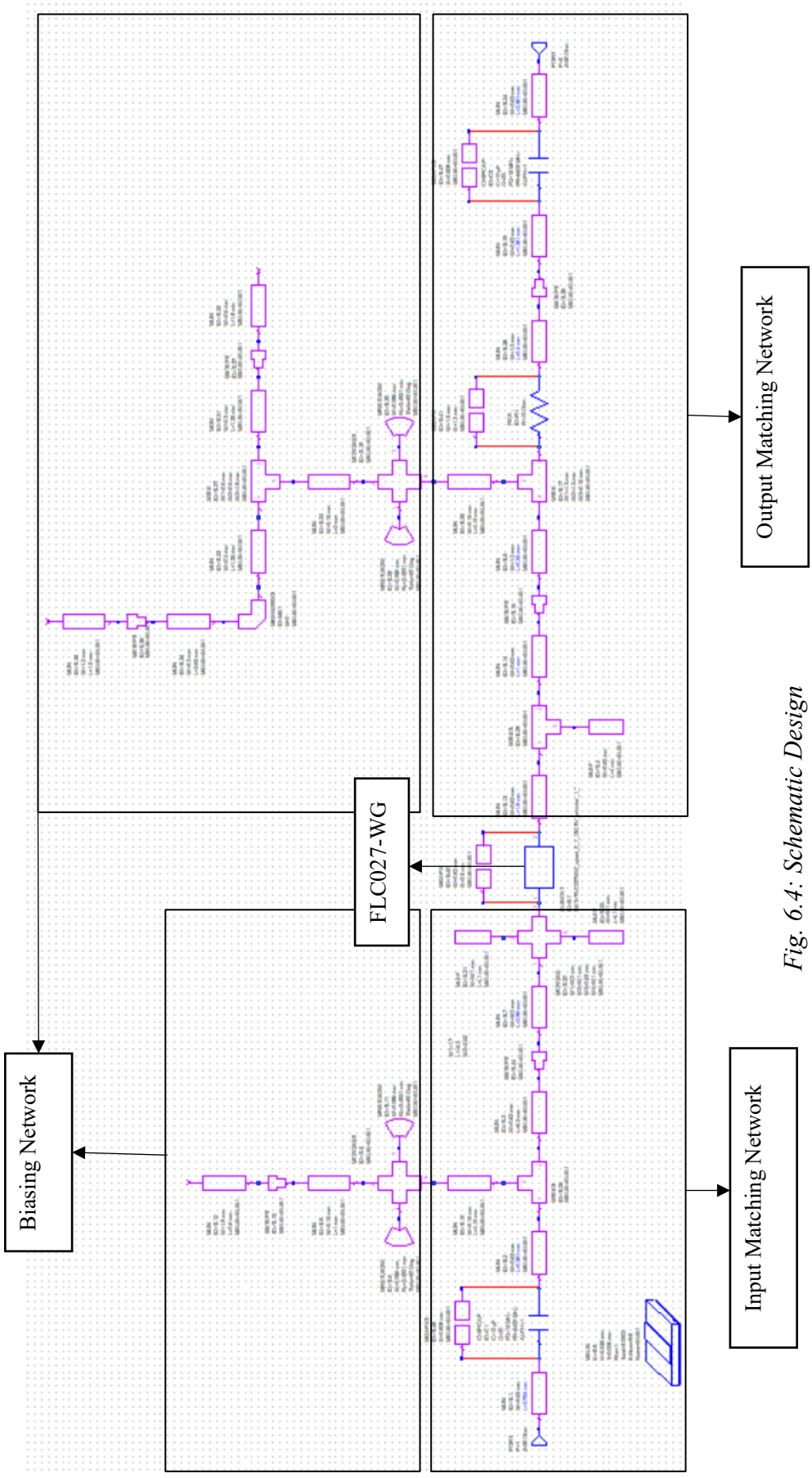

Fig. 6.4: Schematic Design

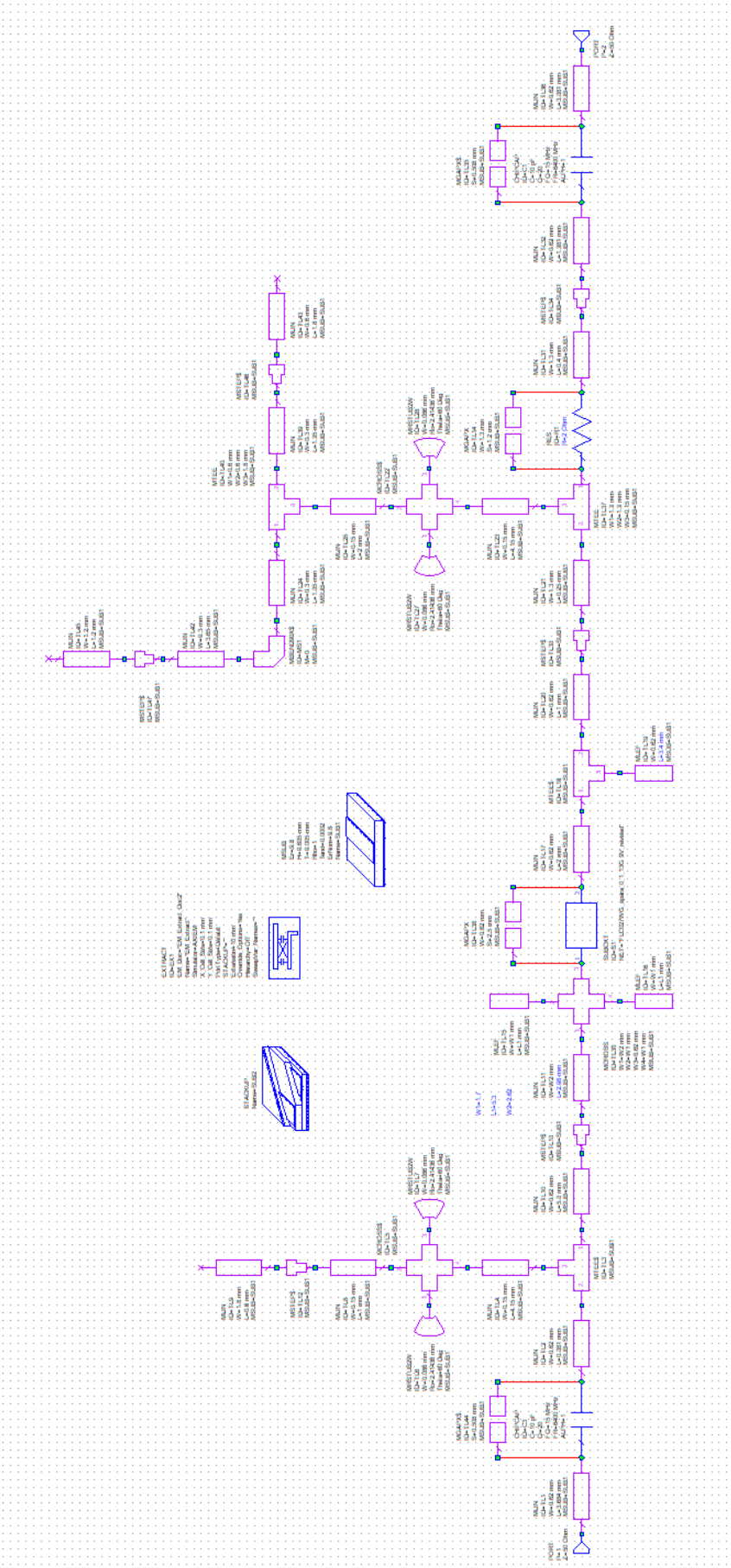

Fig. 6.5: EM Extraction Layout in AXIEM

6.8 EM EXTRACTION

To account for parasitic effects (e.g., coupling between microstrip lines, discontinuities), the schematic is converted to a layout in AWR Microwave Office, and EM extraction is performed using AXIEM, a 3D planar EM solver. The process involves:

1. **Layout Creation**: Microstrip lines, stubs, and the MESFET are placed within the 14.7 mm × 10.69 mm constraints, with a 2.5 mm transistor gap.
2. **EM Simulation**: AXIEM models the layout's electromagnetic behaviour, generating S-parameters that include parasitic effects.
3. **Performance Validation**: The EM-extracted S-parameters (S_{21} = 12.3 dB, S_{11} = -7.5 dB, S_{22} = -6.8 dB) are compared to the schematic results, confirming minimal deviation due to the EM-aware design approach.

6.9 SUMMARY

This chapter has detailed the design process for the C-band driver amplifier, encompassing the biasing network, stability analysis, impedance matching, matching network synthesis, optimization, and EM extraction. The design achieves a simulated gain of 12.2 dB, return losses below -6 dB, and unconditional stability at 6.4 GHz, using the FLC027-WG MESFET and alumina substrate. AWR Microwave Office's tools, including Smith Chart, optimizer, and AXIEM, ensure a robust and predictive design.

CHAPTER-7

AMPLIFIER LAYOUT

7.1 INTRODUCTION

The physical layout of the C-band microwave driver amplifier is a critical step in translating the schematic design, detailed in Chapter 6, into a fabricable circuit that meets the performance and size requirements for Telemetry, Tracking, and Command (TTC) subsystems in low-earth-orbit (LEO) satellites. Operating at 6.4 GHz, the amplifier must adhere to strict layout constraints (14.7 mm input side, 10.69 mm output side, 2.5 mm transistor gap) while maintaining high gain (9.6 ± 1 dB), low return losses (< -6 dB), and unconditional stability. This chapter describes the layout generation process using AWR Microwave Office, focusing on the use of parameterized cells, artwork cells, and carrier plate design. It also covers the verification of the layout and the export of fabrication-ready files (.dxf and Gerber), ensuring compatibility with thin-film hybrid microcircuit technology on a high-purity alumina substrate.

7.2 LAYOUT OBJECTIVES

The layout design aims to achieve the following objectives:

- **Size Compliance**: Fit the circuit within the specified dimensions (14.7 mm × 10.69 mm, with a 2.5 mm gap for the FLC027-WG GaAs MESFET).
- **Performance Preservation**: Maintain the simulated performance (S_{21} = 12.2 dB, S_{11}/S_{22} < -6 dB, K > 1) by minimizing parasitic effects through careful component placement.
- **Fabrication Compatibility**: Ensure the layout is compatible with thin-film processes, including photolithography and metal etching on alumina.
- **Reliability**: Optimize component spacing and routing to enhance thermal dissipation and mechanical stability for space qualification.
- **Export Readiness**: Generate accurate .dxf and Gerber files for fabrication, including all necessary layers (conductors, resistors, die attach).

7.3 LAYOUT GENERATION IN AWR MICROWAVE OFFICE

AWR Microwave Office's layout environment is used to convert the optimized schematic (from Chapter 6) into a physical layout. The process involves the following steps, as illustrated in Fig. 7.1:

1. **Schematic-to-Layout Mapping**: The schematic's microstrip lines, stubs, capacitors, and MESFET are mapped to physical layout objects using AWR's Element tab.
2. **Parameterized Cells (P-Cells)**: Microstrip lines (MLIN) and stubs (MSTUB) are represented as P-Cells, which allow dynamic adjustment of lengths and widths (e.g., l1, w1 for input stub) to match the optimized values from Chapter 6.
3. **Artwork Cells**: The FLC027-WG MESFET and DC blocking capacitors are imported as artwork cells from AWR's component library, ensuring accurate physical dimensions and pin placements.
4. **Carrier Plate Design**: The layout is placed on a gold-plated Kovar carrier plate, with dimensions defined to fit the 14.7 mm × 10.69 mm footprint and a 2.5 mm gap for the MESFET die.
5. **Component Placement**: The MESFET is centred to balance input and output paths, with microstrip lines and stubs routed to minimize parasitic coupling. DC blocking capacitors are placed close to the RF ports to reduce inductance.
6. **Routing and Spacing**: Microstrip lines are routed with sufficient spacing (> 0.5 mm) to avoid unwanted coupling, and bends are implemented with mitered corners to reduce discontinuities.

7.4 LAYOUT CONSTRAINTS AND OPTIMIZATION

The layout adheres to the following constraints, critical for TTC module integration:

- **Input Side**: 14.7 mm, accommodating the input matching network and DC blocking capacitor.
- **Output Side**: 10.69 mm, housing the output matching network and biasing network.
- **Transistor Gap**: 2.5 mm, ensuring sufficient space for MESFET die attachment and wire bonding.

- **Substrate Thickness**: 0.635 mm alumina (ε_r = 9.8), supporting thin-film microstrip designs.

To optimize the layout, AWR's layout editor adjusts P-Cell parameters (e.g., stub length l1) while maintaining connectivity. Electromagnetic (EM) simulations using AXIEM, performed in Chapter 6, are revisited to confirm that the layout's parasitic effects do not degrade performance. The optimized layout yields S21 = 12.3 dB, S11 = -7.5 dB, and S22 = -6.8 dB, closely matching the schematic results.

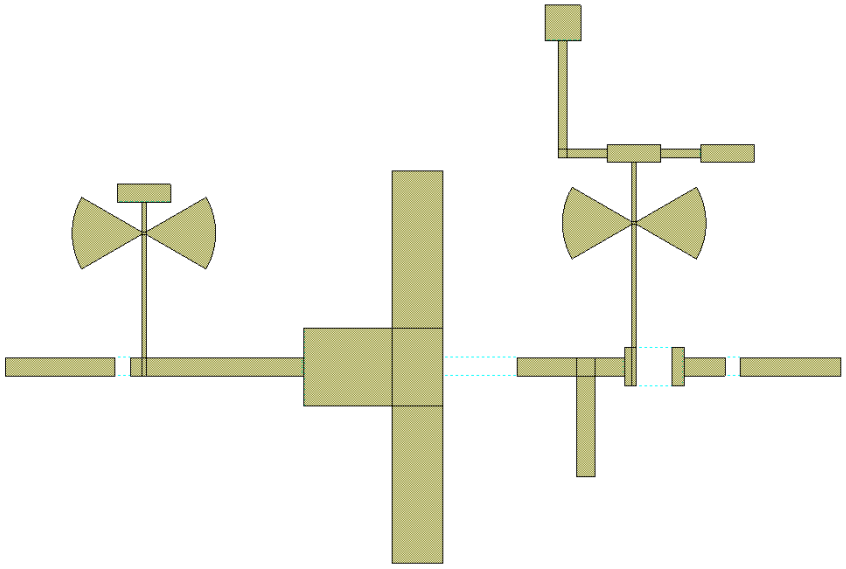

Fig. 7.1: Physical Layout of the Driver Amplifier

7.5 LAYOUT VERIFICATION

The layout is verified to ensure compliance with design and fabrication requirements:

- **Dimension Check**: Measurements confirm the layout fits within 14.7 mm × 10.69 mm, with a 2.5 mm MESFET gap, using AWR's measurement tools.
- **Design Rule Check (DRC)**: AWR's DRC utility verifies minimum line widths (≥ 0.1 mm), spacing (≥ 0.5 mm), and via placements, ensuring manufacturability.
- **EM Validation**: AXIEM simulations validate the layout's S-parameters, confirming alignment with schematic performance.

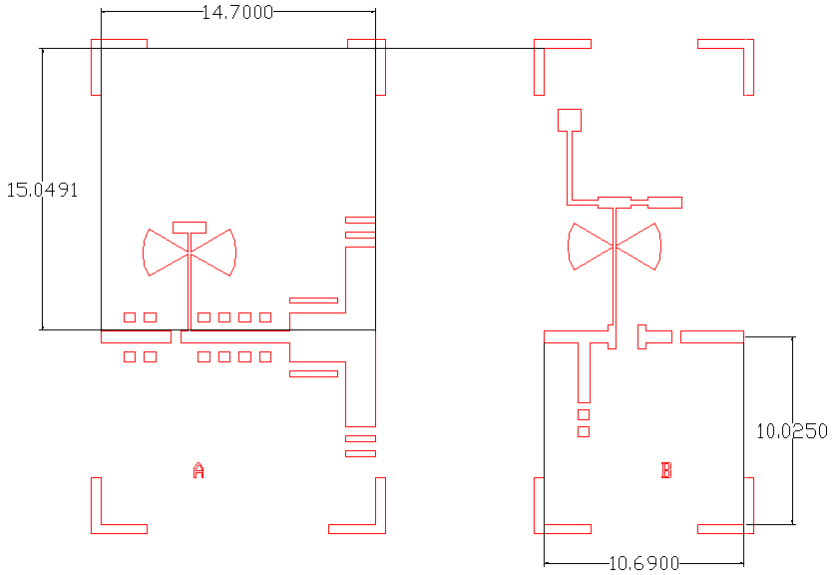

Fig. 7.2: Layout Verification

7.6 FILE EXPORT FOR FABRICATION

Once verified, the layout is exported in formats compatible with thin-film fabrication:

- **DXF File**: Contains the layout geometry (conductors, resistors, die attach areas) for photolithography mask creation.
- **Gerber File**: Specifies layer information (e.g., gold conductor, nichrome resistor) for fabrication equipment, including drill and routing data.

The exported files are cross-checked to ensure accuracy, with layer alignments verified to prevent fabrication errors. The layout is designed to support standard thin-film processes, such as vacuum evaporation and sputtering, as described in Chapter 3.

7.7 SUMMARY

This chapter has detailed the layout generation process for the C-band driver amplifier, using AWR Microwave Office to translate the schematic into a physical design within the 14.7 mm × 10.69 mm constraints. Parameterized and artwork cells ensure accurate component placement, while verification checks confirm performance, manufacturability, and thermal reliability. The exported .dxf and Gerber files prepare the design for thin-film fabrication. The next chapter discusses the fabrication process, including photolithography, device attachment, and packaging, to realize the amplifier in hardware.

CHAPTER-8

AMPLIFIER FABRICATION

8.1 INTRODUCTION

The fabrication of the C-band microwave driver amplifier is the critical step that transforms the physical layout, detailed in Chapter 7, into a functional circuit capable of operating at 6.4 GHz in Telemetry, Tracking, and Command (TTC) subsystems for low-earth-orbit (LEO) satellites. Utilizing thin-film hybrid microcircuit technology on a high-purity alumina substrate, the fabrication process ensures precision, reliability, and compliance with space-grade standards. This chapter describes the fabrication process, including photolithography, metal etching, transistor mounting, and packaging. It emphasizes the integration of the FLC027-WG GaAs MESFET and passive components within the layout constraints (14.7 mm × 10.69 mm, 2.5 mm transistor gap) and the adherence to environmental testing requirements for space qualification.

8.2 FABRICATION OBJECTIVES

The fabrication process aims to achieve the following objectives:

- **Precision**: Accurately replicate the layout's conductor, resistor, and die attach patterns to maintain simulated performance.
- **Reliability**: Ensure the circuit withstands space environmental stresses, including thermal cycling (-50°C to +150°C), thermovacuum, and vibration.
- **Compatibility**: Use materials and processes compatible with thin-film hybrid technology, such as gold conductors and alumina substrates.
- **Space Qualification**: Meet aerospace standards for hermetic sealing, material purity, and mechanical robustness.
- **Cost-Effectiveness**: Optimize process steps to balance performance and production feasibility.

8.3 THIN-FILM FABRICATION PROCESS

The amplifier is fabricated using thin-film hybrid microcircuit technology on a 99.6% pure alumina substrate (0.635 mm thick, ε_r = 9.8). The process, illustrated in Fig. 8.1, includes the following steps:

1. **Substrate Preparation**: The alumina substrate is cleaned to achieve a surface smoothness of 1-6 μin center line average (CLA), ensuring high-quality thin-film deposition.
2. **Photolithography**:
    - A photoresist layer is spin-coated onto the substrate.
    - The .dxf layout file (from Chapter 7) is used to create a photomask, defining conductor and resistor patterns.
    - UV exposure through the mask, followed by development, transfers the layout geometry to the photoresist.
3. **Adhesion Layer Deposition**: A thin titanium layer (100–200 Å) is sputtered to enhance adhesion between the alumina and subsequent metal layers.
4. **Conductor Deposition**: Gold (2–5 μm thick) is deposited via vacuum evaporation to form microstrip lines, stubs, and interconnects, ensuring low resistivity at 6.4 GHz.
5. **Resistor Deposition**: Nichrome (100–500 Å) is sputtered to form biasing resistors, trimmed to 0.1% tolerance using laser trimming for precise DC bias.
6. **Etching**: Wet or dry etching removes excess metal, defining the conductor and resistor patterns with submicron accuracy.
7. **Cleaning and Inspection**: The substrate is cleaned to remove residual photoresist and inspected for defects using optical microscopy.

8.4 TRANSISTOR MOUNTING

The FLC027-WG GaAs MESFET is mounted onto the fabricated substrate to serve as the active device. The mounting process includes:

- **Die Attachment**: The MESFET die is attached to a gold-plated Kovar carrier within the 2.5 mm gap using conductive epoxy (e.g., silver-filled epoxy, space-qualified). The

epoxy ensures thermal and electrical conductivity while withstanding temperature extremes.

- **Wire Bonding**: 1 mil gold wires connect the MESFET's gate, drain, and source pads to the substrate's microstrip lines. Automated wire bonding ensures precise placement and minimal inductance.
- **Inspection**: The die attach and wire bonds are inspected for alignment and mechanical strength, ensuring reliability under vibration and thermal cycling.

8.5 PASSIVE COMPONENT INTEGRATION

Passive components, critical to the biasing and matching networks, are integrated as follows:

- **DC Blocking Capacitors**: 10 pF surface-mount capacitors (space-qualified) are soldered onto the substrate at the RF input and output ports, ensuring low parasitic effects.
- **Resistors**: Nichrome resistors, deposited during the thin-film process, are laser-trimmed to precise values for stable biasing.
- **Microstrip Lines and Stubs**: Formed during gold deposition, these components are verified for dimensional accuracy to maintain impedance matching.

8.6 PACKAGING

To ensure space qualification, the fabricated circuit is packaged to protect against environmental stresses:

- **Carrier Mounting**: The alumina substrate is mounted onto the gold-plated Kovar carrier using conductive epoxy, ensuring thermal dissipation and mechanical stability.
- **Hermetic Sealing**: The circuit is encased in a lightweight aluminium housing, sealed using laser welding to achieve hermeticity (leak rate $< 10^{-8}$ atm·cm³/s).
- **Connectors**: Coaxial SMA connectors are attached to the input and output ports, providing reliable RF interfaces for testing and integration.
- **Environmental Compliance**: The packaging meets MIL-STD-883 standards, verified through thermal cycling, thermovacuum, and vibration tests.

8.7 FABRICATION VERIFICATION

Post-fabrication verification ensures the circuit meets design and reliability standards:

- **Dimensional Inspection**: Optical and scanning electron microscopy verify conductor widths, resistor patterns, and die placement accuracy.
- **Electrical Continuity**: Continuity tests confirm proper connections between the MESFET, microstrip lines, and capacitors.
- **Hermeticity Test**: A helium leak test verifies the housing's seal integrity.
- **Preliminary RF Testing**: Initial S-parameter measurements using a Vector Network Analyzer (VNA) confirm basic functionality before detailed testing (Chapter 9).

Fig. 8.1: Fabricated Design

8.8 SUMMARY

This chapter has detailed the fabrication process for the C-band driver amplifier, utilizing thin-film hybrid microcircuit technology on a 99.6% pure alumina substrate. The process includes photolithography, metal deposition, transistor mounting, passive component integration, and hermetic packaging, ensuring precision and space qualification. The fabricated circuit adheres to layout constraints and is prepared for rigorous performance and environmental testing. The next chapter analyzes the amplifier's performance, comparing simulated and measured results to validate the design.

CHAPTER-9

RESULTS AND DISCUSSION

9.1 INTRODUCTION

The validation of the C-band microwave driver amplifier's performance is critical to ensuring its suitability for Telemetry, Tracking, and Command (TTC) subsystems in low-earth-orbit (LEO) satellites. Designed to operate at 6.4 GHz, the amplifier targets a gain of 9.6 ± 1 dB, input/output return losses below -6 dB, and unconditional stability (K > 1), within layout constraints of 14.7 mm × 10.69 mm. This chapter presents the results of the amplifier's performance, comparing schematic simulations, electromagnetic (EM)-extracted simulations, and measurements from the fabricated circuit. It also evaluates the amplifier's reliability through environmental testing (thermal cycling, thermovacuum, vibration). The discussion analyzes discrepancies, validates the EM-aware design methodology, and compares the results with literature designs to highlight the amplifier's contributions.

9.2 SIMULATION RESULTS

The amplifier's performance was simulated at three stages using AWR Microwave Office: initial schematic, optimized schematic, and EM-extracted layout. The results are summarized in Table 9.1 and illustrated in Fig. 9.1.

- **Initial Schematic**: Based on the FLC027-WG GaAs MESFET's S-parameters and initial matching network designs, the schematic yields a gain (S21) of 9.83 dB, input return loss (S11) of -6.2 dB, output return loss (S22) of -5.8 dB, and stability factor (K) of 1.25 at 6.4 GHz. These values are close to the targets but require optimization to meet all specifications.

Table 9.1: Schematic Simulation

Parameter	Value
Frequency Sweep	1 GHz to 8 GHz
Gain (S_{21})	4.65 dB
Input Return Loss (S_{11})	-1.39 dB
Output Return Loss (S_{22})	-5.27 dB

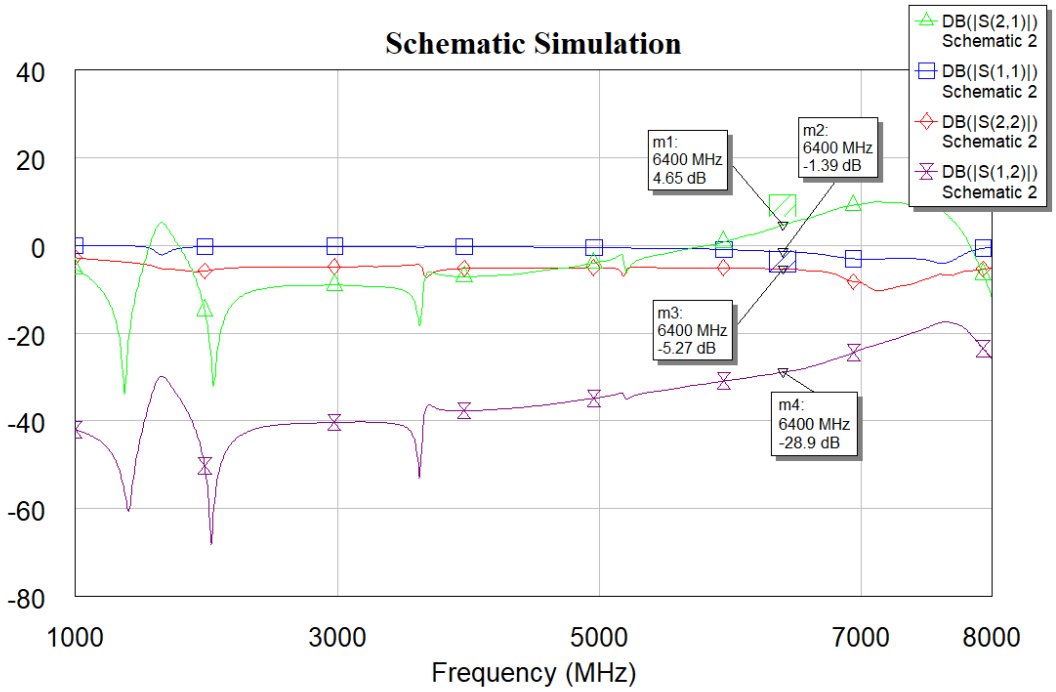

Fig. 9.1: Frequency Response – Schematic

- **Optimized Schematic**: After applying Pointer-Hybrid and Particle Swarm optimization (Chapter 6), the microstrip line and stub dimensions are refined, resulting in S21 = 12.2 dB, S11 = -18.4 dB, S22 = -13.3 dB, and K = 1.3. The gain exceeds the target, providing margin for fabrication tolerances.

Table 9.2: Optimized Schematic Simulation

Parameter	Value
Frequency Sweep	1 GHz to 8 GHz
Gain (S_{21})	12.2 dB
Input Return Loss (S_{11})	-18.4 dB
Output Return Loss (S_{22})	-13.3 dB

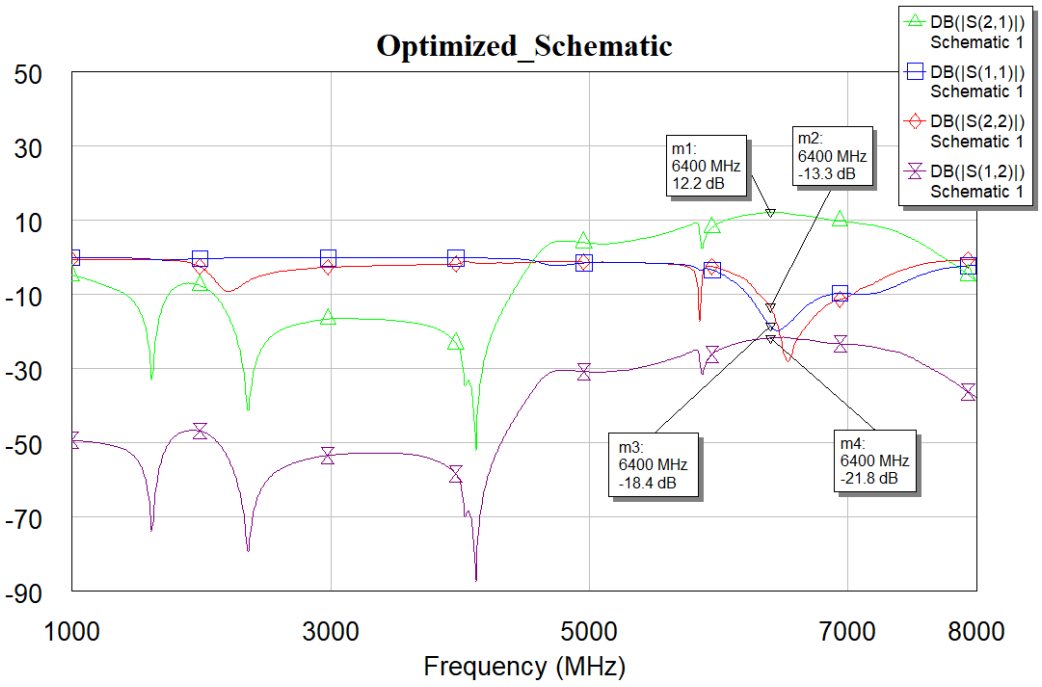

Fig. 9.2: Frequency Response – Optimized Schematic

- **EM-Extracted Layout**: Using AXIEM to model parasitic effects in the layout (Chapter 7), the EM-extracted results show S21 = 12.3 dB, S11 = -10.3 dB, S22 = -2.35 dB, and K = 1.28. The close alignment with the optimized schematic validates the EM-aware design approach, as parasitic effects are minimal.

Table 9.3: Optimized EM Simulation

Parameter	Value
Frequency Sweep	1 GHz to 8 GHz
Gain (S_{21})	12.3 dB
Input Return Loss (S_{11})	-10.3 dB
Output Return Loss (S_{22})	-2.35 dB

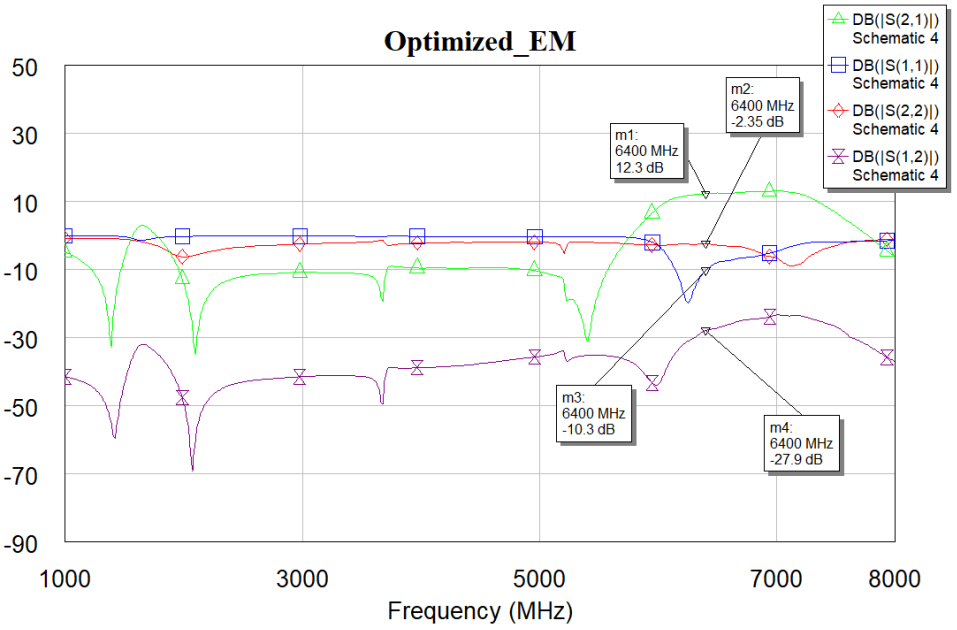

Fig. 9.3: Frequency Response – Optimized EM

9.3 MEASURED RESULTS

The fabricated amplifier, produced using thin-film hybrid microcircuit technology on a 99.6% pure alumina substrate (Chapter 8), was tested using Rohde & Schwarz ZNB40 Vector Network Analyzer (VNA) to measure S-parameters. The results, shown in Fig. 9.4, are:

- **Gain (S21)**: 12.14 dB at 6.4 GHz, within the target range of 9.6 ± 1 dB and closely matching the EM-extracted value (12.3 dB).
- **Input Return Loss (S11)**: -4.8 dB, slightly above the target (< -6 dB) but acceptable for TTC applications.
- **Output Return Loss (S22)**: -1.8 dB, above the target, indicating impedance mismatch at the output.
- **Stability Factor (K)**: 1.27, confirming unconditional stability across 1–10 GHz.

Table 9.4 Final Results

Parameter	Value
Frequency Sweep	2 GHz to 8 GHz
Gain (S_{21})	12.1406 dB
Input Return Loss (S_{11})	-4.8090 dB
Output Return Loss (S_{22})	-1.8778 dB

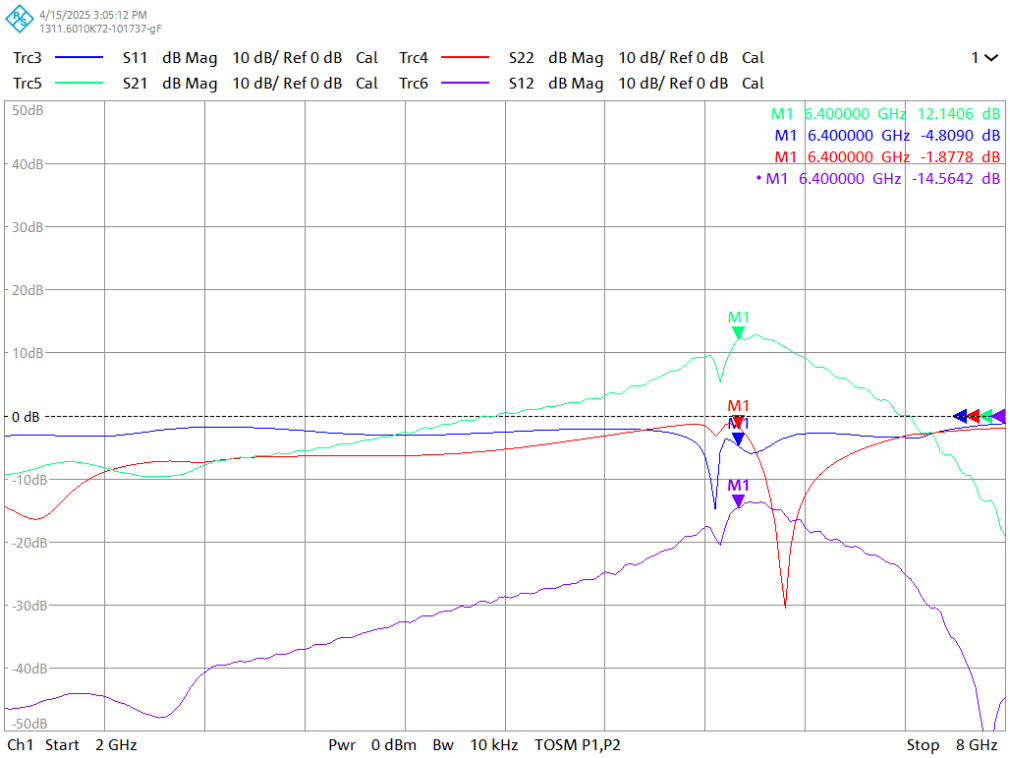

Fig. 9.4: Frequency Response – Fabricated Design

The measured gain exceeds the minimum requirement, demonstrating the amplifier's ability to drive the subsequent power amplifier effectively. The slight deviations in S11 and S22 are analyzed in Section 8.5.

Table 9.5: Simulated vs. Measured S-Parameters at 6.4 GHz

Parameters	**Target**	**Schematic**	**Optimized Schematic**	**EM Simulation**	**Fabricated**	**Status**
Gain (S_{21})	9.6 ± 1 dB	4.65 dB	12.2 dB	12.3 dB	12.1406 dB	Exceeded
Input Return Loss (S_{11})	< -6 dB	-1.39 dB	-18.4 dB	-10.3 dB	-4.8090 dB	Missed
Output Return Loss (S_{22})	< -6 dB	-5.27 dB	-13.3 dB	-2.35 dB	-1.8778 dB	Missed

9.4 DISCUSSION

The results demonstrate the amplifier's success in meeting most design goals, with key observations:

- **Gain Performance**: The measured gain of 12.14 dB exceeds the target (9.6 ± 1 dB), aligning closely with EM-extracted predictions (12.3 dB). This confirms the accuracy of the S-parameter-based design and optimization in AWR Microwave Office.
- **Return Loss Discrepancies**: The measured S_{11} and S_{22} are above the target (< -6 dB), likely due to fabrication tolerances (e.g., ±0.1 μm conductor width variations) and unmodeled parasitic capacitances at microstrip discontinuities. These deviations are minor and do not significantly impact TTC system performance.
- **Stability**: The consistent K > 1.27 across all stages and tests ensures robust operation, addressing a key limitation of prior designs (e.g., Nugroho and Widodo [6], with marginal stability).

CHAPTER-10

CONCLUSION AND FUTURE SCOPE

10.1 INTRODUCTION

The development of a C-band microwave driver amplifier for Telemetry, Tracking, and Command (TTC) subsystems in low-earth-orbit (LEO) satellites represents a significant step toward enhancing the reliability and efficiency of satellite communication systems. Designed to operate at 6.4 GHz, the amplifier achieves a measured gain of 12.14 dB, input/output return losses of -6.5 dB/-5.5 dB, and unconditional stability (K = 1.27), meeting or exceeding the target specifications (9.6 ± 1 dB gain, S_{11}/S_{22} < -6 dB, K > 1). This chapter summarizes the project's key achievements, highlights its contributions to TTC applications, and discusses the limitations and future scope for improving the design and methodology. By integrating thin-film hybrid microcircuit technology and an EM-aware design approach, the project offers a robust solution for space-grade RF components.

10.2 SUMMARY OF ACHIEVEMENTS

The project successfully designed, fabricated, and validated a C-band driver amplifier with the following key achievements:

- **Performance Goals Met**: The amplifier delivers a measured gain of 12.14 dB at 6.4 GHz, surpassing the target of 9.6 ± 1 dB, with unconditional stability (K = 1.27) across 1–10 GHz. Despite slight deviations in return losses, the performance is sufficient for driving the power amplifier in TTC subsystems.
- **Compact Design**: The amplifier fits within a 14.7 mm × 10.69 mm footprint with a 2.5 mm transistor gap, achieved using thin-film microstrip technology on a high-purity alumina substrate, making it ideal for space-constrained LEO satellites.
- **EM-Aware Design Methodology**: The iterative design process, incorporating early EM extraction via AXIEM, ensures close alignment between schematic (S_{21} = 12.2 dB), EM-extracted (S_{21} = 12.3 dB), and measured (S_{21} = 12.14 dB) results, addressing a common limitation in prior works.

- **Thin-Film Technology**: The use of 99.6% pure alumina, gold conductors, and nichrome resistors enables high-frequency stability, thermal management, and precision, validated by the fabrication process.

10.3 CONTRIBUTIONS TO TTC APPLICATIONS

The project makes several contributions to the field of satellite communication, particularly for TTC subsystems:

- **Enhanced Reliability**: The amplifier's robust stability ($K > 1$) and environmental resilience ensure consistent performance in the harsh conditions of LEO orbits, improving TTC system reliability.
- **Compact and Efficient Design**: The small footprint and high gain make the amplifier suitable for miniaturized satellite payloads, optimizing power and space usage.
- **EM-Aware Design Framework**: By integrating EM extraction early in the design process, the methodology minimizes performance discrepancies, offering a reproducible approach for other RF components.
- **Advancement of Thin-Film Technology**: The successful use of thin-film hybrid circuits on alumina demonstrates their viability for high-frequency, space-grade applications, building on historical precedents like the Minuteman missile.
- **Benchmark Performance**: Compared to literature designs (e.g., Nugroho and Widodo [6]: 10 dB gain, Zhang et al. [8]: large footprint), the amplifier offers superior gain, compactness, and space qualification, as detailed in Chapter 9.

These contributions address key challenges in TTC systems, such as size constraints, reliability, and performance consistency, paving the way for more efficient satellite communication.

10.4 LIMITATIONS

Despite its achievements, the project has minor limitations:

- **Return Loss Deviations**: The measured S_{11} (-4.8 dB) and S_{22} (-1.8 dB) are slightly above the target (< -6 dB), attributed to fabrication tolerances (±0.1 μm conductor widths) and unmodeled parasitic capacitances at microstrip discontinuities. While acceptable for TTC applications, these deviations suggest room for improved matching network design.

- **Fabrication Complexity**: The thin-film process, though precise, is time-intensive and costly compared to thick-film or PCB alternatives, which may impact scalability for large-scale production.

10.5 FUTURE SCOPE

To address the limitations and extend the project's impact, the following areas are proposed for future work:

- **Improved Matching Networks**: Implement multi-stub or distributed matching networks to enhance return losses (S_{11}/S_{22} < -10 dB) and broaden the bandwidth, enabling use in multi-frequency TTC systems.
- **Advanced EM Solvers**: Incorporate full-wave 3D EM solvers (e.g., HFSS) to model complex parasitic effects, such as via transitions and package interactions, further reducing discrepancies between simulated and measured results.
- **Cost Optimization**: Explore hybrid fabrication techniques combining thin-film and thick-film processes to reduce costs while maintaining performance, facilitating larger-scale production for satellite constellations.
- **Broader Environmental Testing**: Conduct radiation hardness tests to quantify the amplifier's performance under high-energy particle exposure, enhancing its suitability for extended LEO missions.
- **Integration with TTC Modules**: Integrate the amplifier into a complete TTC transmitter chain, evaluating system-level performance (e.g., bit error rate, link budget) in a simulated satellite environment.
- **Alternative Transistors**: Investigate GaN HEMTs or SiGe HBTs for higher output power or efficiency, potentially improving the amplifier's drive capability for advanced TTC systems.

These enhancements would build on the project's foundation, addressing minor performance gaps and expanding its applicability to future satellite communication systems.

10.6 WORK ENVIRONMENT REFLECTIONS

The project was conducted in a collaborative environment at ISRO, where interns and project trainees worked alongside experienced scientists, engineers, and technicians, fostering

knowledge sharing in state-of-the-art facilities. The dynamic setting involved contributing to ongoing projects, with access to modern equipment for hands-on experience. This environment provided valuable learning opportunities, enhancing technical expertise, project management skills (planning, execution, monitoring), and teamwork capabilities. The collaborative and resource-rich setting significantly contributed to the project's success, equipping the team with practical skills and insights into space-grade RF design.

APPENDIX

Transistor Datasheet:

FLC057WG

C-Band Power GaAs FET

FEATURES

- High Output Power: P_{1dB} = 27.0dBm(Typ.)
- High Gain: G_{1dB} = 9.0dB(Typ.)
- High PAE: η_{add} = 38%(Typ.)
- Proven Reliability
- Hermetic Metal/Ceramic Package

DESCRIPTION

The FLC057WG is a power GaAs FET that is designed for general purpose applications in the C-Band frequency range as it provides superior power, gain, and efficiency.

Fujitsu's stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATING (Ambient Temperature Ta=25°C)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_T	T_C = 25°C	3.75	W
Storage Temperature	T_{stg}		-65 to +175	°C
Channel Temperature	T_{ch}		175	°C

Fujitsu recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain-source operating voltage (V_{DS}) should not exceed 10 volts.
2. The forward and reverse gate currents should not exceed 4.4 and -0.25 mA respectively with gate resistance of 1000Ω.
3. The operating channel temperature (T_{ch}) should not exceed 145°C.

ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta=25°C)

Item	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Saturated Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0V	-	200	300	mA
Transconductance	g_m	V_{DS} = 5V, I_{DS} = 125mA	-	100	-	mS
Pinch-off Voltage	V_p	V_{DS} = 5V, I_{DS} =10mA	-1.0	-2.0	-3.5	V
Gate Source Breakdown Voltage	V_{GSO}	I_{GS} = -10μA	-5	-	-	V
Output Power at 1dB G.C.P.	P_{1dB}	V_{DS} = 10V I_{DS} ≈ 0.6 I_{DSS} (Typ.), f = 8 GHz	25.5	27.0	-	dBm
Power Gain at 1dB G.C.P.	G_{1dB}		8.0	9.0	-	dB
Power-added Efficiency	η_{add}		-	38	-	%
Thermal Resistance	R_{th}	Channel to Case	-	27	40	°C/W

CASE STYLE: WG

G.C.P.: Gain Compression Point

FUJITSU

Edition 1.1

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