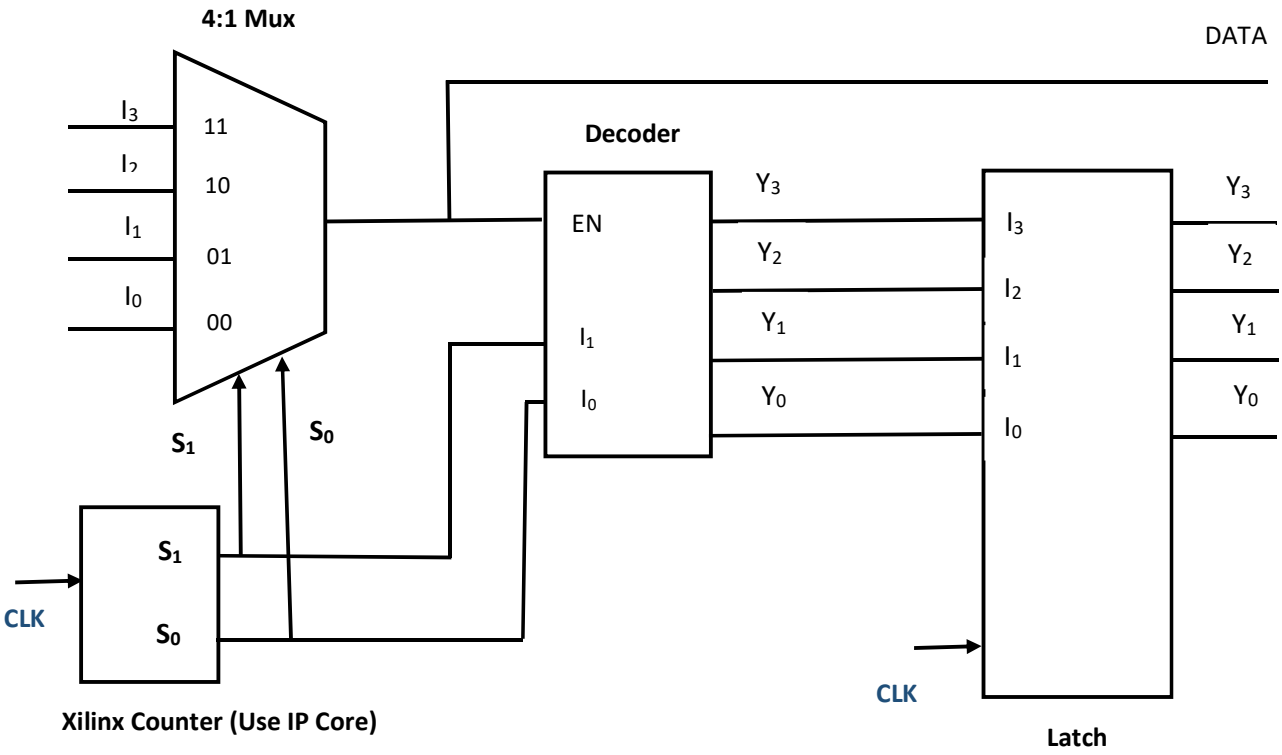
MINI PROJECT



Code the above design in verilog HDL and implement the same on the FPGA Kit allotted to you

Use Virtual input and Output IP Core for giving input I3, I2, I1, I0

CLK from the Kit.

Y3 Y2 Y1 Y0 need to be displayed on Chipscope IP Core.

1. ***4-1 Mux use dataflow***
2. ***Decoder use behaviour modeling***
3. ***Latch use behaviour modeling***
4. ***Counter- Use Xilinx IP Core.***
5. ***Connect everything as miniproject.v and implement on the Kit***