Mini Project

Submitted by:

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Verilog Codes

4 to 1 MUX using dataflow modelling

mux_4_to_1.v | top_module.v | latch.v | decoder_2_to_4.v | hw_ila_1 | hw_vios

/home/arm-33/Desktop/mini_project/mini_project.srcs/sources_1/new/mux_4_to_1.v

```
// Module Name: mux_4_to_1
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module mux_4_to_1(
    input s1,
    input s0,
    input i3,
    input i2,
    input i1,
    input i0,
    output y
    );
assign y = s1 ? (s0 ? i3 : i2) : (s0 ? i1 : i0);
endmodule
```

Decoder using behavioural modelling

mux_4_to_1.v | top_module.v | latch.v | decoder_2_to_4.v | hw_ila_1 | hw_vios

/home/arm-33/Desktop/mini_project/mini_project.srcs/sources_1/new/decoder_2_to_4.v

```
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module decoder_2_to_4(
    input en,
    input [1:0] in,
    output reg [3:0] out
    );
always @(in or en) begin
    if (en) begin
    case (in)
    2'b00: out = 4'b0001;
    2'b01: out = 4'b0010;
    2'b10: out = 4'b0100;
    2'b11: out = 4'b1000;
    default: out = 4'd0;
    endcase
    end
    else out = 4'd0;
end
endmodule
```

Latch using behavioural modelling

mux_4_to_1.v | top_module.v | latch.v | decoder_2_to_4.v | hw_ila_1 | hw_vios

/home/arm-33/Desktop/mini_project/mini_project.srcs/sources_1/new/latch.v

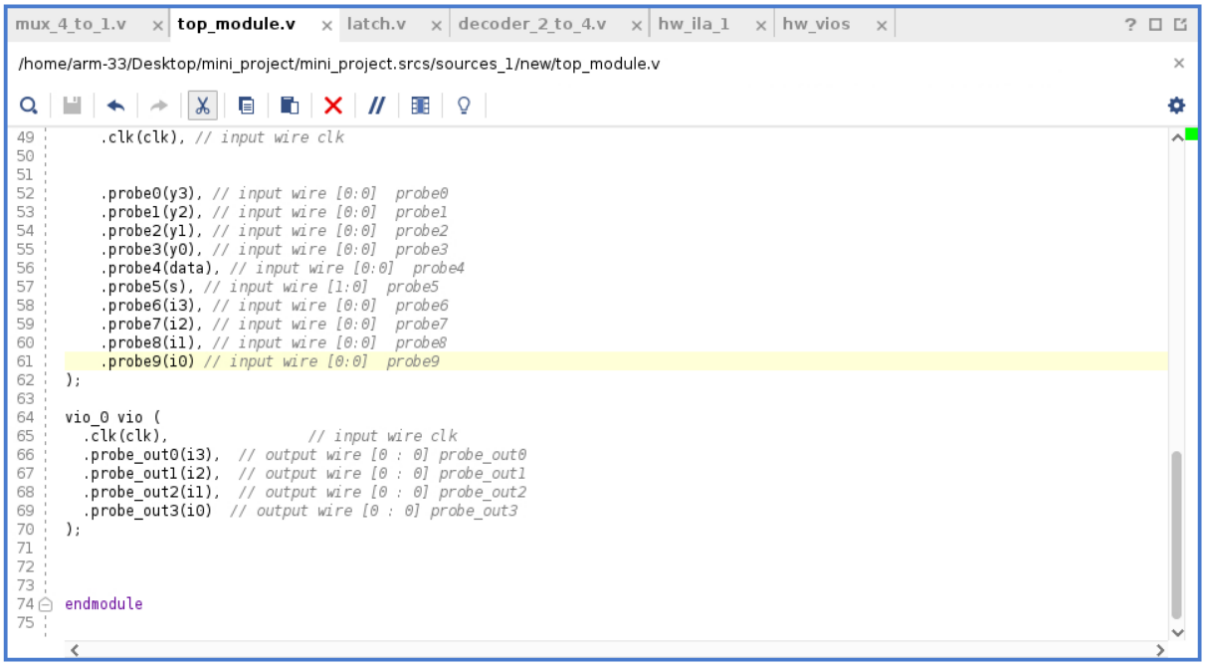
```
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////


module latch(
    input clk,
    input [3:0] in,
    output reg y3,
    output reg y2,
    output reg y1,
    output reg y0
    );
always @(clk or in) begin
    y3 = in[3];
    y2 = in[2];
    y1 = in[1];
    y0 = in[0];
end
endmodule
```

Top level module along with counter IP Core

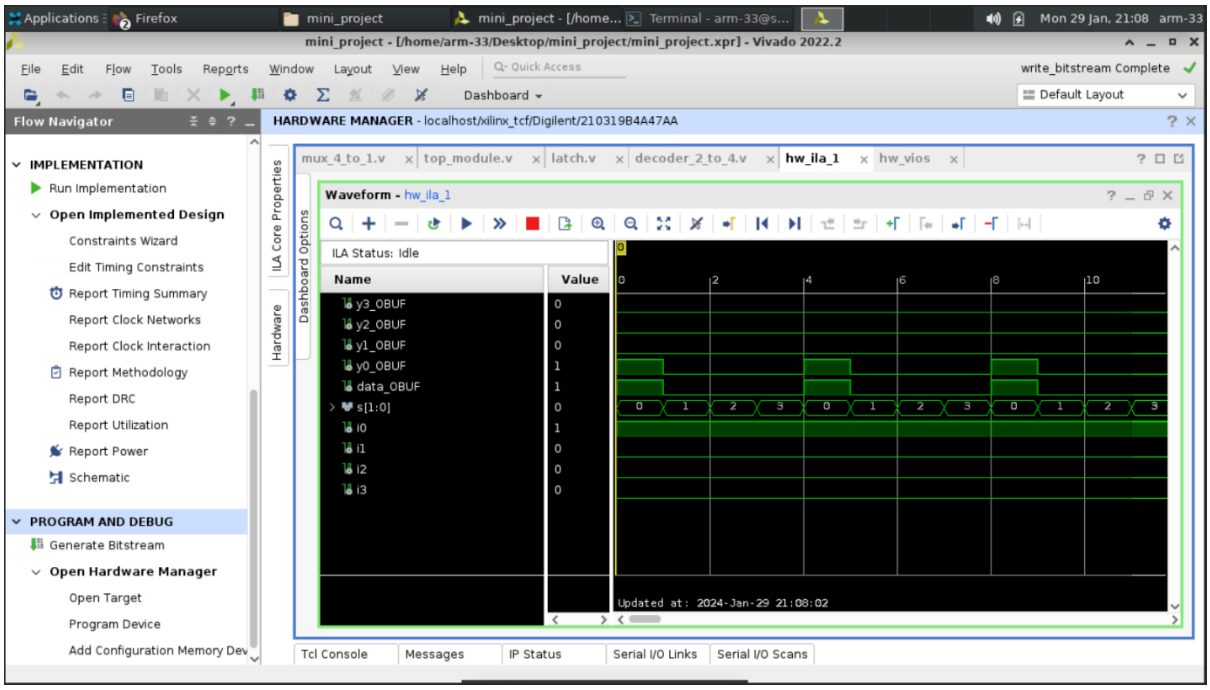
mux_4_to_1.v | top_module.v | latch.v | decoder_2_to_4.v | hw_ila_1 | hw_vios

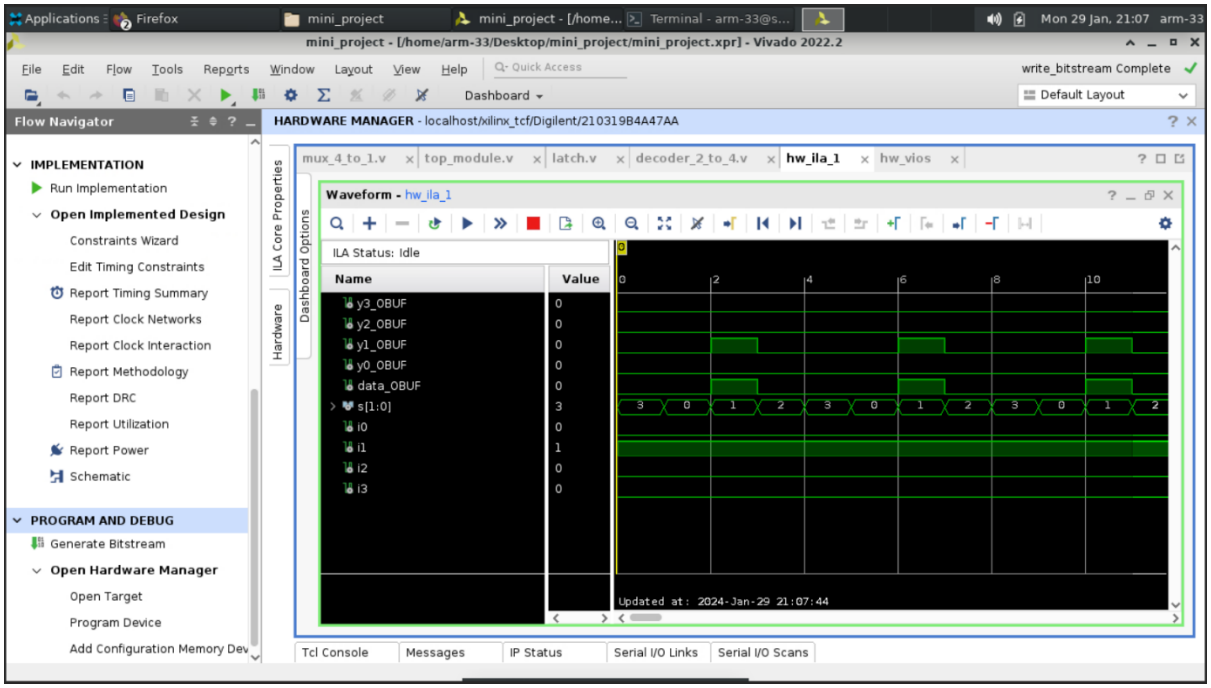
/home/arm-33/Desktop/mini_project/mini_project.srcs/sources_1/new/top_module.v

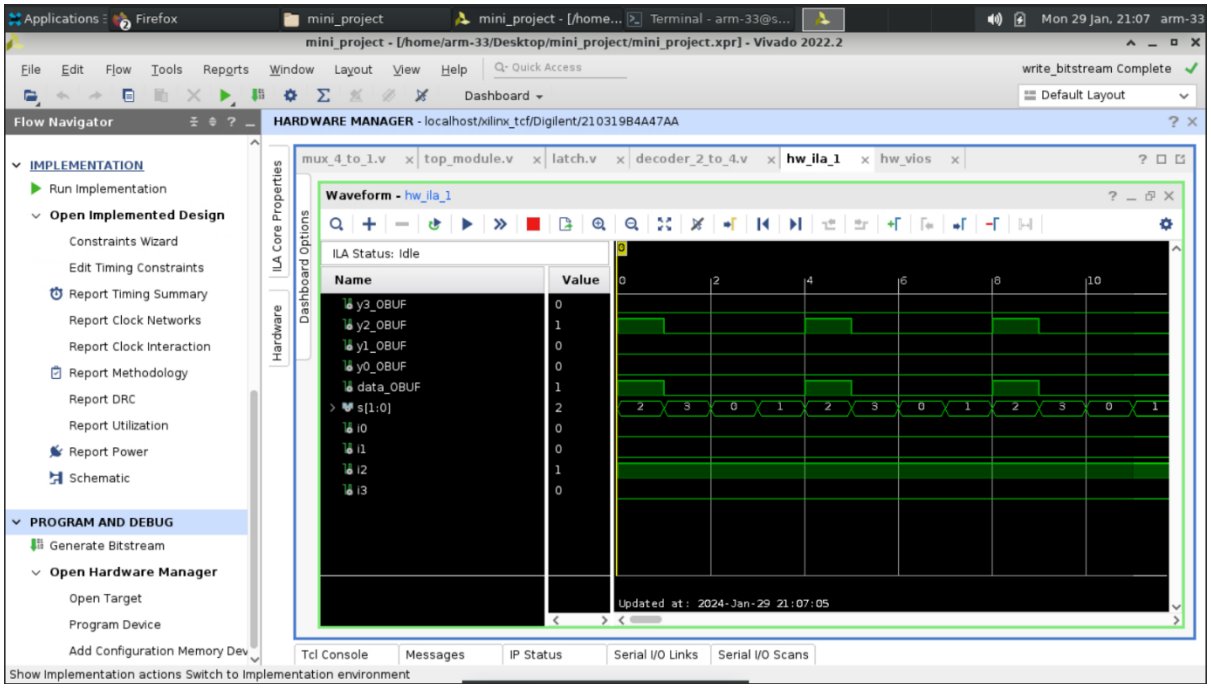
```

module top_module(
    input clk,
    //input i3,
    //input i2,
    //input i1,
    //input i0,
    output data,
    output y3,
    output y2,
    output y1,
    output y0
    );
wire [1:0] s;
wire [3:0] decode_out;
wire mux_out;
c_counter_binary_0 counter (
  .CLK(clk),  // input wire CLK
  .Q(s)      // output wire [1 : 0] Q
);
mux_4_to_1 m1 (s[1], s[0], i3, i2, i1, i0, mux_out);
decoder_2_to_4 d (mux_out, s, decode_out);
latch l (clk, decode_out, y3, y2, y1, y0);
assign data = mux_out;


ila_0 your_instance_name (
```

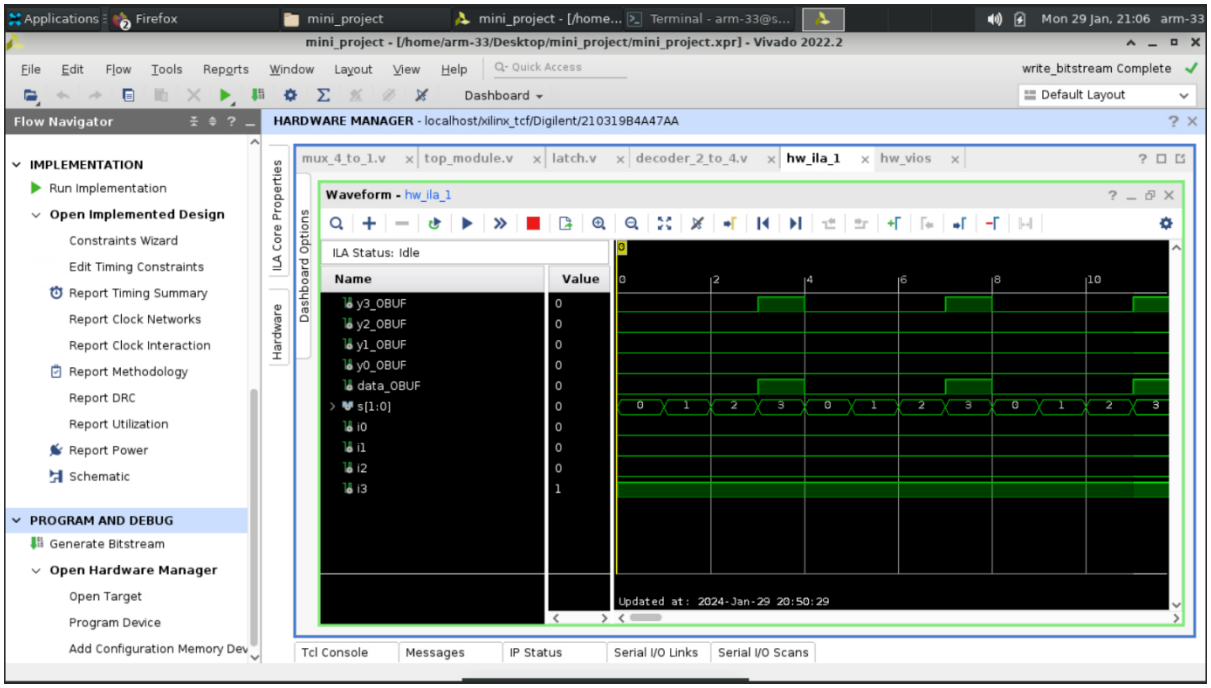


Waveforms simulated and observed using VIO and ILA core IP




mini_project - [/home/arm-33/Desktop/mini_project/mini_project.xpr] - Vivado 2022.2
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210319B4A47AA
Waveform - hw_ila_1
ILA Status: Idle
Name
Value
y3_OBUF 0
y2_OBUF 0
y1_OBUF 0
y0_OBUF 0
data_OBUF 0
s[1:0] 3
i0 0
i1 1
i2 0
i3 0
Updated at: 2024-Jan-29 21:07:44


mini_project - [/home/arm-33/Desktop/mini_project/mini_project.xpr] - Vivado 2022.2
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210319B4A47AA
Waveform - hw_ila_1
ILA Status: Idle
Name
Value
y3_OBUF 0
y2_OBUF 1
y1_OBUF 0
y0_OBUF 0
data_OBUF 1
s[1:0] 2
i0 0
i1 0
i2 1
i3 0
Updated at: 2024-Jan-29 21:07:05


Applications
Firefox
mini_project
mini_project - [/home...
Terminal - arm-33@s...
Mon 29 Jan, 21:06 arm-33
mini_project - [/home/arm-33/Desktop/mini_project/mini_project.xpr] - Vivado 2022.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Dashboard
Default Layout
Flow Navigator
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210319B4A47AA
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory Dev
ILA Core Properties
Dashboard Options
Hardware
mux_4_to_1.v
top_module.v
latch.v
decoder_2_to_4.v
hw_ila_1
hw_vios
Waveform - hw_ila_1
ILA Status: Idle
Name
Value
y3_OBUF 0
y2_OBUF 0
y1_OBUF 0
y0_OBUF 0
data_OBUF 0
s[1:0] 0
i0 0
i1 0
i2 0
i3 1
0 2 4 6 8 10
0 1 2 3 0 1 2 3 0 1 2 3
Updated at: 2024-Jan-29 20:50:29
Tcl Console
Messages
IP Status
Serial I/O Links
Serial I/O Scans