ICD Design Lab – HW2 Testbench

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1. Power Report

```
Loading db file '/home/raid7_2/userb08/b08024/ICDLAB_HW3/fsa0m_a_generic_core_ttlp8v25c.db'
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : alu
Version: R-2020.09-SP5
Date   : Mon Mar  7 18:48:16 2022
****************************************


Library(s) Used:

    fsa0m_a_generic_core_ttlp8v25c (File: /home/raid7_2/userb08/b08024/ICDLAB_HW3/fsa0m_a_generic_core_ttlp8v25c.db)


Operating Conditions: WCCOM   Library: fsa0m_a_generic_core_ss1p62v125c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
alu                   G200K             fsa0m_a_generic_core_ttlp8v25c
alu_DW_mult_uns_0     enG5K             fsa0m_a_generic_core_ttlp8v25c


Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 295.6324 uW   (48%)
  Net Switching Power  = 324.3423 uW   (52%)
                         ---------
Total Dynamic Power    = 619.9747 uW  (100%)

Cell Leakage Power     =  36.2053 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register           0.2129           0.2335          9.1781e+03             0.4464  (  72.00%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational  8.2725e-02        9.0821e-02          2.7027e+04             0.1736  (  28.00%)
--------------------------------------------------------------------------------------------------
Total              0.2956 mW        0.3243 mW       3.6205e+04 pW          0.6200 mW
1
```

2. Timing Report

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : alu
Version: R-2020.09-SP5
Date   : Mon Mar  7 18:48:49 2022
****************************************

Operating Conditions: WCCOM   Library: fsa0m_a_generic_core_ss1p62v125c
Wire Load Model Mode: enclosed

  Startpoint: data_b_reg[0]
              (rising edge-triggered flip-flop clocked by clk_p_i)
  Endpoint: out_r_reg[15]
            (rising edge-triggered flip-flop clocked by clk_p_i)
  Path Group: clk_p_i
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  alu                G200K                 fsa0m_a_generic_core_tt1p8v25c
  alu_DW_mult_uns_0  enG5K                 fsa0m_a_generic_core_tt1p8v25c

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock clk_p_i (rise edge)                               0.00       0.00
  clock network delay (ideal)                             0.50       0.50
  data_b_reg[0]/CK (QDFFRBN)                              0.00       0.50 r
  data_b_reg[0]/Q (QDFFRBN)                               0.52       1.02 r
  mult_39/b[0] (alu_DW_mult_uns_0)                        0.00       1.02 r
  mult_39/U318/O (INV1S)                                  0.21       1.22 f
  mult_39/U298/O (INV1S)                                  0.11       1.34 r
  mult_39/U299/O (INV1S)                                  0.30       1.64 f
  mult_39/U390/O (NR2)                                    0.22       1.86 r
  mult_39/U115/S (HA1)                                    0.23       2.09 f
  mult_39/U113/S (FA1S)                                   0.51       2.60 r
  mult_39/U112/S (FA1S)                                   0.42       3.02 f
  mult_39/U12/CO (FA1S)                                   0.42       3.45 f
  mult_39/U11/CO (FA1S)                                   0.40       3.85 f
  mult_39/U10/CO (FA1S)                                   0.40       4.24 f
  mult_39/U9/CO (FA1S)                                    0.40       4.64 f
  mult_39/U8/CO (FA1S)                                    0.40       5.04 f
  mult_39/U7/CO (FA1S)                                    0.40       5.44 f
  mult_39/U6/CO (FA1S)                                    0.40       5.84 f
  mult_39/U5/CO (FA1S)                                    0.40       6.24 f
  mult_39/U4/CO (FA1S)                                    0.40       6.64 f
  mult_39/U3/CO (FA1S)                                    0.41       7.04 f
  mult_39/U325/O (XOR2HS)                                 0.15       7.19 f
  mult_39/product[15] (alu_DW_mult_uns_0)                 0.00       7.19 f
  U320/O (AO22)                                           0.22       7.41 f
  U96/O (AO112)                                           0.27       7.68 f
  out_r_reg[15]/D (QDFFRBT)                               0.00       7.68 f
  data arrival time                                                  7.68

  clock clk_p_i (rise edge)                              10.00      10.00
  clock network delay (ideal)                             0.50      10.50
  clock uncertainty                                      -0.10      10.40
  out_r_reg[15]/CK (QDFFRBT)                              0.00      10.40 r
  library setup time                                     -0.06      10.34
  data required time                                                10.34
  --------------------------------------------------------------------------
  data required time                                                10.34
  data arrival time                                                 -7.68
  --------------------------------------------------------------------------
  slack (MET)                                                        2.65
```

3. Area Report

```
1:
2: ****************************************
3: Report : area
4: Design : alu
5: Version: R-2020.09-SP5
6: Date   : Mon Mar  7 18:47:59 2022
7: ****************************************
8:
9: Information: Updating design information... (UID-85)
10: Library(s) Used:
11:
12:     fsa0m_a_generic_core_ttlp8v25c (File: /home/raid7_2/userb08/b08024/ICDLAB_HW3/fsa0m_a_generic_core_ttlp8v25c.db)
13:
14: Number of ports:                          101
15: Number of nets:                           531
16: Number of cells:                          404
17: Number of combinational cells:            368
18: Number of sequential cells:                35
19: Number of macros/black boxes:               0
20: Number of buf/inv:                         87
21: Number of references:                      28
22:
23: Combinational area:              8002.612809
24: Buf/Inv area:                     587.462394
25: Noncombinational area:           2227.982376
26: Macro/Black Box area:               0.000000
27: Net Interconnect area:      undefined  (Wire load has zero net area)
28:
29: Total cell area:                10230.595185
30: Total area:                 undefined
31: 1
32:
```

4. Discussion

從上面三個報告可以看出這是一個合理的結果：

- ✓ Power

  可以看出 register 跟 combinational circuit 各佔一部份的 power，而這兩部分分別的 internal, switching 和 leakage power 相加可得出總共的 internal, switching 和 leakage power。

- ✓ Timing

  可以看出在這樣的 cycle time(設為 10ns)，經過各個 transistor 的時間加總最多可以到 10.34ns，但此電路只需 7.68ns，因此在 timing 上十分寬裕。Slack time 即是剩餘寬裕的時間，基本上大於或等於零都代表電路是正常的。

- ✓ Area

  可以看出該電路合成後所需要的 cells, nets, ports 數，以及各部分的 area 數。