

Homework-Verilog-1

Visit <https://hdlbits.01xz.net/> and solve the following problems: NOR, 7420 chip, 3-bit population count, full adder, 3-bit full adder, signed addition overflow. [Problem sets - HDLBits](#)

Upload your answers (with snapshot of the simulation result on <https://hdlbits.01xz.net/>) to the course webpage on canvas system.

https://hdlbits.01xz.net/wiki/Exams/ece241_2013_q2

Problem Set Simulation My Profile Help 01xz.net

Exams/ece241 2013 q2

← kmap4 Previous

A single-output digital system with four inputs (a,b,c,d) generates a logic-1 when 2, 7, or 15 appears 13, or 14 appears. The input conditions for the numbers 3, 8, 11, and 12 never occur in this system. 0,1,1,1, respectively.

Determine the output out_sop in minimum SOP form, and the output out_pos in minimum POS form

Module Declaration

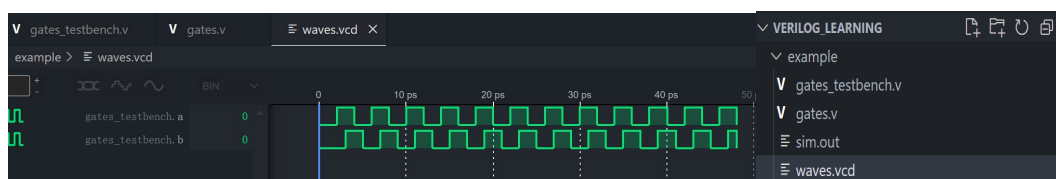
```
module top_module (  
    input a,  
    input b,  
    input c,  
    input d,  
    output out_sop,  
    output out_pos  
);
```

Write your solution here

[Load a previous submission] Load

```
1 module top_module (  
2     input a,  
3     input b,  
4     input c,  
5     input d,  
6     output out_sop,  
7     output out_pos  
8 );
```

1. Configure a verilog simulator environment on your personal computer (e.g. **Icarus Verilog/verilator + GTKwave**) and get familiar with its basic usage.



1. NOR gate

exams/m2014_q4e — Compile and simulate

Running Quartus synthesis. [Show Quartus messages...](#)
Running ModelSim simulation. [Show Modelsim messages...](#)

Status: Success!

You have solved 1 problems. [See my progress...](#)

```
module top_module (  
    input wire in1,  
    input wire in2,  
    output wire out  
);  
    assign out = ~(in1 | in2);  
endmodule
```

2. chip7420

7420 — Compile and simulate

Running Quartus synthesis. [Show Quartus messages...](#)
Running ModelSim simulation. [Show Modelsim messages...](#)

Status: Success!

You have solved 2 problems. [See my progress...](#)

```
module top_module (  
    input wire p1a, p1b, p1c, p1d,  
    output wire p1y,  
    input wire p2a, p2b, p2c, p2d,  
    output wire p2y );  
  
    assign p1y = ~(p1a&p1b&p1c&p1d);  
    assign p2y = ~(p2a&p2b&p2c&p2d);  
  
endmodule
```

3. popcount3

popcount3 — Compile and simulate

Running Quartus synthesis. [Show Quartus messages...](#)
Running ModelSim simulation. [Show Modelsim messages...](#)

Status: Success!

You have solved 3 problems. [See my progress...](#)

```
module top_module(  
    input [2:0] in,  
    output [1:0] out  
);  
    assign out = in[0] + in[1] + in[2];  
endmodule
```

4. full-adder

fadd — Compile and simulate

Running Quartus synthesis. [Show Quartus messages...](#)
Running ModelSim simulation. [Show Modelsim messages...](#)

Status: Success!

You have solved 4 problems. [See my progress...](#)

```
module top_module(  
    input a, b, cin,  
    output cout, sum );  
    assign sum = a ^ b ^ cin;  
    assign cout = (a & b) | (b & cin) | (a & cin);  
endmodule
```

5. adder3

adder3 — Compile and simulate

Running Quartus synthesis. [Show Quartus messages...](#)
Running ModelSim simulation. [Show Modelsim messages...](#)

Status: Success!

You have solved 5 problems. [See my progress...](#)

```

module top_module(
    input [2:0] a, b,
    input cin,
    output [2:0] cout,
    output [2:0] sum
);
    assign sum[0] = a[0]^b[0]^cin;
    assign cout[0] = (a[0]&b[0]) | (b[0]&cin) | (a[0]&cin);
    assign sum[1] = a[1]^b[1]^cout[0];
    assign cout[1] = (a[1]&b[1]) | (b[1]&cout[0]) | (a[1]&cout[0]);
    assign sum[2] = a[2]^b[2]^cout[1];
    assign cout[2] = (a[2]&b[2]) | (b[2]&cout[1]) | (a[2]&cout[1]);

endmodule

```

6.overflow

exams/ece241_2014_q1c — C

Running Quartus synthesis. [Show Quartus messages...](#)
 Running ModelSim simulation. [Show Modelsim messages...](#)

Status: Success!

You have solved 6 problems. [See my progress...](#)

```

module top_module (
    input [7:0] a,
    input [7:0] b,
    output [7:0] s,
    output overflow
);
    assign s = a + b;
    assign overflow = (a[7] == b[7]) && (s[7] != a[7]);
endmodule

```