HW-Lecture 1 & 2

1. Convert the following unsigned binary numbers to decimal and hexadecimal.

   (a) 1010_2 (b) 11110000_2

(a) 10 0x0a (b) 240 0xF0

2. Convert the following two's complement binary numbers to decimal.

   (a) 110110_2 (b) 01110000_2 (c) 10011111_2

(a) -10 (b) 112 (c)-97

What are the largest and smallest 32-bit binary number(show the decimal values) that can be represented with

(a) unsigned numbers?
(b) two's complement numbers?
(c) sign/magnitude numbers?

(a)2^32 0 (b) 2^31-1 -2^31 (c) 2^31-1 –(2^31-1)

3. Convert the following decimal numbers to 8-bit two's complement numbers or indicate that the decimal number would overflow the range.

   (a) 42_{10} (b) -63_{10} (c) 124_{10} (d) -128_{10} (e) 133_{10}

(a)00101010 (b)11000001 (c)01111100 (d)10000000 (e) --overflow

4. extend the following 4-bit two's complement numbers to 8-bit two's complement numbers.

   (a) 0101_2 (b) 1010_2

   Repeat your work if the numbers are unsigned

(a)00000101 (b)11111010 -- signed

(a)00000101 (b)00001010 -- unsigned

5. Perform the following additions of unsigned binary numbers. Indicate whether the sum overflows an 8-bit result.

   (a) $10011001_2 + 01000100_2$ (b) $11010010_2 + 10110110_2$

   Repeat your work, assuming that the binary numbers are in two's complement form.

(a)11011101 (b) 110001000--(8-bits overflow)

(a)11011101 (b)110001000

6. Convert the following decimal and hexadecimal numbers to 8-bit two's complement binary numbers and add them. Indicate whether the sum overflows an 8-bit result.

   (a) $27_{10} + 31_{10}$ (b) $-4_{10} + 19_{10}$ (c) $-28_{10} + (-111_{10})$ (d) $8F_{16} + AD_{16}$

(a)00011011+00011111=00111010

(b)11111100+00010011=00001111

(c)11100100+10010001=1 01110101(overflow)

(d)10001111+10101101=1 01111100(overflow)

7. In a *binary coded decimal* (*BCD*) system, 4 bits are used to represent a decimal digit from 0 to 9. For example, 37_{10} is written as 00110111_{BCD}.

   (a) Write 371_{10} in BCD.

(b) Convert 000110000111_{BCD} to decimal.

(c) Convert 10010101_{BCD} to binary.

(d) Explain the disadvantages of BCD when compared with binary representations of numbers.

(a)0011 0111 0001 (b)187 (c)1011 1111

(d) Lower storage efficiency and higher computational complexity : for example, it cant maximize the amount of information that can be stored – 8-bits can only store (0-99),but binary nums can store (0-255).

8. Is it possible to assign logic levels so that a device with the transfer characteristics shown in Figure 1.1 would serve as a buffer? If so, what are the input and output low and high levels (V_{IL}, V_{OL}, V_{IH}, and V_{OH}) and noise margins (NM_L and NM_H)? If not, explain why not.

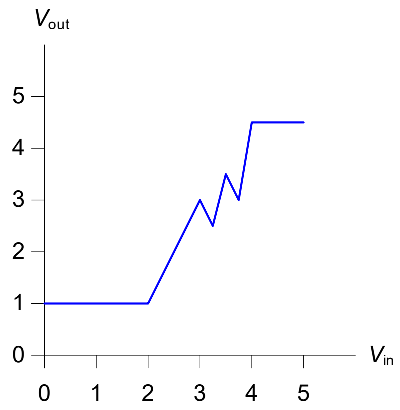

Figure 1.1 Figure 1.1 DC transfer characteristics

Yes, it can be.

V_{IL}=2V, V_{OL}=1V, V_{IH}=4V, V_{OH}=4.5V

NM_L = 0.5V and NM_H = 1V

9. Ben Bitdiddle has invented a circuit with the transfer characteristics shown in Figure 1.2 that he would like to use as a buffer. Will it work? Why or why not? He would like to advertise that it is compatible with LVCMOS and LVTTL logic. Can Ben's buffer correctly receive inputs from those logic families? Can its output properly drive those logic families? Explain.

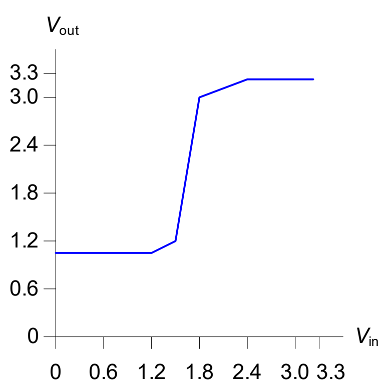

Figure 1.2 Ben's buffer DC transfer characteristics

(1) Yes, it will work. The output of the buffer needs to meet the input level requirements of LVCMOS to ensure that it can properly drive these logic families. VIL=1.6V, VOL=1.2V,

VIH=1.8V, VOH=3V , NML = 0.4V and NMH = 1.2V

(2) It can accept inputs from LVCMOS & LVTTL gates -- output logic levels are compatible with the input levels of the gate. But it cannot drive LVCMOS & LVTTL gates -- 1.2 VOL exceeds the VIL of LVCMOS and LVTTL.

10. The following are voltage transfer characteristics of single-input, single-output devices to be used in a new logic family:

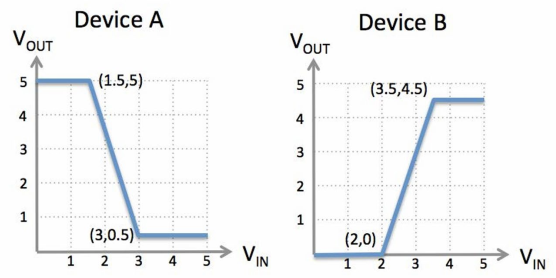

Figure 1.3 DC transfer characteristics of new logic family devices

Your job is to choose a single set of signaling thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} to be used with both devices to give the best noise margins you can.

V_{OL} = ___0.5V___ V_{IL} = ___2V___ V_{IH} = ___3V___ V_{OH} = ___4.5V___

Low Noise Margin = ___1.5V___

High Noise Margin = ___1.5V___

11. Draw the symbol, Boolean equation, and truth table for a three-input OR gate.
12. Sketch a transistor-level circuit for a three-input AND gate, use a minimum number of transistors.
13. A three-input OR-AND-INVERT (OAI) gate shown in Figure 1.4 produces a FALSE output if C is TRUE and A or B is TRUE. Otherwise, it produces a TRUE output. Complete a truth table for the gate.

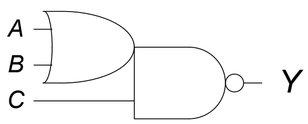

Figure 1.4 OAI

Sketch a transistor-level circuit for this CMOS gates. Use a minimum number of transistors.

14. Write a truth table for the function performed by the gate in Figure 1.5. The truth table should have two inputs, A and B. What is the name of this function?

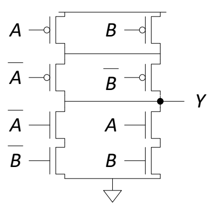

Figure 1.5

The Answers of Problem 11,12,13,14 are as follows

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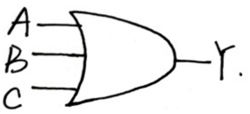
HW L1–L2.

1.11. 3–Inputs OR Gate.

(1) Symbol

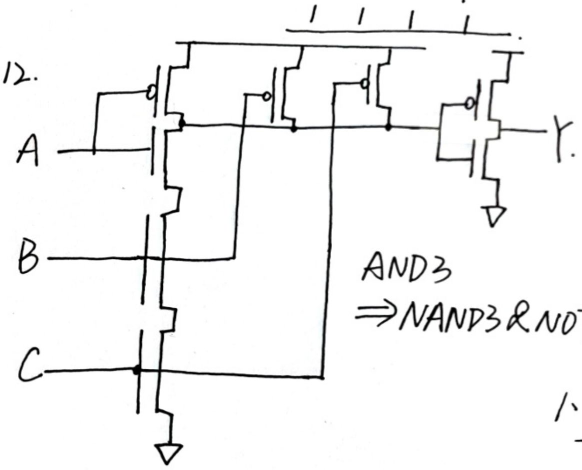


(2). Boolean $Y = A+B+C$.

(3) Truth Table.

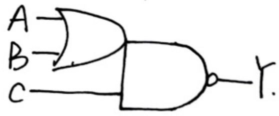
A	B	C	Y.
0	0	0	0
1	0	0	1
0	1	0	1
0	0	1	1
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1

1.12.



AND3
⇒NAND3&NOT

1.13 3-Inputs



A	B	C	Y.
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	1
1	1	0	1
0	1	1	1
1	0	1	1
1	1	1	1

1.14. XOR Gate.

Truth Table.

A	B	$Y = A \oplus B$
0	0	0
1	0	1
0	1	1
0	0	0.