

What to turn in：

1. A completed State Transition Diagram for the FSM.
2. Tables listing (1) next state in terms of current state and inputs, and (2) output in terms of current state and inputs.

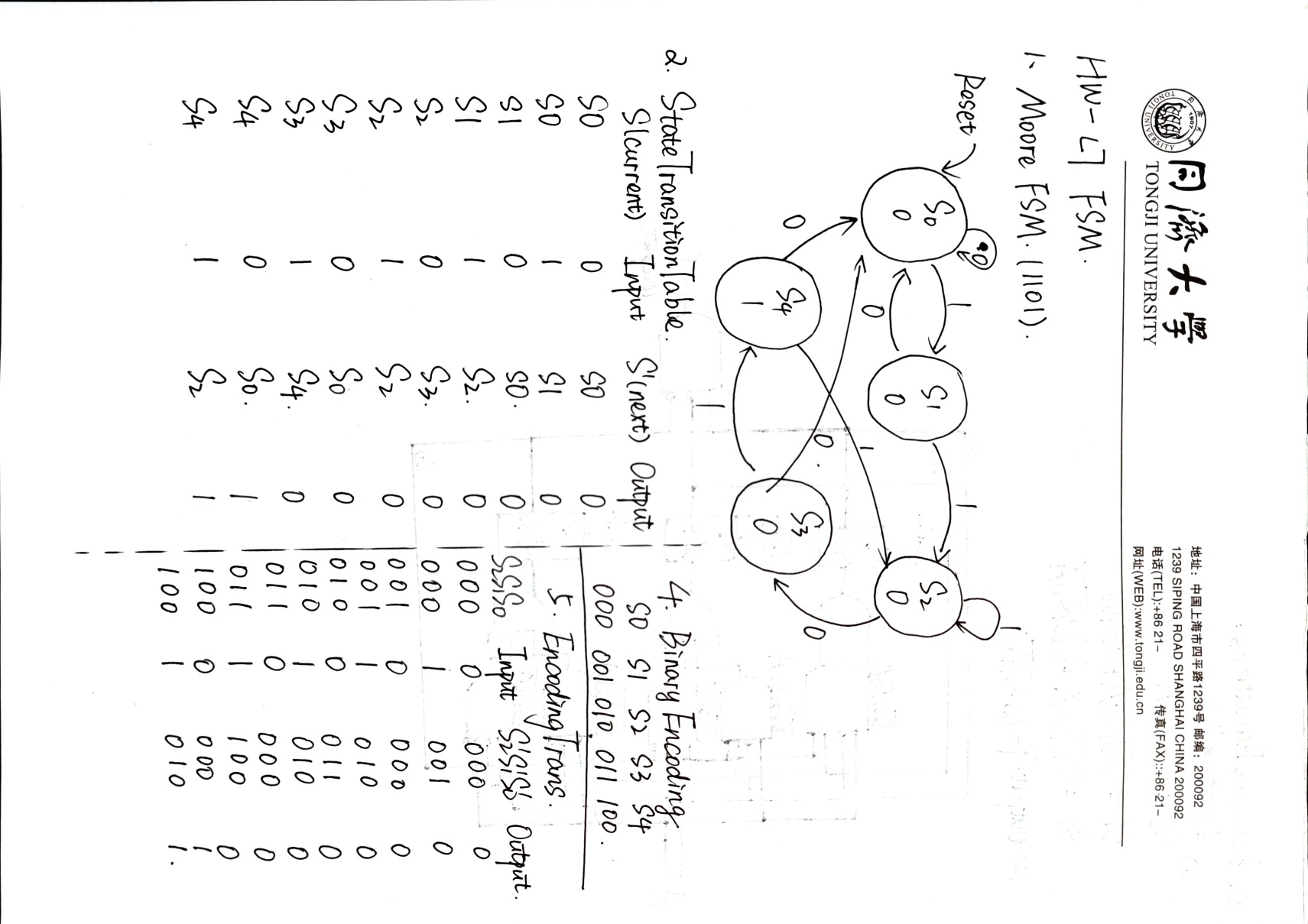
4.      The binary encoding for each state.

5.      The revised copy of your tables, using your binary encoding.

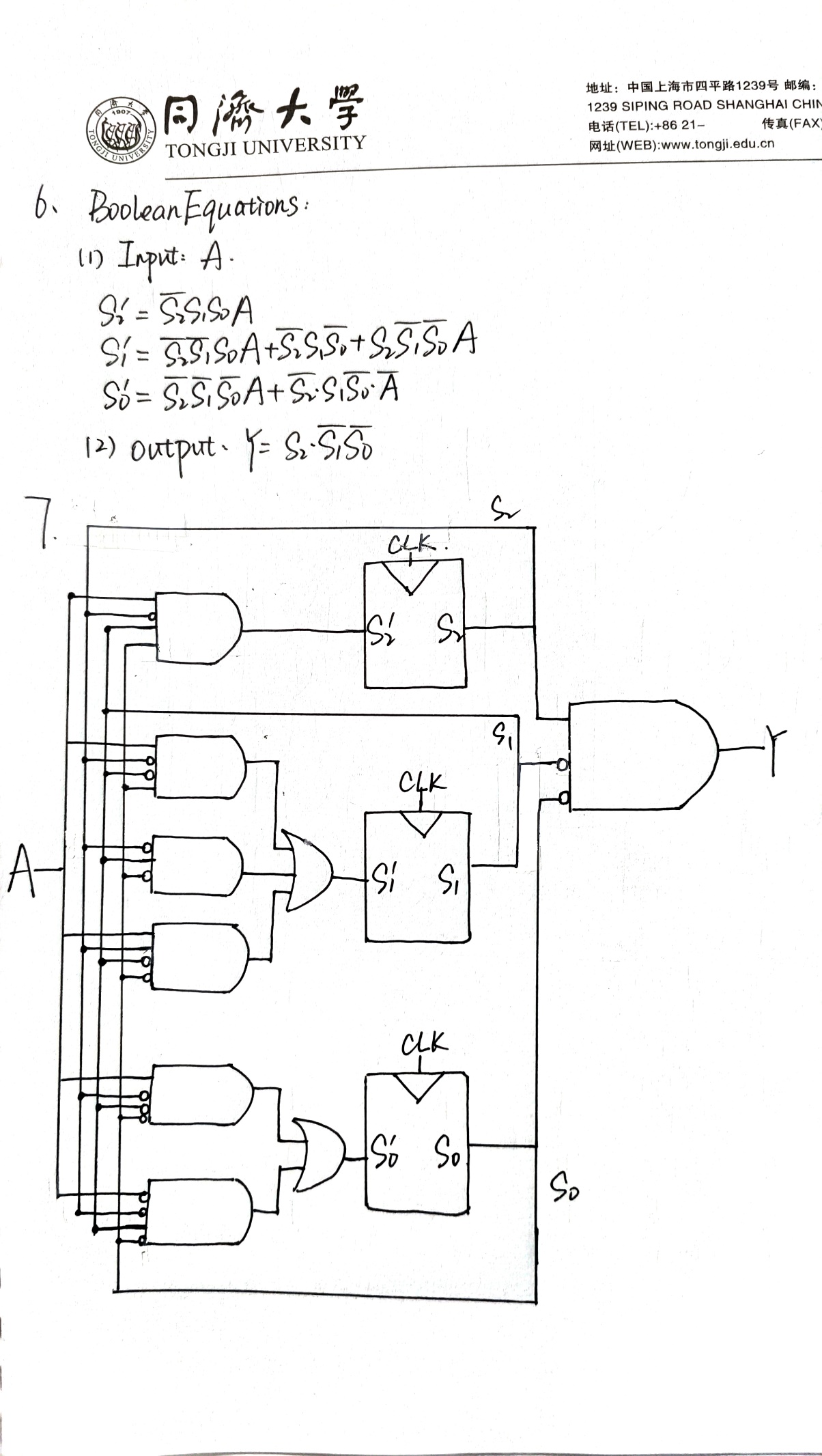
6.      Boolean logic equations for the outputs and each bit of the next state in terms of the state and inputs.

7. schematic of the FSM.

8. Verilog code for the FSM design and testbench, snapshot of the simulation waveform

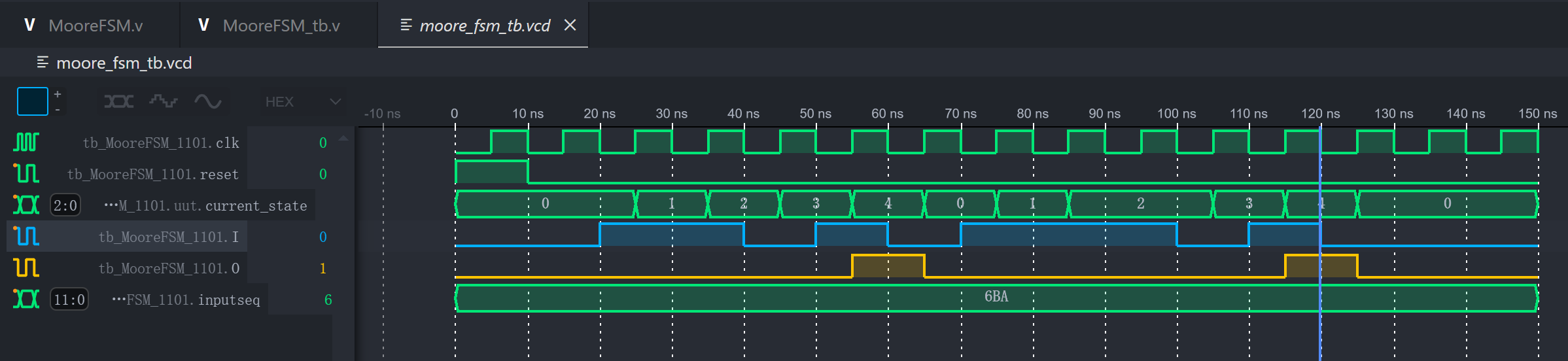


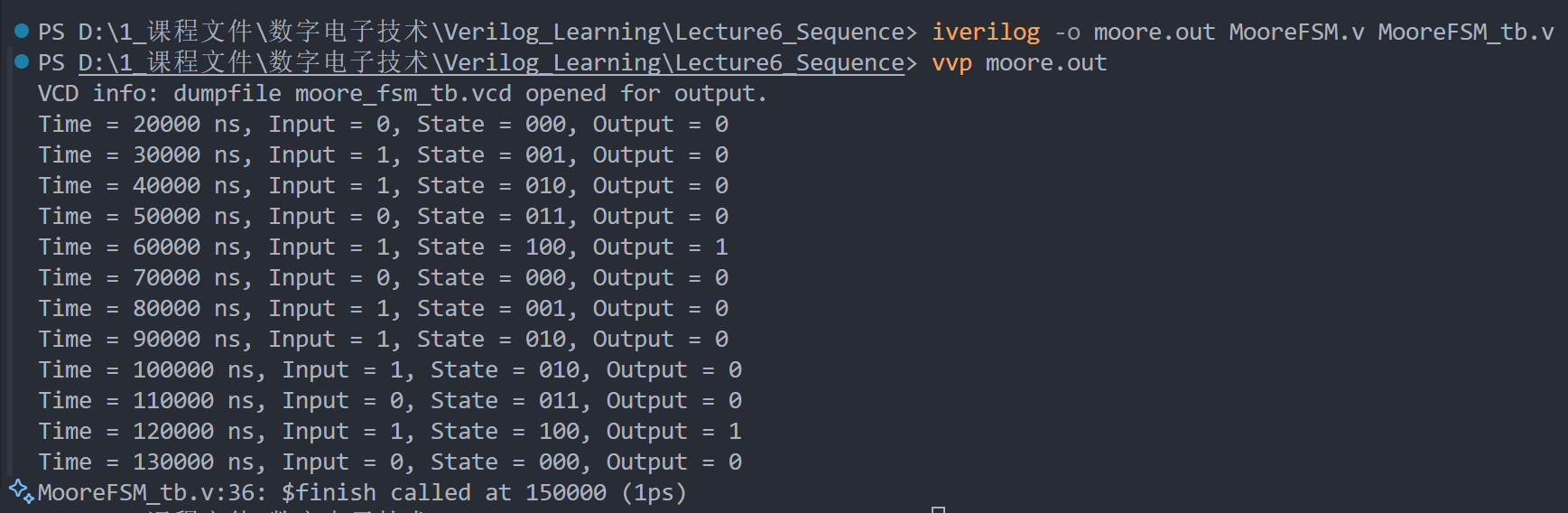
Part 1--Moore FSM

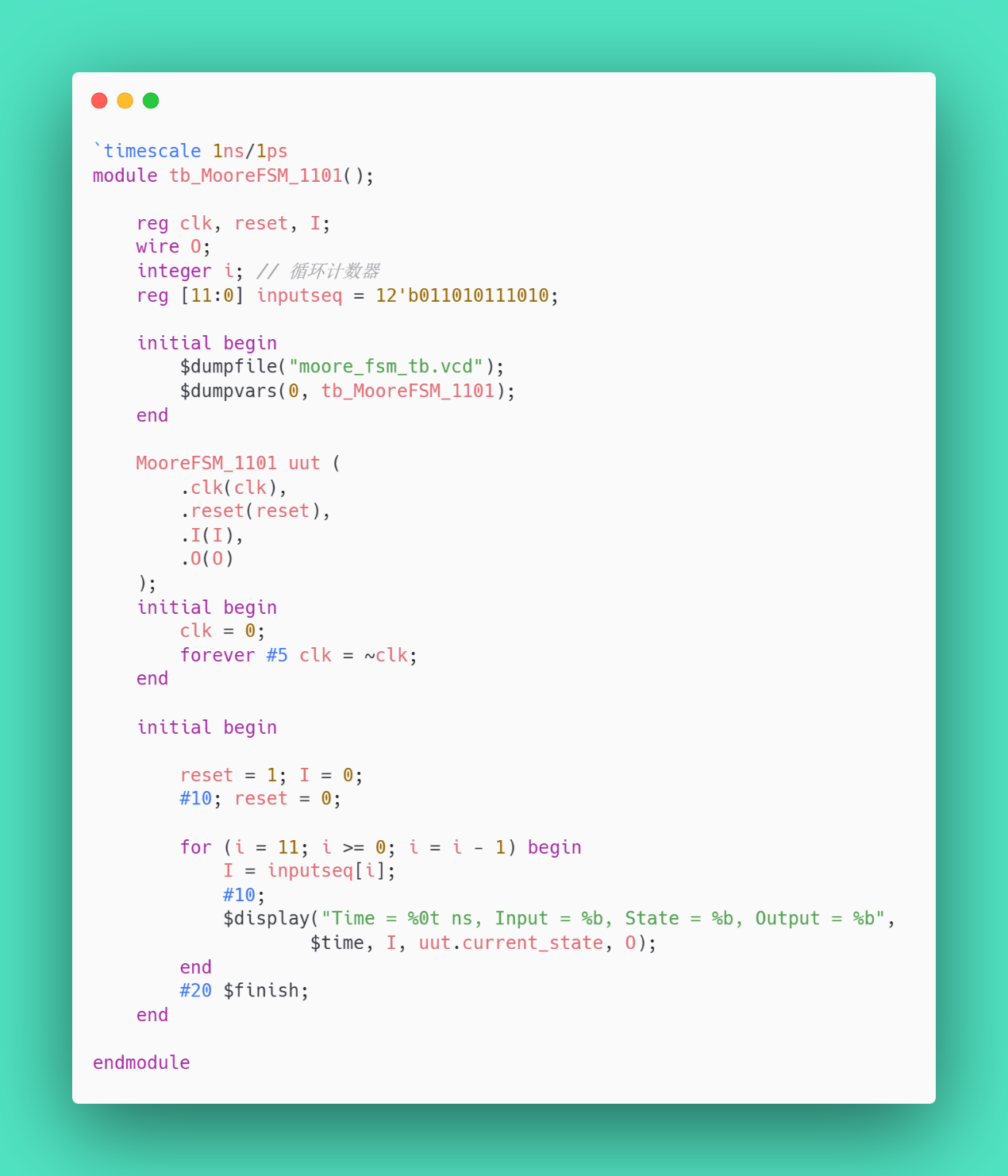
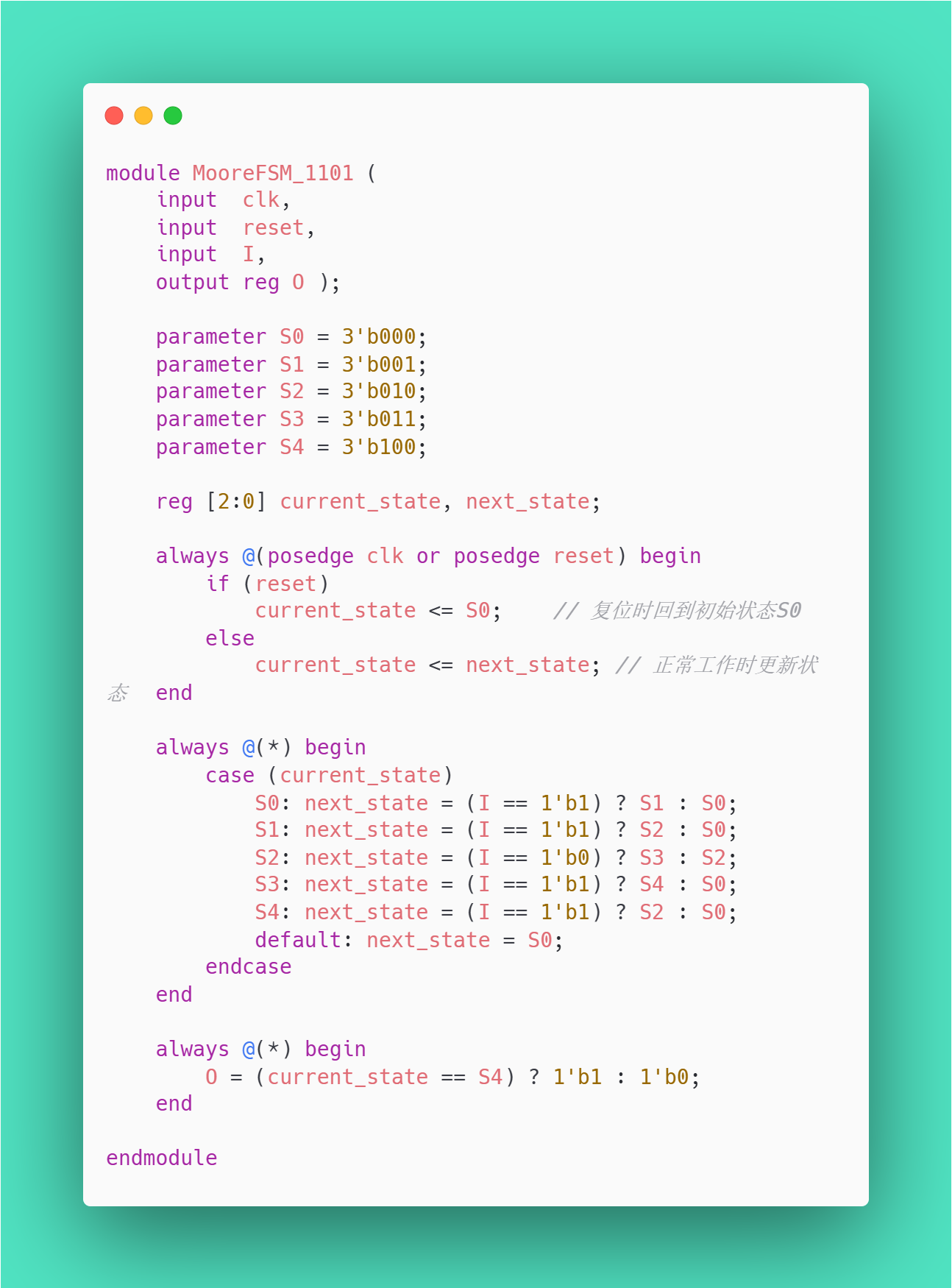
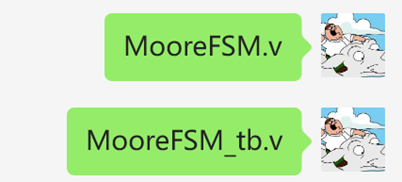


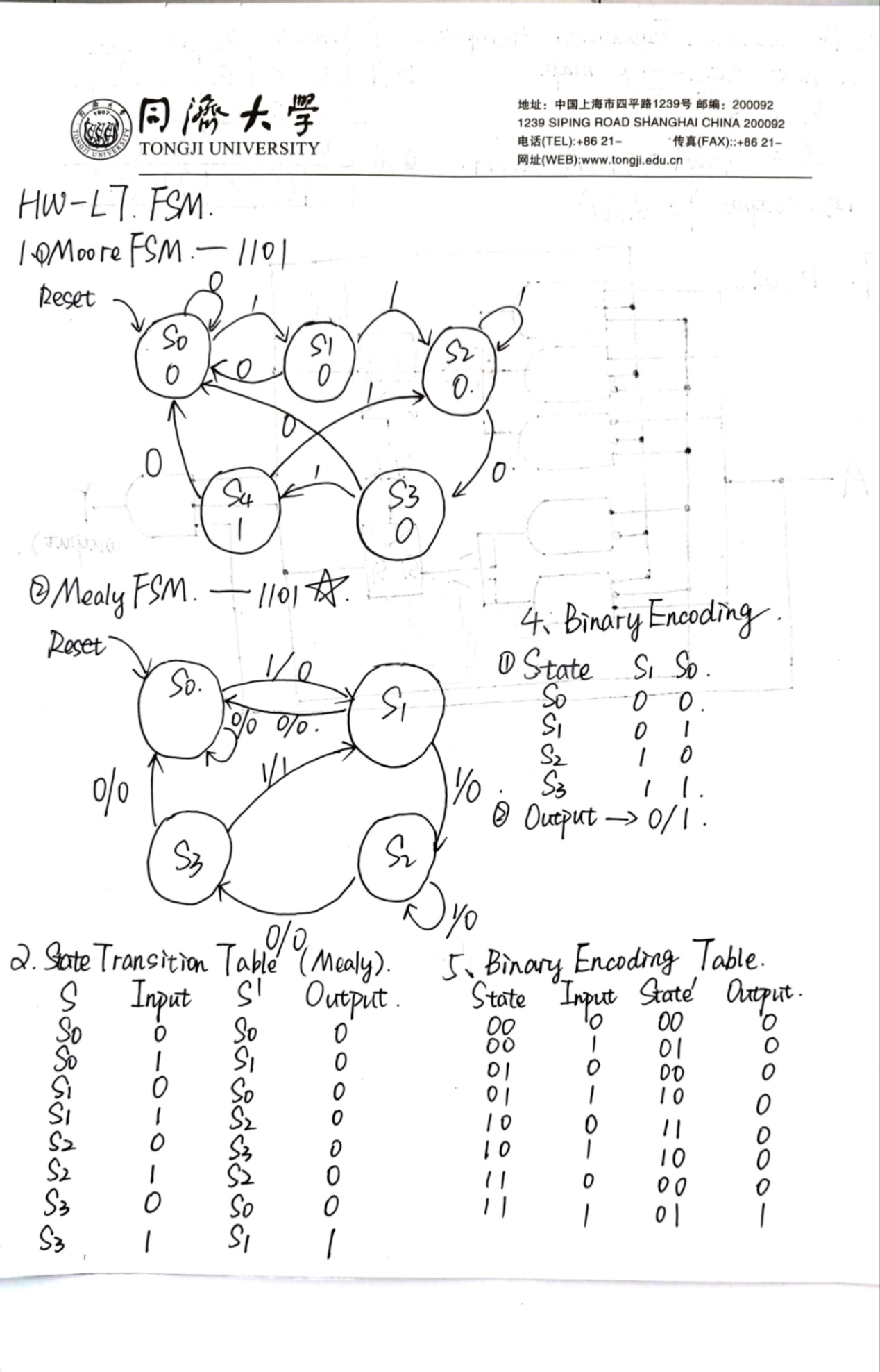
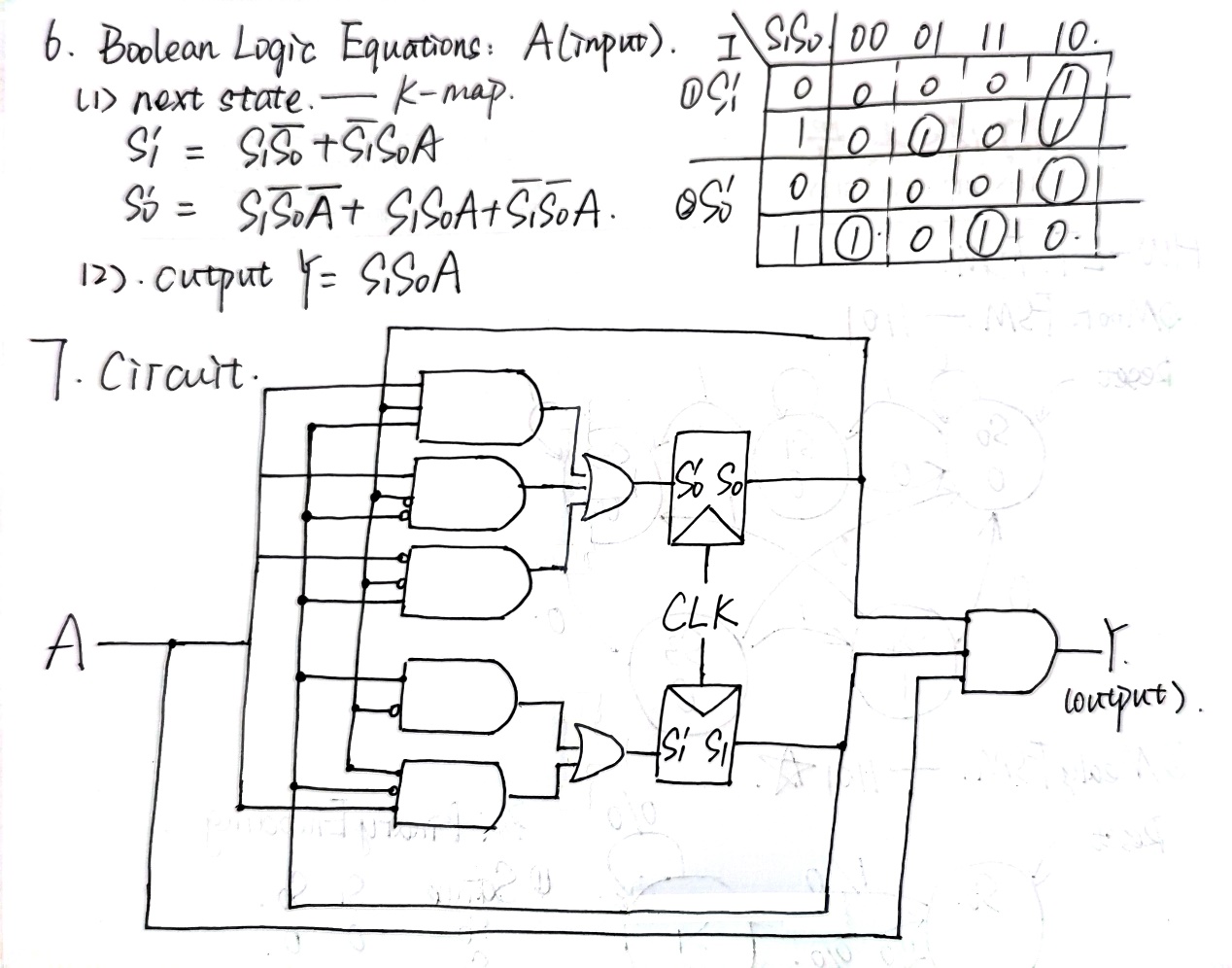
Here are the snapshots of my MooreFSM.

In the sequence 12'b011010111010 ,it turns 1 from 0 at the 6th and 12th clk.

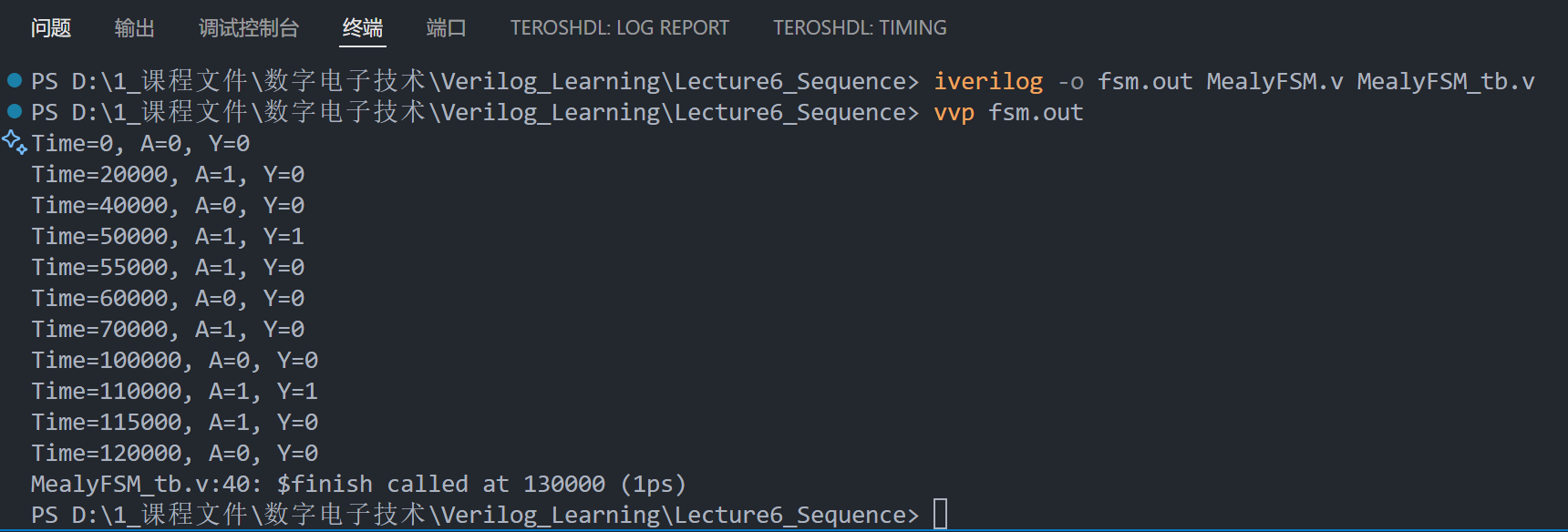


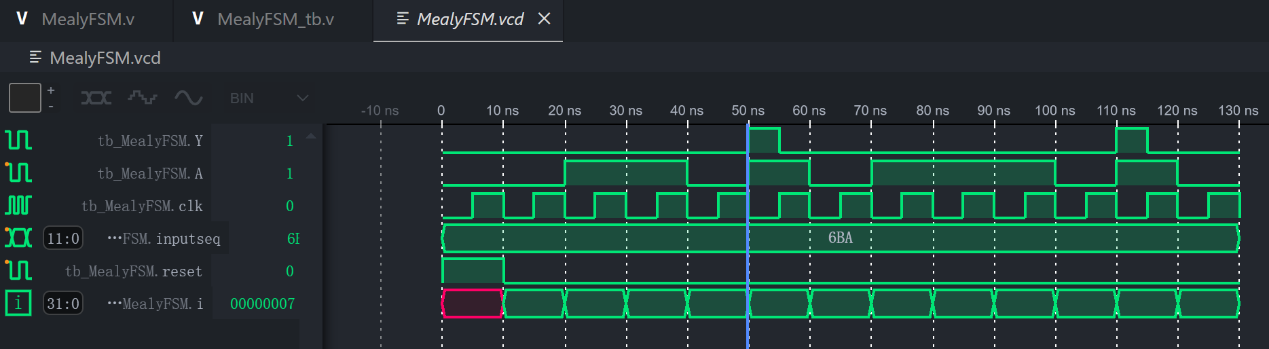




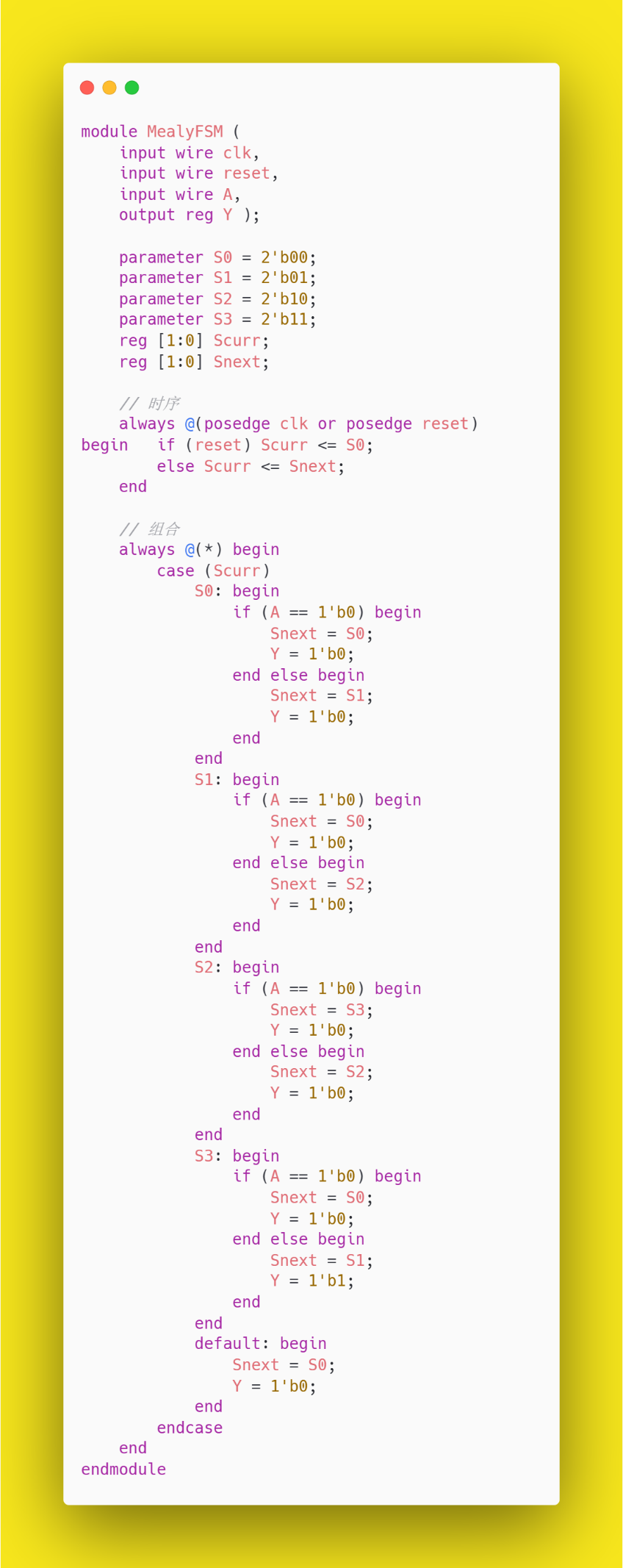
Part 2--Mealy FSM





Here are the snapshots of my MealyFSM.

In the sequence 12'b011010111010 ,it turns 1 from 0 at the 5th and 11th clk.



图片包含 日程表

AI 生成的内容可能不正确。