

op	instruction name	Reg write	Imm src	ALU src	mem write	Result src	Branch	ALU op	sel	jump	jalr register
0-4	R-type	1	XXX	0	0	00	0	based on op	0	0	0
5	lw	1	000	1	0	01	0	000	0	0	0
6-9	I-type	1	000	1	0	00	0	based on op	0	0	0
10	jalr	1	000	1	0	XX	X	000	1	X	1
11	sw	0	001	1	1	XX	0	000	0	0	0
12	jal	1	011	X	0	XX	0	XXX	1	1	0
13-16	B-type	0	010	0	0	X	1	Based on op	0	0	0
17	lui	1	111	X	0	11	0	XXX	0	0	0

```

max = 0;
for(i=0; i<10; i++)
    if(A[i] > max)
        max = A[i];
return max;

```

RISC-V Assembly Code

```

max: r1
i: r2
10: r3
A[i]: r4

```

```

0 addi r1, r1, 0
1 addi r2, r2, 0
2 addi r3, r3, 10
loop 3 bge r2, r3, end-loop
4 lw r4, A(r2)
5 bge r1, r4, end-if
6 addi r1, r4, 0
end-if 7 addi r2, r2, 1
8 jal r5, loop
end-loop

```

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machine code

```

6-1-1-0
6-2-2-0
6-3-3-10
16-2-3-offset(6)
5-4-0-2
16-1-4-offset(2)
6-1-4-0
6-2-2-4
12-5-offset(-5)
2's complement

```