



Service Manual

3913 985 09353

December 1991

This manual is for use with equipment supplied by Harris TVT. Performance figures quoted are typical and subject to normal manufacturing tolerances.

The right is reserved to alter the equipment described in this manual in the light of future technical development.

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STEREO SOUND IN SYNC

LDM 1903/1904

CODER

8928 190 30001

3270



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3913 985 09350

STEREO SOUND IN SYNC
IS DEVELOPED IN COLLABORATION WITH
THE BRITISH BROADCASTING CORPORATION AND USING
BBC PATENT NO. GB 2116403.

IMPORTANT NOTICE

THIS EQUIPMENT IS INTENDED FOR OPERATION ONLY UNDER
THE RESPONSIBILITY OF SKILLED PERSONNEL AS DEFINED
IN PARAGRAPH 3.1 OF IEC PUBLICATION 215,
2ND EDITION, 1977 ("SAFETY REQUIREMENTS FOR RADIO
TRANSMITTING EQUIPMENT").

FIRST AID IN CASE OF ELECTRIC SHOCK

DO NOT TOUCH THE VICTIM WITH YOUR BARE HANDS until the circuit is broken.

SWITCH OFF. If this is not possible, **PROTECT YOURSELF** with dry insulating material and pull the victim clear of the conductor.

THE EXPIRED AIR METHOD OF ARTIFICIAL RESPIRATION *(Approved by the Royal Life Saving Society)*

- 1 Lay the patient on his back with his arms to his sides. If on a slope have the stomach slightly lower than the chest. Make a brief inspection of the mouth and throat to ensure that they are clear of obvious obstruction.
- 2 Kneel on one side of the patient level with his head, place one hand under his neck and the other on top of his head (Fig. 1). **LIFT THE NECK AND TILT THE HEAD BACK AS FAR AS POSSIBLE.**
- 3 Move the hand from under the neck and place it on the chin of the patient, the thumb between the chin and mouth, the index finger along the line of the jaw, the remaining fingers curled (Fig. 2). Whilst positioning the patient, open your mouth and take deep breaths.
- 4 Using the thumb of your hand on the chin to keep the lips sealed, open your mouth wide and make a seal round the patient's nose and blow into it (Fig. 3).
- 5 After blowing, turn your head to observe the rise of the chest (Fig. 4). If no air enters the patient's lungs, the nose may be blocked and the mouth should be opened using the hand on the chin; open your mouth wide and making a seal round his mouth blow into it. Turn the head to observe the chest rise. This may be used as an alternative to blowing into the nose even when the nose is not blocked, but the nose must be sealed either with the cheek or by moving the hand from the top of the head and pinching the nostrils.
THE HEAD MUST BE KEPT AT FULL BACKWARDS TILT.
- 6 Start with ten quick deep breaths and then continue at the rate of twelve to fifteen breaths per minute. This should be continued until the patient revives or a doctor certifies death.
- 7 In the case of facial injuries it may be necessary to do a manual method of artificial respiration (Holger Nielson).
- 8 It is ESSENTIAL to commence artificial respiration without delay and to send for medical assistance immediately.



TREATMENT FOR BURNS

If the patient is also suffering from burns, then, without hindrance to artificial respiration, observe the following:

- (a) **DO NOT ATTEMPT TO REMOVE CLOTHING ADHERING TO THE BURN.**
- (b) If help is available or as soon as artificial respiration is no longer required the wound should be covered with a **DRY** dressing.
- (c) Oil or grease in any form should **NOT** be applied.

Further details of charts and books on artificial respiration may be obtained from:

The Royal Life Saving Society, 14 Devonshire Street, Portland Place, London, W.1.

A M E N D M E N T R E C O R D S H E E T

STEREO SOUND IN SYNC CODER

LDM 1903/00/01 (8928 190 30001)

Publication No. 3913 985 09353

All official amendments issued for this publication should be recorded in the following table.

AL No.	AL Date	Date Incorporated	By Whom	Remarks
1	Dec/90	Dec/90	-	General update incorporated.
2	Jan/91	Dec/91	TVT	New Clock and I/O (Reframer)
3				
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STEREO SOUND IN SYNC CODER

LDM 1903/10/01 (8928 190 30001)

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CODER

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STEREO SOUND IN SYNC CODER

LDM 1903/00/01 (8928 190 30001)

GENERAL DESCRIPTION - CODER

1. INTRODUCTION

This volume contains detailed information on all the modules that can form part of the Coder. At this stage each section contains:

- (a) Detailed circuit description.
- (b) Circuit diagram.
- (c) Printed circuit board assembly drawing.
- (d) Parts lists.

- Notes:
- (i) In some cases the part numbers on the circuit diagram and the assembly drawing differ from that of the title of the section.
 - (ii) The item numbers appearing on the assembly drawing refer to the item numbers in the parts lists.

An outline block diagram of the Coder is shown in Sh. 510-1, and interconnection of the main modules is shown in the functional block diagram, Sh. 536-1.

8928 190 30001
General Description - Coder

STEREO SOUND IN SYNC CODER

LDM 1903/00/01 (8928 193 30001)

GENERAL DESCRIPTION - CODER

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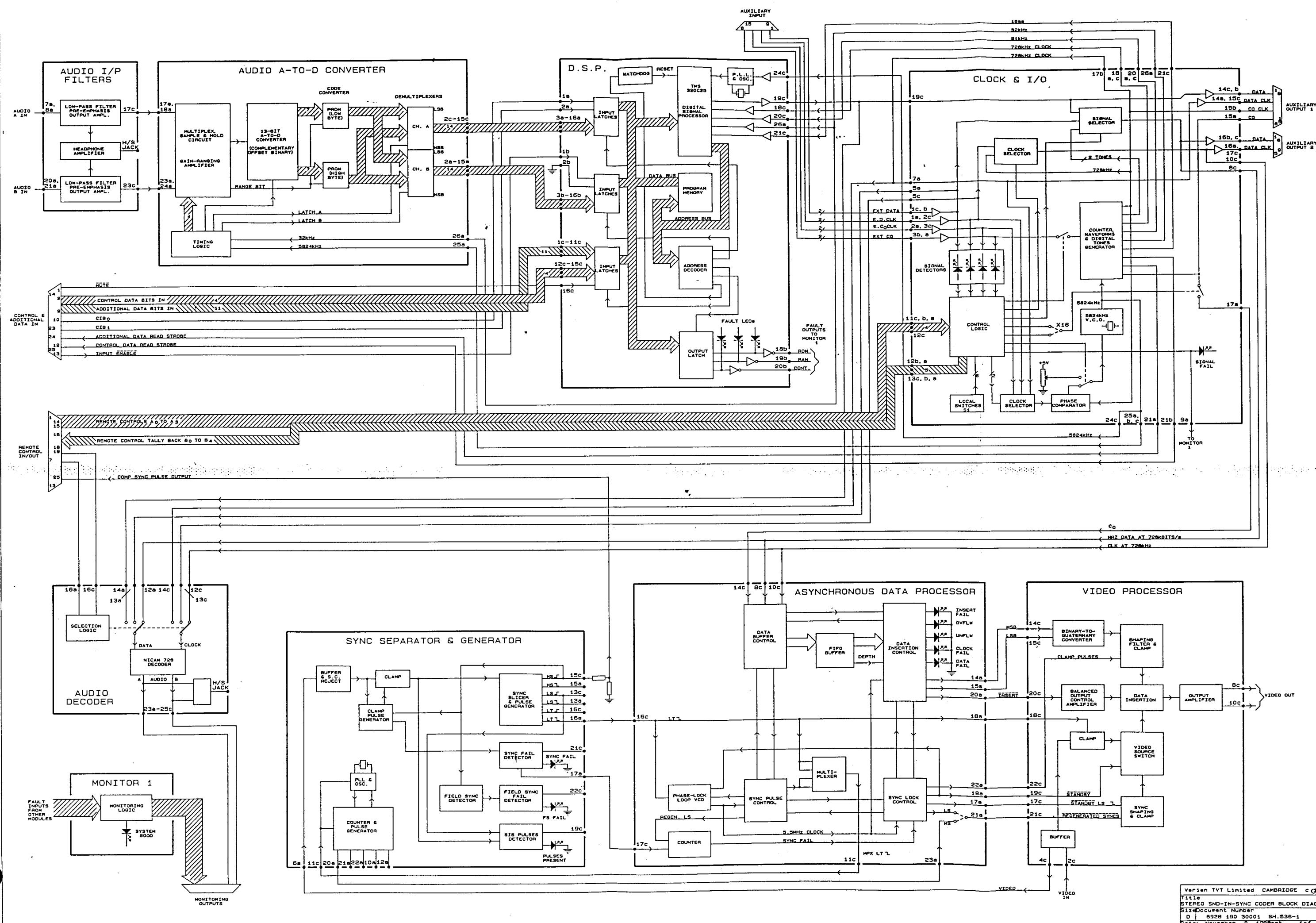
1. INTRODUCTION Sh. 595-1

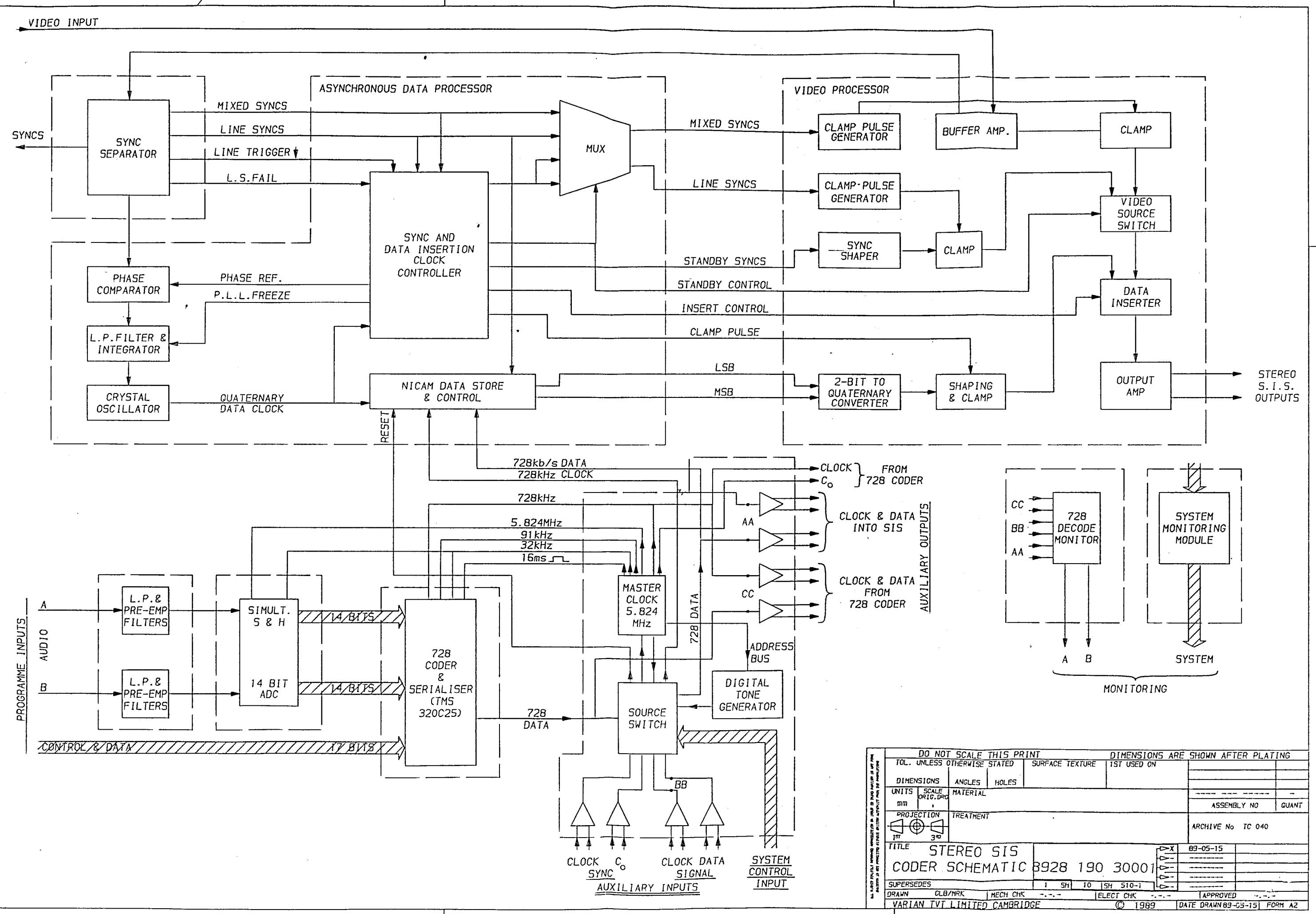
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PSU MODULE

3913 446 74920

(Issue 1)

References	Brief Description of Change	Documents Affected
PGV 3322 5.10.87	F2 changed from 1A, 2422 086 01021 to 1.25A, 2422 086 01023. F3 changed from 1A, 2422 086 01021 to 1.25A, 2422 086 01023.	Parts List Circuit Diagram
PGV 3613 02.04.90	C7 to C9, 100nF capacitors, 3913 200 10052 and C10 to C13, 100nF capacitors, 2012 310 00318 added to improve noise immunity.	Parts List Circuit Diagram Assembly Drawing
PGV 3963 06.07.90	R5, 0R51 resistor, 2113 256 02619 added in series with A3 + and R6, 0R51 resistor, 2113 256 02619 added in series with A3 - to reduce surge at switch-on.	Parts List Circuit Diagram Assembly Drawing Text

PSU MODULE3913 446 749201 FUNCTIONAL DESCRIPTION

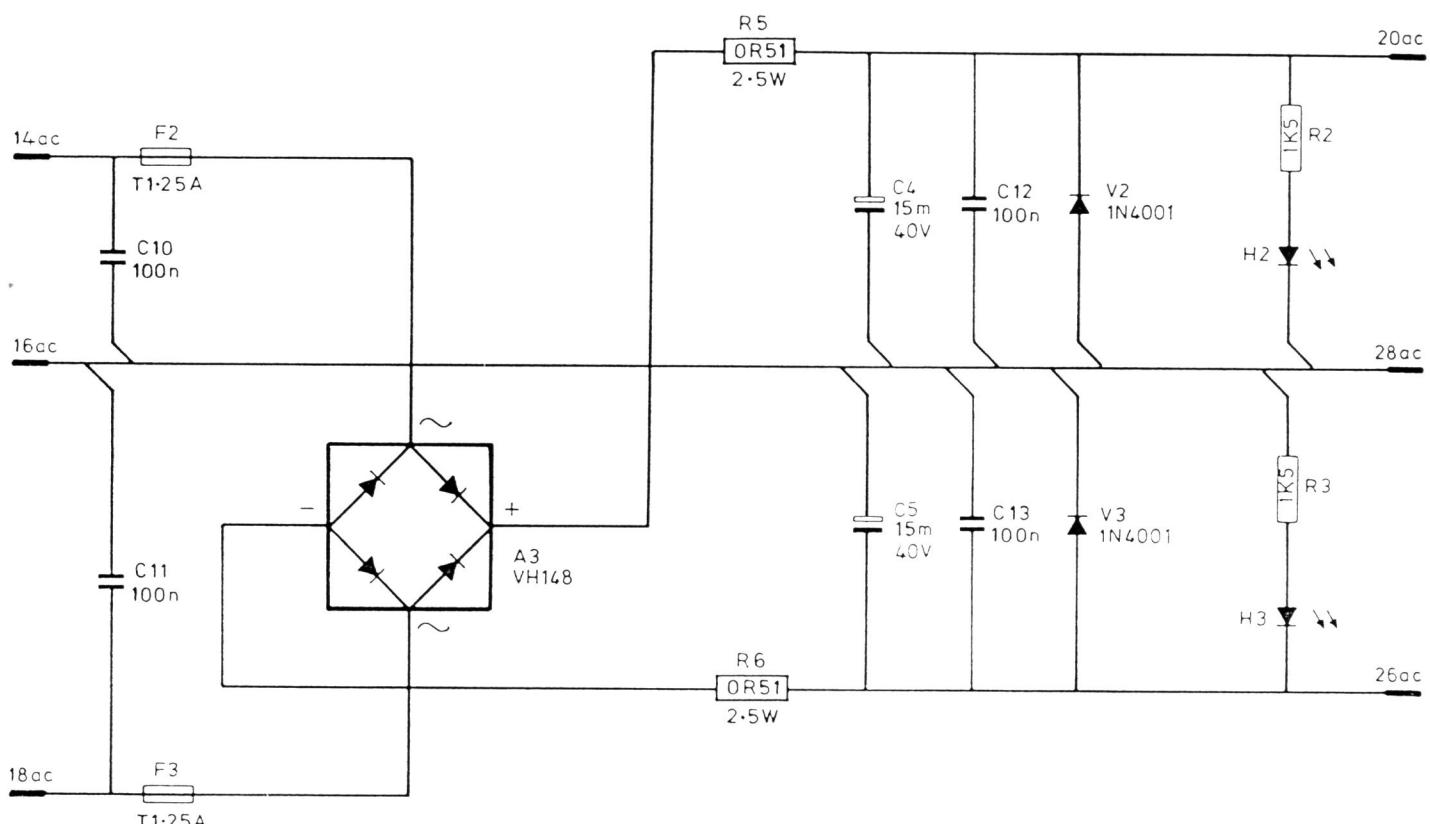
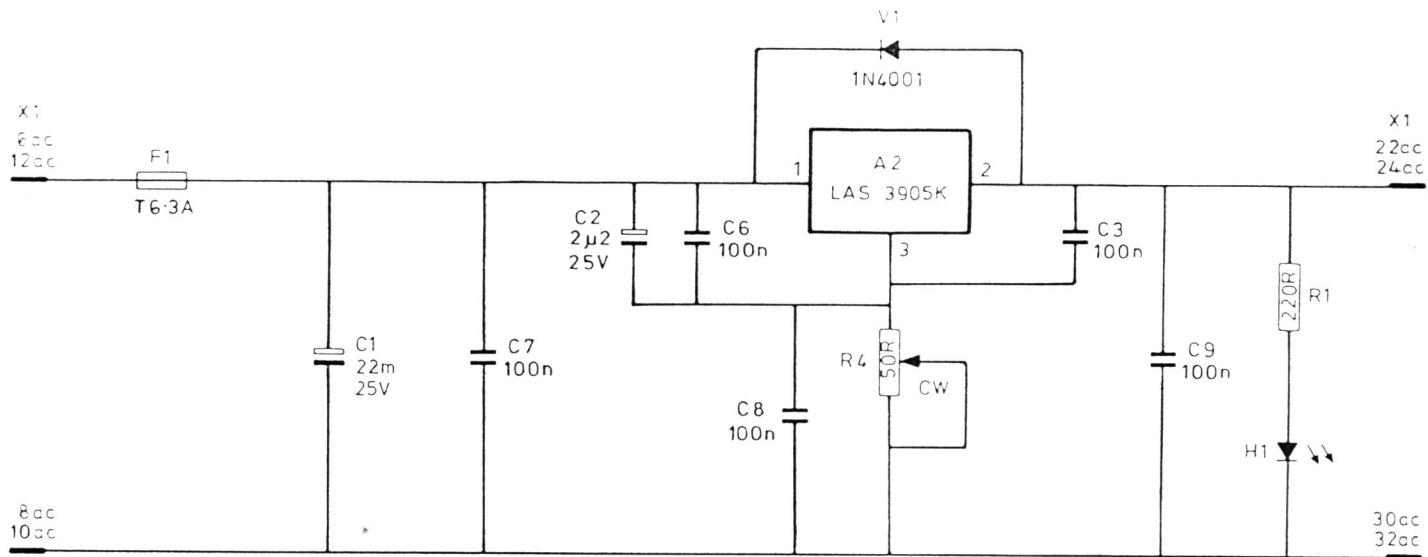
The Power Supply module works in conjunction with the mains transformer and bridge rectifier situated on the back panel of the equipment.

The +5V supply utilises an LAS 3905K regulator IC (A2). It is rated at 8A output and has internal current limiting and thermal shutdown. It is also protected by fuse F1 which, in practice, will normally blow before either the current limit or thermal limit is reached. It is supplied from a 9.1 - 0 - 9.1V centre-tapped secondary of the mains transformer, full-wave rectified by the diode bridge mounted on the back panel. The 5V output voltage is adjusted by R4. Refer to the System Setting-up Instructions in the System Description and User Information Manual.

The ±20V is unregulated. The full-wave bridge rectifier A3, on this board, is supplied from a 16.3 - 0 - 16.3V centre-tapped secondary of the mains transformer. The loaded output voltages should be within 1V of the nominal 20V, if the mains input voltage is at its nominal value. If either of the fuses F2 or F3 should blow, the surviving one will carry the whole load and also blow almost immediately. R5 and 6 reduce the switch-on surge, thus reducing the likelihood of F2 or 3 blowing unnecessarily.

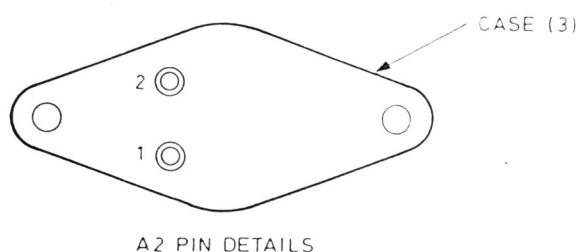
2 FAULT FINDING

If a single diode of a bridge rectifier should fail, the problem may not be immediately apparent, but will be revealed by checking the frequency of the ripple voltage across C1 or C4/C5, which will be 50Hz instead of 100Hz.



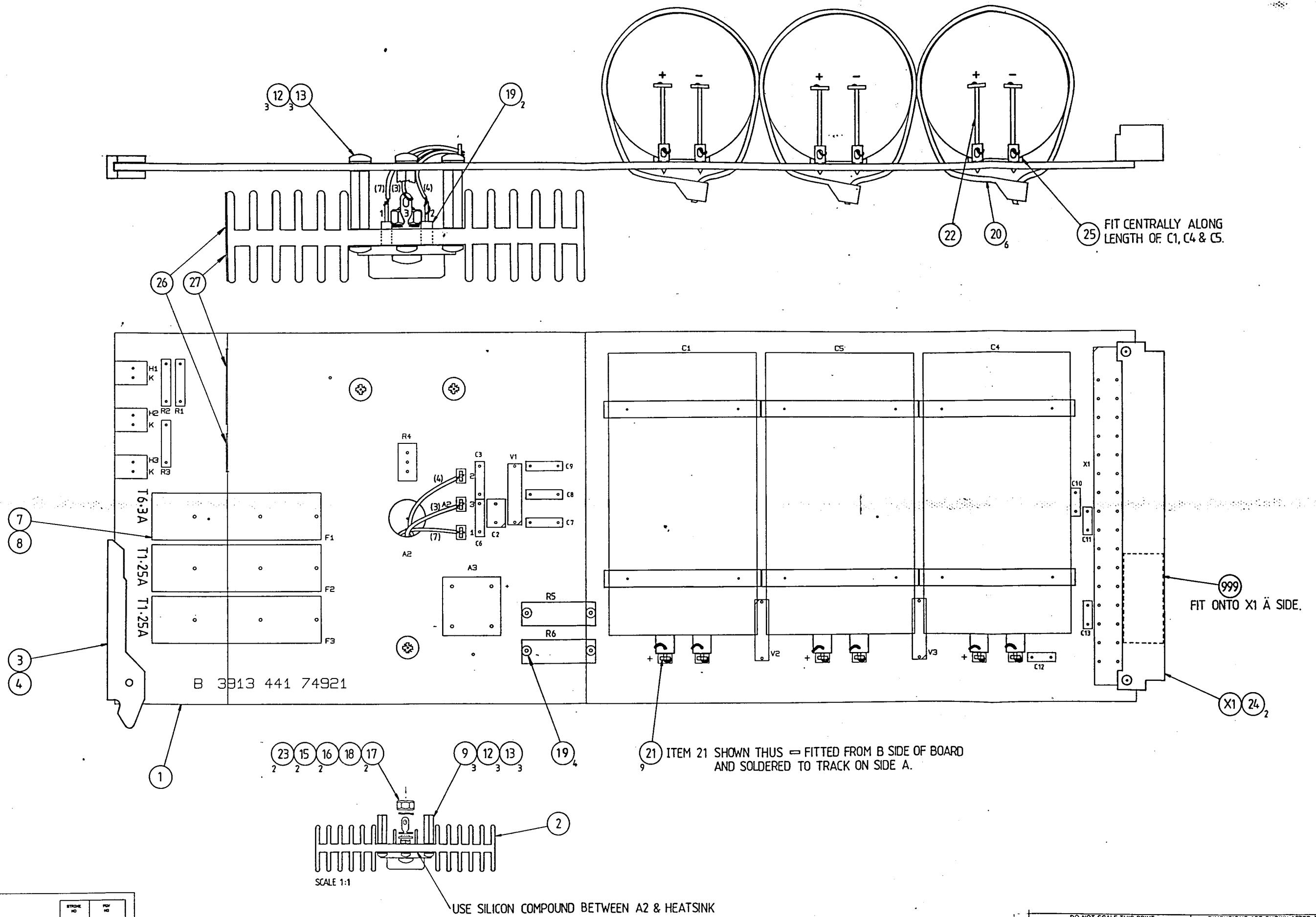
A2 CAN BE REPLACED BY R.S. 659-747

(IP3R18K-05)



A2 PIN DETAILS

POWER SUPPLY UNIT ASSEMBLY CIRCUIT		3913 446 7492	1 880113 3322 1 890330 CA31394 1 890330 3613 1 900709 3963
		SH.130-1	
DRAWN ISI LTD		CHK C. S. Clements APPROVED	
PYE T.V.T LIMITED CAMBRIDGE © 1987		DATE DRAWN 870127 FORM A3	



DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PULLING	
TOL UNLESS OTHERWISE STATED		SURFACE FINISH	
UNITS MM		ANGLES IN DEG	
PROJECTION		TREATMENT	
SEE SEPARATE PARTS LIST		SEE 3913 982 90010 CODE C.	
TITLE PSU PCB ASSY.		3913 446 7492	
SUPersedes		1 3913 446 7492	
DRAWN BY D.J.E.		MECH CHK	
ELECT CHK		APPROVED	
PYE T.V.T. LIMITED CAMBRIDGE (TRANSMITTER DIV.) © 1986 DATE DRAWN 86/10/09 FORM A			

AUDIO INPUT FILTERS

3913 446 74860

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AUDIO INPUT FILTERS

3913 446 74860

References	Brief Description of Change	Documents Affected
PGV 3249 11.5.87	Audio gain changed so that the headroom is defined at 14.8dB below maximum audio coding level with input at 0dB at 2kHz; gain set 2.8dB lower.	Text
PGV 3732 89.09.06	The note on the circuit diagram regarding the setting of R25 in the output amplifier is changed to read: "R25 is adjusted to set the gain to give the headroom specified for NICAM-3 and NICAM 728 (UK) of 14.8dB below the maximum coding level of the ADC. For an input of 0dBu at 2kHz the loss through this module is then 0.43dB at 2kHz or 5.13dB at 1kHz. At this headroom setting an input signal of +8dBm is below the maximum coding level at all frequencies."	

3913 446 74860
Addendum

AUDIO INPUT FILTERS

3913 446 74860

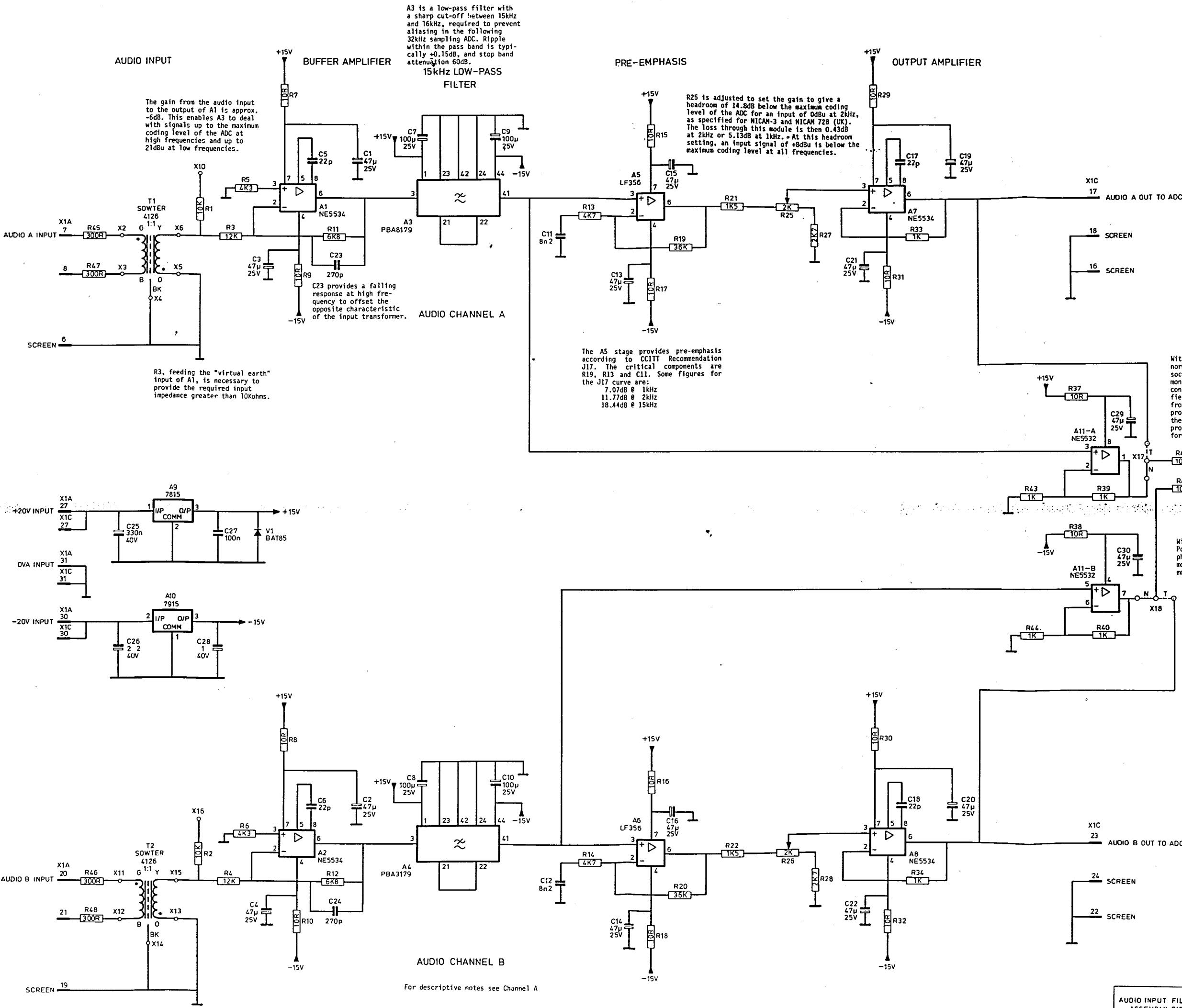
ADDENDUM

The note on the circuit diagram referring to the Output Amplifier should read as follows:

R25 is adjusted to set the gain to give a headroom of 14.8dB below maximum coding level of the ADC for an input of 0dBu at 2kHz, as specified for NICAM-3 and NICAM728 (UK). The loss through this module is then 0.43dB at 2kHz or 5.13dB at 1kHz. At this headroom setting an input signal of +8dBu is below the maximum coding level at all frequencies.

The reasons for this addendum are:

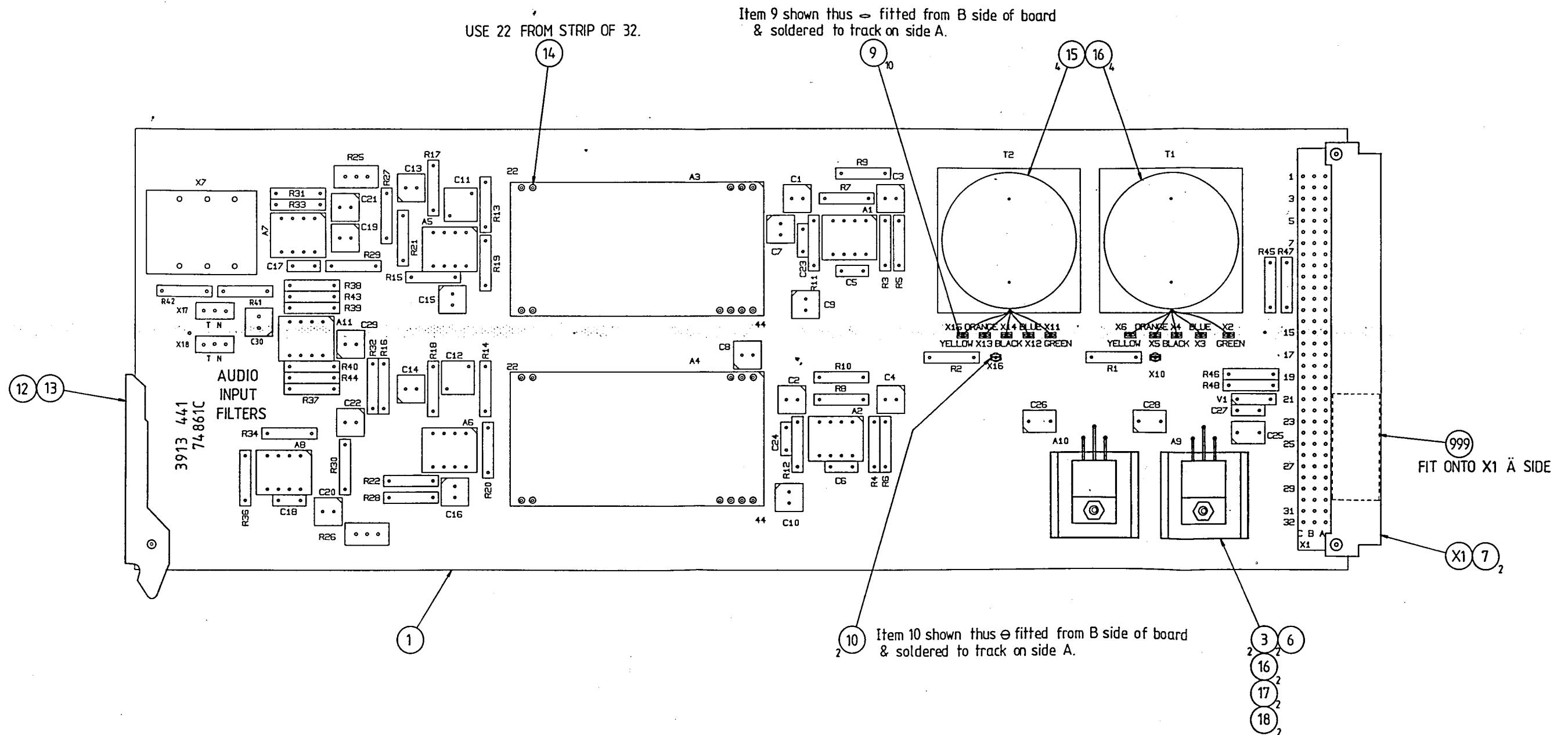
1. To make it clear that the gain is set to the UK standard.
2. EBU headroom has apparently changed recently and it is hoped that it will eventually fall into line with the UK.
3. To fully change to the EBU standard would involve changing EPROMs containing digital data for test tones.



With Links X17 and X18 in the normal position (N), the jack socket X7 provides headphone monitoring of audio input. It is connected via the buffer amplifier A11. The inputs to A11 come from after the 15kHz filter to provide 6dB of gain to compensate for the 6dB loss up to A3.

With Links X17 and X18 in Position T (test), the headphone socket can be used to monitor the output from this module.

3913 446 7486	870723
1 990818	CA34682
1 901129	3732
SH.130-1	
DRAWN ISI LTD	CK T. P. ROGERS APPROVED
PYE TVT LIMITED CAMBRIDGE © 1986	
DATE DRAWN 860909 FORM A1	



STRIKE PLATE INSTRUCTION	
S AFFIX STRIKE PLATE NO 8010 001 0005 IMBED WITH THIS ASSEMBLY IN POSITION INDICATED	
S STRIKE PLATE NUMBERS ON PLATE TO LEVEL INDICATED IN THIS INSTRUCTION	
	
NOTE: THE STRIKE LEVEL SHOWN HERE MUST NOT BE CONFUSED WITH THE ISSUE DATES SHOWN ON ASSOCIATED DRAWINGS & PARTS LIST.	
STRIKE NO	POV NO
1	3249
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DO NOT SCALE THIS PRINT			DIMENSIONS ARE SHOWN IN INCHES		
TOL. UNLESS OTHERWISE STATED		SURFACE TEXTURE		NOT USED ON	
DIMENSIONS	ANGLES	HOLES			
UNITS MM	SCALE ORIG. DEG. 21	MATERIAL 14			
SEE SEPARATE PARTS LIST.			ASSEMBLY NO.		QUANT.
PROJECTION 	TREATMENT SEE	3913 982 90010 CODE C.	PART/ITEM NO.		MODEL NO.
TITLE AUDIO INPUT FILTER PCB ASSY.			3913 446 7486	1886.09.10 1886.11.25	
SUPERSEDES			1 SH 10 SH 100-1		
DRAWN BY PYE T.	CH CMC	ELECT CMC	APPROVED		
LIMITED C.A. BRIDGE (TRANSMITTER DIV.) © 1986			DATE DRAWN 86.09.10		FORM A 1

3913 446 69860
(Version 1)

AUDIO ADC

3913 446 69860

(Version 1)

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References	Brief Description of Change	Documents Affected
PGV 3837 90.01.17	Audio ADC screen 3913 443 67090 added to the PCB. (Versions 8928 190 31001, 31201, 31401 and 31501).	Assembly Drawing Parts List
PGV 3927 02.04.90	A9 Timing PROM, 3913 036 60390 changed to 3913 036 60600. This is to overcome error in data for timing waveforms for A3, that cause distortion at high level, high frequency.	Parts List

AUDIO ADC

3913 446 69860

(Version 1)

1. FUNCTIONAL DESCRIPTION

The basis of the audio analogue-to-digital converter (ADC) system is a 2-channel sample-and-hold amplifier and multiplexer, Analogic MP282A (A3), and a 16-bit Burr-Brown A-to-D converter PCM75JG (A4).

Both audio channels are presented to A3 and, under the control of the latched CHANNEL SELECT input, they are both sampled (Link X10 being in Position S), then one channel is gain-ranged and output to A4. This is held to allow the A/D converter enough time to finish conversion, and then the other channel is gain-ranged and output. The gain ranging that A3 carries out on the signal consists in applying a gain of either x_1 or x_2 to the output signal, with respect to the input, depending upon whether the input signal is respectively, greater than, or less than, a set reference level, nominally half maximum amplitude. Thus, the bit accuracy of the ADC is maintained at low signal levels. A3 also outputs a 'gain bit' which indicates the gain that has been applied to the output signal. Using this system, an ADC with a resolution of n bits can have its resolution at low signal levels increased to $n + 1$ bits, by using the extra gain bit and appropriate code conversion on the ADC digital outputs.

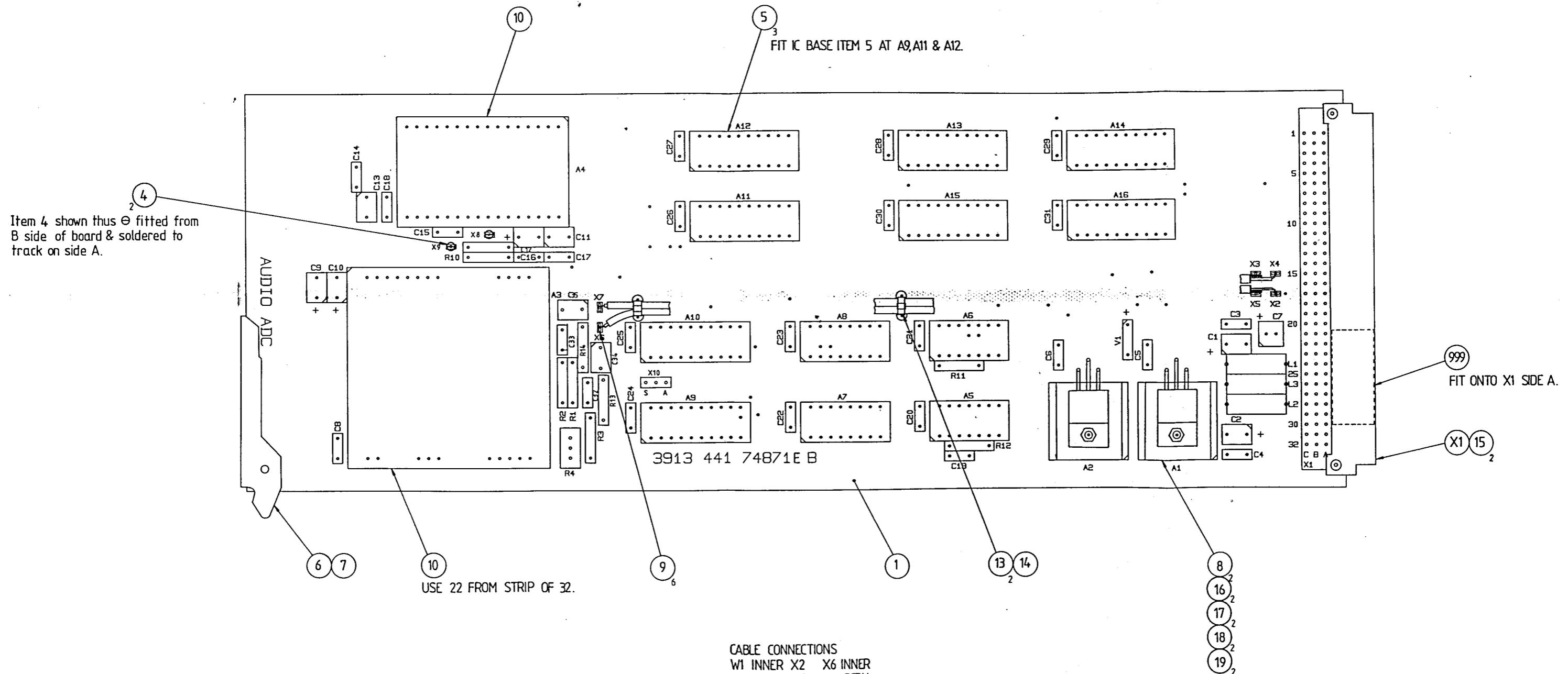
The A/D converter A4 is a 16-bit converter with a guaranteed accuracy of 14 bits. However, in this application, it is 'short-cycled' to 13 bits, which means that it only converts to 13 bits, the 14th bit required for full output accuracy being supplied by the gain bit of A3. 'Short-cycling' the converter has the added advantage that the conversion time is shortened. By biasing pin 23 of A4 ('clock rate control') to around +10V provides a further reduction in conversion time to less than $10\mu s$, allowing two channels to be sampled sequentially at a rate of 32kHz.

The digital outputs of A4 are used to address two PROMS, A11 and A12. These are used to provide the code conversion from complementary offset binary out of the A/D converter, to 2's complement, to be fed to the next module, and also take account of the gain ranging in A3. This is achieved by feeding the gain bit to both PROMS. When the gain bit indicates that a gain of x_2 has been applied to the ADC input signal, then the output code must be divided by 2, i.e. shifted right by one bit. When the gain applied is x_1 no shift is required. Because of this bit shifting, and there being two PROMs, one of the bits will 'cross the boundary' between the PROMs, i.e. it comes from either one or the other PROM, depending upon the shift applied. The two possible sources of that bit are fed into A6c, A6c and A6d forming an AND gate so that a logic 1

on one input allows the other input to appear directly at the output. Hence, the PROM which is not supplying the bit outputs a logic 1 and the bit from the other PROM is fed to the output latches.

Since the ADC is sampling two channels sequentially, the PROM outputs are latched onto the card outputs by means of A13, A14 for channel A and A15, A16 for channel B.

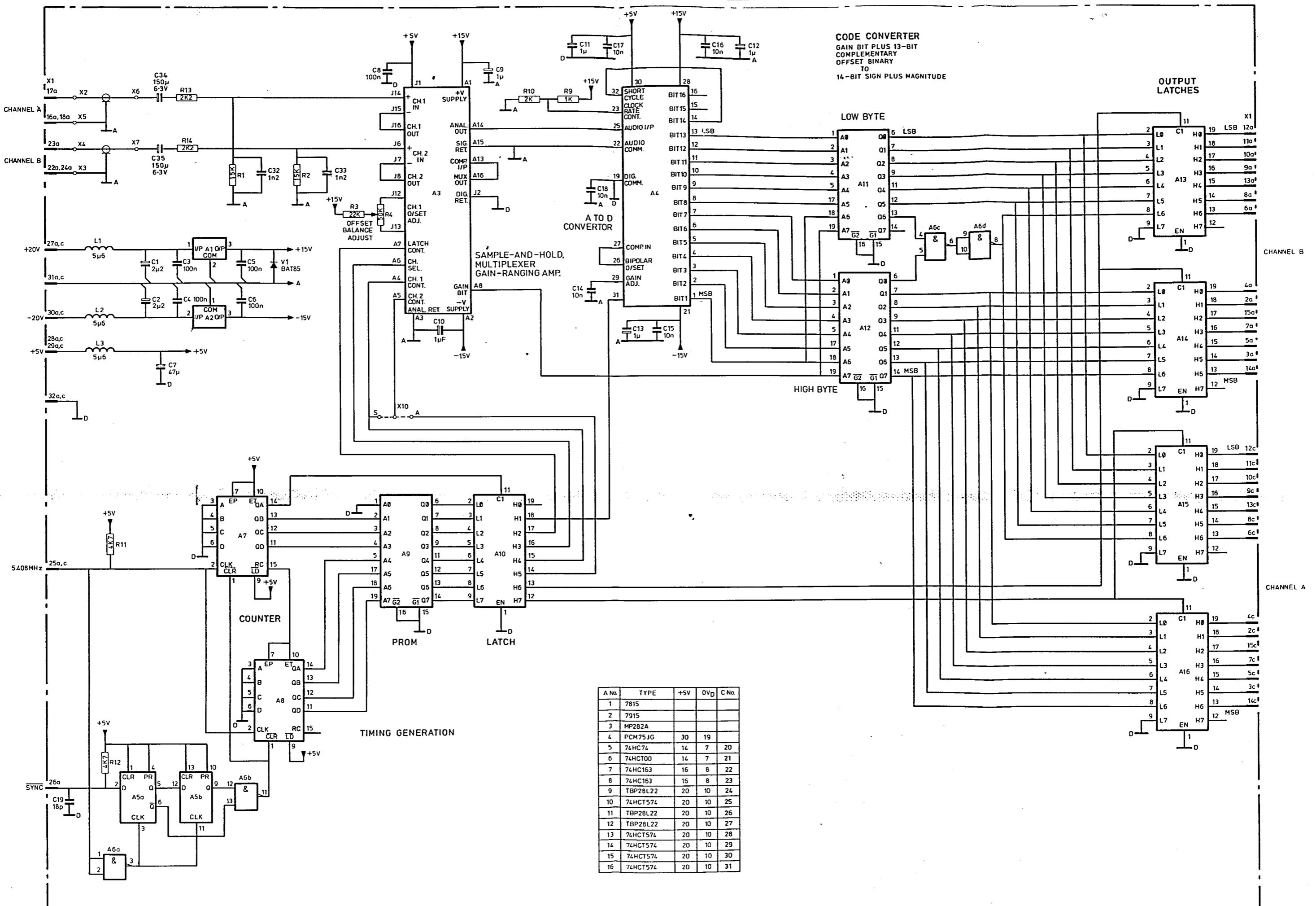
All the appropriate timing signals for A3, A4, and clocking for the output latches, are generated from A5 - A10. The 5.824MHz and 32kHz sync signals are supplied, phase locked, from the Clock and I/O module. The 5.824MHz clock drives the two counters A7 and A8. On the falling edge of sync, a reset pulse is generated from A5 and A6a,b, which resets A7 and A8 to zero, giving a count of 182 (0 to 181). The outputs from the counters produce the address for the timing PROM, A9, and the data are clocked through A10 to ensure accurate timing, A10 being clocked by the LSB from the counters, which is a 2912kHz square wave. PROM data are such that they change only on falling edges of this clock, and are then clocked through A10 on the rising edge of the same.



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CABLE CONNECTIONS
W1 INNER X2 X6 INNER
W1 SCRН X5 — SCRН
W2 INNER X4 X7 INNER
W2 SCRН X3 — SCRН

DO NOT SCALE THIS PRINT				DIMENSIONS ARE SHOWN AFTER PLATING			
TOL UNLESS OTHERWISE STATED		SURFACE TEXTURE		AS USED ON			
DIMENSIONS	ANGLES	HOLES	MATERIAL				
UNITS MM	SCALE ORIG. DIA. 2-1						
SEE SEPARATE PARTS LIST.							
PROJECTION 	TREATMENT					ASSEMBLY NO. QUANT	
SEE 3913 982 90010 CODE C.						PATTERN NO.	MODEL NO.
THE AUDIO ADC PCB ASSEMBLY DRAWING.				3913 446 7487		11 860930	
SUPERSEDES				1 34 10 5m 100-		11 870707 97	11 870606 97 PGV 3270
DRAWN BY	TP	MECH CHN	ELECT CHN			APPROVED	
PYE T.V.T LIMITED CAMBRIDGE (TRANSMITTER DIV.) © 1976				1976		DATE DRAWN B80930 FORM A	



DRAWN ISI LTD	3913 446 7487	1 880113 CA34005
SH.130-1	1 880120 3270	
PTE LTD CAMBRIDGE © 1986		DATE DRAWN 860909 FORM A1

DIGITAL SIGNAL PROCESSOR PCB ASSEMBLY3913 446 75400Contents

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DIGITAL SIGNAL PROCESSOR PCB ASSEMBLY

3913 446 75400

References	Brief Description of Change	Documents Affected
PGV 3913 26.03.90	Handle mounting pad replaced with non-conducting one. Track to H7 and H8 re-routed to avoid possibility of short circuit to +5V rail.	Parts List
PGV 4181 19.10.90	A2, Nicam 728 Lo-byte Coder, 3913 036 60510 changed to 3913 036 60640. A3, Nicam 728 Hi-byte Coder, 3913 036 60520 changed to 3913 036 60650. This is to change code for Range 7 Nicam 728 from 000 to 001 because some decoders do not decode 000 correctly.	Parts List

DIGITAL SIGNAL PROCESSOR PCB ASSEMBLY3913 446 754001. GENERAL DESCRIPTION

This module is based on the Texas second generation Digital Signal Processor chip TMS320C25. This will run at a clock rate of up to 40MHz, giving a execution speed of 10 MIPS, and has 544 words of on-chip data memory (RAM), 256 words of which can be re-allocated under software control to the program memory space, and 4K words of on-chip program memory (mask programmable ROM). A military version of the chip, the TMS320C26, is identical to the TMS320C25 except that it has 1568 words of on-chip data RAM, up to 1536 words of which can be re-allocated to the program memory space in blocks of 512 words, and only 256 words of on-chip program ROM. In this application, the DSP is connected to always operate in the microprocessor mode, i.e. with all program memory external. The module has been designed so as to be as general purpose as possible by fitting alternative components, which are described in the following sections.

2. FUNCTIONAL DESCRIPTION

2.1 Memory

Program memory is provided by A2 and A3, 8K x 8 fast EPROMs, A2 being the low byte and A3 being the high byte. External program memory addressing begins at address 0. For the maximum clock rate of 40MHz to be used, 35ns access time devices must be fitted. Using 45ns devices, the maximum clock rate is limited to 37.5MHz. Data memory is provided by A4 and A5, 2K x 8 static RAMs, A4 being the low byte and A5 the high byte. External data memory addressing begins at 400hex, the first 1K of data memory being internal and reserved memory. Again, for a clock rate of 40MHz, 35ns devices must be used. Note that the memory addresses are not fully decoded, so that the program memory will repeat in 8K blocks throughout the memory map, and the data memory will repeat in 2K blocks throughout the memory map.

2.2 Input/Output Ports

The module has three input/output ports 16 bits wide, designated Ports 0, 1 and 2. The decoding of the port addresses is carried out by A6, and A7a, A7b and A7c produce control signals for the input and output buffers A10 to A21. Each port may be either an input port, by fitting for example for port 0 A10 and A12, or an output port, by fitting for example for Port 0 A11 and A13. The selection of input or output for a particular port is entirely in hardware, and only one pair of buffers may be fitted for each port. The pull-up resistors for each line are individual resistors, not resistor packs, and series resistor positions are also provided, to allow individual bits of a port to be protected for external connections. Port 2 also has the facility of having the series resistors replaced by open-collector output buffers, A29 and A30. Thus, Port 2 may be configured in hardware as an open-collector output port.

2.3 LED Port

Port 6 is configured as an 8-bit output port, on the lower eight bits of the data bus, with A7d providing the clock signal to the output buffer A8. The port drives up to eight LEDs on the front of the module, and an open-collector buffer, A9. A logic 0 on a particular bit will light the appropriate LED and cause the open-collector output to go high (i.e. turn off).

2.4 Watchdog

A25 is a combined voltage monitor and watchdog timer. The timeout period of the watchdog is set to approximately 32ms by R100 and C3, and the watchdog is reset by executing an OUT instruction to Port 7, the decoded pulse from A6 being lengthened by two of the D-type flip-flops in A24 and A26a. A25 monitors the voltage on C2, which is divided down from the

regulated 5V supply by R98 and R99. V4 provides a fast discharge path for C2 if the 5V supply drops, and S1 is a manual reset button which acts by discharging C2. An external Reset pulse may also be applied, via A23 and V3. X2 disconnects A25 from the reset pin of A1, which is required when the module is operated with the Texas Software Development System.

2.5 Oscillator and PLL

The module clock can be derived in one of three ways: from an external clock input at the correct frequency, via A22 and X3, from the on-board crystal oscillator built around V2 and B1 and free running, or from the same oscillator locked to an external input. When the oscillator is to be locked, A27 is fitted and the division ratio of 2 to 16 inclusive is chosen by changing the counter preload value using R113 to R116 and selecting the appropriate output using R109 to R112. Appendix 1 at the end of this note gives the resistors that must be fitted for the appropriate division ratio. A31a acts as a phase comparator between the divided down oscillator frequency and the incoming locking frequency, the output of A31a charging up C4 to adjust the capacitance of the varicap diode V1. A31b, A31c and V5 form an active pull-up circuit to provide the clock drive to A1.

2.6 Control Signals

A22 and A23 act as buffers for the various input and output control signals used by the DSP. These include the serial input and output port signals, the three maskable interrupts, and the hardware branch input (BIO) and the external flag output (XF). The BIO input signal is passed through one D-type flip-flop in A24 to provide correct synchronisation with the internal clock phases in A1. The three interrupts do not require external synchronisation as they are internally synchronised. R117 to R120 allow the mode in which the serial output port is to operate to be selected, in conjunction with software. By fitting R117 and R118, transmit frame sync pulses output from A1 will be buffered out to the edge connector by A22; by fitting R119 and R120, transmit frame sync pulses input to the edge connector will be buffered into A1 by A22.

DIGITAL SIGNAL PROCESSOR PCB ASSEMBLY

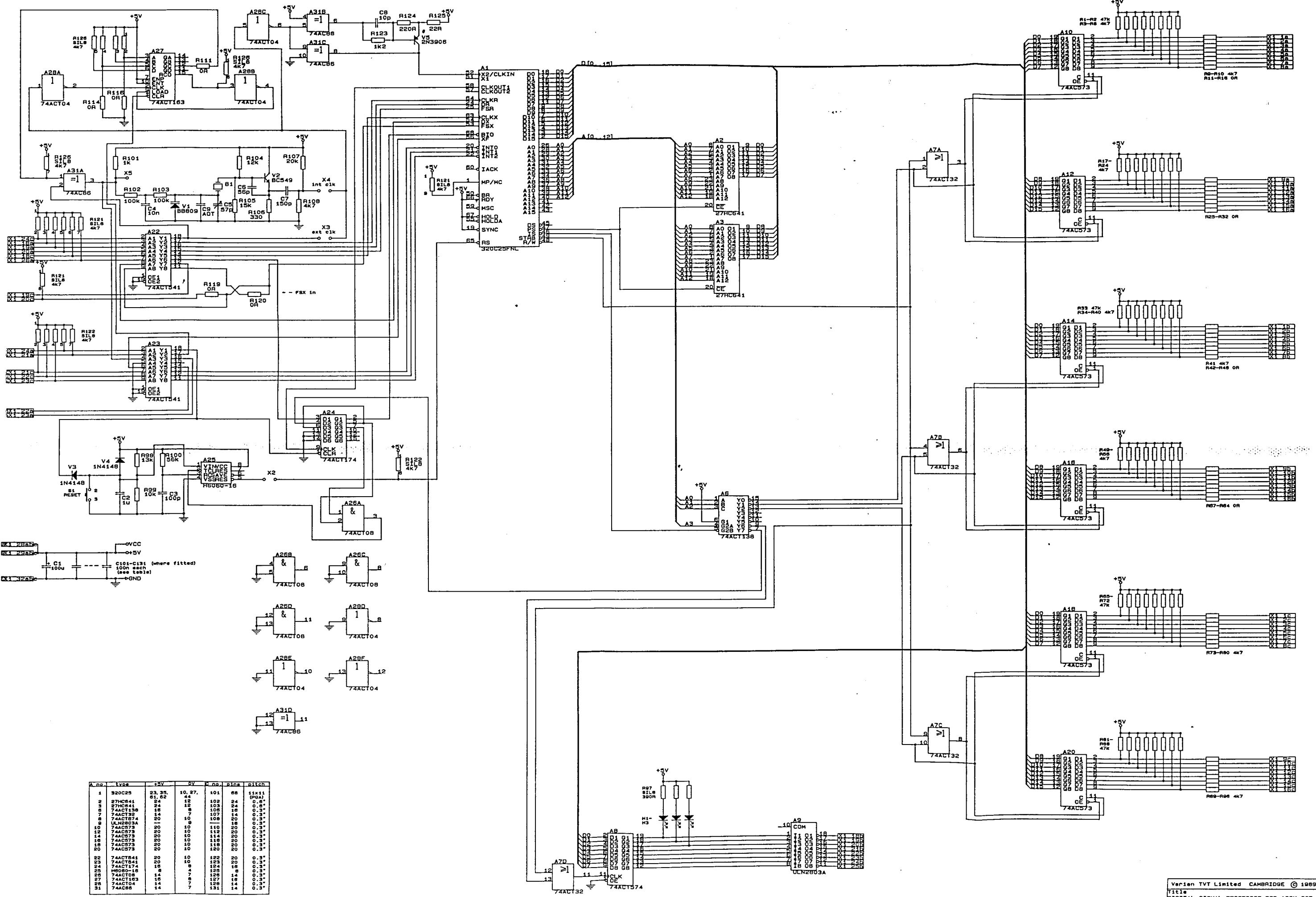
3913 446 75400

APPENDIX 1

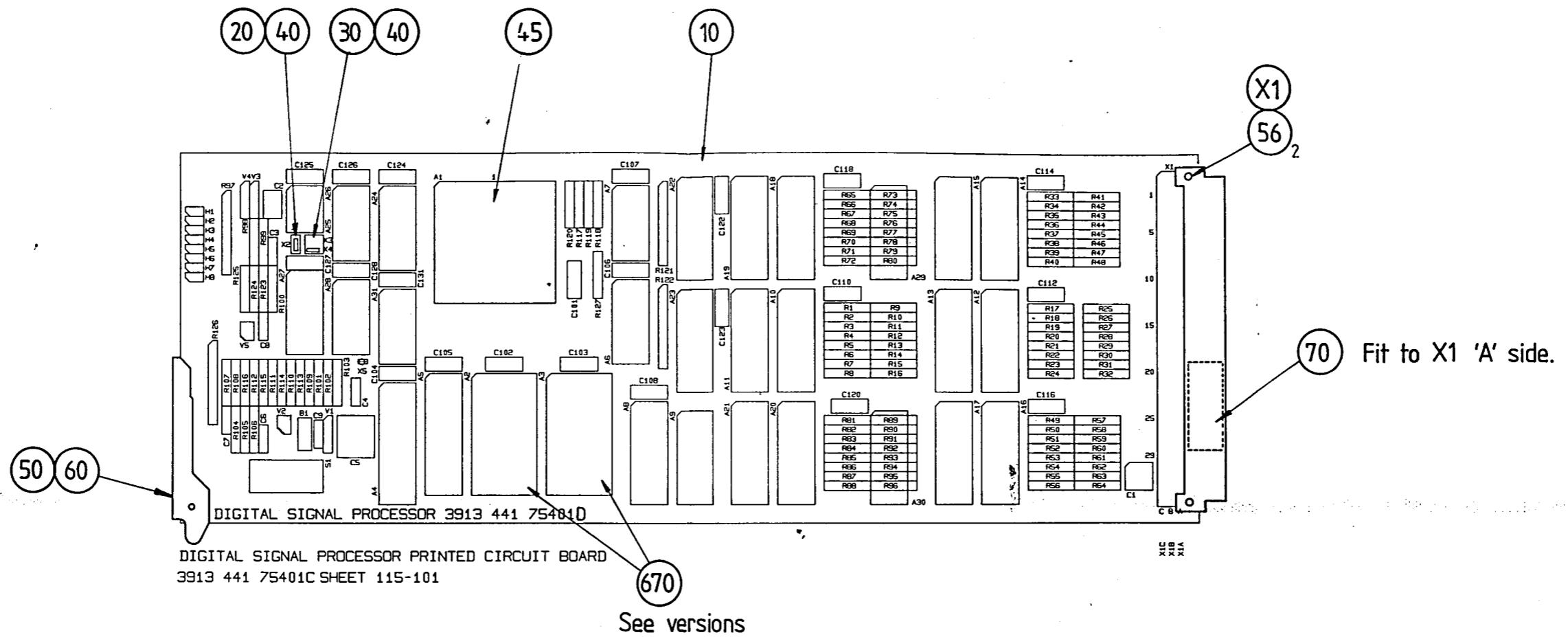
SELECTION OF PLL COUNTER DIVISION RATIOS

Division Ratio	Preload Resistor Selection				Output Resistor
	R113	R114	R115	R116	
2			X	X	R109
3			X		R110
4			X	X	R110
5		X			R111
6		X		X	R111
7		X	X		R111
8		X	X	X	R111
9	X				R112
10	X			X	R112
11	X		X		R112
12	X		X	X	R112
13	X	X			R112
14	X	X		X	R112
15	X	X	X		R112
16	X	X	X	X	R112

X = resistor to be fitted



A.no	type	+5V	0V	C.no	pins	pitch
1	320C25	23, 35, 61, 62	10, 27, 12	101	66	(15x11) 0.5x0.6
2	27HC841	24	12	102	24	0.5x0.6
3	27HC161	24	12	103	24	0.5x0.6
4	74ACT136	14	8	105	20	0.3x0.6
7	74ACT32	14	7	107	14	0.3x0.6
8	74ACT574	20	10	108	20	0.3x0.6
9	74ACT573	20	10	109	20	0.3x0.6
10	74ACT573	20	10	110	20	0.3x0.6
12	74ACT573	20	10	112	20	0.3x0.6
14	74ACT573	20	10	114	20	0.3x0.6
15	74ACT573	20	10	115	20	0.3x0.6
16	74ACT573	20	10	116	20	0.3x0.6
17	74ACT573	20	10	120	20	0.3x0.6
22	74ACT841	20	10	122	20	0.3x0.6
23	74ACT841	20	10	123	20	0.3x0.6
24	74ACT174	15	9	125	10	0.3x0.6
25	74ACT165	15	9	126	10	0.3x0.6
26	74ACT80	14	7	128	14	0.3x0.6
27	74ACT163	15	8	127	14	0.3x0.6
28	74ACT164	14	7	129	14	0.3x0.6
31	74AC80	14	7	131	14	0.3x0.6



DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING	
TOL. UNLESS OTHERWISE STATED		SURFACE TEXTURE	1ST USED ON
DIMENSIONS	ANGLES	HOLDS	
UNITS MM	SCALE DRIC.DRG 1:1	MATERIAL	
SEE SEPARATE PARTS LIST			
PROJECTION		TREATMENT	
1ST	3RD	SEE 3913 982 90010 CODE C	
TITLE DIGITAL SIGNAL PROCESSOR PCB ASSY DRG		3913 446 7540	
SUPERSEDES		1 SH.	SH. 110-1
DRAWN	MECH.DRG.	ELECT.DRG.	APPROVED
VARIAN TTV TD CAMBRIDGE (c) 1989 DATE DRAWN 18-10-89 FORM			

CLOCK AND I/O PCB ASSEMBLY

3913 446 75410

VERSION 2 - DECODER

Contents

CHANGE SUMMARY	Sh. 508-1
1. GENERAL DESCRIPTION	Sh. 595-1
2. FUNCTIONAL DESCRIPTION	Sh. 595-2
2.1 Master Oscillator	Sh. 595-2
2.2 Signal Selection and Routing	Sh. 595-2
2.3 Locking and Synchronisation	Sh. 595-2
2.4 Signal Selection and Synchronisation	Sh. 595-5
2.5 Tally-backs	Sh. 595-6

ILLUSTRATIONS

Circuit Diagram	Sh. 130-1
Assembly Drawing	Sh. 110-1

PARTS LISTS

C H A N G E S U M M A R YCLOCK AND I/O PCB ASSEMBLY

3913 446 75410

(Versions 1 and 2)

References	Brief Description of Change	Documents Affected
PGV 3802 89.11.15	R51, 4k7, 2322 156 14702 added. R38 component outline added to Version 1 circuit diagram. Minor mechanical change.	Circuit Diagram (Version 1) Parts Lists
PGV 3776 89.10.23	Pins 1 and 13 of A12 and A22 connected to +5V through R51, 4k7.	Circuit Diagram Assembly Drawing
PGV 3733 89.09.06	Waveform PROM A18 changed from 3913 036 60480 to 3913 036 60540. Control PROM A4 changed from 3913 036 60470 to 3913 036 60530 (Version 2). Contents changed.	Parts Lists
PGV 3734 89.09.07	Socket, DIL, 28-way, 2432 490 00073 added. Waveform PROM A18 changed from 3913 036 60540 to 3913 036 60560. C27 and C62 100n, 2012 310 00318 added. C61, 330n, 2012 310 00322 added. Header X19, 1 x 3, 3913 445 50120 added. Test pin X17, 1.3 x 1.02, 2413 015 02201 added. Header X18, 2 x 10, 3913 445 50550 added. Header X20, 2 x 3, 3913 445 50480 added. 3 Sockets, 2W, 2422 549 26016 added. Tones PROM A27, 3913 036 60550 added. Regulator A28, 5V, 1A, μ A7805, 3913 935 00001 added. R49, 100R, 2.5W w/w, 2113 256 02264 added. R50, 100k, 2322 156 11004 added. Parts Lists created for Tones and Waveform PROMS.	Circuit Diagram Assembly Drawing Parts Lists Text
PGV 3747 89.09.27	R4 changed from 220k to 560k, 2322 156 15604 Parts List errors corrected.	Circuit Diagram Parts List.
PGV 3752 89.10.02	C63, 100pF, 2222 683 34101 added between X1 Pin 9a/A26 Pin 11 and 0V.	Circuit Diagram Assembly Drawing Parts List.
PGV 3820 04.12.90	Waveform PROM A18 changed from 3913 036 60560 to 3913 036 60690 to correct reserve sound switching flag (C_4) in tone 2B to '0'.	Parts List
PGV 3776 Issue 2 18.01.90	Mounting of A28 Regulator changed to avoid shorting to PCB track.	Assembly Drawing

C H A N G E S U M M A R Y

CLOCK AND I/O PCB ASSEMBLY

3913 446 75410

(Versions 1 and 2)

References	Brief Description of Change	Documents Affected
PGV 3959 06.07.90	Mounting hole for A28 Regulator incorrectly aligned, causing short circuit between 0V and 5V planes. Metallic fixings replaced with nylon ones. PCB layers being realigned.	Assembly Drawing
PGV 4053 16.07.90	C61, 330nF, 2012 310 00322 changed to 330nF, 2012 310 03124.	Parts List

CLOCK AND I/O PCB ASSEMBLY

3913 446 75410

VERSION 1 - CODER

1. GENERAL DESCRIPTION

The primary functions of this module are:

- (a) To provide timing signals for coding, either free-running or locked to an appropriate reference.
- (b) To select data and clock signals for routing between other modules and the rear panel, and for locking of the internal timing reference oscillator and counter.
- (c) To provide digitally generated test tone data as an alternative to programme sound.

2. FUNCTIONAL DESCRIPTION

2.1 Master Oscillator

A5 is a 5824kHz oscillator on which depends the accuracy of the frequency of the 728 kbit/s bitstream generated by the Coder. Its frequency is controlled by the direct voltage applied to Pin 4. Its free-running frequency, which is set by R14, has a stability within ± 0.5 ppm over the temperature range, and with time should vary by less than 0.5 ppm per year (less in later years).

The oscillator output is buffered by A11 and divided by 2 to 2912kHz by A12A; this frequency is used to clock the counter chain A15, A16, A17. The counter outputs address the EPROM A18, which, at a count of 2910, outputs a pulse (delayed by one clock period by the latch A19) to reset A15, A16 and A17 from a count of 2911 to 0 so that they repeat a 1ms count sequence. The same pulse also clocks the 16-frame counter A20.

Other outputs of A18 provide timing reference signals to the DSP module in the Coder, digital test tones and also timing strobes to the rear panel, which indicate when the Application Control bits and Additional Data are read.

2.2 Signal Selection and Routing

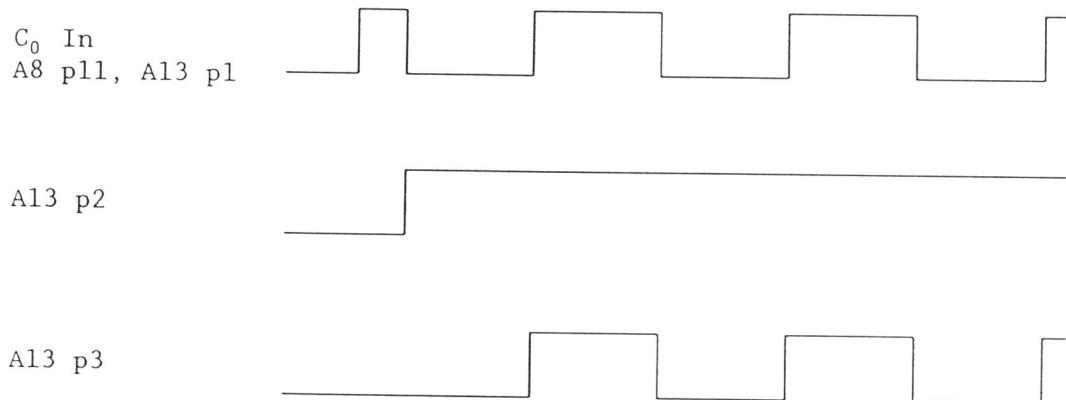
The normal signal routing through the module is data in from the DSP and out to the Asynchronous Data Processor (for subsequent insertion into the video signal's sync pulses). The Clock and I/O module also supplies clock for the DSP module and for the Asynchronous Data Processor, and other synchronous timing signals for the DSP module.

Alternatively, External Data and Clock applied via the Auxiliary Input on the rear panel to A1A inputs can be routed to the Asynchronous Data Processor, or one of the tones generated in A18 or A27 can be selected. Signal selection is made by the lower three switches of S1, or by remote control lines A2 and A3, provided the top switch of S1 is set to Remote. X18 enables Tone 2 to be selected from one of two tones in A18 or eight tones in A27. Auxiliary Output 1 gives rear panel access to data from the DSP and synchronous clock and C_0 from the Clock and I/O module. (C_0 is the Application Control bit which is low for 8 frames and high for 8 frames, thus defining a 16-frame sequence; at this output it goes high as the first bit of frame 1 is output, and low as the first bit of frame 8 is output). Auxiliary Output 2 gives rear panel access to whatever signal (and clock) is being sent to the Asynchronous Data Processor. C_0 is not available from Auxiliary Output 2 as the only source of it is from the internal clock and counter, which may not be synchronised to the External clock and data even when these are the selected signal source.

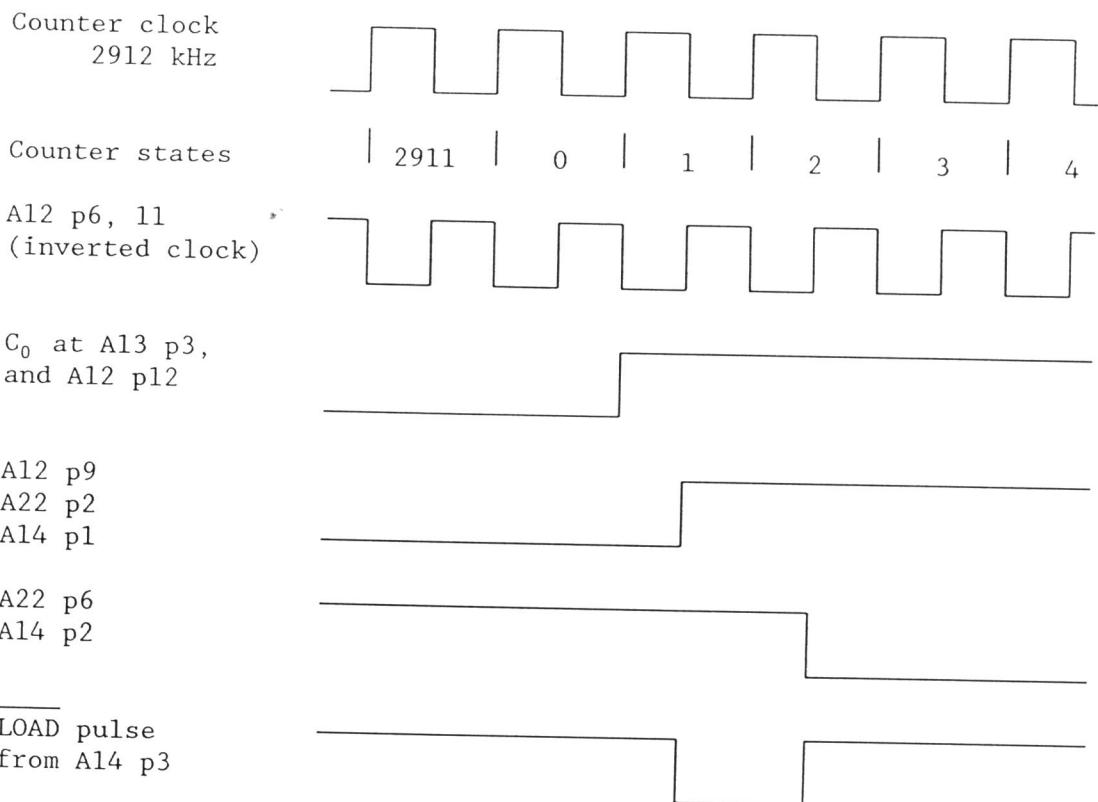
2.3 Locking and Synchronisation

The Auxiliary Input includes two clock inputs: one to go with the External Data input, and one to go with a C_0 input. These two clocks may be synchronous or asynchronous. Under the control of the top three switches of S1 and remote control lines A0 and A1, the internal oscillator may be free-running or synchronised to either of these clocks. Any clock selected for locking is routed through A6 (section Y) to the Signal In (SIN) pin of the Phase Locked Loop (PLL) controller A7. A7's output is routed through A9 (analogue demultiplexer) to the frequency control pin of the oscillator. PLL control filtering is provided by R13, R12, C55 and C56. R11 provides the right source impedance for the required frequency range of A5. The clock being used for locking is also fed to A8A which controls one section of A9, such that if the clock should fail, the output from A7 is prevented from reaching A5 before it can send the oscillator frequency to one end of its range.

For two coders to code audio in synchronism with each other, not only must their clocks be synchronous, but their frame sequences must also be synchronous. This is achieved by C_0 locking. C_0 may be input at the coder's Auxiliary input, with related clock, and used to synchronise the 16-frame sequence of the counter chain. Its rising edge will then define the time of output of bit 1 of frame 1 of the audio bitstream. When selected by the switches S1 and/or remote control inputs, C_0 is routed through A6 (section X) to A8B and A13A. Their purpose is to prevent the C_0 locking system locking to the first edge of a newly applied C_0 input signal. The waveform diagram shows how it works.



The next set of waveforms, on a different scale, shows how the counter LOAD pulse is produced from the positive edge of the waveform at A13 pin 3.



This system produces a LOAD pulse one clock cycle wide which straddles the counter clock normally causing the counter state to change from 1 to 2. Therefore the pre-load value for the counter is 2, i.e. all pre-load pins (3,4,5 and 6) of A15, A16 and A17 are 0V except A15 Pin 4, requiring Link X9 to be in Position 'C' (Coder). Because the clock frequency (2912 kHz) for the counter chain is four times the clock frequency (728 kHz) for the phase comparator, the two least significant preload pins of A15 are not connected directly to 0V or 5V, but to signals which ensure the two least significant bits of the counter chain are not affected by the preload operation; by this means the clock locking and C_0 locking do not interfere with each other. For A15, A16 and A17, the pre-load is synchronous, i.e. clocked. A20 however is pre-loaded asynchronously, the resulting address change on A18 and A27 always occurring a little after the data is latched into A19, due to the propagation delays of A12B, A14A and A20. The internal C_0 is derived from the QD output of A20 after it has been delayed by one clock cycle and inverted by the latch A22B. It is then in phase with the incoming C_0 shown in the waveforms above.

2.4 Nibble Reset

For two Coders to run fully synchronously, their Asynchronous Data Processors must divide the bitstream into groups of four bits (nibbles) in the same way. To enable this to happen there is a reset input which may be fed from the Clock and I/O board with a C_0 pulse. However, there is the possibility that the internally produced C_0 may not be synchronous with the data being sent to the Asynchronous Data Processor, and in this case the C_0 pulse must not be sent to the Asynchronous Data Processor. The following table shows the conditions under which the C_0 reset is sent from Pin 17a of the Clock and I/O connector. X16 is a link on the board which the user can set according to whether the External Data and Clock are synchronous with the External Clock and C_0 .

C_0 to Asynchronous Data Processor.

Lock Condition	X16	Signal Source		
		Int	Ext	Tones
Free	A	Yes		Yes
	S	Yes		Yes
Ext Clock	A	Yes	Yes	Yes
	S	Yes	Yes	Yes
Ext C_0 and Clock	A	Yes		Yes
	S	Yes	Yes	Yes

2.5 Signal Selection and Synchronisation

Switches on the front of the module provide local control of signal selection and synchronisation mode. Their functions are indicated on the circuit diagram and on the inside of the front panel of the equipment. When the top switch is set for 'Remote' then the input lines A3, A2, A1, and A0 become effective for controlling these selections remotely. They may be 5V logic, or pull-downs to indicate a zero and open circuit to indicate a 1. The presence of External input signals is monitored by retriggerable monostable ICs (A2 and A3). The lack of any such signals is indicated by LEDs H1-H4, and fed to A4. A4 also receives the logic signals from the remote control inputs and the local control switches, and controls other ICs involved in synchronisation and signal selection. It also provides a Signal Fail indication if any requested signal selection or synchronisation mode depends upon a signal which is not present (see below).

2.5.1 Locking and Remote/Local

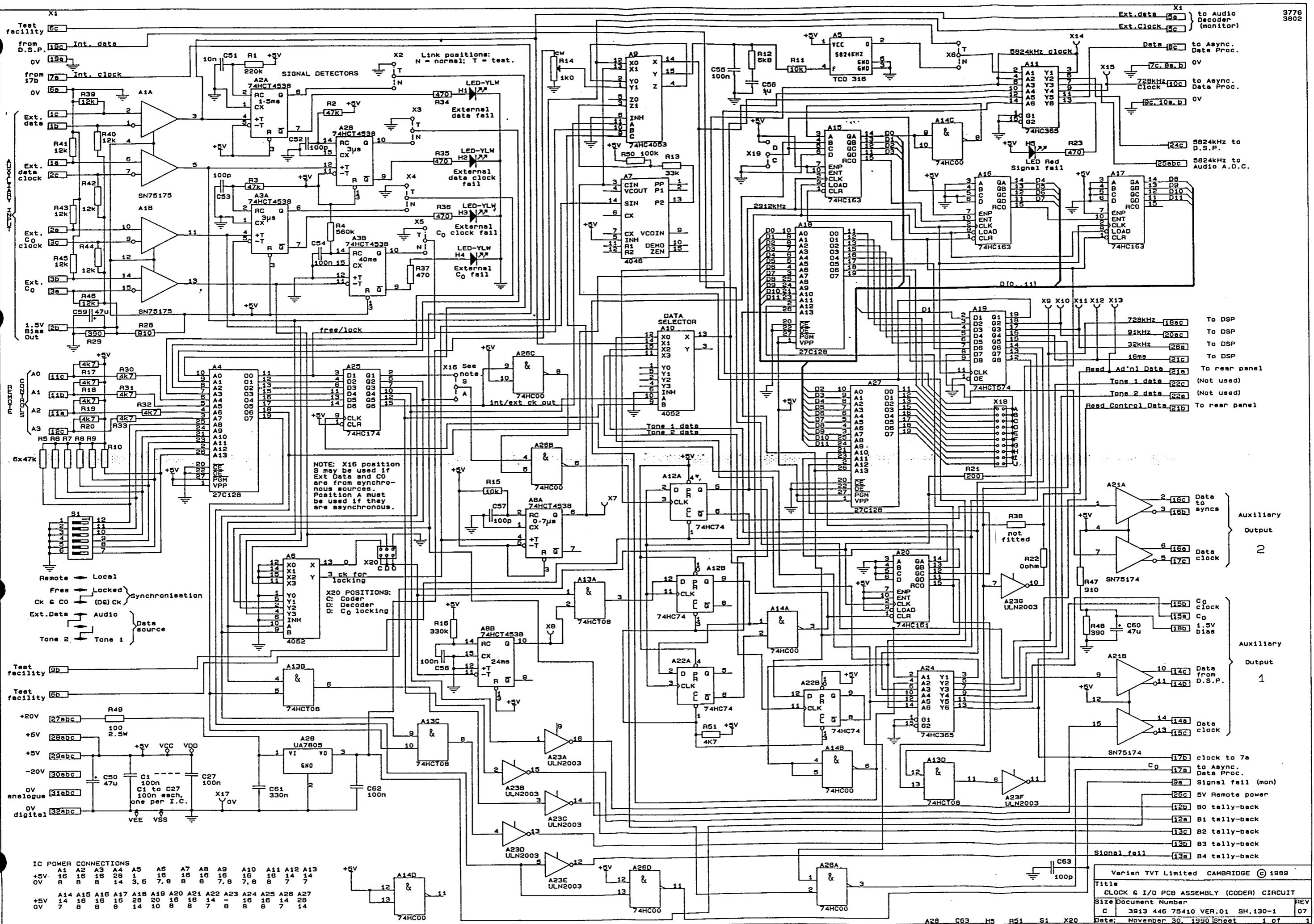
A3	A2	
1	1	Local control (overrides 'Remote' selected locally).
1	0	Free-running.
0	1	Locked to External Data Clock. If it fails, falls back to free-running; Signal Fail indicated.
0	0	Locked to Ext. C_0 clock and C_0 . If either fails, falls back to free-running; Signal Fail indicated.

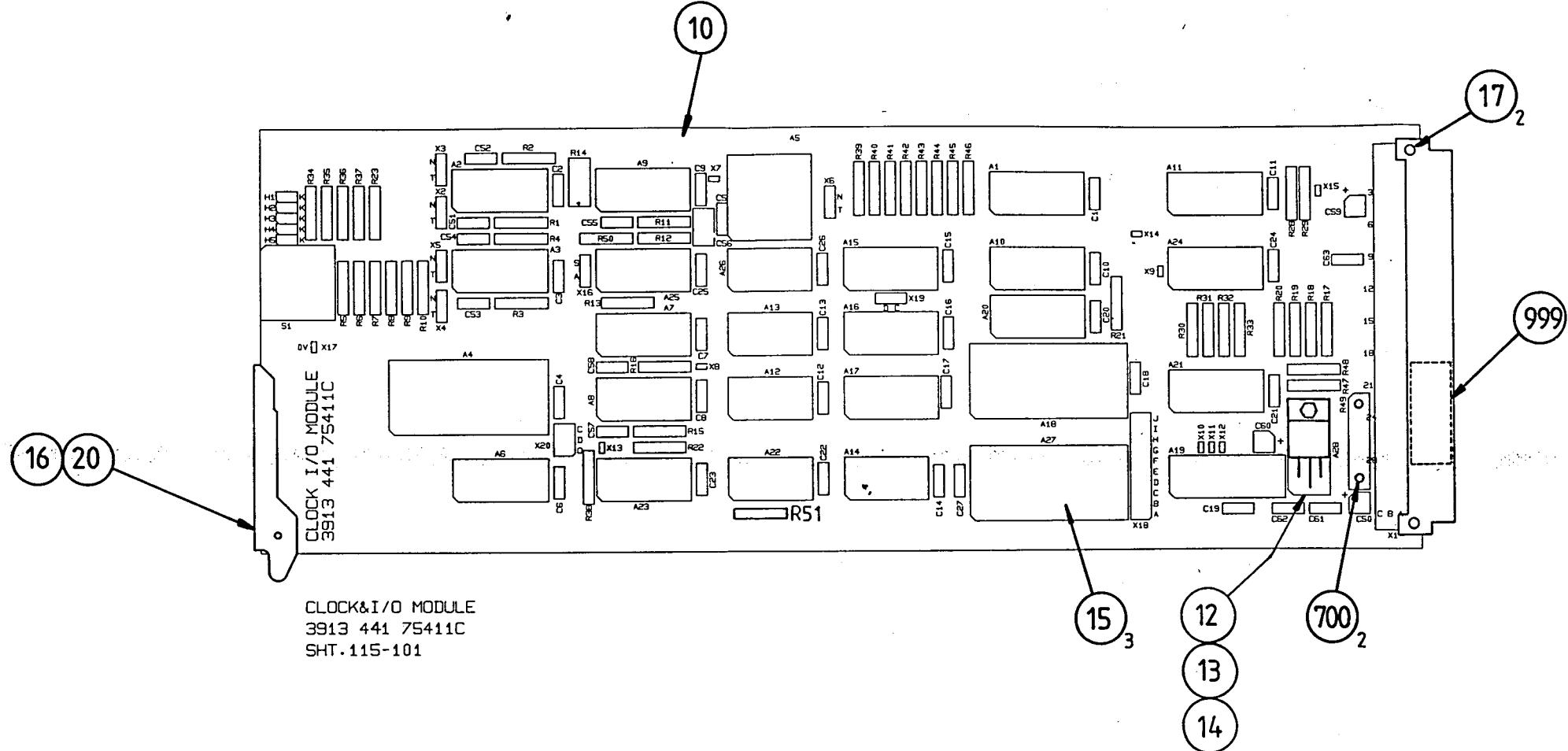
2.5.2 Signal Selection to Asynchronous
Data Processor For Insertion in Sync Pulses

A1	A0	
1	1	Bitstream generated from analogue audio inputs.
1	0	External Data and Clock. If data fails, falls back to Tone 2; Signal Fail indicated. If Clock fails, use internal clock; Signal Fail indicated.
0	1	Tone 1.
0	0	Tone 2.

2.6 Tally-backs

B0 to B3 tally-backs follow the coding of A0 to A3, indicating fall-back conditions due to signal failure when relevant, rather than requested conditions. If Local Control is selected, either locally or remotely, B3 and B2 are 1, to indicate 'Local' and they do not indicate the lock condition selected. B4 is a remote Signal Fail indication. H5 is the on-board Signal Fail indicator.





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DIMENSIONS		ANGLES	HOLES	
UNITS	SCALE	ORIG.DRG.	MATERIAL	
MM	1:1			
PROJECTION		TREATMENT		
 1ST		SEE SEPARATE PARTS LIST		
3RD				
ASSEMBLY NO. QUANT.				
SEE 3913 982 90010 CODE C				
CLOCK & I/O MODULE ASSY DRG		3913 446 7541		
SUPERSEDED		1 SA.	SA. 110-1	-D
DRAWN		MECH.CHR.	ELECT.CHR.	APPROVED
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AUDIO DECODER

3913 446 75440

VERSION 2 - AUDIO MONITORING

Contents

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2. FUNCTIONAL DESCRIPTION	Sh. 595-2
3. SETTING-UP PROCEDURE	Sh. 595-4
3.1 General	Sh. 595-4
3.2 Procedure	Sh. 595-4

ILLUSTRATIONS

Circuit Diagram	Sh. 130-1
Assembly Drawing	Sh. 110-1

PARTS LISTS

C H A N G E S U M M A R Y

AUDIO DECODER

3913 446 75440

(Version 2)

References	Brief Description of Change	Documents Affected
PGV 3739 89.09.22	R13 and R51, potentiometers, 10k, 2113 391 00577 added.	Circuit Diagram Assembly Drawing Parts List
PGV 3749 89.09.28	R73, 39R, 2.5W, 2113 256 02292 added between the output of A2 and the input of A30.	Circuit Diagram Assembly Drawing Parts List
PGV 3799 89.11.16	Parts List up-dated. On the circuit diagram R73, 39R re-numbered R74. C11 changed from 10μ to 47μ F. A30, 5V regulator, changed from 9332 110 51742 to 7805, 3913 935 00001. Potentiometers R13 and R51 deleted. Socket DIL, 24-way x 0.6 deleted. Minor mechanical changes.	Circuit Diagram Parts List
PGV 4222 12.11.90	R72, 3k9, 2322 156 13902 changed to 5k1, 2322 156 15102 and made adjustable on test. Two solder tags, 2413 015 14168 added.	Circuit Diagram Assembly Drawing Parts List Text

3913 446 75440
(Version 2)

AUDIO DECODER

3913 446 75440

VERSION 2 - AUDIO MONITORING

1. GENERAL DESCRIPTION

The input to the decoder board is made via a dual one-of-four data selector which is controllable externally. Audio output from the board is in the form of balanced 600-ohm lines plus a headphone socket. The output from the decoder chip is in an I²S bus format. This is fed to a digital filter chip which also performs four-fold oversampling and error interpolation on the signal.

The output from the digital filter is then fed to the DAC still in the I²S bus format. De-emphasis and the remaining filtering of the audio signal are performed in a multiple operational amplifier (A22) which also provides a headphone output. A pair of low-noise dual operational amplifiers is then used to provide a balanced, though not isolated, line output signal to the outside world.

2. FUNCTIONAL DESCRIPTION

NICAM 728 clock and data are brought into the board via A29 which is a dual one-of-four data selector; the two control lines are normally held high but can be controlled via the remote control socket.

The selected clock and data are then fed to the decoder chip via a buffer (A6). Reconstituted 728kHz clock and 8.192MHz clock are produced from two phase-locked crystal-controlled oscillators of 5.824MHz and 16.384MHz respectively.

If the incoming signal has more than 1 in 100 parity errors and the MUTEEN pin is low then the decoder chip will provide a mute signal which is fed to the digital filter chip A3. When the MUTEEN pin is taken high this mute is disabled allowing signals with fewer than 1 in 100 errors to be output.

A low on C4EN will provide a mute signal if control bit C4 is low, indicating that the FM transmission and the stereo signal are different. A high on C4EN will unmute the decoder allowing test transmissions to proceed.

Output from the decoder chip to the digital filter chip is in I²S bus format. This I²S bus is also buffered in A6 and fed to the edge connector this is so that a good isolated and balanced output can be obtained from another board. Error LEDs H1 (MUTE) and H2 (PARITY) are also fed from this point, with the feed to H2 being via V5, R65, R66 and C42 which stretches the parity pulse so that it is long enough to be seen.

Remote control of the mute feed into the digital filter is achieved via the AND gate made up of A27C, A26C and the control links MUTESEL and LOC/REM.

The digital filter chip digitally filters the audio signal and provides an effective four-fold oversampled output to the DAC A5. If an erroneous signal is sent to the digital filter chip it will interpolate between the last good signal and the next good signal to provide a click-free signal to the DAC. In the event of a mute error the digital filter will step down to zero using a raised cosine function in 32 steps.

Still in the I²S bus format the signal is then passed to the dual 16-bit DAC. Biasing of the outputs on the DAC is performed partly by its own internal biasing and partly by R7, R8, R9 and C18. DC blocking is provided by C37 and C38, while R6 and R10 provide bias for the first operational amplifier in A22.

The various operational amplifiers in A22 are used to provide the de-emphasis and anti-aliasing filtering for the audio signal. A22 also provides the headphone feed and a feed to a pair of low-noise operational amplifiers, A23, A24. These operational amplifiers are arranged to produce a balanced 600-ohm line signal which is fed to the rear connector. Both the headphone and the line output levels are adjustable independently of each other.

Due to the method by which the decoder chip generates its mute there is a

delay during which time a lot of erroneous signals can be produced. In order to prevent this breaking through an additional mute signal is produced by D3, D4, R67, R68, R69 and C43. This signal is fed through a buffer in A7 to the mute pin of A22 which, with C14, normally provides a mute at switch-on.

3. SETTING-UP PROCEDURE

3.1 General

This procedure assumes an untested and brand new board.

Test equipment required:

Voltmeter, e.g. Fluke or AVO.

20MHz bandwidth oscilloscope.

x10 oscilloscope probes.

Accurate NICAM 728 clock and data generator with presetable Control, Additional and Nordic data bits.

Power supplies:

+20V and -20V at 500mA

+5V at 1A, i.e. Coder or Decoder Rack Frame Assembly and extender card.

Audio distortion/noise meter.

3.2 Procedure

(1) Set the links to the following positions:

X3 Low
X4 High
X15 High
X16 Local
X17 Low
X18 High.

(2) Connect all the power supplies and check that the following voltages exist between OV (X12) and the following points:

A4 Pin 1 or Pin 21 +5V
A22 Pin 26 -12V
A22 Pin 28 +12V
A22 Pin 1 +5V.

All the above voltages should be within 5%.

(3) Check that Pins 2 and 14 of A29 are held high; if not and

you are using a Coder or Decoder Rack Frame, check the input select on the Clock and I/O module.

- (4) Connect NICAM 728 data to X1 Pin 12a and NICAM 728 clock to X1 Pin 12c. Set the NICAM generator to stereo silence with all control, additional and Nordic data bits off. Check that the voltage between A5 Pin 6 and OV (X12) and A5 Pin 5 and OV (X12) is +2.5V +0.5V, -0.3V. If not select a value for R72 to achieve this.
- (5) Using the oscilloscope and a x10 probe look on Pin 7 of A29 and check that NICAM 728 data is present. NICAM 728 clock should be present on Pin 9 of A29.
- (6) Connect the oscilloscope probe to X5 and adjust C31 for a stable even mark/space square wave. Check on X6 for a 5.824MHz square wave of approximately 5V p-p.
- (7) When this condition is obtained repeat (6) for X7 and X8 but at a frequency of 16.384MHz, using C35.
- (8) Check on Pin 40 of A4 for a clock signal of 8.192MHz.
- (9) Compare the waveforms present on Pins 3, 4 and 33 of A4 to those in Figure 1 and ensure that they are the same. The same signals should also appear on Pins 2, 1 and 3 of A5.

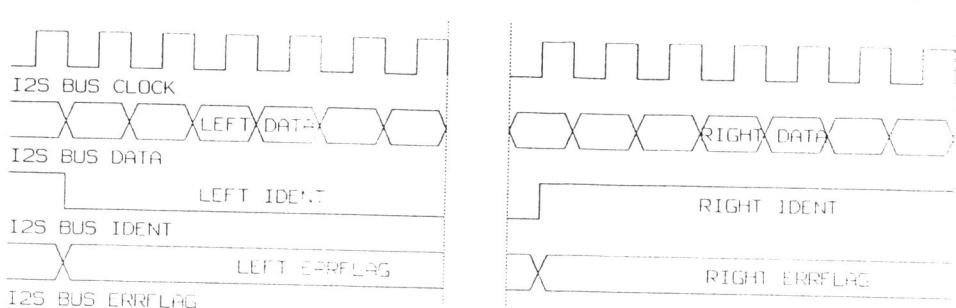
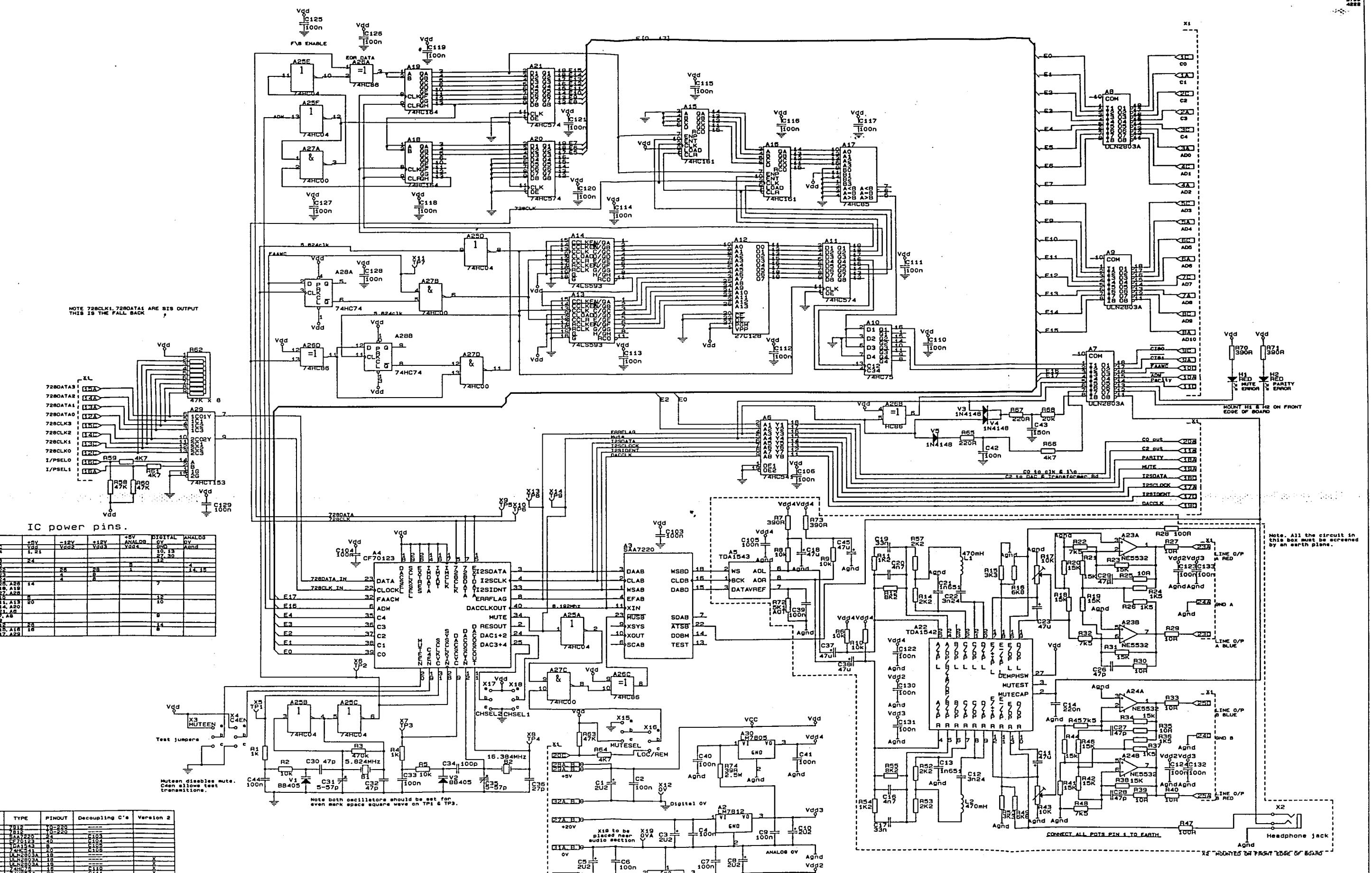


Figure 1 - I²S Bus Waveforms

- (10) Connect a 600-ohm audio level and distortion measurement set to X1 Pins 23a and 23c (Channel A) and set the NICAM generator for 14.7dBu at 2kHz. Adjust R17 for 14.7dBu on the output.
- (11) Move the audio test measurement set to X1 Pins 25c and 25a and repeat (10) for Channel B using R43 to adjust the level.

- (12) Check that the distortion, frequency response, crosstalk and noise meet specification on both channels.
- (13) Insert a pair of 600-ohm headphones into the jack socket X2. Using tones and/or program, check that the signal is clean and that there are no spurious noises.
- (14) Muting: Set C3 on the NICAM generator to on; H1 (MUTE) LED should come on and all audio outputs should be muted. Set X3 to high; the mute LED should go out and the audio output should be distorted. Set X3 and X4 to low, and C3 to 0 on the NICAM generator; the output should be muted and H1 will be on. Turn on C4 on the NICAM generator; H1 should be extinguished and the audio should be clear and unmuted. Set X4 to high and C4 on the NICAM generator to OFF. Set X16 to REMOTE and check that short-circuiting X1 Pin 20c to 0V causes the audio to be muted and the MUTE LED H1 to come on.
- (15) Restore all links and control bits to their initial conditions.

The unit is now ready to be used.

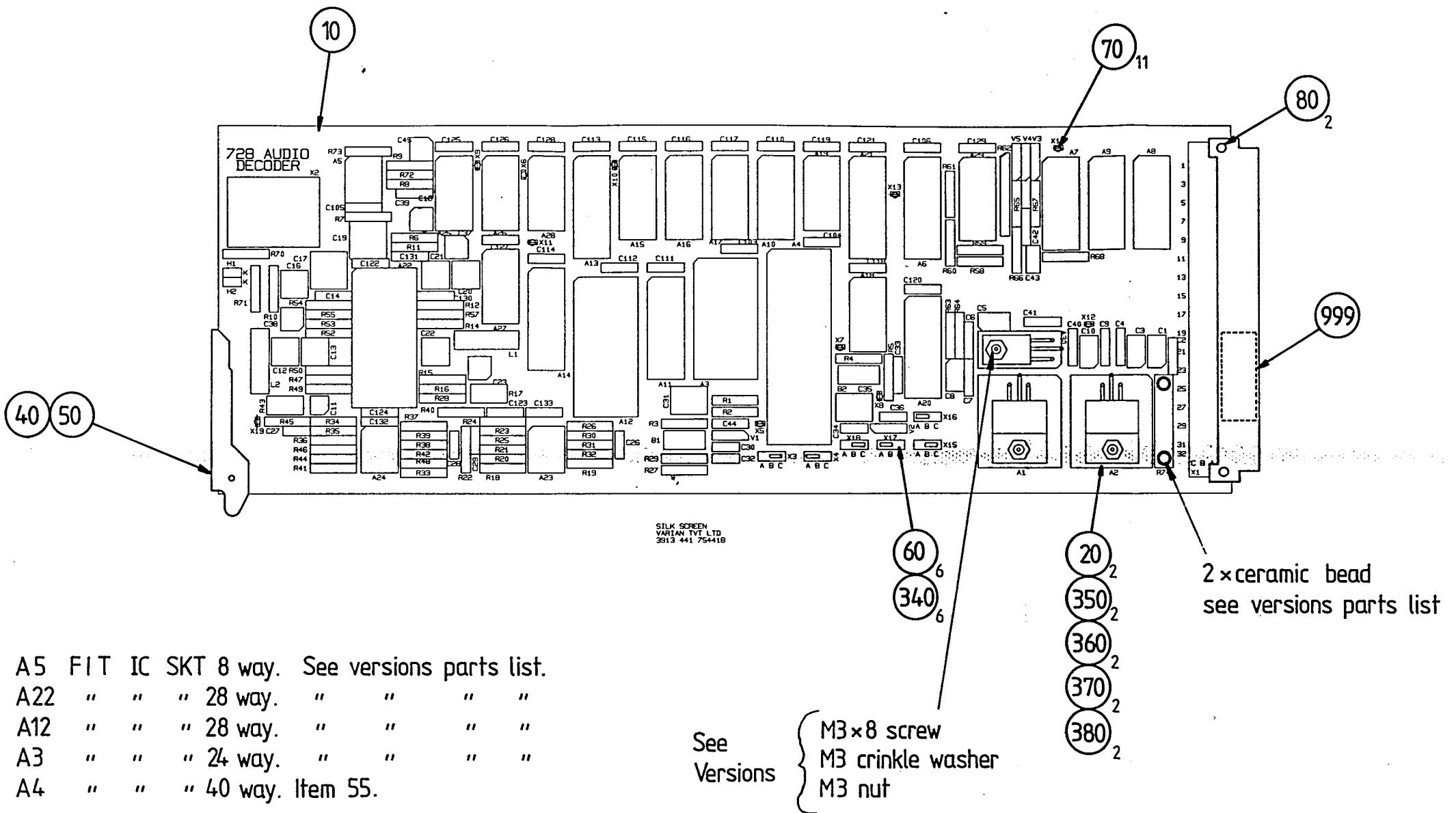


IC No	Type	Pinout	Decoupling C's	Version 2
A2	74LS22	10-220		
A3	SAA7220	24	C103	
A5	74HC04	20		
A5	74LS14	20	C105	
A6	74HC541	20	C108	
A7	LM2803A	18		
A8	LM2803A	18		
A9	LM2803A	18		
A10	74HC04	20	C110	X
A11	74HC574	20	C111	X
A12	74LS552	20	C113	X
A14	74LS523	20	C114	
A15	74LS523	18	C116	
A16	74HC04	18	C117	
A17	74HC04	18	C118	
A18	74HC04	14	C119	
A19	74HC04	14	C120	
A20	74HC04	20	C120	
A22	74LS152	28	C121, 130, 131	
A23	NE5532	8	C123, 132	
A24	NE5532	8	C124, 133	
A25	74HC04	14	C125	
A26	74HC04	14	C126	
A27	74HC04	14	C127	
A28	74HC04	14	C128	
A29	74HC04	14	C129	X

NOTE All components are fitted for version 1
x = where decoupling capacitors marked with
x are not fitted for version 2.

VERSION 01 AS SHOWN.
VERSION 02 SEE TABLE FOR COMPONENTS NOT FITTED.

Varian TTV Limited CAMBRIDGE © 1989
Title: AUDIO DECODER PCB ASSEMBLY CIRCUIT
Size/Document Number D 3913 446 75440 SH.130-1 REV 03
Date: November 13, 1989 Sheet 1 of 1



DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING			
TOL. UNLESS OTHERWISE STATED		SURFACE TEXTURE		1ST USED ON	
DIMENSIONS	ANGLES	HOLEs			
UNITS MM	SCALE 1:1	PROJECTION	SEE SEPARATE PARTS LIST. SEE 3913 982 90010 CODE C		
ORIG. DRG.		1ST 3RD	ASSEMBLY NO. QANT.		
TITLE: AUDIO DECODER 728 PCB ASSY DRG					
SUPERSEDES 3913 446 7544					
DRAWN TECH. DRW. ELECT. DRW. APPROVED					
VARIAN T.V.T. LTD CAMBRIDGE (c) 1989 DATE DRAWN 12-10-89 FORM					

MONITOR 13913 446 69880Contents

CHANGE SUMMARY	Sh. 508-1
1. GENERAL DESCRIPTION	Sh. 595-1
2. FUNCTIONAL DESCRIPTION	Sh. 595-1
2.1 CPU and Memory	Sh. 595-1
2.2 Fault Inputs	Sh. 595-1
2.3 Fault Outputs	Sh. 595-2
2.4 Input/Output Ports	Sh. 595-2
2.5 Power Supplies	Sh. 595-2

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Circuit Diagram	Sh. 130-1 and 2
PCB Assembly Drawing ..	3913 446 74930
	Sh. 110-1

PARTS LISTS

C H A N G E S U M M A R Y

MONITOR 1

3913 446 69880

References	Brief Description of Change	Documents Affected
CA 35542 30.01.90	3913 036 55420 should be described as a PAL not an EPROM (A26, 27, 28).	Parts List

MONITOR 13913 446 698801. GENERAL DESCRIPTION

The Monitor 1 module is a Z80-based processor system which, under the control of its software, monitors the fault outputs from the other modules in a Stereo Sound in Sync coder or decoder and declares faults when appropriate. For more information on the actual monitoring process, refer to the section on Monitoring in the associated system handbook (see Information Finder).

2. FUNCTIONAL DESCRIPTION2.1 CPU and Memory

The Z80 CPU, A5, runs at a clock rate of 4MHz. This is produced by the 8MHz oscillator around B1/V1, the D-type flip-flop A2a used as a divide-by-2, and the active pull-up, V2, which ensures fast rise and fall times for the clock edges. 32K of ROM and 16K of RAM are provided for the system. 16K of ROM, A6, contains a BBC BASIC interpreter, and a further 16K of ROM, A7, contains the software. On switching on, the contents of A7 are loaded into A8 and A9, two 8K RAMs, and the software is run from the RAM. By fitting R24 instead of R25, a 32K ROM may be fitted for A6. Memory decoding is provided by A3, A10a and parts of A11 and A16. A real-time clock facility is provided by the CTC device, A25.

2.2 Fault Inputs

24 fault input lines are provided, not all of which are used. These are taken to A26, A27 and A28, programmable logic devices programmed as octal R/S flip-flops, which are set by the fault input going active. The outputs of the flip-flops appear as three read-only ports at address 00, 20 and 40 Hex. The flip-flops assigned to each port are reset by the program reading from that port.

2.3 Fault Outputs

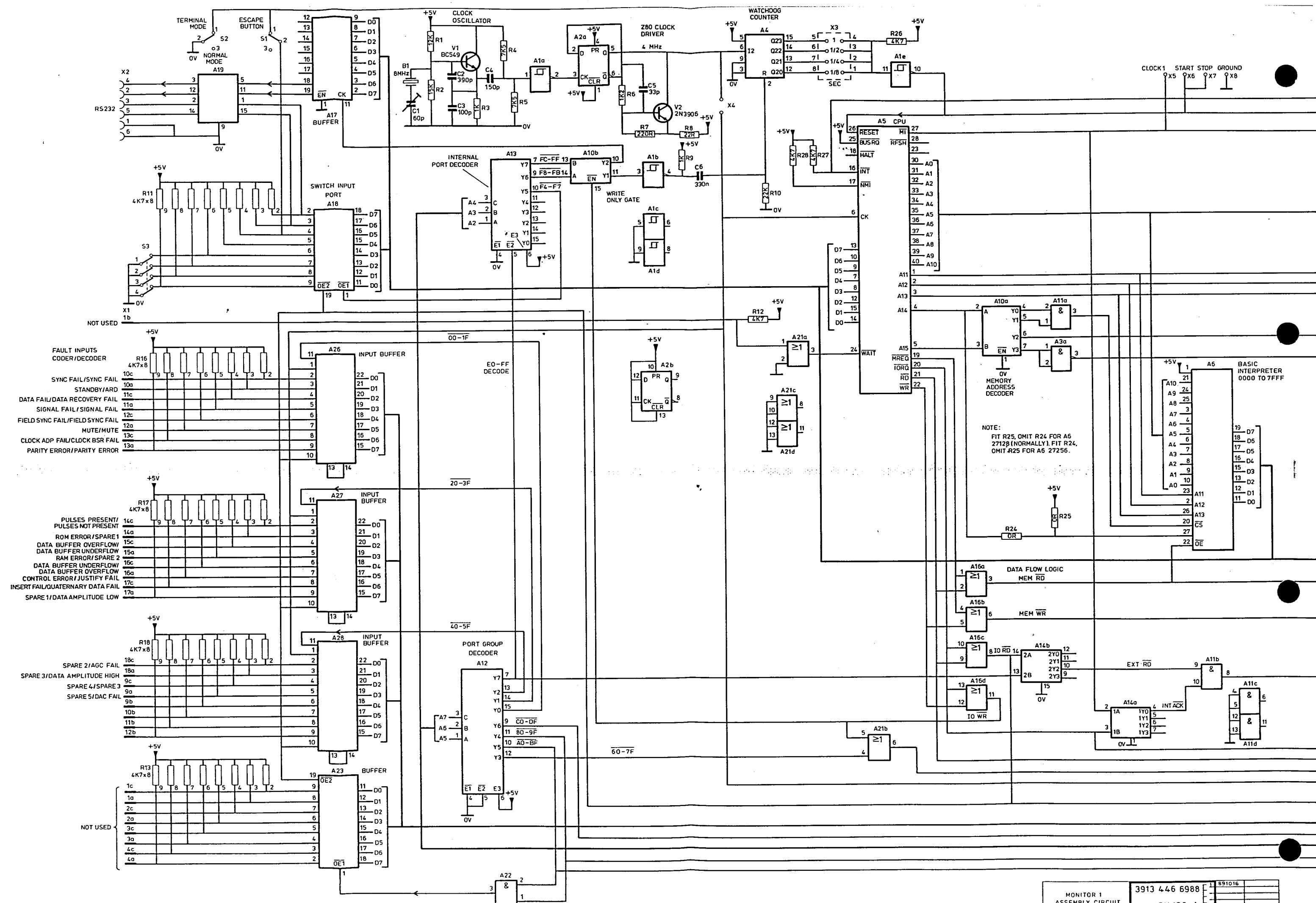
A main fault output (Green LED H1 and relay K1, driven by V4), and a secondary fault output (relay K2, driven by V5) are provided along with six open-collector outputs, A30, mimicked by red LEDs H2 to H8. All the fault outputs, except the main, are latched by A29, which also provides sufficient sink current to drive H2 to H8. The main fault output is driven from a monostable which has to be regularly triggered by the program to keep the output in the 'system good' state. This is so that, if the program crashes, the monitor will declare a fault. The main and secondary fault outputs and the open-collector outputs are driven from a write-only port at 60 Hex. The open-collector outputs are provided with an associated return path to OV.

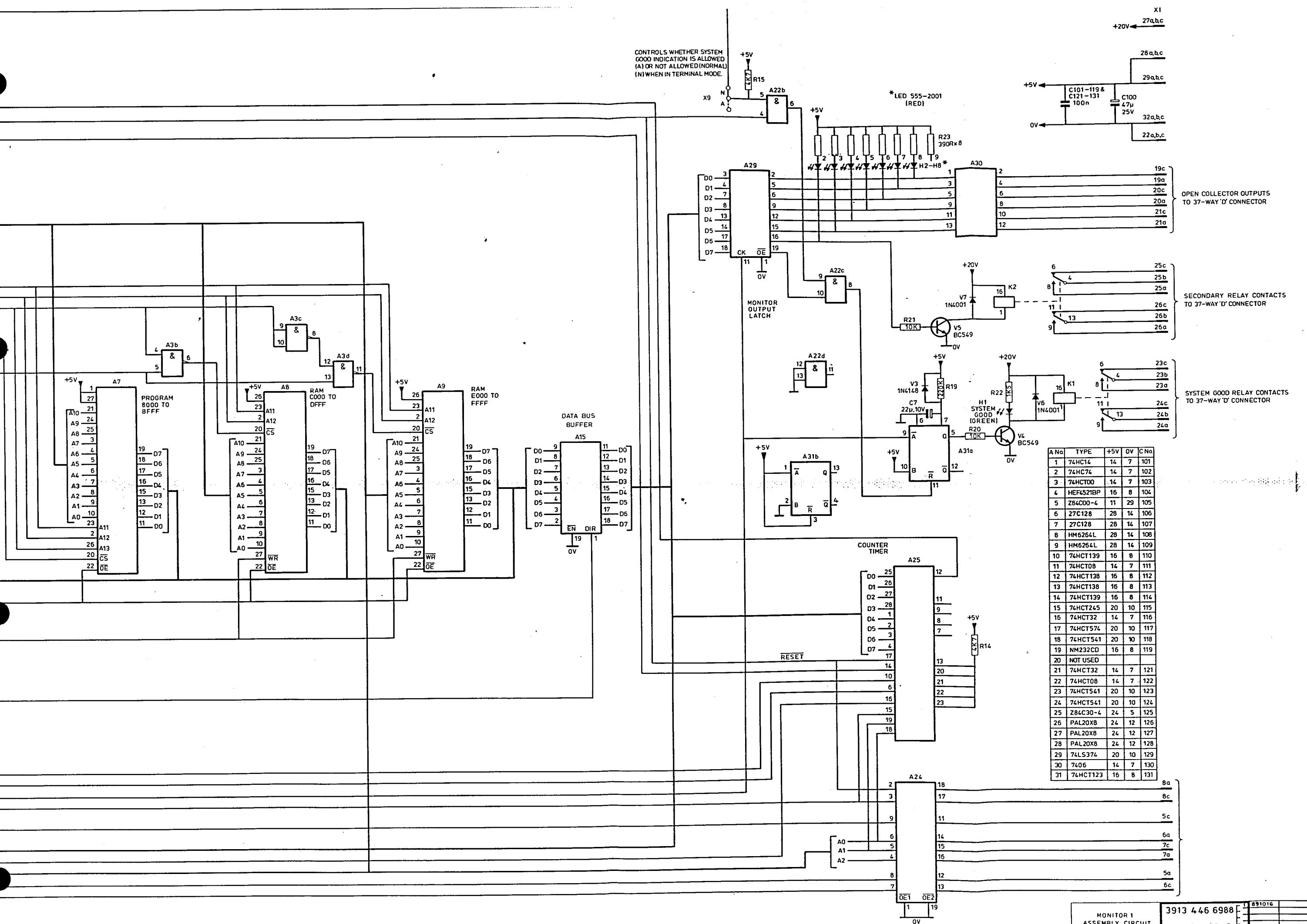
2.4 Input/Output Ports

A18 acts as an input port onto the data bus, buffering S3 and two RS232 input lines. S3 is set to indicate to the software the circumstances in which the card is working: as coder or decoder, with or without audio modules, and with or without audio comparison (Decoder only). A17 provides an output port for two RS232 output lines. The two RS232 ports are taken to X2 on the front of the module via A19, an RS232 driver. One is used for interactive control or modification of the software via a terminal; the other for loading a program from a microcomputer or sending a program from RAM to a PROM Programmer. For information on connections and data formats, refer to the Monitoring section in the associated system handbook. A TERMINAL ENABLE switch and ESCAPE button, S2 and S1, are provided for use with these facilities. A24 provides an 8-bit output bus, though this is not used. Port decoding and READ and WRITE signals are produced by A12, A13 and parts of A16, with A14 and A11b controlling the direction of the bi-directional data bus buffer, A15.

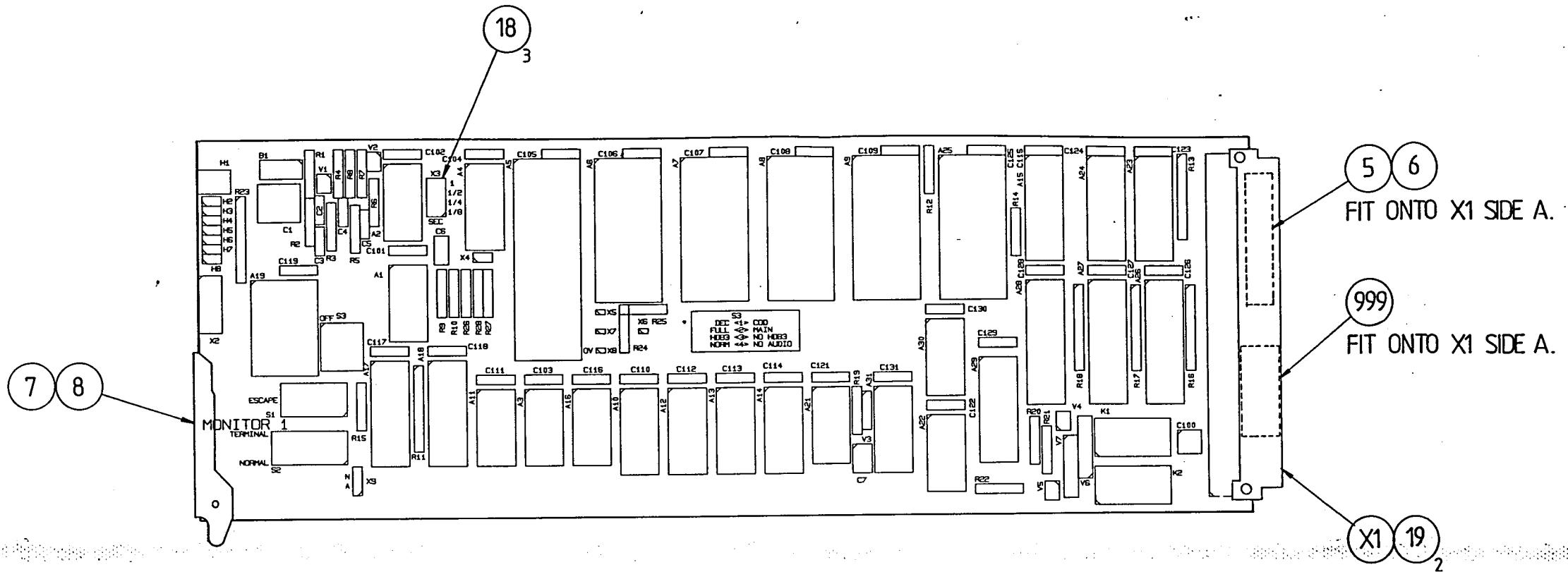
2.5 Power Supplies

+5V for the majority of the circuitry is obtained from the main rack power supply. The SYSTEM GOOD LED, H1 and the relays K1 and K2 are powered from the +20V supply in the rack, which is smoothed but not regulated. Hence, this may have up to 1V of ripple on it, but this does not affect the LED or relay operation.





MONITOR 1 ASSEMBLY CIRCUIT	3913 446 6988	1 891016
	2 SH	SH.130-2
DRAWN I.S LTD.	CHC.5 (Signature)	APPROVED
VARIAN TTV LTD, CAMBRIDGE	© 1989	DATE DRAWN 891016 FORM A1



FIT IC BASE ITEM 15 AT A6,A7,A8,A9,A25.

FIT IC BASE ITEM 16 AT A5.

FIT IC BASE ITEM 17 AT A26,A27,A28.

MOD. LEVEL STRIKE PLATE INSTRUCTIONS

1. AFFIX STRIKE PLATE No. 3913 081 66620, ISSUED WITH THIS ASSEMBLY, IN POSITION INDICATED.

2. STRIKE OFF NUMBERS ON PLATE TO LEVEL INDICATED IN THIS DETAIL.

THE STRIKE LEVEL SHOWN HERE MUST NOT BE CONFUSED WITH THE ISSUE DATES SHOWN ON ASSOCIATED DRAWINGS & PARTS LISTS.

STRIKE No.	P.G.V. No.
1	
2	3342
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9	
10	
11	
12	

DO NOT SCALE THIS PRINT				DIMENSIONS ARE SHOWN AFTER PLATING	
TOL UNLESS OTHERWISE STATED			SURFACE TEXTURE	1st USED ON	
DIMENSIONS		ANGLES	HOLDS		
UNITS	SCALE	ORIG.DRG.	MATERIAL		
MM	1-1				
SEE SEPARATE PARTS LIST.					
 1st 3rd		PROJECTION TREATMENT: SEE 3913 982 90010 CODE C.			
TITLE: MONITOR 1 PCB ASSY DRG.		3913 446 7493 15 870320 1C 87/11/13 PGV 3342			
SUPERSEDES DRAWN T.P.		1 SH	10	SH. 110-1	
MECH.CHRK. ELECT.CHRK.		APPROVED			
PYE T.V.T LIMITED CAMBRIDGE(TRANSMITTER DIV.) © 1987 DATE DRAWN 870320 FORM A 2					

CODER VIDEO PROCESSOR3913 446 69870Contents

CHANGE SUMMARY	Sh. 508-1
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Circuit Diagram ..	3913 446 69870
	3913 446 74800
	Sh. 130-1
Assembly Drawing ..	3913 446 74800
	Sh. 110-1
PARTS LIST	

C H A N G E S U M M A R YCODER VIDEO PROCESSOR3913 446 69870

References	Brief Description of Change	Documents Affected
PGV 3602 89.01.18	<u>On PCB Assembly 3913 446 74800:</u> Potentiometer R119, 2k2, 2111 369 00083 added between A5 Pins 8 and 5. C36 to C40 removed from base parts list and added to parts lists of appropriate versions. C64 added to the parts lists of the appropriate versions.	Circuit Diagram Assembly Drawing Parts Lists Text
PGV 3660 89.05.31 Issue 1. 89.10.11 Issue 2.	Diode V33, BAW62, 9331 012 20112 added, anode to OV and cathode to the junction of R43, R44 and C11.	Circuit Diagram Assembly Drawing Parts List
PGV 3766 89.10.16	R96 and R97, 74R1, changed from 2322 163 47419 to 2113 112 03105. C38 changed from 330pF to 510pF, 2013 400 03131. C46 re-designated C40 (Parts List error).	Parts List
PGV 3718 10.08.89	C65, L3 and R120 added in parallel, between R89/C31 and R87/V20 base to improve video frequency response. The following components added to parts list: C65, 1nF, 2013 400 03127; R120, 22R, 2322 156 12209; L3, 1.5 micro-H, 2413 535 00683.	Circuit Diagram Assembly Drawing Parts List

CODER VIDEO PROCESSOR

3913 446 69870

1. FUNCTIONAL DESCRIPTION

Video input to the module is via the differential input stage comprising A13 and its associated components, which provides a high degree of common-mode rejection for the incoming video signal. V31 provides a buffered output immediately after A13 to supply video to the Sync Separator module (3913 446 67350). V7 also buffers A13 output, for a monitoring point at the front of the board and for clamping, via the clamp capacitor C11. V8 clamps the bottom of sync to 0V, and is driven by A8, which produces a $1.9\mu s$ wide clamp pulse, triggered by the sync pulse to drive the gate of V8. Clamped video then passes through a cascode stage, A6, and an emitter follower, V30, which provides a low-impedance source for the Video Source Switch, A3. V29 provides V_{be} correction for V30.

A3 consists of four analogue switches, two being used for each video source and connected in a shunt-series configuration, i.e. the unused video source has one switch shorting the signal to ground, and the other switch open circuit to the video path. To provide as low an 'on' resistance as possible A3 is powered from +15V, and hence V26 and A10 are required to produce the necessary level translation of the standby control signal from the Asynchronous Data Processor (3913 446 67530), which is high for input video present.

In the event of a failure of the incoming video, regenerated line syncs are used as an alternative source of video. These are buffered into the module from the Asynchronous Data Processor by A5d, A5c and V11, with R119 providing timing adjustment in the stereo application, and passed through a 1.5MHz Gaussian filter Z1, which provides sync shaping. After clamping by V13, in the same way that V8 clamps the video, they pass through the cascode stage A9 into the other input of the video source switch. R57 provides a regenerated sync level control. Regenerated line syncs are normally generated by the Asynchronous Data Processor and locked to incoming video. In the event of a failure of video, however, their phasing is held, and they are used to carry quaternary data by being selected by the video source switch.

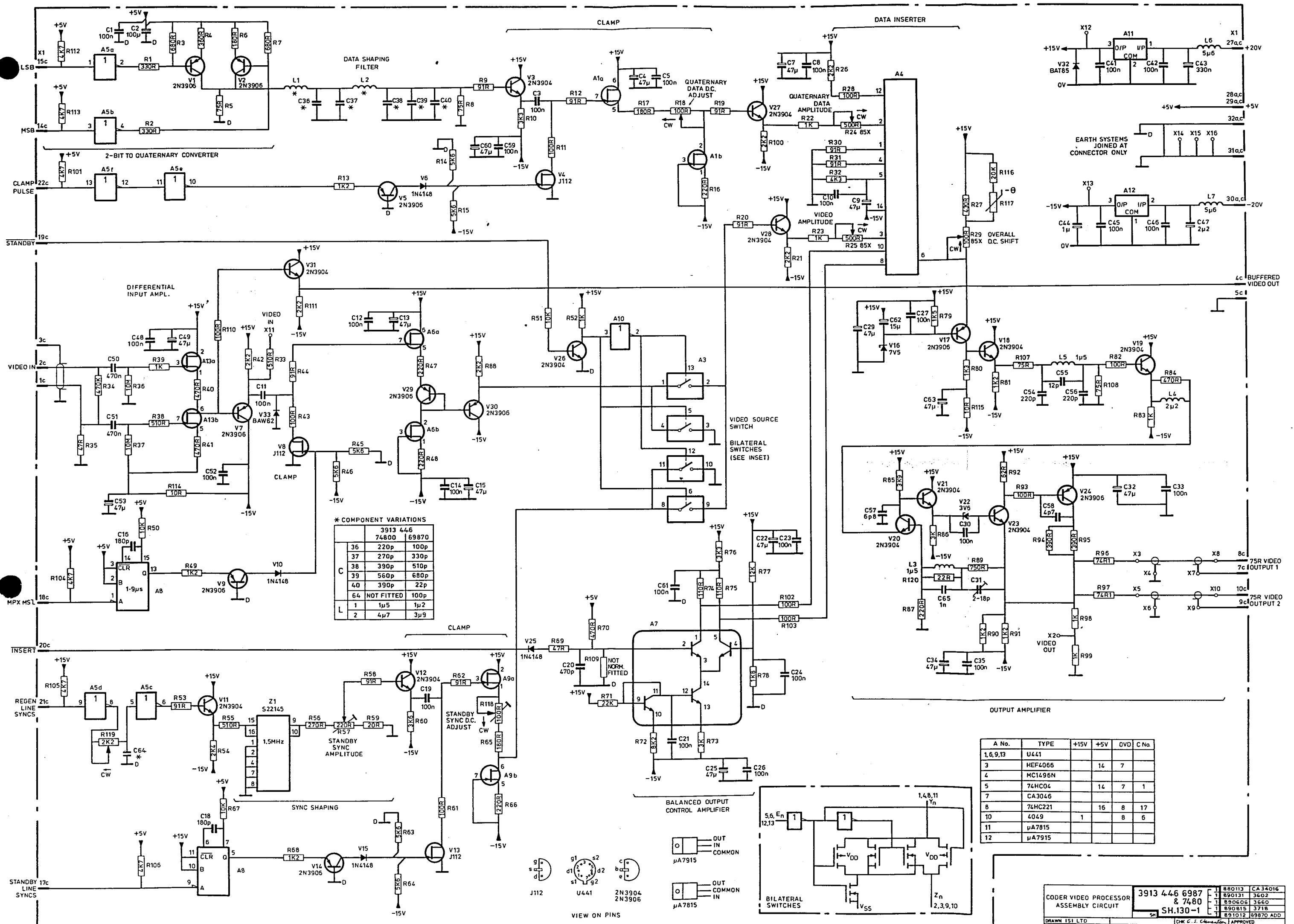
Two bits of data, LSB and MSB, are buffered into the module by A5a and A5b and combined to produce Quaternary Digits (Quits) by V1 and V2. V1 and V2 are each a current source, current being set in the correct proportion by R4 and R6 respectively, and these individual currents being summed into R5. This is followed by a data shaping filter, which band-limits the quits to 5.5MHz, and V3, which provides a low-impedance drive to the clamp capacitor C3. The clamp transistor V4 is driven by pulses

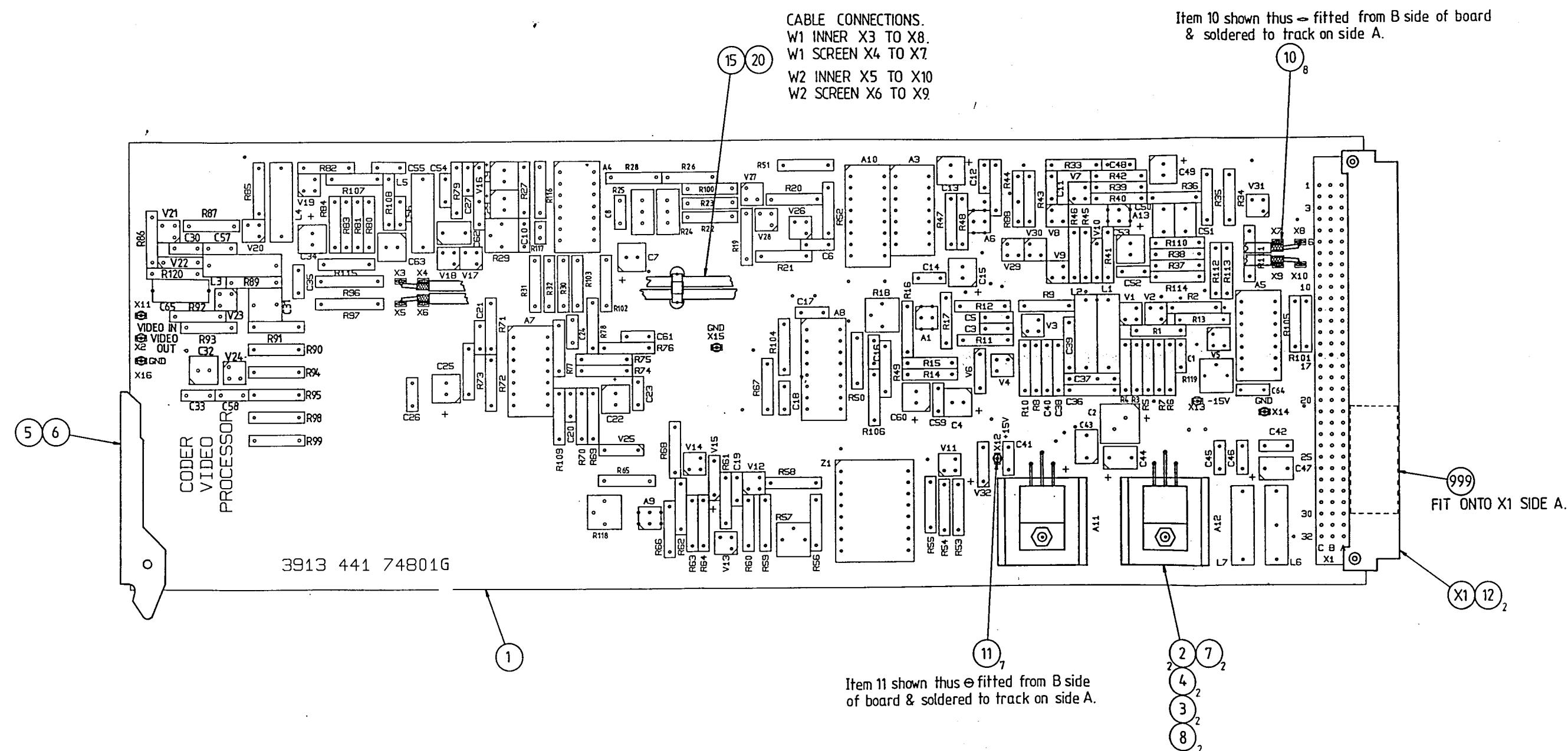
which are provided by the Asynchronous Data Processor, buffered by A5f and A5e, and level translated by V5 and V6. The quaternary data is clamped to 0V, i.e. bottom of sync level, by two clamp pulses, occurring immediately before and immediately following the quits. The cascode stage A1 incorporates a quaternary data DC control, to allow the bottom of the data to be accurately matched in DC level to the bottom of sync.

The quaternary data and the input video (having passed through A3) are fed into the balanced modulator A4 by V27 and V28 respectively, R24 and R25 providing data and video amplitude adjustments. The switching of A4 is controlled by an INSERT command from the Asynchronous Data Processor (low to insert data). A7 is connected as a long-tailed pair of transistors to give differential switching signals to switch A4, which inserts the quaternary data into the line sync pulses of the video. As the base of V17 is held at a constant voltage by V16, pin 6 of A4 is also at a constant voltage, and so a constant current flows through R27 and R29. This current is divided at A4 pin 6, part of the current flowing into A4 and the rest, representing the sound-in-sync signal, flowing down through V17 and developing a voltage across R80.

The (now sound-in-sync) video is driven into an 11MHz filter by V18, and then into the base of V19, which is the non-inverting input of the video amplifier. The complete amplifier consists of V19 to V24 and their associated components. V24 is a current booster for V23 to provide two 75-ohm outputs. The stage gain is fixed by R87 and R89 to give 1V p-p video outputs and the frequency response is set by C31. R89 and C31 form a negative feedback path to the inverting input of the amplifier.

Power to the digital sections of circuitry (+5V) is provided from the main rack power supply. +15V and -15V is provided from regulators A11 and A12, which are fed from +20V and -20V, smoothed but unregulated, once again from the rack power supply.





STRIKE NO	PCP
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8	
9	
10	
11	
LR	

NOTE: STRIKE PLATE INSTRUCTION
1. STRIKE PLATE NO. ONLY BE ISSUED WITH THIS
ASSEMBLY IN POSITION INDICATED
2. NUMBERS ON PLATE TO LEVEL INDICATED IN THIS
DRAWING & PARTS LIST
NOTE: THE STRIKE LEVEL SHOWN HERE MUST NOT BE CONFUSED
WITH THE STRIKE DATA SHOWN ON ASSOCIATED
DRAWINGS & PARTS LIST

DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING	
TOL UNLESS OTHERWISE STATED		SURFACE TEXTURE	NOT USED ON
DIMENSIONS		ANGLES	HOLDS
UNITS	SCALE	MATERIAL	
MM	1:100	OR C.D.	
PROJECTION		TREATMENT	
SEE 3913 982 90010 CODE C.			
SEE 3913 446 7480			
TITLE: CODER VIDEO PROCESSOR PCB ASSY		1 1/2" 10 S.H. 110-1	10 1/2" 03 07
SUPERSEDES		1 1/2" 01 10	10 1/2" 01 07
DRAWN DJF		MECH CDR	ELECT CDR
APPROVED		APPROVED	
PYE T.V.T LIMITED CAMBRIDGE (TRANSMITTER DIV.) © 1986 DATE DRAWN 86 09 12 FORM A			

3913 446 67530
3913 446 67550
3913 446 69750

ASYNCHRONOUS DATA PROCESSOR

3913 446 67530 (NICAM 625)
3913 446 67550 (NICAM-3, 525)
3913 446 69750 Version 1 (NICAM 728, 625)
3913 446 69750 Version 2 (NICAM 728, 525)

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2.2 Coder Data Insertion Controller (CDIC)	Sh. 595-2
2.3 Coder Sync Pulse Controller (CSPC)	Sh. 595-2
2.4 Coder Sync Lock Controller (CSLC)	Sh. 595-2
2.5 Phase-locked Loop	Sh. 595-2
2.6 Auto Reset	Sh. 595-3
2.7 Data Clock Monitor	Sh. 595-3
2.8 Fault Indications	Sh. 595-3
2.9 Power Supplies	Sh. 595-4

ILLUSTRATIONS

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PARTS LISTS

C H A N G E S U M M A R Y

ASYNCHRONOUS DATA PROCESSOR

3913 446 67530,
3913 446 67550, 3913 446 69750

References	Brief Description of Change	Documents Affected
PGV 3207 12.5.87	<p>On PCB 3913 446 74870:</p> <p>A25 Pins 9 and 10 disconnected from 0V; Pin 9 connected to A10a Pin 7.</p> <p>A10a Pin 6 disconnected from A6 Pin 19, A12 Pin 19 and A13 Pin 19; these connected to A15 Pin 8.</p> <p>A25 changed from 74HC00 to 74HC132. C49, 47µF; R50, 10k and V9, 1N4148 connected to A25 Pin 10.</p>	Circuit Diagram Parts List
PGV 3247 14.5.87	<p>On PCB 3913 446 74780:</p> <p>Connection between A14 Pin 7 and X1 Pin 18a deleted.</p> <p>Connection added between X1 Pin 18a and X1 Pin 16C.</p>	Circuit Diagram
PGV 3259 27.5.87	<p>On PCB 3913 446 74780:</p> <p>C50, 39p added between A22 Pins 3 and 5. C51, 100p added between A22 Pin 5 and 0V; on the circuit diagram. C51 reads '100p - NOT NORMALLY FITTED'.</p>	Parts List Circuit Diagram Assembly Drawing
PGV 3274 19.6.87	<p>On PCB 3913 446 74780:</p> <p>A9 to A11 changed from 3913 935 35009 to 9333 243 30602.</p>	Parts List Circuit Diagram
PGV 3346 30.11.87	<p>On PCB 3913 446 74780:</p> <p>A3 changed from 3913 036 60130 to 3913 036 60230. A6 changed from 3913 036 60140 to 3913 036 60240.</p>	Parts List Circuit Diagram
PGV 3592 13.01.89	<p>Parts List 3913 446 74780 discontinued and all items shown on it transferred to new parts list of the various versions, as applicable.</p> <p>New Parts List 3913 446 69750 created.</p> <p>Circuit diagram 3913 446 67530 now holds for versions 3913 446 67530, 67550 and 69750.</p> <p><u>Version 3913 446 67540 only:</u> New circuit diagram created.</p> <p>Changes of capacitor values detailed on PGV 3593.</p> <p>Connection added between A3 Pin 2 and X1 Pin 14C.</p> <p>Circuit level made to read "CO" (NICAM 728 only)</p> <p>Crystal frequency table removed from circuit diagram.</p>	Circuit Diagrams Parts Lists

C H A N G E S U M M A R Y

ASYNCHRONOUS DATA PROCESSOR

3913 446 67530,
3913 446 67550, 3913 446 69750

References	Brief Description of Change	Documents Affected
PGV 3593	<u>On PCB Assembly 3913 446 74780:</u> C27 changed from 82pF to 68pF, 2222 683 34689. C48 changed from trimmer 4 - 37pF to trimmer 5 - 57pF, 2222 809 08003.	Circuit Diagrams Parts Lists
PGV 3647 16.05.89	<u>On PCB Assembly 3913 446 74780:</u> Link X18, 2422 549 26016 added. A12 Pins 4, 15 and A7b Pin 5 now connected to the top of X18. X1 Pin 21a now connected to the middle of X18. X1 Pin 23a now connected to the bottom of X18.	Circuit Diagram Assembly Drawing Parts Lists
CA 35516 89.10.17	Parts List errors corrected.	Parts List
PGV 4053 16.07.90	C33, 47nF, 2012 310 00316 changed to 47nF, 2012 310 03122.	Parts List

3913 446 67530
3913 446 67550
3913 446 69750

ASYNCHRONOUS DATA PROCESSOR

3913 446 67530 (NICAM 625)
3913 446 67550 (NICAM-3, 525)
3913 446 69750 Version 1 (NICAM 728, 625)
3913 446 69750 Version 2 (NICAM 728, 525)

1. GENERAL DESCRIPTION

The function of the Asynchronous Data Processor is to convert a continuous data stream, which is asynchronous with respect to video, into bursts of synchronous data which are suitable for insertion into video. In doing this the module must be phase-locked to incoming video, and must also take appropriate action under conditions such as the failure of video or data. The functioning of the module is largely controlled by the four Field Programmable Logic Sequencers (FPLSs) A3, A6, A12 and A13.

2. FUNCTIONAL DESCRIPTION

2.1 Coder Data Buffer Controller (CDBC)

The Coder Data Buffer Controller, A3, controls the two First-in First-out (FIFO) registers A4 and A5, which form a data buffer, converting incoming data into four-bit wide 'nibbles' for insertion into the buffer, and ensuring that the buffer always remains, on average, half full. On switch-on, or after a fault condition, it is assumed that the buffer contains invalid data, and so before any data is inserted into video, the buffer must be half filled with data. During this set-up period, when data is going into the buffer without being read out, A3 switches the Coder Data Insertion Controller, A6, to insert Amplitude Reference Data (ARD) into video. ARD consists of four pulses, level 0 and level 3 only, which enable the Quaternary ADC system in the decoder to operate normally and to be set up ready to receive valid data. Once sufficient data has entered the buffer, A3 signals A6 to start inserting real data into the video. A3 then continues to monitor the buffer for an overflow indication, and also look for an underflow indication from A6.

3913 446 67530
3913 446 67550
3913 446 69750

2.2 Coder Data Insertion Controller (CDIC)

The Coder Data Insertion Controller, A6, controls the insertion of data into video,..and converts the four-bit nibbles from the buffer into two-bit wide samples which will be formed into the actual Quaternary data in the Coder Video Processor. When indicated by A3, it will instead output two-bit wide samples which will form ARD. A6 also monitors the buffer and in the event of buffer underflow will provide an indication back to A3. This fault condition will only be reset once A3 signals A6 to output ARD, since this means that A3 has accepted the fault indication and is attempting to refill the buffer.

2.3 Coder Sync Pulse Controller (CSPC)

The Coder Sync Pulse Controller, A12, provides the line repetitive signals required in the coder, including standby line syncs, which are used to carry data if input video fails. This standby line sync is routed via X18 (Position LS), if required, but in Position MS mixed sync (generated in the Sync Separator board) is selected. A12 also generates a phase reference signal for the Phase-locked Loop (PLL) to ensure that the Asynchronous Data Processor is locked to video. A12 is clocked at the data insertion rate (as are A6 and A13), which is an integer multiple of line frequency, NICAM-3 data insertion rate being 352 times video line frequency, and NICAM 728 data insertion rate being 382 times video line frequency. These figures apply to both 525 and 625 line systems, with the appropriate change in actual clock frequency.

2.4 Coder Sync Lock Controller (CSLC)

The Coder Sync Lock Controller, A13, controls the synchronisation process of this module to video, and also monitors for video fail, switching to standby in this event. In the Stereo version, the link X18 selects whether standby line sync from A12 or standby field sync from the Sync Generator module is fed to the Video Processor in the event of video failure. Video fail can be detected in two ways: the first way is for A13 to carefully monitor the data bursts being inserted. If one burst of data is not inserted when it should be, indicating a missed sync pulse, A13 immediately switches to standby, switching back when a sync pulse is once again found. Video fail can also be detected by a SYNC FAIL signal coming via A15. This again switches A13 to standby, and also loads A15. When SYNC FAIL is released, A15 counts up from this preloaded value, clocked by regenerated line syncs from A12, and when it reaches full count releases SYNC FAIL into A13, switching A13 back to normal video. Hence, there is a built-in number of sync pulses delay (normally set to 5) before A13 returns to normal video, to validate the input video.

3913 446 67530
3913 446 67550
3913 446 69750

2.5 Phase-locked Loop

The first stage of the PLL which synchronises the module to input video is the filter formed by L1 and C26. This produces an 'S'-shaped curve from the falling Phase Reference edge produced by A12, and the delay of this curve, and hence fine phasing of the system clock, is adjusted using C48. This S-curve then passes into the gated op-amp A18, the gating pulse being derived from the line trigger edge from the Sync Separator by C35 and R38, and passed through V5 to A18. The sampled S-curve from the output of A18 is buffered by the dual FET A19 into A20, which is connected as an integrator, the PLL time constant being set by the integrator time constant. A21 is an analogue switch and is normally open, but when input video fails, A21 closes under control of A13, shorting A20 input and output, thereby holding A20 output to 0V. The output of A20 controls the varicap diode V2, which is part of an oscillator loop consisting of crystal B1, A22, and their associated components. In the absence of a signal to which it can lock, the action of A21 causes the oscillator to run at its nominal frequency. The output of A22 provides a differential signal to drive V3 and V4, the final clock drive being taken from the collector of V4. This is then used to clock A6, A12 and A13, the clock frequency being the quaternary data rate, which is itself a multiple of video line frequency.

2.6 Auto Reset

A17 and A25a act as an activity monitor to detect a 'lock-up' situation in one or more of the FPLSSs. One input to A25a monitors INSERT INHIBIT (low to inhibit data insertion), and the other input monitors the INSERT FAIL output (high for insertion failure). Normally, with INSERT INHIBIT high and INSERT FAIL low, A25 will hold A17p11 (RESET) high, A17 being a 12-stage ripple counter, and so A17 will not count. If, however, INSERT FAIL goes high without INSERT INHIBIT being low, a fault has occurred and A17 is released to count, clocked by the input data clock. A17p14 will go high after a count of 512, so if the fault is cleared before this, A17 will be reset and normal operation will continue; otherwise, A10a will be triggered to produce a reset pulse to A6, A12 and A13.

2.7 Data Clock Monitor

A9a acts as an input data clock monitor. In the presence of a data clock, A9a is continuously retriggered, so A9ap7 remains low and no fault indication, or reset to A3, is given. If data clock fails, however, A9a will time out, producing a fault indication and resetting A3, the latter being essential since A3 is clocked by the data clock and so will not operate in its absence. The return of data clock will trigger A9a, releasing the fault indication and the reset to A3.

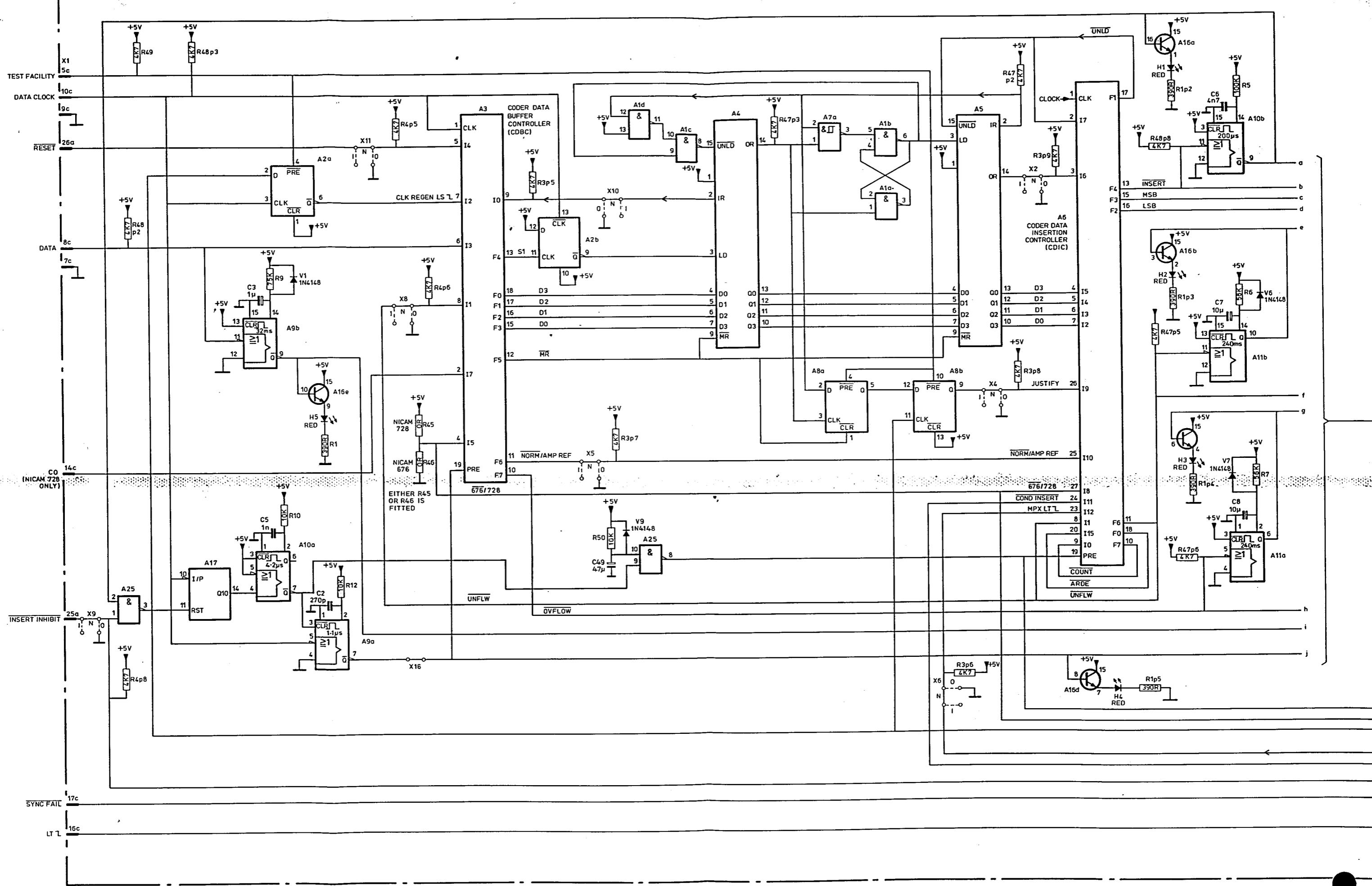
3913 446 67530
3913 446 67550
3913 446 69750

2.8 Fault Indications

Other fault indications for Data Fail, Insert Fail, Data Buffer Underflow and Data Buffer Overflow are provided by A9b, A10b, A11b and Alla respectively, A9b and A10b being continuously retriggered and timing out in the event of a fault, and Alla and A11b being triggered by actual fault outputs from A3 and A6 respectively. The remaining visual indication, of Standby, is produced directly by A13.

2.9 Power Supplies

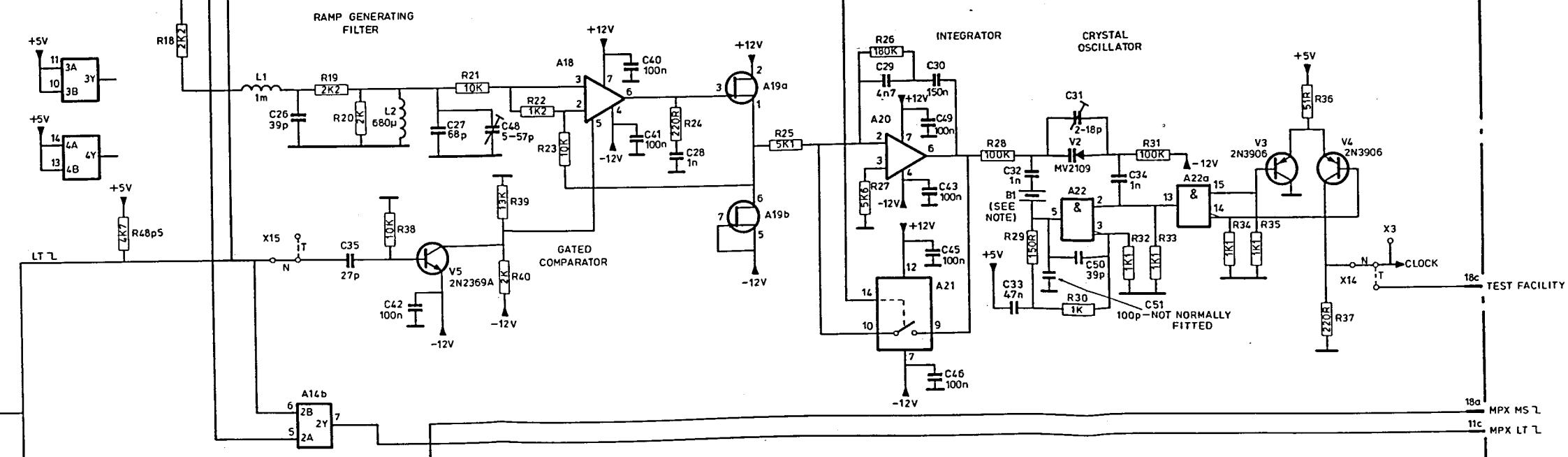
Power to the digital sections of circuitry (+5V) is provided from the main rack power supply. +12V and -12V is provided from regulators A23 and A24, which are fed from +20V and -20V, smoothed but unregulated, once again from the rack power supply. V8 prevents A23 being held off if, due to loads between the positive and negative rails, the output of A23 falls below the OV line during switch-on.



X1
 25c^a INSERT FAIL
 20ac^b INSERT
 16a^c DATA MSB
 15a^d DATA LSB
 24c^e DATA BUFFER UNFLW
 16a^f TEST FACILITY
 23c^g DATA BUFFER OVFLW
 19c^h TEST FACILITY
 21cⁱ DATA FAIL
 22c^j DATA CLOCK FAIL

A No.	TYPE	+5V	0V	C No.
1	HC00	14	7	*
2,8	HCT74	14	7	*
3,6,12,13	PLS105N	28	14	*
4,5	74LS224	16	8	*
7	HC132	14	7	*
9,10,11	HEF4528B	16	8	*
14	HC157	16	8	*
15	HC191	16	8	*
16	CA3082	15		
17	4040	16	8	
18	CA3080E			
19	2N3958			
20	LF351			
21	DG-200 ACJ		3	
22	MC10109	1,16	8	47
23	μ A78L12			
24	μ A79L12			
25	74HC132	14	7	

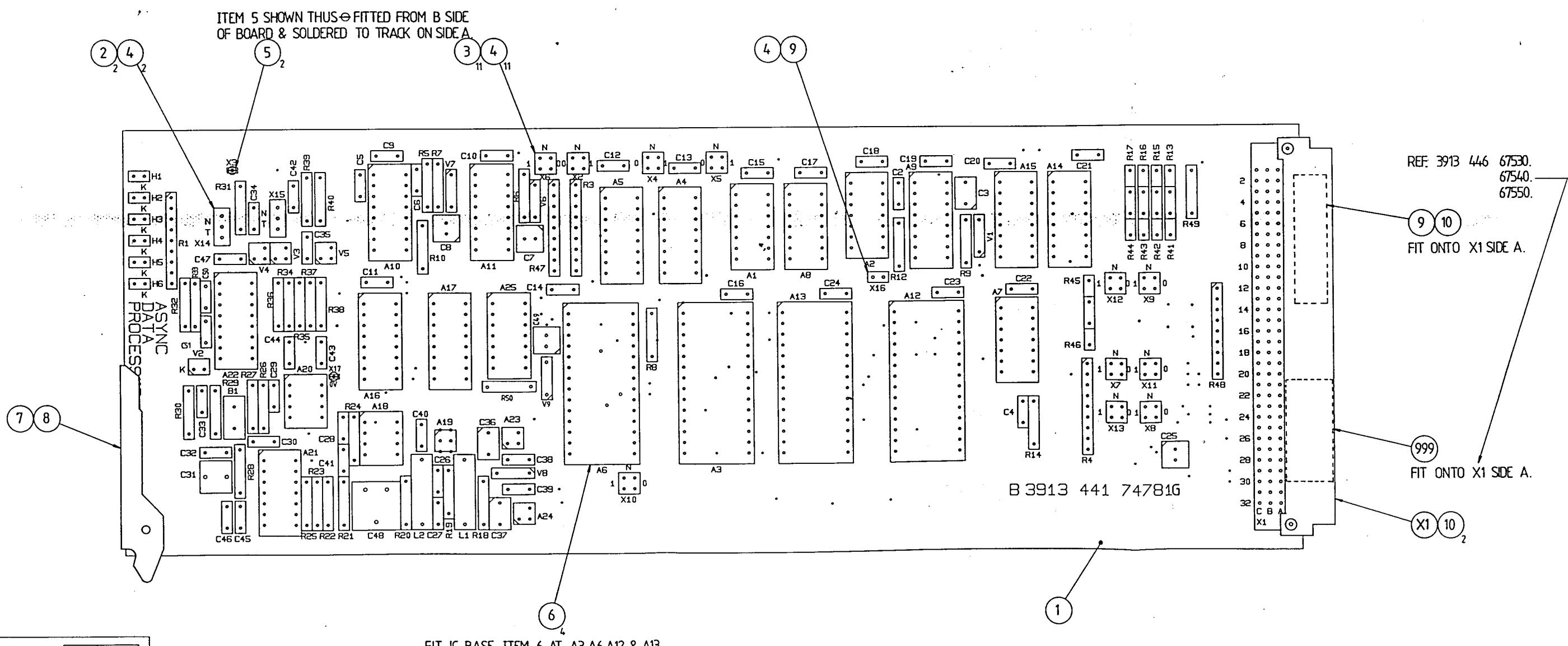
*C9 TO C24 ONE CAPACITOR PER I.C.



NOTE:

B1 FREQUENCY:-
 NICAM-3, 625 : 5.5MHz
 NICAM-3, 525 : 5.538461MHz
 NICAM-728, 625: 5.96875MHz
 NICAM-728, 525 6.010489MHz

ASYNCHRONOUS DATA PROCESSOR ASSEMBLY CIRCUIT	3913 446 6753
SH.130-2	SH.130-2
DRAWN ISI LTD	3913 446 6753
PYE T.V.T LIMITED CAMBRIDGE © 1986	DATE DRAWN 861024 FORM A1



PCB STRIKE PLATE INSTRUCTION	
1 AFFIX STRIKE PLATE NO 3913 982 90010 WITH THIS ASSEMBLY IN POSITION INDICATED	
2 STRIKE OFF NUMBER OF PLATE TO LEVEL INDICATED IN THIS DETAIL	
NOTE THE STRIKE LEVEL INDICATED MUST NOT BE CONFUSED WITH THE ZINKE LEVELS SHOWN ON ASSOCIATED DRAWINGS & PARTS LIST	
STRIKE NO	POW NO
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

FIT IC BASE ITEM 6 AT A3,A6,A12 & A13.

DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING	
TOL UNLESS OTHERWISE STATED		SURFACE TEXTURE	AS USED ON
UNITS	SCALE	ANGLES	HOLDS
MM	1:1 OR DIA: 2:1	SEE SEPARATE PARTS LIST	
PROJECTION		TREATMENT	ASSEMBLY NO
		SEE 3913 982 90010 CODE C.	PATTERN NO
NOTE		MODEL NO	
ASYNC DATA PROC. PCB ASSY DRG.		3913 446 7478	
SUPERSeded		15 09 07 31	
DRAWN	TP	MECH CHM	ELECT CHM
APPROVED			
HYE-TV LIMITED CAMBRIDGE (TRANSMITTER DIV.) © 1976 DATE DRAWN 860925 FORM A			

3913 446 67350
3913 446 67360
Version 1

SYNC SEPARATOR

3913 446 67350 (PAL)

3913 446 67360 (NTSC)

Version 1

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1.3 Clamping Circuit	Sh. 595-1
1.4 Sync Pulse Generation	Sh. 595-1
1.5 Clamp Pulse Generation	Sh. 595-2
1.6 Sync Fail Detector	Sh. 595-2
1.7 Field Trigger Generation	Sh. 595-2
1.8 Field Sync Fail Detector	Sh. 595-3
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1.10 Sync Generation	Sh. 595-3

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Circuit Diagram	..	3913 446 67330	
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Assembly Drawing	..	3913 446 75480	Sh. 110-1

PARTS LISTS

C H A N G E S U M M A R Y

SYNC SEPARATOR

3913 446 67350 (PAL), 3913 446 67360 (NTSC)

Version 1

References	Brief Description of Change	Documents Affected
PGV 3244 06.05.87	<p><u>On PCB 3913 446 74770:</u></p> <p>C15 changed from 100n, Polyester to 10n, ceramic, 2222 629 19103.</p> <p>C56, 150p, 2222 683 34151 added.</p> <p>R91, potentiometer, 10k, 2111 369 00085 added.</p> <p>R92, 27k added.</p> <p>R24 changed from 56k to 47k.</p> <p>R25 changed from 36k to 27k.</p> <p>R88 changed from 56k to 47k.</p>	Parts List Circuit Diagram Assembly Drawing
PGV 3254 20.05.87	<p><u>On PCB 3913 446 74770:</u></p> <p>C19 changed from $100\mu F$, 2012 310 00318 to $1\mu F$, 2222 122 57108.</p> <p>C57, $100\mu F$, 2012 310 00318 added.</p> <p>R5 changed from 3k0, 2322 156 13002 to 1k0, 2322 156 11002.</p> <p>R93, 470k, 2322 156 14704 added.</p> <p>R94, 10R, 2322 156 11009 added.</p> <p>V10 changed from BC559, 9331 977 60112 to 2N3906, 9330 791 70702.</p> <p>V26, 2N2369A, 9330 295 71112 added.</p> <p>Test Point X11, 2413 015 02201 added.</p>	Circuit Diagram Parts List Assembly Drawing
PGV 3361 08.01.88	<p><u>On PCB 3913 446 74770:</u></p> <p>R95, 4k7, 2322 156 14702 added in series with A3 Pin 3.</p> <p>C60, 5p6, 2222 683 09568 added between A5 Pins 3 and 4.</p>	Parts List Circuit Diagram Assembly Drawing
PGV 3611 07.02.89	<p><u>On PCB 3913 446 74770:</u></p> <p>R96, 300R, 2322 156 13001 added between A14 Pin 6 and X1 Pin 15a.</p>	Circuit Diagrams Parts Lists Assembly Drawing
PGV 3644 06.06.89	<p>Decoupling capacitors, 100n, 2012 310 00318 added to A5 and A21.</p> <p>Resistors 10R, 2322 156 11009 added into the +15V and -15V supplies to A3, A5 and A21.</p>	Circuit Diagram Assembly Drawing Parts List
PGV 3653 06.08.89	<p><u>Version 01 created:</u></p> <p>All, A12, A13, A15, A17, A18, A19 and its associated components.</p> <p>Parts List 3913 446 74770 discontinued and its contents integrated into Parts Lists 3913 446 67350 and 67360, Version 1.</p>	Circuit Diagram Assembly Drawing Parts List Text
PGV 3754 05.10.89	<p>C45 changed from 4-40pF to 5-57pF, 2222 809 08003.</p>	Circuit Diagram Parts List

C H A N G E S U M M A R YSYNC SEPARATOR3913 446 67350 (PAL), 3913 446 67360 (NTSC)

Version 1

References	Brief Description of Change	Documents Affected
PGV 3764 12.10.89	V14, transistor 2N2369A, 9330 295 71112 added. V15, V16, transistors 2N3906, 9330 791 70702 added. V23, diode MV2109, 9332 795 10702 added. V24, diode IN4148, 9330 839 90112 added.	Circuit Diagram Assembly Drawing Parts List
PGV 3782 89.11.27	R24 changed from 47k to 33k, 2322 156 13303. A6a pulse width is set to $42 \pm 5\mu s$ by means of R87.	Circuit Diagram Parts List Text
PGV 3782 89.11.27	A18 is re-programmed to 3913 036 60580 with new PLS105 program. A6 Pin 5 disconnected from existing network and connected to A18 Pin 17. R101 deleted. R24 changed from 47k to 33k, 2322 156 13303. A6a pulse width is set to $42 \pm 5\mu s$ by means of R87.	Circuit Diagram Assembly Drawing Parts List Text
PGV 3782 Issue 2 08.01.90	A18 reprogrammed to 3913 036 60570.	Parts List
PGV 3864 30.03.90	R30, 10k, 2322 156 11003 changed to 1k, 2322 156 11002 to improve reliability of circuit operation with attenuated input signals.	Circuit Diagram Parts List
PGV 3855 30.03.90	A14 pin 1 disconnected from X8/A6 pins 7 and 11. V27, V28 and V29 diodes BAW62, 9331 012 20112 added: anodes connected to A14 pin 1. Cathodes: V27 to A5 pin 11; V28 to A6 pin 5/A18 pin 17; V29 to A5 pin 8/A6 pin 9. R112 39k, 2522 156 13903 added between A14/1 and +5V	Circuit Diagram Assembly Diagram Parts List
PGV 3944 01.05.90	R30, 1k, 2322 156 11002 changed to 4.7k, 2322 156 14702. R112, 39k, 2322 156 13903 changed to 10k, 2322 156 11003. C60, 5.6pF, 2222 683 09568 added.	Circuit Diagram Assembly Drawing Parts List
PGV 3961 02.05.90 Cont. Next Page	V30, A23, R113, R122, C70 to C73 added as redesigned Sync Fail Detector: V30, transistor BC559, 9331 977 60112; A23, LM311, 9332 233 10682; R113, 470k, 2322 156 14704; R115, R117, 82R, 2322 156 18209; R116, 3k, 2322 156 13002; R114, R118, R119, 10R, 2322 156 11009;	Circuit Diagram Assembly Drawing Parts List ..

C H A N G E S U M M A R YSYNC SEPARATOR3913 446 67350 (PAL), 3913 446 67360 (NTSC)

Version 1

References	Brief Description of Change	Documents Affected
PGV 3961 02.05.90 Cont.	R120, 9k1, 2322 156 19102; R121, 1k, 2322 156 11002; R122, 22k, 2322 156 12203; C70, 10nF, 2222 629 19103; C71, C72, C73, 100nF, 2012 310 00318. Capacitors C74 to C80, 100nF, 2012 310 00318 added between +5V and OV supply pins of A5, A7, A9, A14, A19, A20 and A21. OV test point, 2413 015 02201 added near A4,5. R97 replaced by X13, 1x2 Berg Header, 3913 445 50110. Socket 2-way, 2422 549 26016 added (X13). <u>The above changes are incorporated in new PCB 3913 446 75480 that replaces 3913 446 74770.</u>	
PGV 3990 08.06.90	R35, 100k, 2322 156 11004 changed to 1M, 2322 156 11005. R117, 82R, 2322 156 18209 changed to 150R, 2322 156 11501. C60, 5.6pF, 2222 683 09568 changed to 68pF, 2222 683 34689.	Circuit Diagram Parts List
PGV 4053 16.07.90	C18, 330nF, 2012 310 00322 changed to 330nF, 2012 310 03124. C34, 47nF, 2012 310 00316 changed to 47nF, 2012 310 03122.	Parts List
PGV 4140 19.09.90	C60, 68pF, 2222 683 34689 changed to 33pF, 2222 683 34339.	Circuit Diagram Parts List

3913 446 67350
3913 446 67360
Version 1

SYNC SEPARATOR

3913 446 67350 (PAL)

3913 446 67360 (NTSC)

(Version 1)

1. FUNCTIONAL DESCRIPTION

1.1 General

The same printed circuit board is used for both PAL and NTSC versions; differences are small. Line trigger, field trigger and non-standard mixed sync outputs are generated from the incoming video signal. From this, standard mixed sync is fully regenerated and used to provide standby mixed sync if the incoming video should fail.

1.2 Input Buffer and Subcarrier Rejection

The video or sound-in-sync input signal is AC coupled into A3. R4 and R3 set the gain to about 3. C6 provides high frequency roll-off. L2, C8 give rejection of colour subcarrier, which is necessary to prevent false triggering of the sync detector on low-luminance, high-chrominance signals. R5 dampens the tuned circuit to reduce ringing on luminance steps.

1.3 Clamping Circuit

Transistor V1 provides a low-impedance source before the clamp capacitor C10. Clamping of black level to 0V is achieved during the back porch with FETs V2 (soft clamp) and V5 (hard). Generation of the clamp pulses is described in Para. 1.5.

1.4 Sync Pulse Generation

The two matched FETs of A4, connected in cascode, buffer the clamped video signal without changing the DC level. The output of the Sync Slicer A5 changes state as the video signal on pin 3 passes through the sync half-amplitude voltage, which is supplied to pin 4. The sync tip voltage is first detected by V10 (aided by V26), stored (with V_{be} offset) on C18, further smoothed by R36/C19, corrected for V_{be} offset by V11 (aided by V30) and halved by R38 and R21.

A6a is triggered by the output of A5 and in turn triggers A6b. The $5\mu s$ pulses fed back from A6b to A5 prevent A5 responding to sound in sync digits if they are present in the input signal. The other input to A6a is from A18, and is a pulse which remains low from shortly after a leading edge of line sync is detected to within $1\mu s$ of the time that the next leading edge is due. Thus A6a cannot respond to mid-line equalising and broad pulse edges nor to spurious sub-black during active line time. Thus A6a and A6b generate line trigger and line sync pulses undisturbed by the field sequence or by spurious sub-black pulses. The mixed sync pulses at A5 Pin 9 and at Pin 15a of the board connector have alternate equalising pulses widened to $5\mu s$ by the feedback from A6b, and so are non-standard in this respect. The negative-going line trigger pulses on Pin 16a of the board connector are delayed by R69 and C44 so that the LTedge is delayed by 165 - 200ns relative to the leading edge of sync in the incoming video.

1.5 Clamp Pulse Generation

The video from the subcarrier rejection circuit is passed to the emitter follower V8 with a little additional filtering by R26 and C14. V9 is a simple sync pulse detector which triggers the non-retriggerable monostable A8a to produce a $1.8\mu s$ clamp pulse from the trailing edge of sync. During start-up conditions these clamp pulses are fed to V2 via A7c and V4. This clamps the video adequately for the sync slicer to start to work, whereupon the Normal Clamp Pulse Generator A8b operates. The Clamp Pulse Changeover Control A9a is a retriggerable monostable, triggered via A7d when the Start-up and Normal clamp pulses occur at the same time. Then Normal clamp pulses from A8b are fed to both soft and hard clamps, through A9a's control of A7a, A7b and A7c. When the video input fails, A9a is no longer triggered, its outputs change state after $670\mu s$ and clamping falls back to the Start-up Clamp Pulse Generator. A8b is triggered by the trailing edge of the sync slicer output, via A22b. A22b is a non-retriggerable monostable which is set to give a $62\mu s$ pulse, and therefore prevents the production of a clamp pulse from spurious sub-black during picture time. During the field sequence when there are half line pulses, A22b can still only trigger once per line, so maintaining a steady clamp efficiency apart from slipping nearly half a line at the beginning of the broad pulses and just over half a line at the end of the field sequence. In order to check the $670\mu s$ pulse length of A9a, X7 is provided with 'Normal' and 'Test' positions; in 'Test' A9a receives field trigger pulses so that it is not retriggered before the end of its natural pulse length.

1.6 Sync Fail Detector

The Sync Fail Detector A23 is a voltage comparator which takes the detected Sync Tip voltage on V11e and compares it with a fixed voltage produced by the potential divider consisting of R115 and R116. R120 and R117 provide hysteresis so that it will change state decisively. Its output controls the Sync Fail indicator LED H2, and provides outputs to other modules.

1.7 Field Trigger Generation

The Mixed sync pulses from A5 are fed to the 'Field Sync Detector' via A14d. Between sync pulses, C22 is kept discharged by V12. When a pulse is present V12 is turned off and C22 starts to be charged by current through R42. If the pulse is short, i.e. a line sync or equalising pulse, C22 will not have time to charge to the turn-on voltage of V13. If the pulse is a broad field pulse, V13 will be turned on and monostables A10a and A10b will be triggered. The pulse width ($350\mu s$) of A10a masks the second and following broad pulses. A10b provides the desired pulse width of $4.5\mu s$.

1.8 Field Sync Fail Detector

The field sync pulses are passed to monostable A9b and continuously retrigger it, keeping its \bar{Q} output low. If these pulses stop, \bar{Q} will go high after 55ms and LED H3 will light to indicate the fault.

1.9 Sound Pulses Present Detector

A21 is to detect the presence of sound in sync pulses in the incoming video. It is fed with the same clamped video as A5, but its reference voltage on Pin 4 is 0V (between quaternary levels 1 and 2). A16a gives a 100ns pulse triggered from the leading edge of sync. The trailing edge of this 100ns pulse triggers A16b to give a $1.6\mu s$ pulse to gate the output of A21 (Pin 9). This output therefore goes low only if the clamped video on A21 pin 3 is above 0V during a period of from $0.1\mu s$ to $1.7\mu s$ after leading edge of sync; such an occurrence implies that sound in sync pulses are present and A20a is repeatedly retriggered to indicate the fact. R76 is fitted so that the LED H1 is lit and the Fault output on Pin 19c of the board connector is high for the unexpected situation, i.e. pulses present.

1.10 Sync Generation

Integrated circuits A17 and A18 are Field Programmable Logic Sequencers (FPLS), of the Signetics Integrated Fuse Logic (IFL) family. They are clocked by the output from an oscillator running at a multiple of TV line frequency. At each clock pulse the outputs change state according to:

- (a) Their previous states.
- (b) The previous states of internal registers.
- (c) The input states.
- (d) How the devices have been programmed.

1.10.1 Power-on Reset

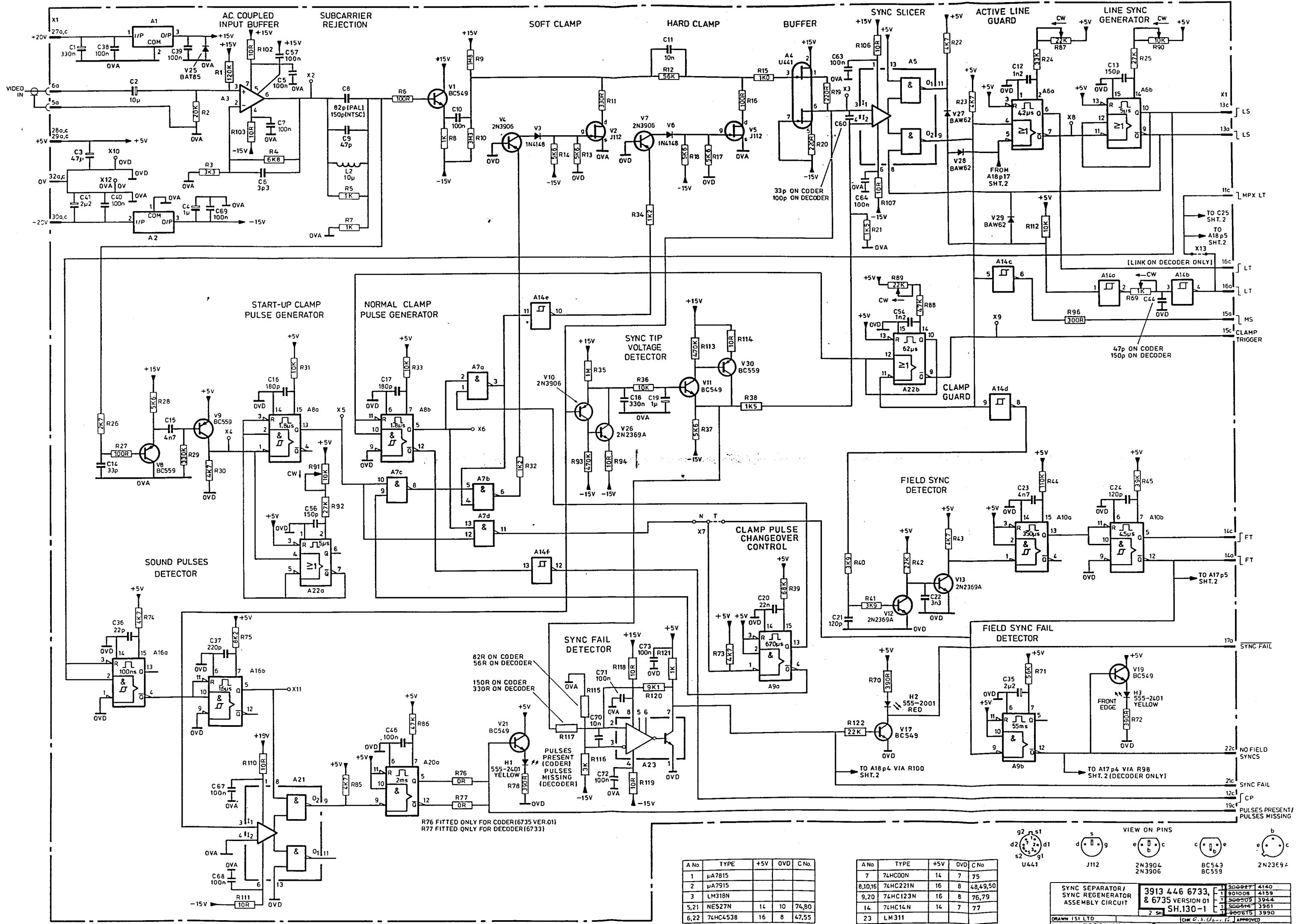
A short time after switch-on, the rising voltage on C42 triggers monostable A20b which in turn provides a reset pulse to the two IFLs.

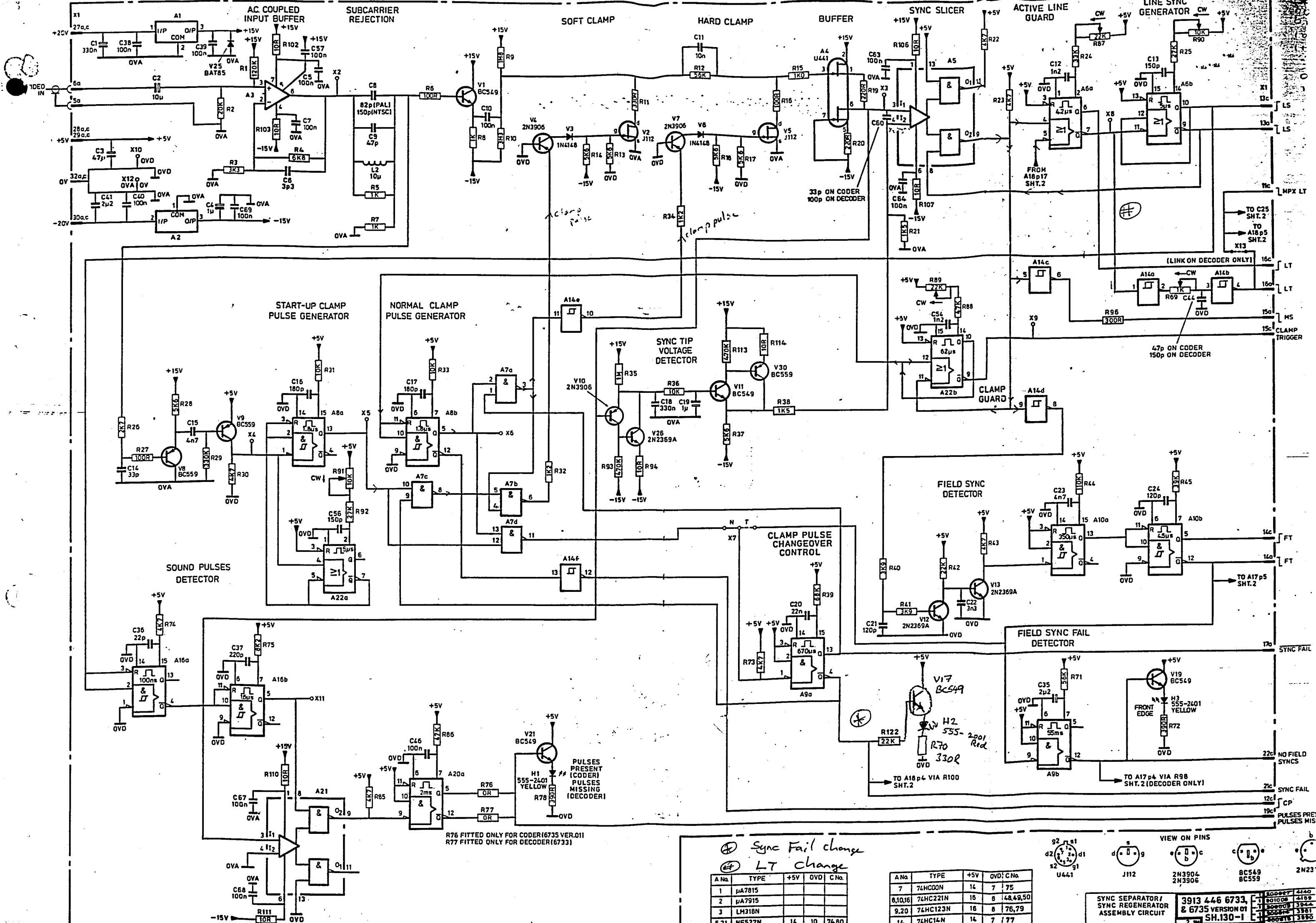
1.10.2 Voltage-controlled Oscillator

The oscillator frequency is 328 times line frequency. FPLS A18 (Decoder Line Sync Generator, DLSG) in conjunction with counter A19 produces a phase reference pulse every 328 clock cycles. The filter consisting of L3, L4 and the associated components shapes the phase reference pulse into a voltage ramp which is sampled by the transconductance amplifier A11 at the moment the leading edge of the line trigger pulse occurs. The sampling pulse on Pin 5 of A11 is produced by V14, its short duration being due to the time constant of R53 and C25. The output of A11 is a pulse of current to add to or subtract from the charge on C28 according to the ramp voltage at the moment of sampling. The voltage on C28 is buffered by A12 and fed to A13 which is connected as an integrating amplifier. The output of A13 is used to control the capacitance of the varicap diode V23. This acts as fine tuning to the crystal oscillator and thus keeps a constant phase relationship between Line Trigger and Phase Reference. Trimmer capacitor C32 across the varicap diode should be set so that the output from A13 is 0V when the system is locked. Trimmer C45 in the ramp generating filter is used to match the timing of standby mixed sync to that of incoming sync (allowing for overall delay through the video processor), so that the timing of the leading edge of sync relative to the marker pulse remains the same when the Coder goes to standby.

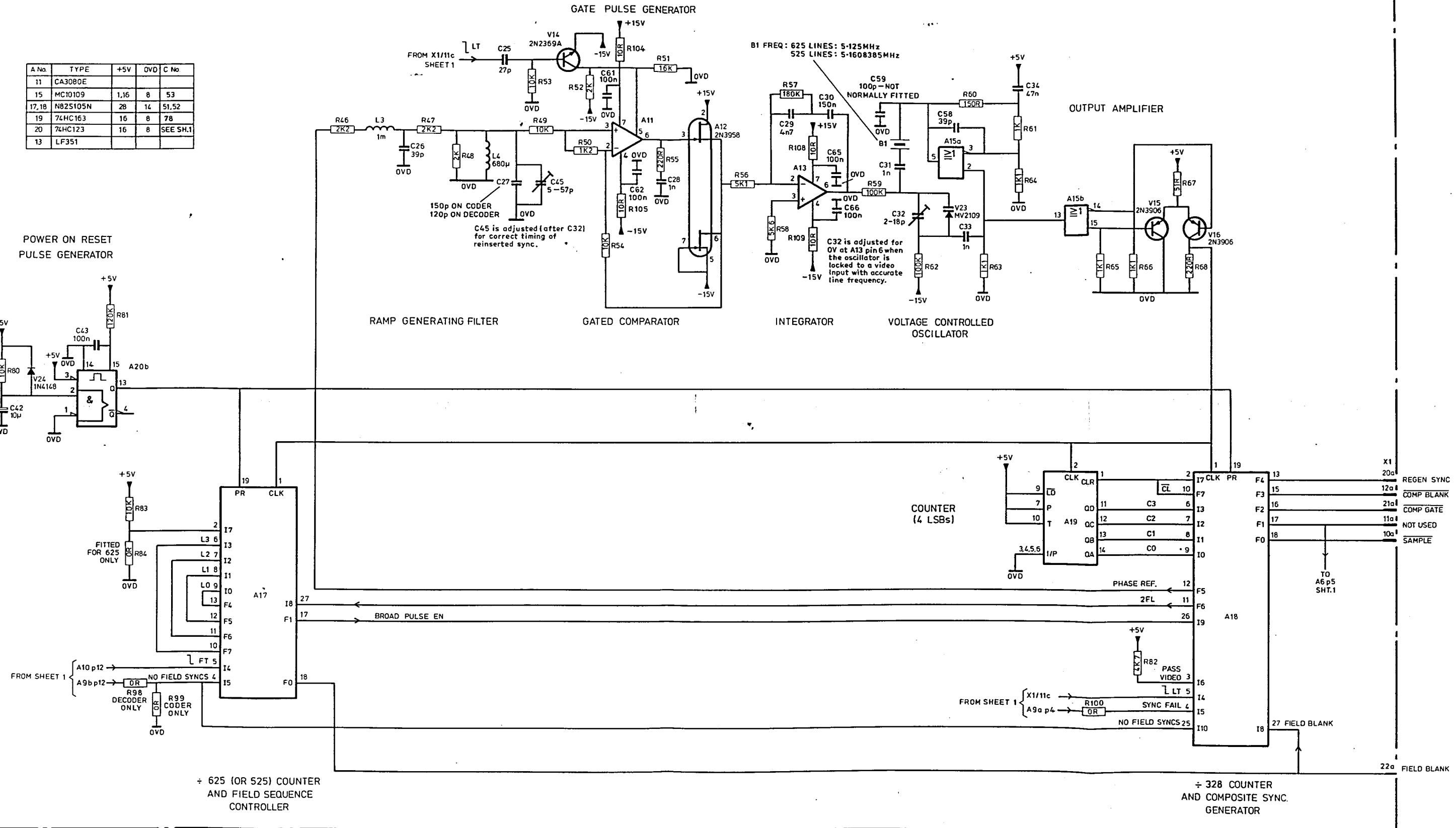
1.10.3 Line and Field Sync Generator

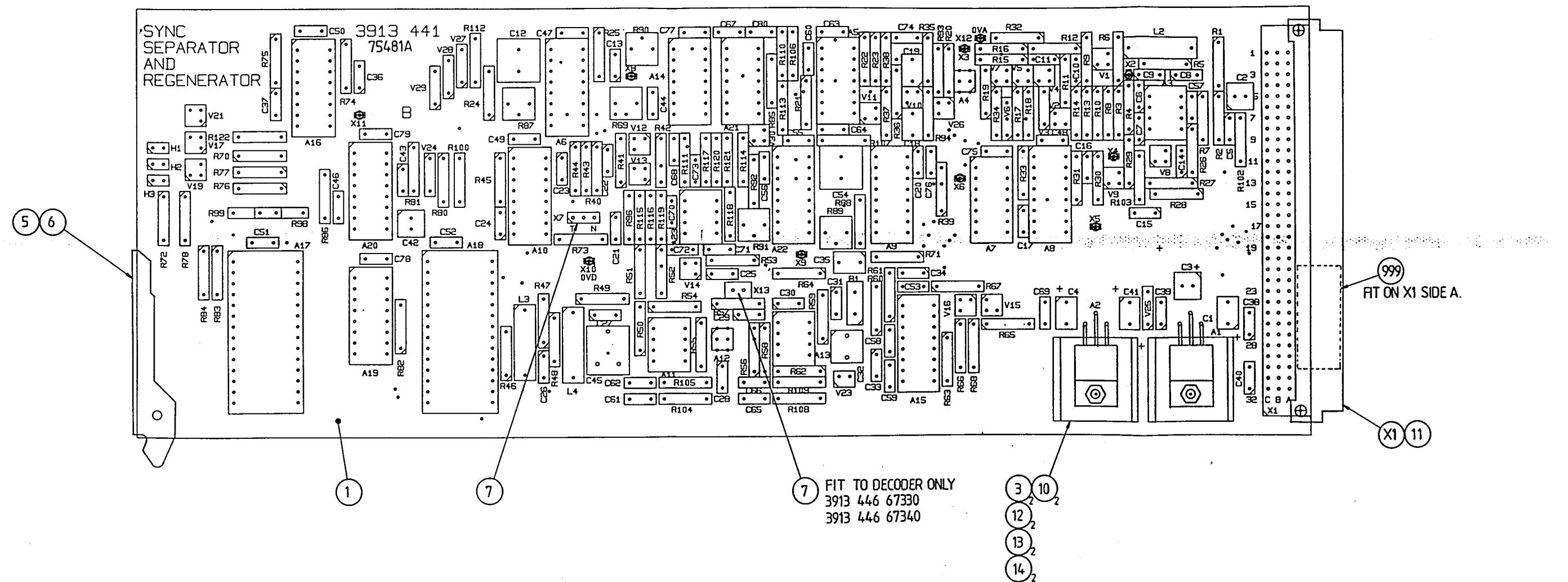
As well as providing a phase reference pulse for the line-locked oscillator, A18 provides half-line repetition rate pulses $\overline{2FL}$ for the Decoder Field Sync Generator (DFSG) A17 which counts through a 625 (or 525) half-line sequence to determine the correct times for equalising pulses and broad pulses. Under the control of outputs from A17, A18 produces the full sequence of Regenerated Sync, Composite Blanking, Composite Gate (for control of reinsertion of regenerated sync) and Sample (for control of sampling of input broad pulse amplitude). A18 also provides the active line guard pulse mentioned as being fed to A6a (see 1.4). To ensure that the whole sequence is in phase with the incoming signal, DLSG has a Line Trigger input and DFSG has a Field Trigger input.





A No.	TYPE	+5V	OVD	C No.
11	CA3080E			
15	MC10109	1,16	8	53
17,18	N825105N	28	14	51,52
19	74HC163	16	8	78
20	74HC123	16	8	SEE SH.1
13	LF351			





PCB STRIKE PLATE INSTRUCTION	
1. APPLY STRIKE PLATE NO. 3913 982 90010 STICKED WITH THIS ADHESIVE ON POSITION INDICATED	
2. OFF NUMBERS ON PLATE TO LEVEL INDICATED IN THIS DRAWING	
NOTE: THE STRIKE LEVEL SHOWN HERE MUST NOT BE CONFUSED WITH THE ZINKE DATES SHOWN ON ASSOCIATED DRAWINGS & PARTS LIST	
STRIKE NO.	OFF
1	
2	
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DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING	
DIMENSIONS		INCHES	MILLIMETERS
TOL. UNLESS OTHERWISE STATED		SURFACE TEXTURE	NOT USED ON
MATERIAL PROJECTION 2:1	MATERIAL DRAINAGE	NOTES	NOTES
SEE 3913 982 90010 CODE C.			
TITLE: SYNC SEP. & REGENERATOR PCB.		3913 446 7548	
DRAWN BY: D.J.F. HELD BY: VARIAN I.V.T. LTD CAMBRIDGE (c) 1990 DATE DRAWN: 90/04/30		APPROVED BY: ELECT. CHG. APPROVED BY: ELECT. CHG.	

CODER RACK FRAME ASSEMBLY3913 446 69790Contents

CHANGE SUMMARY	Sh. 508-1
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Motherboard - Circuit Diagram	Sh. 130-1
Power Transformer Wiring - Circuit Diagram	Sh. 130-2
Coder Ribbon Cables	Sh. 130-3
Rear Panel Layout	8928 190 30001 Sh. 512-1
Motherboard PCB Assembly - Side B	3913 446 75420 Sh. 110-1
Motherboard PCB Assembly - Side A	3913 446 75420 Sh. 110-2

PARTS LISTS

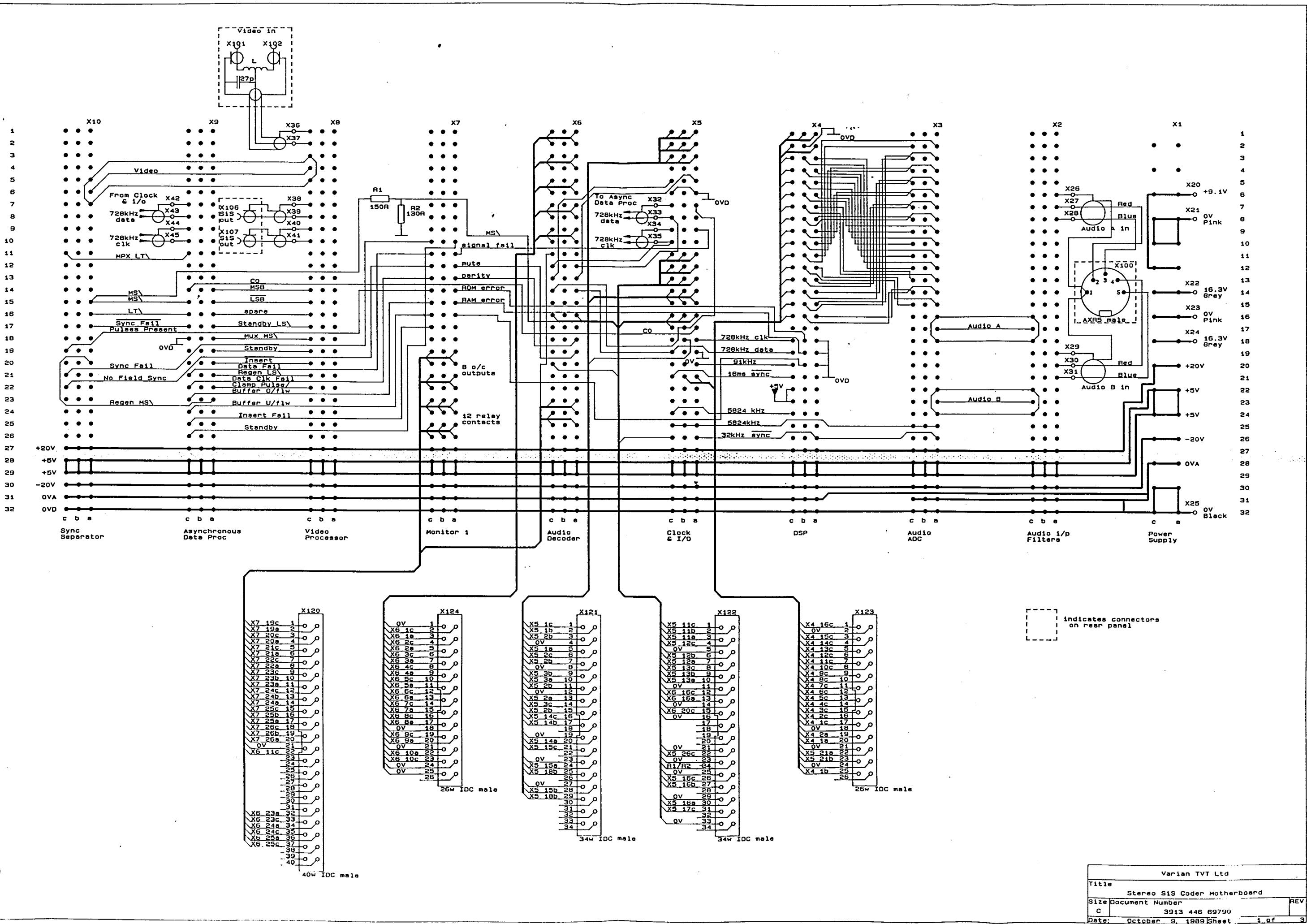
C H A N G E S U M M A R YCODER RACK FRAME ASSEMBLY3913 446 69790

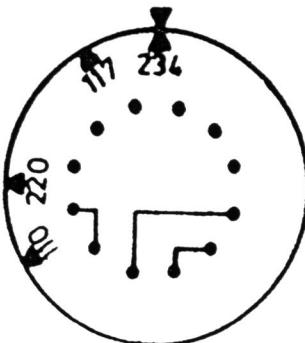
References	Brief Description of Change	Documents Affected
PGV 3929 03.04.90	End piece 2712 028 00816 changed to 2700 028 01087.	Parts List
PGV 3810 Issue 2	Label containing BBC patent GB2116403 information placed on rear panel.	
PGV 3980 22.05.90	Specification of Mains Toroidal Transformer 3913 449 51380 updated.	
PGV 4002 08.06.90	Lockwasher 2522 616 04140 added between transformer and rear panel.	Parts List
PGV 4033 21.06.90	Specification of Mains Toroidal Transformer 3913 449 51380 further updated.	
PGV 4059 23.07.90	Neoprene gasket, supplied as part of transformer 3913 449 51380, fitted between transformer and rear panel in place of 'Tesmol' tape 1222 100 15056 and lockwasher 2522 616 04140.	Parts List Assembly Drawing

CODER RACK FRAME ASSEMBLY3913 446 697901. GENERAL DESCRIPTION

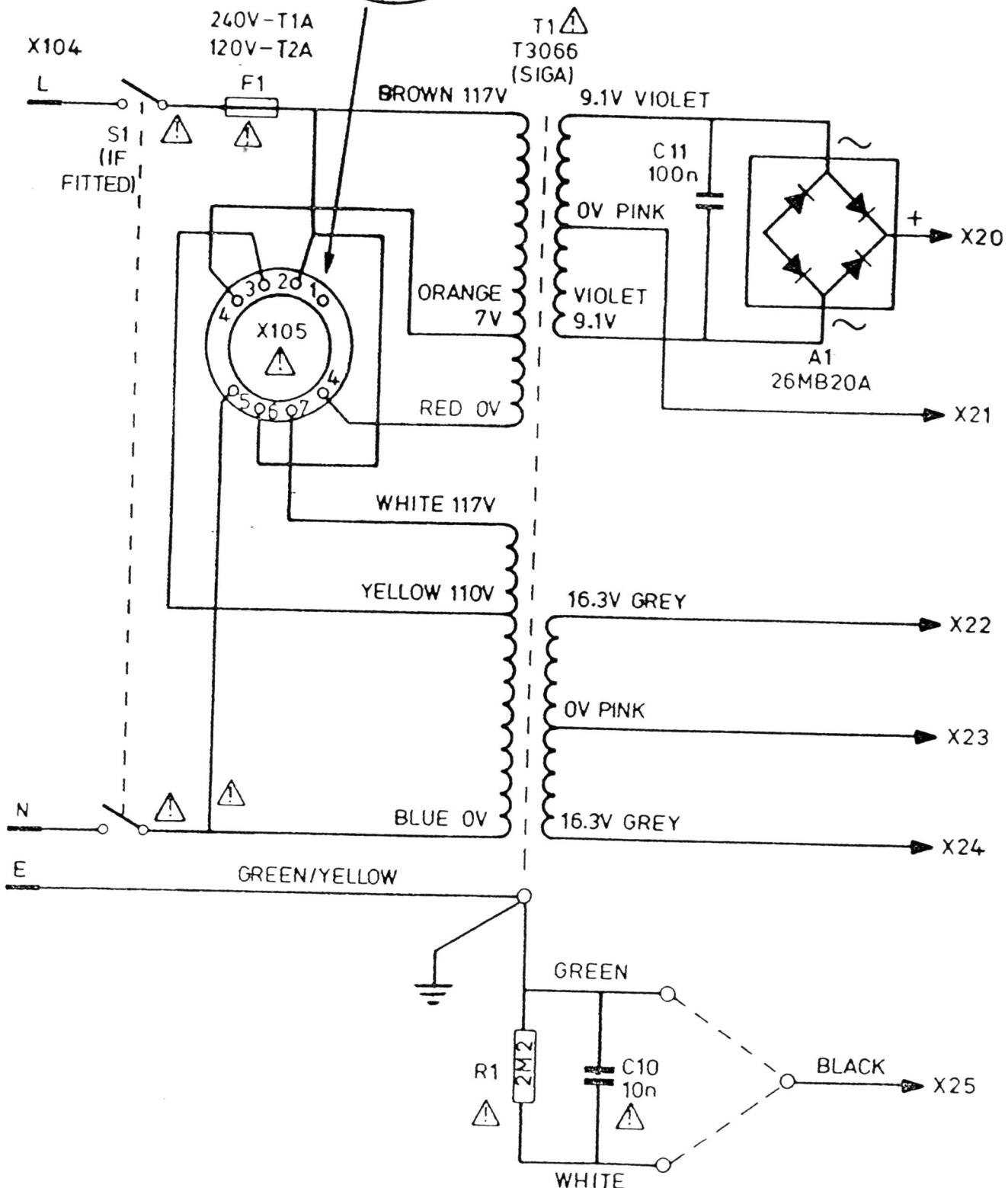
This unit comprises:

- (a) A motherboard assembly, containing the sockets which the various modules are plugged into, the internal wiring between modules and the connectors for the ribbon cables that take the interface connections to and from the rear panel.
- (b) Module runners.
- (c) Rear panel assembly, supporting the following components:
 - (i) Mains transformer and rectifier to provide the module supplies.
 - (ii) Mains voltage selector and power wiring.
 - (iii) Video input balun.
 - (iv) All input and output connectors.
- (d) Front panel providing access to audio sockets and certain operational indicators.
- (e) Side panels.

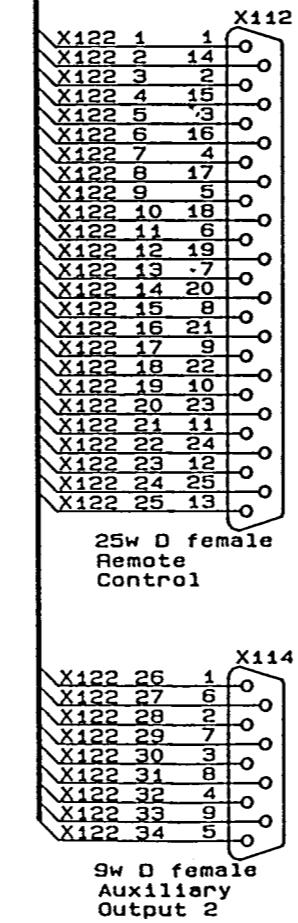
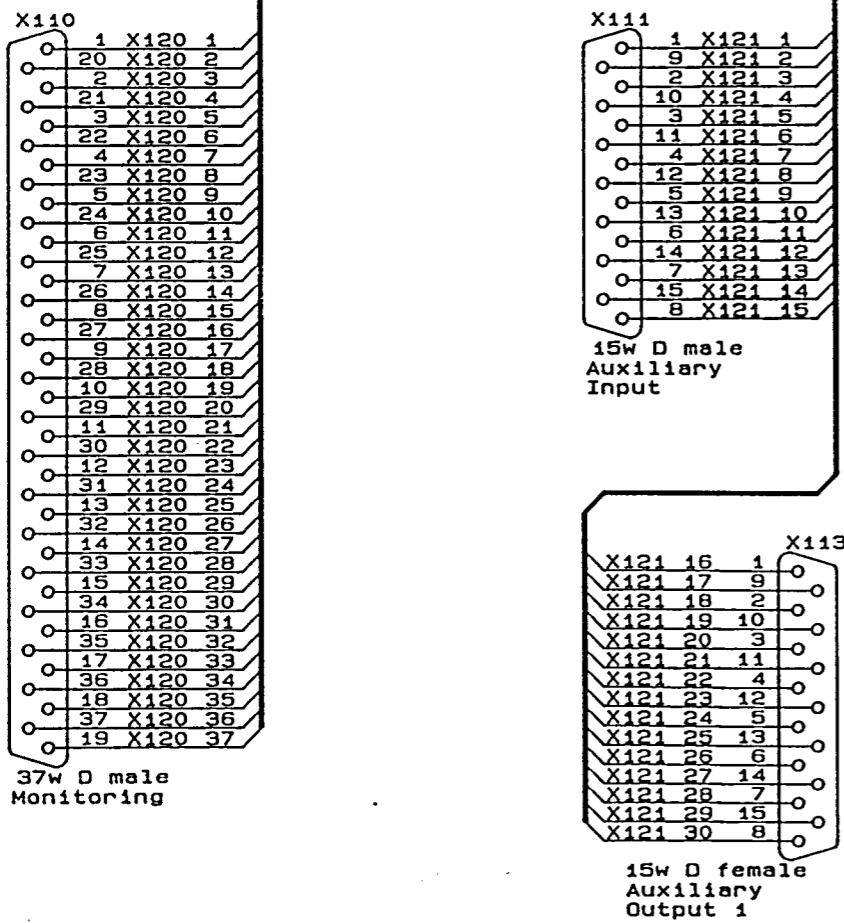
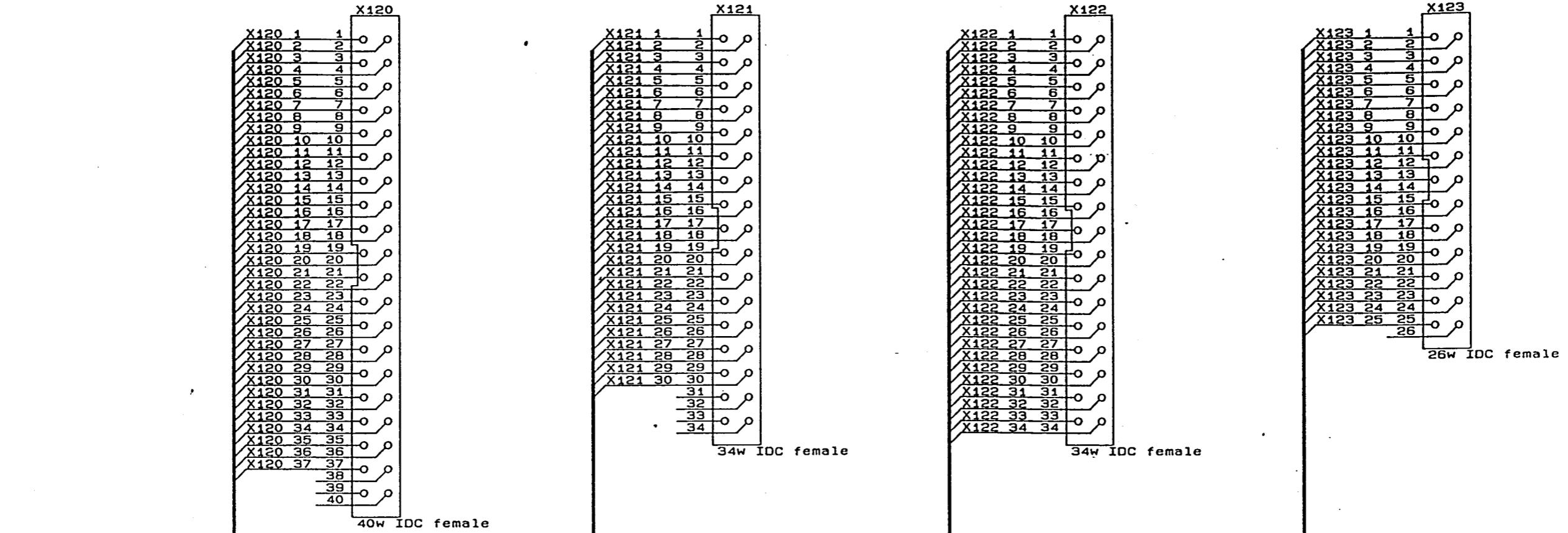




ROTATABLE
CONTACTS OF
MAINS VOLTAGE
SELECTOR

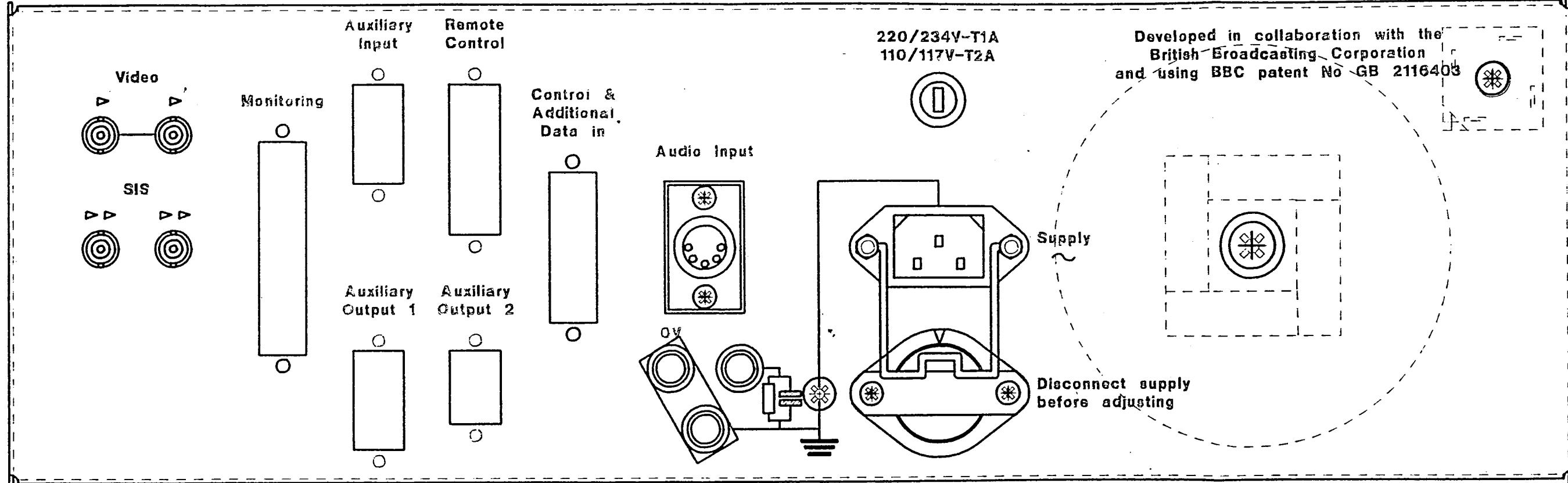


STEREO SIS POWER TRANSFORMER WIRING		3913 446 6979	891016	
		& 6982		
		SH 130-2		
DRAWN ISI LTD/JEG		3 SH		
VARIAN T.V.T LTD CAMBRIDGE © 1989		CHK C.S. Clementson	APPROVED	
		DATE DRAWN 891016 FORM A 4		



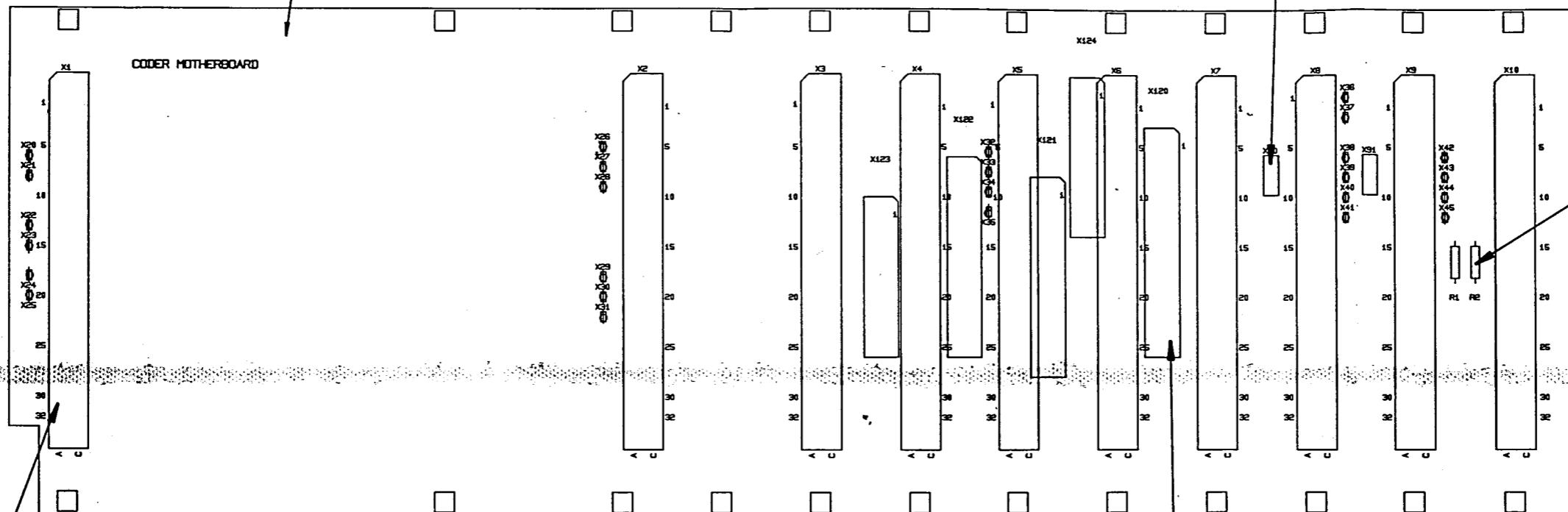
View on
Rear Panel

Varian TTV Limited CAMBRIDGE © 1989		
Title		
Size	Document Number	REV
B	3913 446 69790 SH.130-3	00
Date:	January 4, 1990	Sheet 3 of 3



TITLE REAR PANEL LAYOUT		89-11-29				
STEREO SOUND IN SYNC CODER		8928 190 30001				
ARCHIVE No		1	St	10	SH	512-1
DRAWN	N.BROWN	MECH CHK		ELECT CHK		APPROVED
ARIAN TVI LIMITED CAMBRIDGE		© 1989		DATE DRAWN 89-11-29		FORM A3

D190_30001S1



SIDE B

DO NOT SCALE THIS PRINT				DIMENSIONS ARE SHOWN AFTER PLATING		
DIMENSIONS		TOL. UNLESS OTHERWISE STATED		SURFACE TEXTURE		1ST USED ON
UNITS	SCALE	ORIG.DRG.	ANGLES	HOLEs		
MM	1:1					
SEE SEPARATE PARTS LIST						ASSEMBLY NO.
						QUANT.
PROJECTION		TREATMENT:				
LST	3RD	SEE 3913 982 90010 CODE C				
TITLE		CODE		3913 446 7542		18891019
CODER MOTHERBOARD		PCB ASSY DRG				
SUPERSDES		2 SH.		SH. 110-1		
DRAWN		REDL.CH.		ELECT.CH.		APPROVED
VARIAN TTV LTD CAMBRIDGE						(c) 1989 DATE DRAWN 19-10-89 FORM

NOTE:

W3, W4 see wire prep sh 231-1

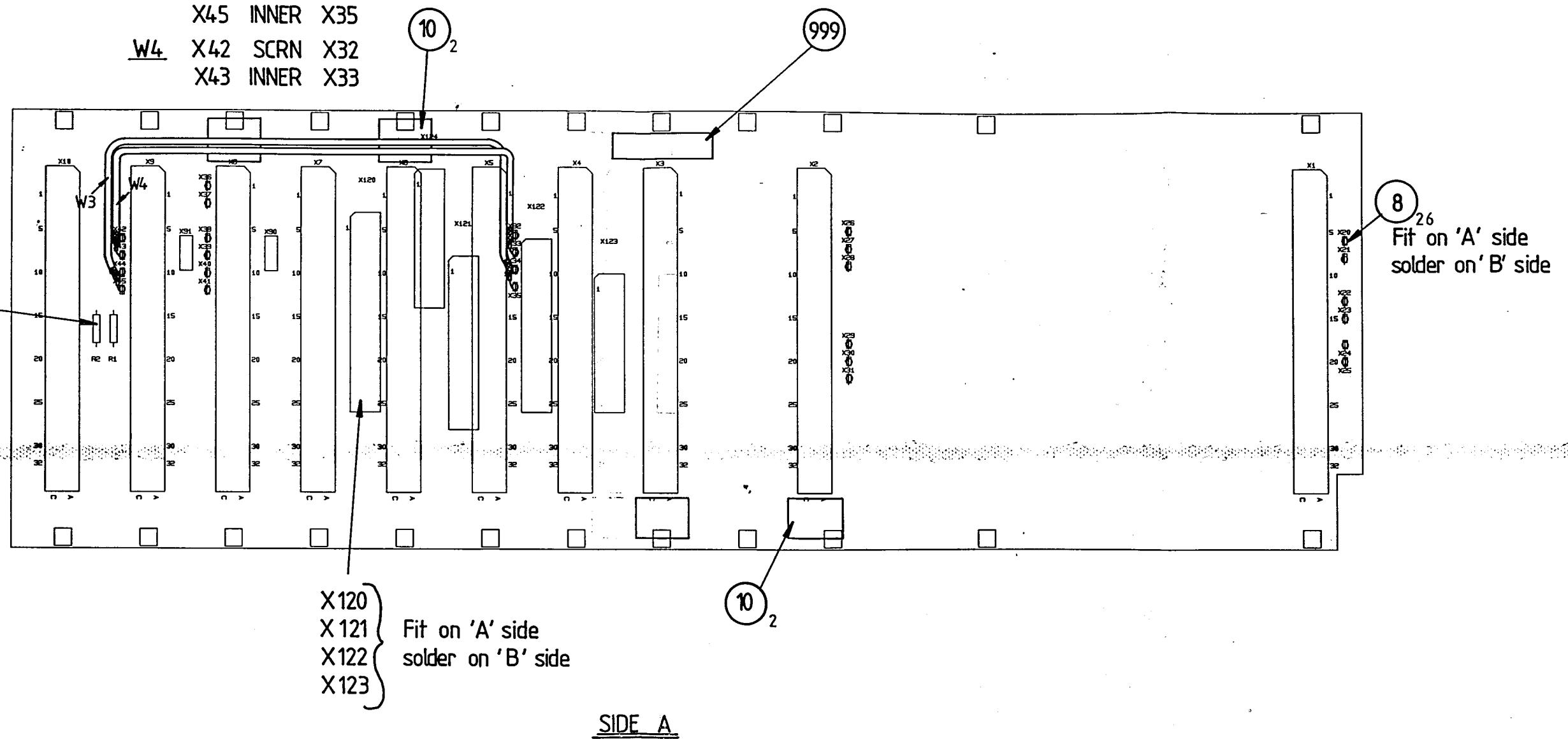
W3 X44 SCRN X34

X45 INNER X35

Wk. X1.2 SCRPN X32

W4 X42 SCR N X32
X43 INNER X33

R1, R2
Fit on 'A' side
solder on 'B' side



DO NOT SCALE THIS PRINT				DIMENSIONS ARE SHOWN AFTER PLATING		
TOL. UNLESS OTHERWISE STATED		SURFACE TEXTURE		1ST USED ON		
DIMENSIONS	ANGLES	HOLES				
UNITS	SCALE	MATERIAL				
MM	1:1	SEE SEPARATE PARTS LIST				ASSEMBLY NO.
PROJECTION	TREATMENT:					
	SEE 3913 982 90010 CODE C					
1ST	3RD	CODE		DRAWN BY		
TYPE			3913 446 7542		1B 1891019	
CODER MOTHERBOARD PCB ASSY DRG						
SUPERSEDES			2. 94	94. 110-2	→	
DRAWN			ELEC. CHK.		APPROVED	
VARIAN T.V.T LTD CAMBRIDGE			(c) 1989		DATE DRAWN 19-10-89 FORM	