

SERVICE MANUAL

**STEREO SOUND IN SYNC
LDM 1903/1904**

System Description

and

User Information

3913 985 09364

HARRIS

8928 190 30001 and 40001

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A M E N D M E N T R E C O R D S H E E T

STEREO SOUND IN SYNC LDM 1903/1904

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2	Jan/91	Dec/91	TVT	New Clock and I/O (Reframer)
3	Apr/96	Apr/96	Harris	New ADC and various.
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GENERAL DESCRIPTION

1. INTRODUCTION

SOUND IN SYNC is a system in which a video link, for example between studio centres, is used for transmission of broadcast quality sound together with the video signal.

At the sending end of the link the audio signal is inserted in digitally coded form in the line synchronising periods of the composite video signal. At the receiving end the decoder converts the received digital information into the original audio signal and restores the video signal to normal.

This system is a development of the Two-channel Sound in Sync system which used the NICAM-3 bitstream. This system uses the NICAM 728 bitstream. It is suitable for either stereophonic or dual-language transmissions. It consists of a Coder Type LDM 1903 and a Decoder Type LDM 1904.

A number of versions of the system are available. These are detailed in the table in Para. 3.

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2. PRINCIPLES OF OPERATION

Refer to the outline block diagrams (Sheets 510-1) and the functional block diagrams (Sheets 536-1).

2.1 Audio Digitisation

Each audio channel is pre-emphasised, band-limited to 15kHz and sampled at 32kHz. The two channels are sampled simultaneously and digitised in a 14-bit A-to-D Converter.

2.2 Compression and Bit Stream Generation

The digitised samples from the two audio channels are dealt with separately by a process of near instantaneous compression in a NICAM 728 compander system; this compresses the samples from 14 to 10 bits. Each set of 32 samples is coded into one of five gain ranges, each range being determined by the greatest magnitude found in the set. The digital coding format used for the samples is 2's complement, but for ease of explanation and understanding the following description of the compression process assumes sign-plus-magnitude coding.

For each sample, the sign bit is sent,

As many of the four most significant magnitude bits (MSBs) as are zeros in all the samples are dropped; the following nine bits are sent. Note that in the example in Fig. 1 there are three leading zeros; the 9-bit block would be shifted to the left or the right if there were two or four leading zeros.

Sample 1	+	0	0	0	1	1	1	0	1	0	1	1	0	1
2	+	0	0	0	0	1	1	0	1	1	1	0	0	1
3	-	0	0	0	1	0	0	1	0	1	0	1	0	1
4	-	0	0	0	0	0	1	1	1	0	0	1	0	0
		All zeros.												
Sample 32	+	0	0	0	1	1	0	1	1	0	0	1	0	1

Fig. 1

A range code sent with each set of samples tells the decoder how many

zeros to re-insert after the sign bit. Thus the signals of highest amplitude are encoded to 10-bit accuracy, while for the low-level signals the full 14-bit accuracy is retained.

For 2's complement coding, which is actually used, the most significant bit (MSB) can be regarded as the sign bit in the above description, and the next most significant bits which are the same as the MSB can be regarded as leading magnitude bits of value zero.

For each 10-bit compressed sample word, a parity bit is added, based upon the six most significant bits. The parity is even. The range codes for each 1ms block of samples are conveyed by two 3-bit scale factors (one for each channel) 'hidden' in the parity bits; the 64 parity bits are divided into six groups of nine (with 10 over), each group being allotted to one scale factor bit; if the scale factor bit is a zero, the parity bits are unchanged; if the scale factor bit is a 1, the parity bits are complemented, i.e. the parity becomes odd. In the decoder, majority decision logic is used to extract the scale factor bits and reveal genuine parity errors. Some countries intend using the remaining 10 parity bits in two groups of five for transmission of two extra data bits, sometimes called Binary Control Information or CIBs.

If the two channels comprise a stereo signal, the bits for the two channels are interleaved on a sample basis, i.e. 11 bits (including parity) for a sample of channel A are followed by the corresponding 11 bits for channel B. If the bitstream is for one or two monophonic signals, the bits for the two channels are interleaved on a frame basis, i.e. a 1ms frame containing samples for 2ms of channel M1 audio is followed by a 1ms frame containing samples for 2ms of channel M2 audio. The frame boundaries correspond to the compression block boundaries. This is followed by a process of bit interleaving within each frame (whether stereo or mono) such that adjacent bits from a sample word occur at least 16 bits apart in the bitstream. Each 1ms frame has an 8-bit frame alignment word at the beginning, followed by five Application Control bits, 11 Additional Data bits and then the 704 (= 64 x 11) sound data bits, making a total of 728 bits per frame. All but the frame alignment word bits are 'scrambled' for energy dispersal, i.e. the bits are complemented or not according to a defined pseudo-random sequence.

2.3 Conversion to Quaternary Form

To insert the digitised audio information in the line sync period of the video signal, pairs of bits are combined to form quaternary (4-level) digits ('quits'). This process enables data at an instantaneous rate of about 12 Mbits/second to appear at 6 Mquits/second, which is well within the bandwidth limits of video circuits.

Quit Level 0 is at peak sync level and Level 3 is 700mV more positive (Fig. 2).

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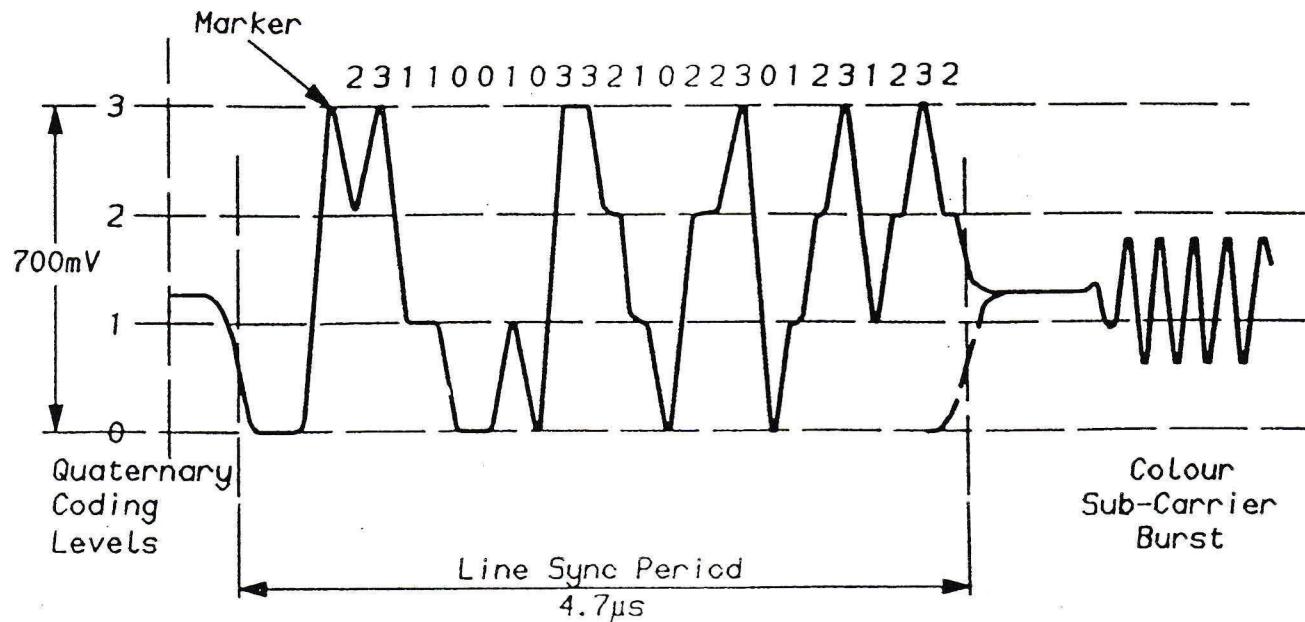


Fig. 2

Since the data rate and the TV line rate are not interrelated the insertion process has to be asynchronous: most sync pulses contain a marker pulse plus 24 quits, but every two or three lines a marker and only 22 quits. The marker and following digits start late, rather than end early. The marker is a Level 3 quit which serves as a timing reference for the following data.

The two bits taken to form each quaternary digit are taken from adjacent bits in the bitstream (Fig. 3). The conversion from bits to quits is done on the basis of the Gray code, i.e. only one bit changes between adjacent quit levels, so that if the decoder detects a quit value incorrectly by one level, only one bit error is produced.

The Gray coding scheme is inverted after the first, third, fifth, etc quit in each sync pulse. This inversion is necessary for a NICAM-3 bitstream and is retained for NICAM 728 although the reason does not apply.

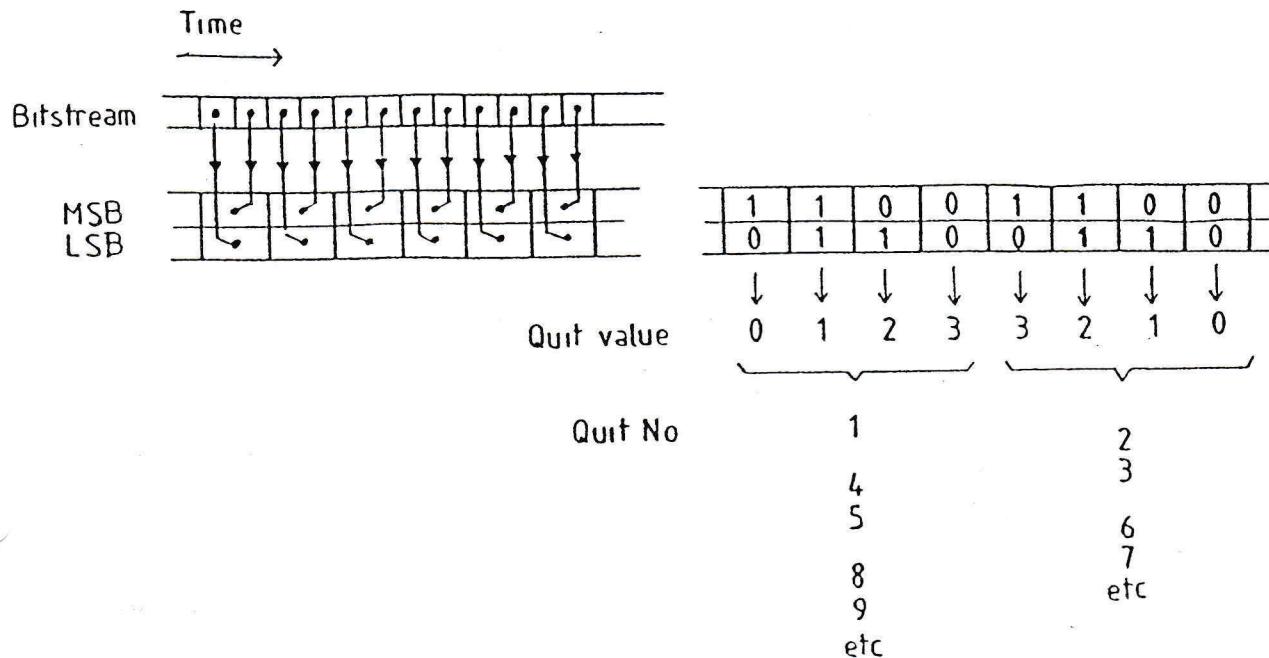


Fig. 3

The asynchronous data insertion is controlled by four Field Programmable Logic Sequencer (FPLS) ICs which monitor the depth of data in a FIFO memory and provide standby sync pulses if the video source should fail. These standby sync pulses may be line sync only or composite sync; the selection is made by the 2-position link X18 on the Asynchronous Data Processor module. Data insertion itself is done in analogue circuitry of mainly discrete components which introduces minimal distortion of the video signal.

2.4 Data Recovery

In the decoder the quits are decoded by a process which is designed to achieve reliable results even after moderate distortion of the signal during transmission. Each quit is sampled and converted to a 6-bit number by a fast ADC: by examining the range of numbers produced, a microprocessor determines the reference voltages to be used by the ADC, thus compensating for any loss or gain in the transmission path. The program for the microprocessor is written in FORTH and stored in an 8kbyte EPROM. The microprocessor has a built-in FORTH interpreter.

The reference voltages to be used by the 6-bit ADC are produced by an 8-bit DAC. Timing is controlled by another FPLS which determines, from the position of the marker pulse after the sync leading edge, whether there are 24 or 22 following quits.

As the microprocessor takes time to respond to changes in quit amplitude, further immediate processing is done on each set of 24 or 22 6-bit quit values: each value within the range expected for a Quit Level 0 or 3 is used to produce an error value which is averaged for each of levels 0 and 3 throughout the set. The two error values (for Levels 0 and 3) are used to select one of 256 look-up tables for correction of the whole set of 6-bit values as they are converted to the original pairs of bits they represent.

2.5 Bit Stream Regeneration

Each pair of bits recovered is fed into a FIFO memory, and the contents of the memory are fed out at a constant rate as a 728kbit/second bit stream equivalent to that in the coder. The bit stream clock regeneration is under the control of a programmed FPLS which maintains a steady clock rate in spite of the erratic rate of arrival of the recovered data.

2.6 Reframing

Any discontinuity in the bit stream will cause the audio decoder to receive spurious data, which may result in unpleasant noises followed by a mute as the decoder circuitry re-locks to the framing data in the bit stream. To avoid the worst effects of any such discontinuity, reframing circuitry is included in the Clock and I/O module.

The reframer stores the incoming data in a memory and reads it out between 1 and 17ms later. As it is stored, the bit stream is checked for the Frame Alignment Word (FAW) which should occur every millisecond (every 728 bits). If the FAW is missing, then the source of data being read out is switched to a bit stream representing silence, held in ROM (Read Only Memory), before the suspect frame has been read out. When the framing of incoming data has been found again and confirmed, reading of data is switched back to RAM. The effect is a short period of silence, typically 30ms, which for much programme material will be unnoticed. The reframer also checks the 16-frame sequence (defined by the C_0 bit immediately following the FAW), again switching to ROM if necessary. At a discontinuity it also checks for a change between stereo and mono and signals the format change 16 frames in advance as required by the NICAM 728 specification.

For situations where a 17ms delay is considered detrimental, the reframer may be set to a mode in which the maximum delay is 2ms for a Stereo signal and 3ms for a Mono signal; but in this case the 16-frame sequence is not maintained though the structure within each frame is maintained.

2.7 Bit Stream Decoding

Decoding the bit stream is done with an Integrated Circuit developed for use in television receivers, followed by a Digital Oversampling Filter

and other ICs as used in Compact Disc players. The oversampling filter reduces considerably the complexity of the filtering which is needed after D-to-A conversion. It increases the effective sampling rate four-fold, by interpolating between samples, while band-limiting the audio to 15kHz. It also applies $\sin x/x$ correction suitable for the following D-to-A converter. A simple analogue active filter following the ADC suppresses the unwanted lobes around the multiples of 128kHz in the spectrum of the DAC's output, while another filter applies de-emphasis before the output amplifier. Circuitry has been added to extract the Additional Data bits and the CIBs mentioned in connection with the coding process.

2.8 Restoration of Video

Blanking the data in the line sync pulse period is not sufficient to restore the video to normal: apart from the fact that the data encroach on the trailing edge of sync pulses, they also overrun alternate equalising pulses which consequently have been widened from $2.3\mu s$ to about $4.7\mu s$. Composite sync therefore has to be fully regenerated and switched into the video waveform in place of the syncs with sound data. An oscillator, in a phase-locked loop controlled by incoming line sync edges, clocks an FPLS, producing line sync, equalising pulses and broad pulses, while another FPLS selects these in turn to form the correct field sequence. A broad pulse detector ensures that the regenerated field sequence occurs at the same time as the incoming field sequence and triggers a sync amplitude sampling circuit which automatically adjusts the amplitude of regenerated syncs.

2.9 Digital Input and Output, and Synchronisation

Facilities are provided for input of Control and Additional Data and CIBs to a Coder and their output from a Decoder.

Facilities are also provided for input and output of 728 kbit/s bit streams and clocks, so that an externally derived bit stream may be inserted in the sync pulses in a Coder, and/or the internally derived NICAM 728 bit stream may be fed out. The interfaces are to the RS-422 standard. Additionally, there are clock and C_0 inputs and outputs which allow two coders to be synchronised in their bit stream generation and in their insertion of quots into the sync pulses, so that switching a decoder between two coders may be accomplished without the decoder losing lock. (C_0 is a NICAM 728 control bit which is alternately 1 for 8 frames and 0 for 8 frames, thus defining a 16-frame sequence).

Similarly, a decoder provides a 728 kbit/s bit stream output as well as audio outputs, and the option of decoding an external bit stream instead of the bit stream extracted from the sync pulses. An external bitstream, if selected, is passed through the reframer circuitry before being decoded.

Both coder and decoder include built-in digital tone generators which may be selected remotely or by switches behind the front panel. One of these

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tones is selected automatically as a 'fall back' source if the signal being used should fail. The fall-back tone is usually set to silence, especially in the decoder, which uses the fall-back tone in the reframing process.

The Decoders provide a C_0 output as well as clock and data, so increasing the possibility of synchronising various signal sources.

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3. SYSTEM VERSIONS

3.1 Stereo Sound in Sync Module Requirements

All modules are 3913 446 xxxx0 version vxx as follows (except for Audio ADC, which is 3913 466 xxxx0):

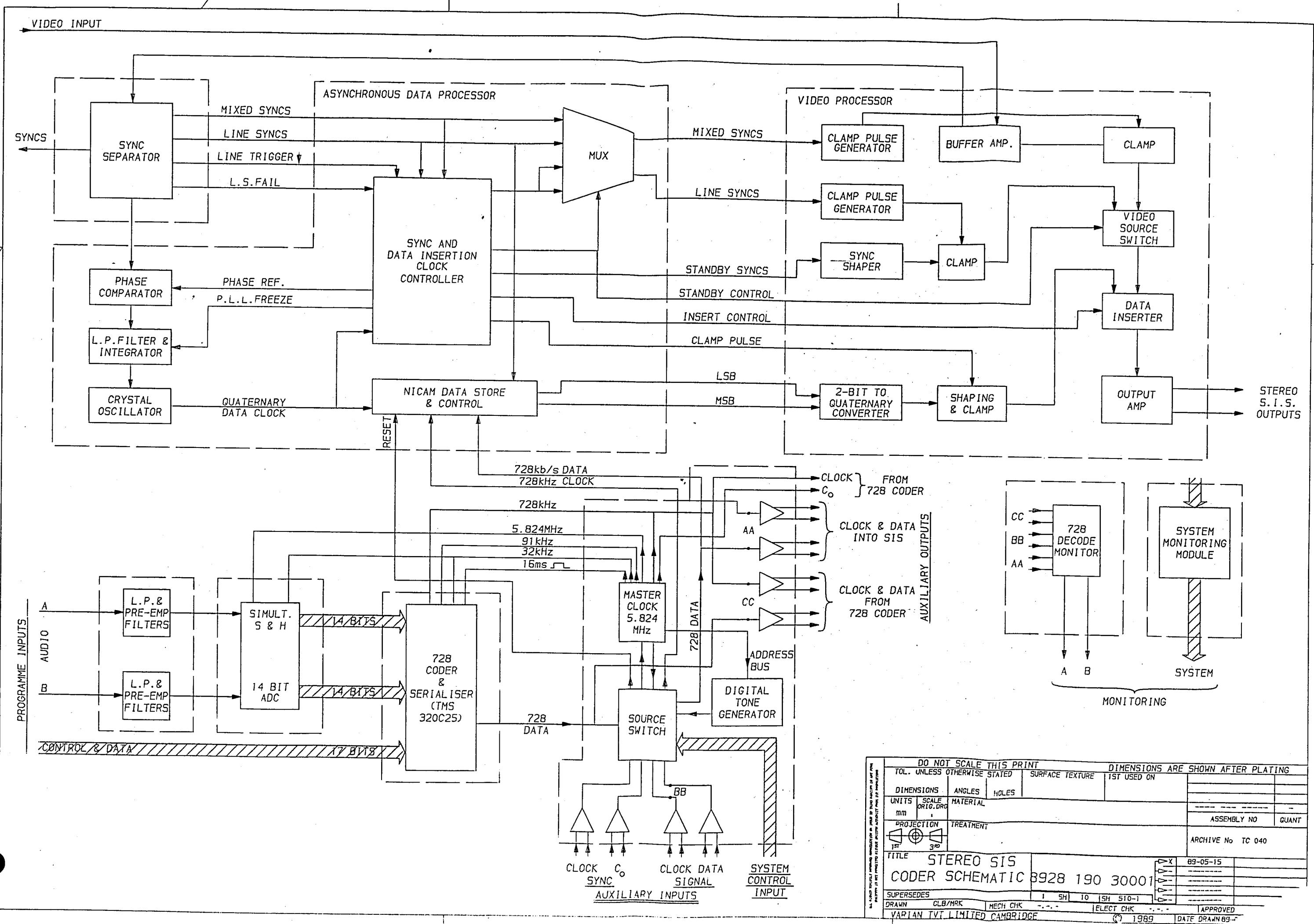
<u>Coder LDM 1903</u>	<u>/12</u>	<u>/14</u>
Power Supply Module	7492	v00
Audio Input Filters	7486	v00
Audio ADC	7890	v00
Digital Signal Processor	7540	v01
Clock and I/O	7541	v01
Audio Decoder	7544	---
Monitor 1	6988	v01
Coder Video Processor	6987	v00
Async Data Processor	6975	v01
Sync Separator PAL	6735	v01
NTSC	6736	---
Rack Frame Assembly	6979	v00

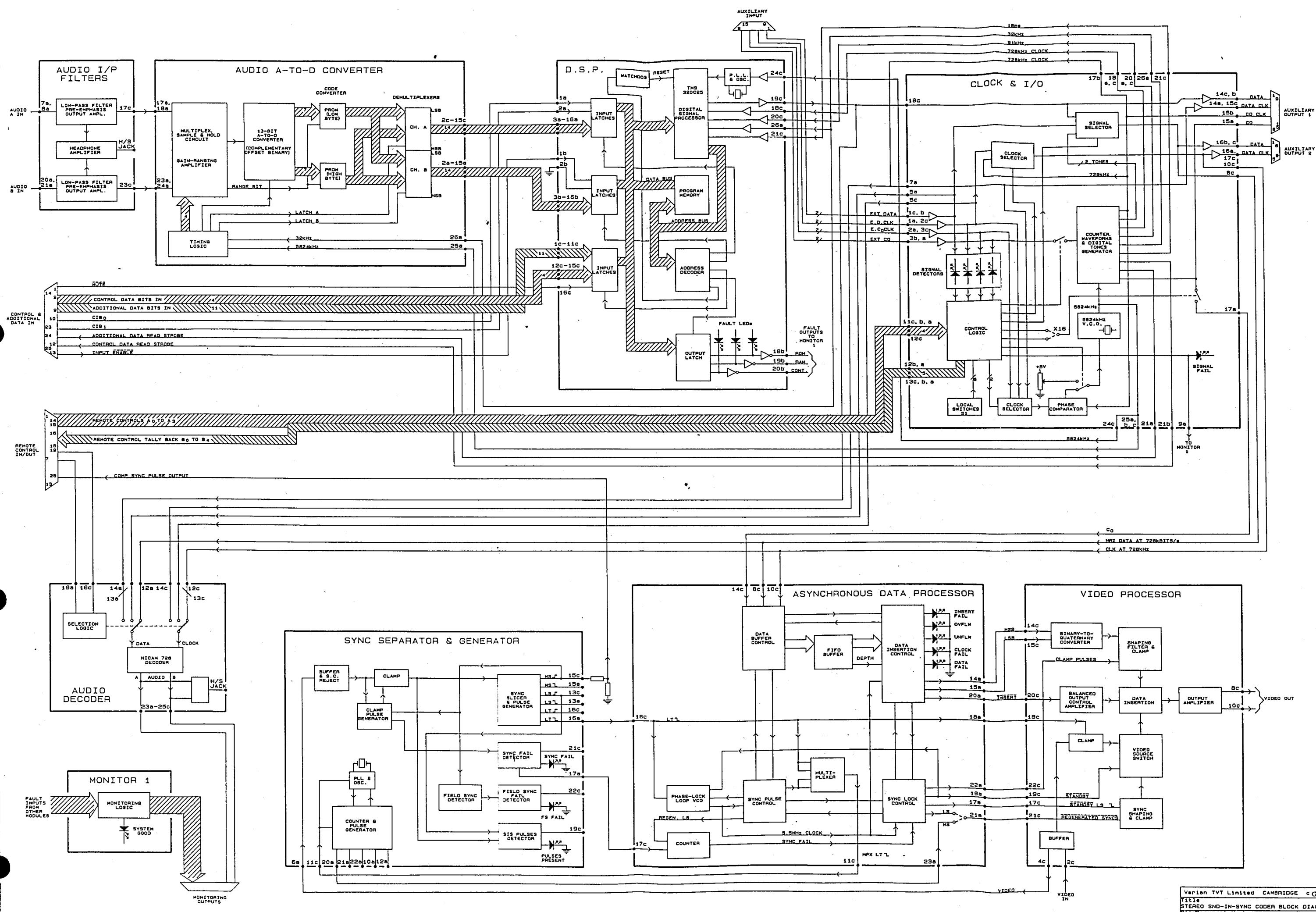
<u>Decoder LDM 1904</u>	<u>/12</u>	<u>---</u>
Power Supply Module	7492	v00
Dec Video Processor PAL	6953	v00
NTSC	6758	---
Sync Sep and Regen PAL	6733	v00
NTSC	6734	---
Quaternary ADC	6976	v01
Data Recovery	6977	v01
Bitstream Regenerator	6760	v02
Monitor 1	6988	v01
Clock and I/O (Reframer)	7549	v00
Audio Decoder	7544	v01
DAC and Transformers	7545	v00
Rack Frame Assembly	6982	v00

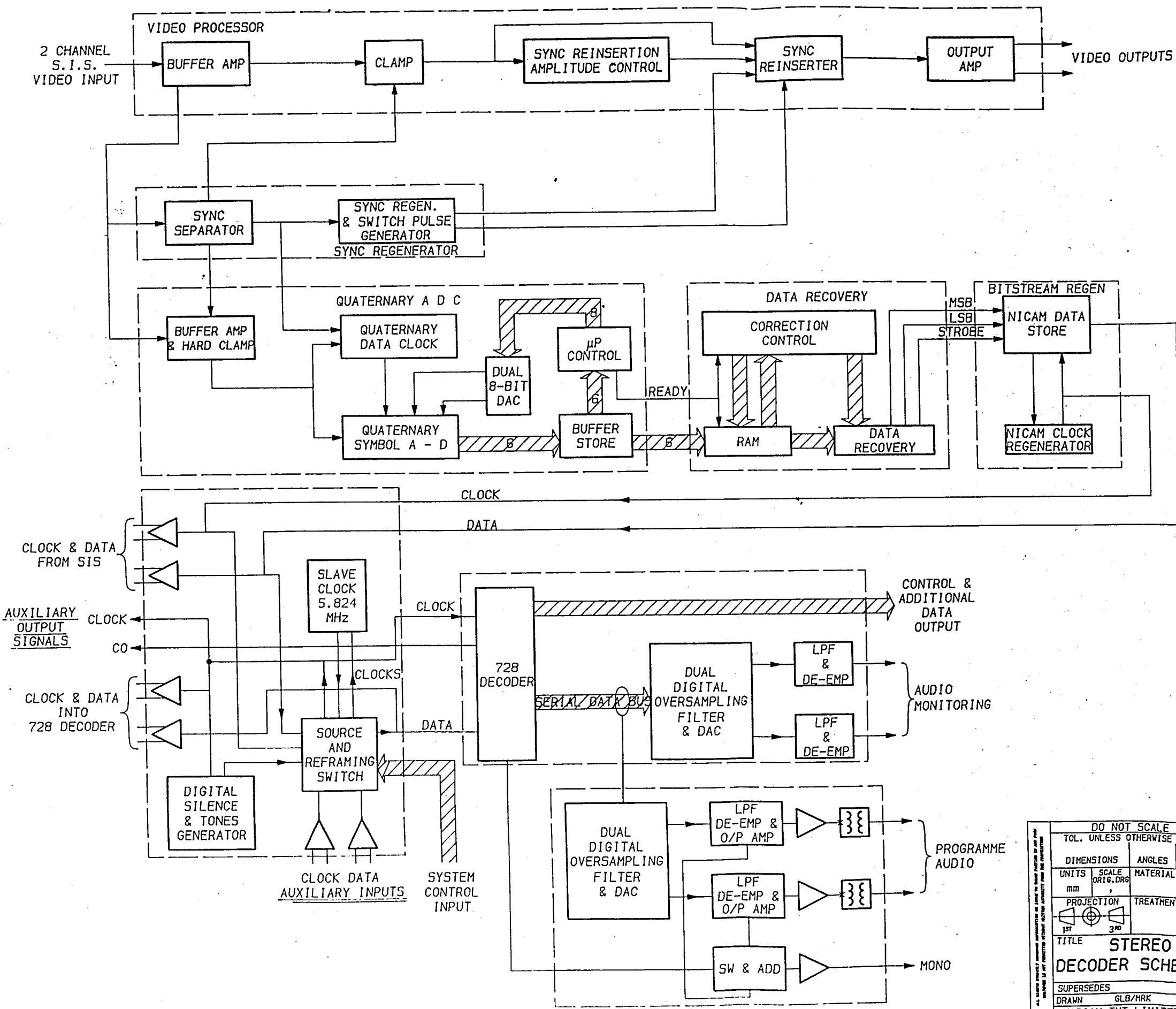
3.2 Version Differences

/12 PAL/625 & NICAM-728, system monitoring
/14 PAL/625 & NICAM-728, system and audio monitoring

/80 Listed Customer Variants
/90 Listed Customer Variants

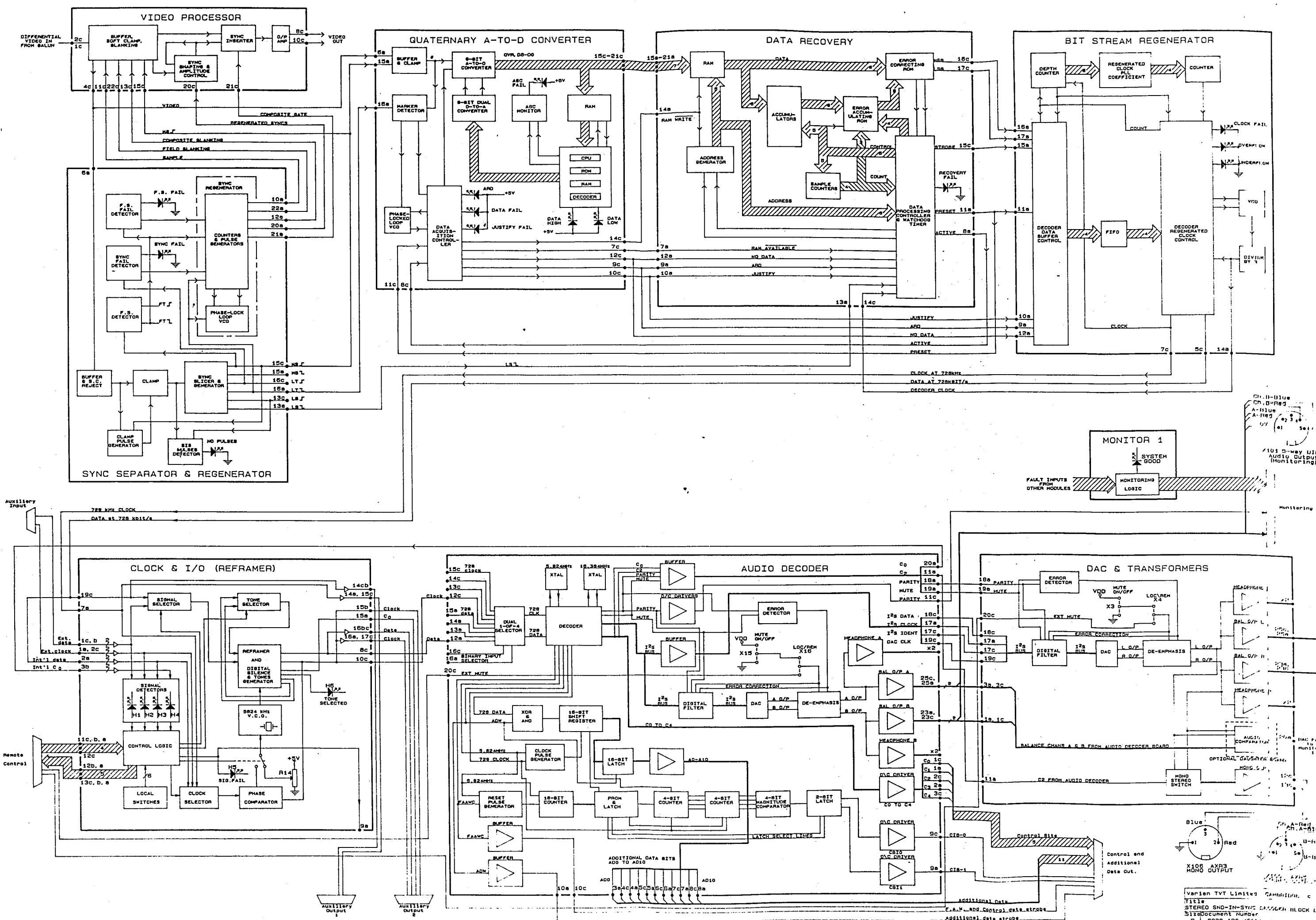






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STEREO SIS		91-01-10				
DECODER SCHEMATIC		--				
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SUPERSEDES		1	SH	10	SH	S10-1
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Decoder Rear Panel Layout	Sh. 512-1

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1. INSTALLATION INSTRUCTIONS

The following procedure should be carried out carefully to ensure safe, efficient and trouble-free operation of the Sound in Sync system.

- (1) Install the equipment in a room that is reasonably dust-free.
- (2) Ensure that there is sufficient space around each unit to allow adequate ventilation. Note that if the equipment is to work in the vicinity of other equipment or a source of heat, the temperature of the air reaching the equipment must be within the upper limit of 45°C.
- (3) Ensure that all equipment and interconnecting cables are undamaged and lay the cables in such a way that there is no risk of them being chafed or otherwise damaged.
- (4) Run a 3-core cable from each unit to the most convenient mains outlet, but leave the mains end disconnected. If the outlet is a circuit breaker switch it off and remove the fuses.
- (5) Check that each unit is fitted with a fuse of the correct rating for the mains supply voltage in use, as designated on the rear panel, adjacent to the fuseholder.
- (6) Ensure that the equipment is effectively earthed via the 3-core mains cable, and that all relevant local regulations are complied with. Note that the green earth terminal on the rear panel of each unit is provided for the convenience of the user and is not intended as the primary means of earthing.

- (7) Connect the earthing link on the rear panel of each unit to provide one of the following selected conditions for the electrical earth (0V) line of the circuit:
- (i) Black to Green: Normal condition of direct connection between Circuit Electrical Earth (0V) and Safety Earth (Dead Earth) ($\overline{\overline{E}}$) of the power supply.
- (ii) Black to White: Indirect connection of Circuit Electrical Earth (0V) through a high-pass filter to Safety Earth ($\overline{\overline{E}}$). This connection is used to eliminate hum induction and other undesirable effects when direct connection is used.
- (iii) Green to White: Circuit Electrical Earth (0V) isolated, with the earthing link serving no electrical function. A circuit configuration used when separate power supply and technical earth lines are available in the system.
- (8) Check that the voltage selector on each unit is set for the mains supply voltage in use.
- (9) Make all connections to the station's control and indicating equipment, in accordance with the interface information in the relevant system manual.
- (10) Connect the equipment to the mains outlet and switch on the mains supply.
- (11) Switch on the equipment, and after allowing a few minutes for it to settle at normal operating temperature, carry out the following initial test:
- (i) If a coder and decoder are available together, feed video and audio at standard level into the encoder and check the video and audio outputs from the decoder.

- (7) Connect the earthing link on the rear panel of each unit to provide one of the following selected conditions for the electrical earth (0V) line of the circuit:
- (i) Black to Green: Normal condition of direct connection between Circuit Electrical Earth (0V) and Safety Earth (Dead Earth) () of the power supply.
- (ii) Black to White: Indirect connection of Circuit Electrical Earth (0V) through a high-pass filter to Safety Earth (). This connection is used to eliminate hum induction and other undesirable effects when direct connection is used.
- (iii) Green to White: Circuit Electrical Earth (0V) isolated, with the earthing link serving no electrical function. A circuit configuration used when separate power supply and technical earth lines are available in the system.
- (8) Check that the voltage selector on each unit is set for the mains supply voltage in use.
- (9) Make all connections to the station's control and indicating equipment, in accordance with the interface information in the relevant system manual.
- (10) Connect the equipment to the mains outlet and switch on the mains supply.
- (11) Switch on the equipment, and after allowing a few minutes for it to settle at normal operating temperature, carry out the following initial test:
- (i) If a coder and decoder are available together, feed video and audio at standard level into the encoder and check the video and audio outputs from the decoder.

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- (ii) If the coder alone is available, feed video and audio in at standard level and monitor the SIS output to verify that quaternary digits are inserted in the line sync period.

2. SAFETY

Some components are designated by this component safety symbol  , either on the parts list or the circuit diagram, or both. Refer to the relevant service manual (see Information Finder).

If any designated component has to be replaced, it must, for safety reasons, be replaced only by a component of the type specified and the wiring to and from the fuseholder and voltage adaptor must be double-insulated.

3. CONNECTIONS

- Notes:
1. Connector types refer to connectors installed on rear panel.
 2. All open collector outputs are rated for 50V/500mA individual maximum. Advised individual limit is 50V/60mA, based on a conservative assessment of IC package rating.
 3. All relay contacts are rated for 125V/2A maximum.
 4. All +5V logic inputs are pulled up to +5V and protected with series resistors.
 5. Rear panel connections for monitoring are detailed in Part 4.

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3.1 Coder

3.1.1 Video

Loop-through input for 1V p-p composite video. If the loop-through facility is not required the feed must be terminated at the unused socket with 75 ohms.

3.1.2 SIS

Two Sound-in-Sync 75-ohm outputs are provided for sending to Sound in Sync Decoders. Correct level is obtained when the outputs are terminated with 75 ohms.

Sound-in-Sync is produced by inserting pulses into the line sync pulses of the incoming video signal. If for any reason this is not present, pulses are inserted into the internally generated standby sync. This may be either line sync or composite (mixed) sync, selection being made by setting Link X18 on the Asynchronous Data Processor module to LS or MS, respectively.

3.1.3 Audio Connections

Audio Input	
Pin 1	Ground
Pin 2	Channel A (Red)
Pin 3	Channel A (Blue)
Pin 4	Channel B (Red)
Pin 5	Channel B (Blue)

3.1.4 Auxiliary Input

An external 728 kbits/s NICAM-728 bitstream, with its accompanying clock, can be input here for insertion into video. Also a C_0 signal, with its accompanying clock, can be input here for synchronising the coder. The inputs accept RS-422 balanced 5V signals; each input also has a +1.5V bias, which, if connected to an RS-422 inverse input, allows the corresponding true input to accept a TTL-level input signal.

15-way D-type plug

Pin No.	Function
1	728 kbits/s data in (RS-422 true)
9	728 kbits/s data in (RS-422 inverse)
2	+1.5V bias out
10	0V
3	728 kHz data clock in (RS-422 true)
11	728 kHz data clock in (RS-422 inverse)
4	+1.5V bias out
12	0V
5	C_0 in (RS-422 true)
13	C_0 in (RS-422 inverse)
6	+1.5V bias out
14	0V
7	C_0 clock in (RS-422 true)
15	C_0 clock in (RS-422 inverse)
8	+1.5V bias out

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3.1.5 Auxiliary Output 1

A 728 kbits/s NICAM-728 bitstream from the internal NICAM coder, with its accompanying clock, is output here. A C_0 signal, synchronised to the NICAM-728 bitstream, with its accompanying clock, is also output here. The data and data clock are in RS-422 balanced 5V format; the C_0 and C_0 clock are 5V HCMOS logic signals, each with a +1.5V bias to allow a one-to-one connection between this output and a coder auxiliary input.

15-way D-type socket

Pin No.	Function
1	728 kbits/s data out (RS-422 true)
9	728 kbits/s data out (RS-422 inverse)
2	Not connected
10	0V
3	728 kHz data clock out (RS-422 true)
11	728 kHz data clock out (RS-422 inverse)
4	Not connected
12	0V
5	C_0 out (+5V HCMOS)
13	+1.5V bias out
6	Not connected
14	0V
7	C_0 clock out (+5V HCMOS)
15	+1.5V bias out
8	Not connected

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3.1.6 Auxiliary Output 2

The 728 kbits/s NICAM-728 bitstream that is inserted into the video, with its accompanying clock, is output here. The data and data clock are in RS-422 balanced 5V format. This output may be directly connected to the top 9 pins of a coder auxiliary input, or a one-to-one connection made to a decoder auxiliary input.

9-way D-type socket

Pin No.	Function
1	728 kbits/s data out (RS-422 true)
6	728 kbits/s data out (RS-422 inverse)
2	Not connected
7	0V
3	728 kHz data clock out (RS-422 true)
8	728 kHz data clock out (RS-422 inverse)
4	Not connected
9	0V
5	Not connected

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3.1.7 Remote Control

3.1.7.1 Clock and I/O Control

When the Clock and I/O module is in Remote mode, the input lines A3, A2, A1, and A0 become effective for remotely controlling signal selection and lock mode. They may be either 5V logic or pull-downs to indicate a zero and open circuit to indicate a 1.

(i) Locking and Remote/Local

A3 A2

- | | |
|--------|-----------------------------------------------------------------------------------------------------------|
| 1 1 | Local control (overrides 'Remote' selected locally). |
| 1 0 | Free-running. |
| 0 1 | Locked to External Data Clock. If it fails, falls back to free-running; Signal Fail indicated. |
| 0 0 | Locked to Ext C_0 clock and C_0 . If either fails, falls back to free-running; Signal Fail indicated. |

(ii) Signal Selection to Asynchronous Data Processor for Insertion in Sync Pulses

A1 A0

- | | |
|--------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 1 | Bitstream generated from analogue audio inputs. |
| 1 0 | External Data and Clock. If data fails, falls back to Tone 2; Signal Fail indicated. If Clock fails, uses internal clock; Signal Fail indicated. |
| 0 1 | Tone 1. |
| 0 0 | Tone 2. |

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(iii) Tally-backs

The open-collector tally-back outputs B0 to B3 follow coding of A0 to A3, indicating fall-back conditions due to signal failure when relevant, rather than requested conditions. If Local Control is selected, either locally or remotely, B3 and B2 are 1, to indicate 'local' and they do not indicate the lock condition selected. B4 is a remote Signal Fail indication.

3.1.7.2 Audio Decoder Control Inputs

The two Select inputs select the bitstream source for monitor decoding as follows:

S1	S0	
1	1	Data to be inserted in video.
1	0	External data.
0	1	Data from internal NICAM coder.
0	0	Not used.

3.1.7.3 Mute Control

The active low MUTE signal acts to mute the audio output of the Audio Decoder.

3.1.7.4 Auxiliary Power

+5V at 100mA maximum for powering external remote control equipment.

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3.1.7.5 Composite Sync Output

A composite sync output, 1V across 75 ohms.

25-way D-type socket

Pin No.	Function
1	A0 remote control input (+5V logic)
14	A1 remote control input (+5V logic)
2	A2 remote control input (+5V logic)
15	A3 remote control input (+5V logic)
3	0V
16	B0 tally-back output (open collector)
4	B1 tally-back output (open collector)
17	B2 tally-back output (open collector)
5	B3 tally-back output (open collector)
18	B4 tally-back output (open collector)
6	0V
19	Audio Decoder Select 0 input (+5V logic)
7	Audio Decoder Select 1 input (+5V logic)
20	0V
8	Audio Decoder MUTE input (+5V logic)
21	0V
9	Not connected
22	Not connected
10	Not connected
23	Not connected
11	0V
24	+5V/100mA max auxiliary power output
12	0V
25	Composite Sync output (2V unloaded/1V across 75R)
13	0V

3.1.8 Control and Additional Data In

All the inputs may be 5V logic or pull-downs to indicate a zero and open circuit to indicate a 1. The Control, Additional and Nordic data bits are only read if input ENABLE is low; MUTE is unaffected by input ENABLE. Additional and Nordic data must be stable when the Additional Data Read Strobe is low; Control data must be stable when the Control Data Read Strobe is low.

25-way D-type plug

Pin No.	Function
1	MUTE in (+5V logic)
14	0V
2	C ₁ control data bit in (+5V logic)
15	C ₂ control data bit in (+5V logic)
3	C ₃ control data bit in (+5V logic)
16	C ₄ control data bit in (+5V logic)
4	AD ₀ additional data bit in (+5V logic)
17	AD ₁ additional data bit in (+5V logic)
5	AD ₂ additional data bit in (+5V logic)
18	AD ₃ additional data bit in (+5V logic)
6	AD ₄ additional data bit in (+5V logic)
19	AD ₅ additional data bit in (+5V logic)
7	AD ₆ additional data bit in (+5V logic)
20	AD ₇ additional data bit in (+5V logic)
8	AD ₈ additional data bit in (+5V logic)
21	AD ₉ additional data bit in (+5V logic)
9	AD ₁₀ additional data bit in (+5V logic)
22	0V
10	CIB ₀ Nordic data bit in (+5V logic)
23	CIB ₁ Nordic data bit in (+5V logic)
11	0V
24	Additional Data Read Strobe out (open collector)
12	Control Data Read Strobe out (open collector)
25	0V
13	Input ENABLE in (+5V logic)

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3.2 Decoder

3.2.1 SIS

Loop-through input for 1V p-p composite sound-in-sync video. If the loop-through facility is not required the feed must be terminated at the unused socket with 75 ohms.

3.2.2 Video

Two 75 ohm video outputs are provided. Correct level is obtained when the outputs are terminated with 75 ohms.

3.2.3 Audio Connections

Audio Output (Stereo and Monitoring)	
Pin 1	Ground
Pin 2	Channel A (Red)
Pin 3	Channel A (Blue)
Pin 4	Channel B (Red)
Pin 5	Channel B (Blue)

Audio Output (Mono)	
Pin 1	Ground
Pin 2	Red
Pin 3	Blue

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3.2.4 Auxiliary Input

An external 728 kbits/s NICAM-728 bitstream, with its accompanying clock, can be input here for decoding by the internal NICAM decoder. The inputs accept RS-422 balanced 5V signals; each input also has a +1.5V bias, which, if connected to an RS-422 inverse input, allows the corresponding true input to accept a TTL-level input signal.

9-way D-type plug

Pin No.	Function
1	728 kbits/s data in (RS-422 true)
6	728 kbits/s data in (RS-422 inverse)
2	+1.5V bias out
7	0V
3	728 kHz data clock in (RS-422 true)
8	728 kHz data clock in (RS-422 inverse)
4	+1.5V bias out
9	0V
5	Not connected

3.2.5 Auxiliary Output 1

A 728 kbits/s NICAM-728 bitstream extracted from the SIS video, with its accompanying clock, is output here. The data and data clock are in RS-422 balanced 5V format. This output may be directly connected to the top 9 pins of a coder auxiliary input, or a one-to-one connection made to a decoder auxiliary input.

9-way D-type socket

Pin No.	Function
1	728 kbits/s data out (RS-422 true)
6	728 kbits/s data out (RS-422 inverse)
2	Not connected
7	0V
3	728 kHz data clock out (RS-422 true)
8	728 kHz data clock out (RS-422 inverse)
4	Not connected
9	0V
5	Not connected

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3.2.6 Auxiliary Output 2

The 728 kbits/s NICAM-728 bitstream that is fed to the internal NICAM decoder, with its accompanying clock, is output here. A C_0 signal, synchronised to the NICAM-728 bitstream, with its accompanying clock, is also output here. The data and data clock are in RS-422 balanced 5V format; the C_0 and C_0 clock are 5V HCMOS logic signals, each with a +1.5V bias to allow a one-to-one connection between this output and a coder auxiliary input.

15-way D-type socket

Pin No.	Function
1	728 kbits/s data out (RS-422 true)
9	728 kbits/s data out (RS-422 inverse)
2	Not connected
10	0V
3	728 kHz data clock out (RS-422 true)
11	728 kHz data clock out (RS-422 inverse)
4	Not connected
12	0V
5	C_0 out (+5V HCMOS)
13	+1.5V bias out
6	Not connected
14	0V
7	C_0 clock out (+5V HCMOS)
15	+1.5V bias out
8	Not connected

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3.2.7 Remote Control

3.2.7.1 Clock and I/O (Reframer) Control

When the Clock and I/O (Reframer) module is in Remote mode, the input lines A3, A2, A1, and A0 become effective for remotely controlling signal selection and lock mode. They may be 5V logic or pull-downs to indicate a zero and open circuit to indicate a 1.

(i) Locking and Remote/Local

While Tone 1 or Tone 2 is selected, the local oscillator is locked or free-running as follows:

A3 A2

- | | | |
|---|---|-------------------------------------------------------------------------------------------------------|
| 1 | 1 | Local control of signal selection and lock mode (overrides 'Remote' selected locally). |
| 1 | 0 | Locked to Clock regenerated from SIS. If data from SIS fails, free running; Signal Fail is indicated. |
| 0 | 1 | Locked to Ext Clock. If Ext Clock fails, free running; and Signal Fail indicated. |
| 0 | 0 | Free running. |

(ii) Remote Signal Selection

This depends upon control lines A1 and A0 as follows:

A1 A0

- | | | |
|---|---|-------------------------------------------------------------|
| 1 | 1 | From SIS. If data fails, Tone 2; and Signal Fail indicated. |
| 1 | 0 | Ext data. If data fails, Tone 2; and Signal Fail indicated. |
| 0 | 1 | Tone 1. |
| 0 | 0 | Tone 2. |

(iii) Tally-backs

The open-collector tally-back outputs B0 to B3 follow coding of A0 to A3, indicating fall-back conditions due to signal failure when relevant, rather than requested conditions. If Local Control is selected either locally or remotely B3 and B2 are 1, to indicate 'Local' and they do not indicate the Lock condition selected. B4 is a remote Signal Fail indication.

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3.2.7.2 Mute Controls

The appropriate active low MUTE signals to mute the audio outputs of the Audio Decoder and DAC and Transformer modules.

3.2.7.3 Auxiliary Power

+5V at 100mA maximum for powering external remote control equipment.

3.2.7.4 Composite Sync Output

A composite sync output of 1V across 75 ohms.

25-way D-type socket

Pin No.	Function
1	A0 remote control input (+5V logic)
14	A1 remote control input (+5V logic)
2	A2 remote control input (+5V logic)
15	A3 remote control input (+5V logic)
3	OV
16	B0 tally-back output (open collector)
4	B1 tally-back output (open collector)
17	B2 tally-back output (open collector)
5	B3 tally-back output (open collector)
18	B4 tally-back output (open collector)
6	OV
19	Not connected
7	Not connected
20	OV
8	Audio Decoder <u>MUTE</u> input(+5V logic)
21	OV
9	DAC and Transformers <u>MUTE</u> input (+5V logic)
22	OV
10	Not connected
23	Not connected
11	OV
24	+5V/100mA max auxiliary power output
12	OV
25	Composite Sync output (2V unloaded/1V across 75R)
13	OV

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3.2.8 Control and Additional Data Out

All the outputs are open collector. Additional Data and Nordic Data change when the Additional Data Write strobe is low; Control Data changes when the Control Data Read strobe is low.

25-way D-type socket

Pin No.	Function
1	0V
2	C ₀ control data bit out (open collector)
3	C ₁ control data bit out (open collector)
4	C ₂ control data bit out (open collector)
5	C ₃ control data bit out (open collector)
6	C ₄ control data bit out (open collector)
7	AD ₀ additional data bit out (open collector)
8	AD ₁ additional data bit out (open collector)
9	AD ₂ additional data bit out (open collector)
10	AD ₃ additional data bit out (open collector)
11	AD ₄ additional data bit out (open collector)
12	AD ₅ additional data bit out (open collector)
13	AD ₆ additional data bit out (open collector)
14	AD ₇ additional data bit out (open collector)
15	AD ₈ additional data bit out (open collector)
16	AD ₉ additional data bit out (open collector)
17	AD ₁₀ additional data bit out (open collector)
18	0V
19	CIB ₀ Nordic data bit out (open collector)
20	CIB ₁ Nordic data bit out (open collector)
21	0V
22	Additional Data Write Strobe out (open collector)
23	Control Data Write Strobe out (open collector)
24	0V
25	0V

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4. LINK-SELECTABLE USER OPTIONS

4.1 Coder

4.1.1 Synchronisation of External Data and C₀

The External Data and External C₀ inputs at the Auxiliary Input have separate associated input clocks, which may be either synchronous or asynchronous. The extent to which a Coder can be synchronised to these external references depends, in some cases, upon whether these two clocks are synchronous or not. The link X16 on the Clock & I/O module needs to be set to 'A' (asynchronous) or 'S' (synchronous) accordingly. If in doubt, the safe position is 'A'. A fuller explanation is given in the section for the module in the associated Coder handbook (see Information Finder).

4.1.2 Tone 2

There are four sources of sound data for insertion into the sync pulses:

- (a) Data generated from analogue audio inputs.
- (b) External Data at the Auxiliary Input.
- (c) Tone 1; internal digitally generated line-up tone.
- (d) Tone 2; internal digitally generated link-selectable tone.

Any one of the four sources can be selected either remotely or by switches accessible behind the front panel. Tone 2 is also a fall-back tone, selected automatically if the External Data, when selected, should fail. Tone 2 itself is link-selectable from a choice of 10 tones/sounds; the link used is X18 on the Clock & I/O module, which has positions labeled 'A' to 'J'. The following table and notes give details of the tones available:

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	C_{1-4}	AD_{0-10}	CIBs	Ch A/Mono 1/Left	Ch B/M2/Right
Tone 1	0001	00000000000	00	1kHz, 0dBu	1kHz, 0dBu
Tone 2A	0001	00000000000	00	Silence	Silence
B	0000	00000000000	00	1kHz, -20dBu	2kHz, -20dBu
C	0000	10000000000	00	62.5Hz, 0dBu	125Hz, 0dBu
D	0000	01000000000	00	250Hz, 0dBu	375Hz, 0dBu
E	0000	00100000000	00	375Hz, 0dBu	500Hz, 0dBu
F	0000	00010000000	00	250Hz, 0dBu	312.5Hz, 0dBu
G	0000	00001000000	00	250Hz, -3dBu 312.5Hz, -3dBu	937.5Hz, 0dBu 312.5Hz, -3dBu
H	0000	00000100000	00	312.5Hz, 0dBu 375Hz, -3dBu	500Hz, 0dBu 375Hz, -3dBu
I	0000	00000010000	00	625 Hz, 0dBu 750 Hz, -3dBu	937.5Hz, 0dBu 750Hz, -3dBu
J	0000	00000001000	00	Multitone	Multitone

Notes 1. Application Control bits C_{1-3} have the following significance:

$C_1 \ C_2 \ C_3$

0 0 0 Stereo signal comprising alternate A-channel and B-channel samples.

0 1 0 Two independent mono sound signals (designated M1 and M2) transmitted in alternate frames.

1 0 0 One mono signal and one 352 kbit/s transparent data channel transmitted in alternate frames. (Not valid for this equipment unless coded externally.)

1 1 0 One 704 kbit/s transparent data channel. (Not valid for this equipment unless coded externally.)

2. Application Control bit C_4 is the Reserve Sound Switching Flag, set to '1' to signal to a receiver that the digital sound signal is the same programme as the FM signal, but to a '0' if the signals are different. This enables a receiver to decide whether to switch to FM sound if the digital sound should fail, or intermediate broadcaster's equipment to decide whether to mute the digital sound and/or switch to an alternative source if the digital signal is a test signal rather than programme. (See 4.1.5 below). For this reason Tone 2 which is the fall-back tone has C_4 set to '0' in all cases except 2A which is silence.
3. Levels in the table assume equipment set up to the UK NICAM 728 audio headroom specification, i.e. 14.8dB for a 0dBu signal at 2kHz.
4. Tone 1 is intended as a line-up tone.
5. Tone 2 is intended as a fall-back tone to indicate a fault condition, or as an alternative test tone.
6. The choice of tone 2 from the ten available is made by a moveable link (X18) on the Clock & I/O module.
7. Eight of the 11 tones can be identified by the Additional Data bits AD_{0-10} , and all are chosen to be identified audibly, as follows:

Tone 1 is the only tone having the same single frequency on left and right channels.

Tone 2A is silence.

Tone 2B is the only tone at -20dBu.

Tone 2C has left : right frequency ratio of 1 : 2 (musically an octave).

Tone 2D has left : right frequency ratio of 2 : 3 (musically a fifth).

Tone 2E has left : right frequency ratio of 3 : 4 (musically a fourth).

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Tone 2F has left : right frequency ratio of
4 : 5 (musically a major third).

Tone 2G is three tones, musically a major triad, lowest note on the left, highest on the right and middle note in the centre.

Tone 2H - as 2G but first inversion of the major triad.

Tone 2I - as 2G but a minor triad.

Tone 2J is the only multitone.

- 8 Tones 2B to 2I all have left channel lower pitch than right channel, giving an easy means to check that left and right are routed correctly.
9. The multitone gives a means of checking the frequency response from a single test signal by using a spectrum analyser. It consists of 16 tones, each at -12.04dBu, giving a combined amplitude of 0dBu. The frequencies are spaced approximately evenly on a logarithmic scale and are (in Hz) 62.5, 125, 187.5, 250, 375, 562.5, 812.5, 1125, 1562.5, 2187.5, 3000, 4125, 5687.5, 7812.5, 10687.5, 14500.
10. By negotiation with Varian TVT Limited, alternative frequencies can be supplied with the following limitations:
 - Tone 1, Tone 2A and Tone 2B must be 1kHz or multiples thereof either singly or in combination.
 - Tones 2C to 2J must be 62.5Hz or multiples thereof, either singly or in combination.
 - Amplitude levels cannot exceed those set by the NICAM 728 specification.

4.1.3 System Good in Terminal Mode

X9 on the Monitor 1 module controls whether 'System Good' indication is allowed ('A'), or not allowed ('N') when Monitor 1 is operating in Terminal Mode. For normal operation X9 has no effect.

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4.1.4 Language Selection
 During Dual-language Transmissions

X17 and X18 on the Audio Decoder module allow the user to select either or both languages during dual Monophonic broadcasts, according to the following table.

LINKS		OUTPUTS	
X17	X18	Left	Right
b-c	b-c	M1	M1
a-b	b-c	M1	M2
b-c	a-b	M2	M1
a-b	a-b	M2	M2

4.1.5 Response to Reserve Sound Switching Flag

In the NICAM 728 data stream, Application Control Bit 4 (C_4) indicates whether the FM mono broadcast and the stereo broadcasts are transmitting the same material. If this bit is logic 0, indicating that the broadcasts are different, while X4 on the Audio Decoder module is in its normal position (b-c), the decoder IC will mute; but if X4 is in Position a-b, the decoder will not mute, allowing test transmissions to be monitored.

4.1.6 Mute Enable

With X3 on the Audio Decoder module in its normal position (b-c), the decoder IC will mute when greater than 1 in 100 parity errors are detected, and unmute when the parity error rate drops below 1 in 400. Under test or experimental conditions, it may be useful to disable this mute function by setting X3 to Position a-b.

4.1.7 Line Sync or Composite Sync on Standby

Standby Sync can be selected to be Line Sync only or Composite (Mixed) Sync by setting X18 on the Asynchronous Data Processor module to 'LS' or 'MS' respectively.

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4.2 Decoder

4.2.1 System Good in Terminal Mode

X9 on the Monitor 1 module controls whether a 'System Good' indication is allowed ('A'), or not allowed ('N') when Monitor 1 is operating in Terminal Mode. For normal operation X9 has no effect.

4.2.2 Tones 1 and 2

4.2.2.1 Sources of Sound Data

There are four sources of sound data for decoding:

- (a) Data extracted from the SIS input.
- (b) External Data at the Auxiliary Input.
- (c) Tone 1: internal digitally generated tone, normally a line-up tone.
- (d) Tone 2: internal digitally generated 'tone', normally silence.

Any one of the four sources can be selected remotely or by switches accessible behind the front panel. Tone 1 and Tone 2 are both link-selectable from a choice of eight tones/sounds/silence, listed below. As well as being selected deliberately, Tone 2 is the fall-back tone, selected automatically if either the SIS Data or the External Data, when selected, should fail, or when the Reframer circuitry detects a discontinuity in the incoming bit-stream. Tone 2 should therefore normally be silence; though another tone could be chosen for test purposes, e.g. to make the reframing deliberately audible.

Tone 1 and Tone 2 are selected at X12 on the Clock and I/O (Reframer) module, from the following:

Tone A:	Stereo and Mono: Left and Right:	$C_4=0$, $AD_{0-10}=0$, CIBs=0. 1kHz, 0dBu (UK headroom).
Tone B:	Stereo and Mono: Left and Right:	$C_4=0$, $AD_{0-10}=0$, CIBs=0. 1kHz, 0dBu (EBU headroom).
Tone C:	Stereo and Mono: Left and Right:	$C_4=0$, $AD_{0-10}=0$, CIBs=0. 1kHz, -3dBu (UK headroom)

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Tone D:	Stereo: Left : Right:	$C_4=0$, $AD_{0-10}=0$, CIBs=0. 750Hz, 0dBu (UK headroom). 1250Hz, 0dBu (UK headroom).
	Mono: M1: M2:	$C_4=0$, $AD_{0-10}=0$, CIBs=0. 250Hz, 0dBu (UK headroom). 1750Hz, 0dBu (UK headroom).
Tone E:	Stereo and Mono: Left and Right:	$C_4=0$, $AD_{0-10}=0$, CIBs=0. Multitone, 0dBu (UK headroom).
Tone F:	Stereo and Mono: Left and Right:	$C_4=0$, $AD_{0-10}=0$, CIBs=0. Multitone, 0dBu (EBU headroom).
Tone G:	Stereo and Mono: Left and Right:	$C_4=1$, $AD_{0-10}=1$, CIBs=0. Silence.
Tone H:	Stereo and Mono: Left and Right:	$C_4=1$, $AD_{0-10}=0$, CIBs=0. Silence.

4.2.2.2 Stereo and Mono Format of Tones

Stereo or Mono format of tones is normally selected automatically according to the format of the last-used incoming bit-stream; hence, tone D can be used for audible identification of the format of an incoming signal, or identification of left and right or M1 and M2. However, X11 link on the Clock and I/O (Reframer) module may be set for Mono or Stereo for test purposes, but should always be in position 'N' for normal operation, otherwise an improperly signalled format change could occur during reframing.

Except for silence, C_4 is set to 0, so that test tones may be monitored on one piece of equipment whilst muted on another, and so not pass on into the FM sound, for example.

Tones E and F can be used for checking the frequency response of a decoder using a spectrum analyser. Each multitone is composed of 10 components, each at -10dBu, making a combined level of 0dBu. The frequencies are spaced approximately evenly on a logarithmic scale and are (in Hertz):

250, 500, 750, 1250, 1750, 2500, 3750, 6000, 9250, 14 500.

The different Additional Data bits in tones G and H could be used to identify which of two reframers in a signal path is reframing or has fallen back to Tone 2 due to loss of signal.

Tones D, E and F repeat every 4 frames (except for C_0). The other tones are frame-repetitive (except for C_0).

By negotiation with Varian TVT Limited, alternative signals can be supplied with the limitations that all signal components must be multiples of 250Hz and amplitude levels cannot exceed those set by the NICAM 728 specification.

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4.2.3 Reframing Mode

The Reframer circuitry has two modes of operation:

- (a) FULL reframing, in which the 16-frame sequence is maintained, and the data may be delayed for up to 17ms.
- (b) MINimum delay reframing, in which the maximum delay of data is 2ms for a Stereo Signal, or 3ms for a Mono signal, but the 16-frame sequence is not maintained.

FULL or MIN mode is selected by two moveable links, X24 and X25 on the Clock and I/O (Reframer) module.

4.2.4 Language Selection During Dual-language Transmissions

X17 and X18 on the Audio Decoder module allow the user to select either or both languages during dual Monophonic broadcasts, according to the following table:

LINKS		OUTPUTS	
X17	X18	Left	Right
b-c	b-c	M1	M1
a-b	b-c	M1	M2
b-c	a-b	M2	M1
a-b	a-b	M2	M2

4.2.5 Response to Reserve Sound Switching Flag

In the NICAM 728 data stream, control bit 4 (C4) indicates whether the FM mono broadcast and the stereo broadcasts are transmitting the same material. If this bit is logic 0, indicating that the broadcasts are different, while X4 on the Audio Decoder module is in its normal position (b-c), the decoder IC will mute; but if X4 is in Position a-b, the decoder will not mute, allowing test transmissions to be monitored.

4.2.6 Mute Enable

With X3 on the Audio Decoder module in its normal position (b-c), the decoder IC will mute when greater than 1 in 100 parity errors are detected, and unmute when the parity error rate drops below 1 in 400. Under test or experimental conditions, it may be useful to disable this mute function by setting X3 to Position a-b.

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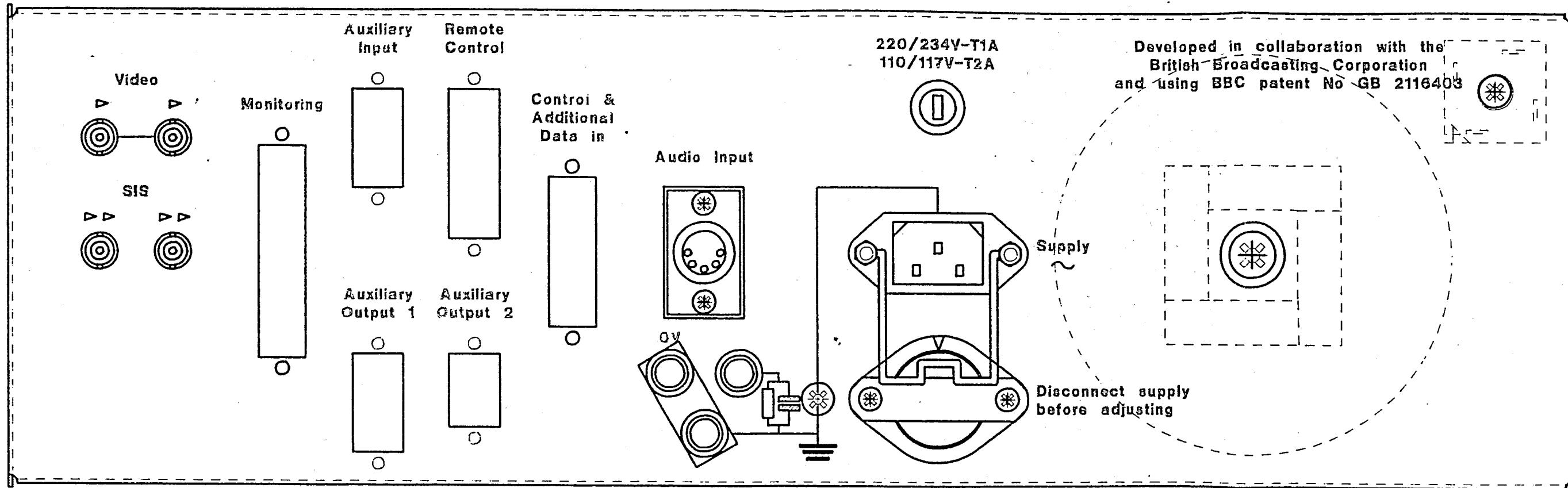
4.2.7 Overriding Mute (Audio Decoder Module)

With X16 on the Audio Decoder module in Position b-c, the audio may be muted remotely by 0V applied to Pin 8 of the Remote Control Connector on the rear panel. With X16 in Position a-b, this mute is controlled by X15: Position a-b to mute; b-c to unmute.

4.2.8 Overriding Mute (DAC and Transformers Module)

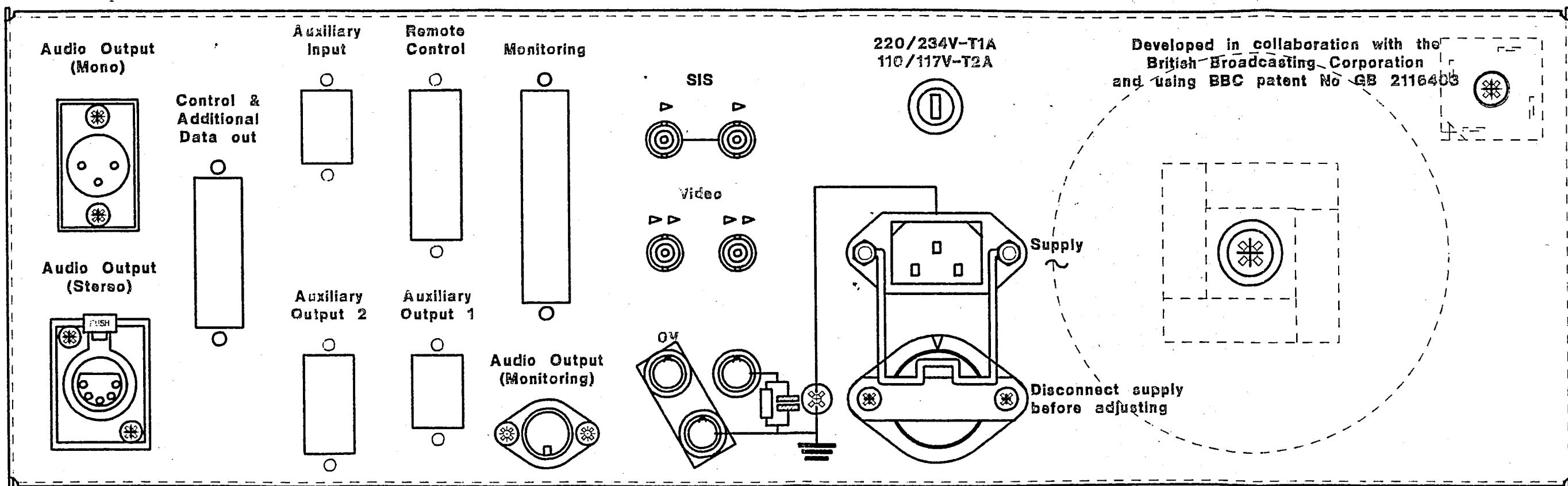
With X4 on the DAC and Transformers module in Position a-b, the audio may be muted by setting X3 to Position a-b, or unmuted by setting X3 to Position b-c.

With X4 on the DAC and Transformer module in Position b-c, the audio may be muted remotely by 0V applied to Pin 9 of the Remote Control Connector on the rear panel. By applying C₄ from the Control and Additional Data Output connector on the back panel to this remote mute input, the outputs of the DAC and Transformers module (stereo and mono) can be made to mute when a test tone (or fall-back tone) is selected (at the Coder or Decoder) while the test or fall-back tone is audible locally from the Audio Decoder module. (See Para. 4.2.2 and 4.2.5 above).



TITLE		REAR PANEL LAYOUT			
STEREO SOUND IN SYNC CODER		8928 190 30001		89-11-29	
ARCHIVE No		1	5H	10	5H 512-1
PAWN		N.BROWN	MECH CHY	ELECT CHK	APPROVED
ARIAN I.V.T. LIMITED CAMBRIDGE				O 1989	DATE DRAWN 89-11-29 FORM A3

D190_30001S1



TITLE		REAR PANEL LAYOUT					
STEREO SOUND IN SYNC DECODER		8928 190 40001					
ARCHIVE NO.		1	CH	1C	SH	512-i	
DRAWN	N. BROWN	MECH CHK		ELECT CHK		APPROVED	
VARIAN T.V. LIMITED CAMBRIDGE		1968		DATE DRAWN 69-11-29		FORM	

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Technical Data

STEREO SOUND IN SYNC

LDM 1903/00/01 (8928 190 30001)

LDM 1904/00/01 (8928 190 40001)

TECHNICAL DATA

Contents

1.	GENERAL	Sh. 595-1
2.	VIDEO PERFORMANCE	Sh. 595-3
3.	AUDIO PERFORMANCE	Sh. 595-5
4.	LINK DISTORTIONS FOR NEGLIGIBLE DEGRADATION OF SOUND PERFORMANCE	Sh. 595-8

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Technical Data

STEREO SOUND IN SYNC

LDM 1903/00/01 (8928 190 30001)

LDM 1904/00/01 (8928 190 40001)

TECHNICAL DATA

1. GENERAL

Dimensions:

Height	:	133 mm (5.25 in) (3RU)
Width	:	480 mm (19 in)
Depth	:	381 mm (15 in)

Weight:

Coder	:	7.5 kg (17 lb)
Decoder	:	8 kg (18 lb)

Power Requirements:

Coder	:	85VA (approximately)
Decoder	:	100VA (approximately)

Ambient Temperature : 0 - 45°C

Audio Monitor Points : P0 (type B) jack, for 600-ohm headphones

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Connectors:

Video	:	75-ohm BNC
Audio Input	:	5-way AXR plug
Audio Output (Stereo)	:	5-way AXR socket
Audio Output (Monitoring)	:	5-way 240° DIN socket
Monitoring	:	37-way D-type plug
Remote Control	:	25-way D-type socket
Auxiliary Input (Coder)	:	15-way D-type plug
Auxiliary Output 1 (Coder)	:	15-way D-type socket
Auxiliary Output 2 (Coder)	:	9-way D-type socket
Auxiliary Input (Decoder)	:	9-way D-type plug
Auxiliary Output 1 (Decoder)	:	9-way D-type socket
Auxiliary Output 2 (Decoder)	:	15-way D-type socket
Control and Additional Data In	:	25-way D-type plug
Control and Additional Data Out	:	25-way D-type socket
Mains Supply	:	CEE22 plug

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Technical Data

2. VIDEO PERFORMANCE

- Notes:
1. Parameters marked with an asterisk are only checked on a batch basis.
 2. Two asterisks indicate design parameters not normally checked in production.
 3. For definitions of parameters see CCIR Rec 567-1.

Return Loss at 5MHz : better than 36dB

Non-useful DC Output Component : $0 \pm 0.1V$

Insertion Gain : $0 \pm 0.2dB$

Noise

(Relative to 700mV Luminance):

Continuous Random Noise
(RMS):

10kHz - 5MHz
weighted : better than -67dB

10kHz - 5MHz
unweighted * : better than -60dB

Periodic Noise (p-p):

Power Supply Hum * : better than -55dB

Single-frequency **
Noise 1kHz - 5.5MHz : better than -70dB

Non-linear Distortion:

Luminance Signal

Normal Level : less than 1%

+3dB Level * : less than 2%

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Intermodulation Product
(Luminance to Chrominance):

Differential Gain:

Normal Level : less than 0.5%
+3dB Level * : less than 1.5%

Differential Phase:

Normal Level : less than 0.5°
+3dB Level * : less than 1°

Intermodulation Product
(Chrominance to Luminance):

Normal Level : less than ±1%
+3dB Level * : less than ±2%

Synchronising Signal
Distortion:

Steady State:

Normal Level : less than 2%
+3dB Level * : less than 3%

Transient:

Normal Level * : less than 2%
+3dB level * : less than 4%

Linear Distortion:

Field time Waveform
Distortion * : less than ±1%

Line Time Waveform
Distortion:

Bar top * : less than ±1%
Base line * : less than ±1%

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Short-time Waveform
Distortion:

2T Pulse to Bar : 100 ±2%
2T Pulse K : less than 0.5%

Chrominance-luminance
Inequalities:

Gain Inequality : less than 0.2dB
Delay Inequality : less than 10ns
Teletext Decoding Margin : less than 5% reduction

Spurious Signals in the : less than 25mV p-p
Blanking Period *

Offset of Re-inserted
Blanking Level:

Direct Connection : less than 9mV
Connection via
Reference Circuit ** : less than 15mV

3. AUDIO PERFORMANCE

Notes: 1. Parameters marked with an asterisk are only checked on a batch basis.
2. Two asterisks indicate design parameters not normally checked in production.

Coder Input Impedance : greater than 10k ohms,
balanced.
Decoder Output Impedance : typically 30 ohms, balanced.

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Voltage Gain at 1kHz : Adjusted to 0dB.

Maximum Input Level : +14.8dBm at 2kHz. At other frequencies as related to 2kHz by the CCITT J17 pre-emphasis curve shown on Sh. 595-6, subject to an absolute maximum of +21dBm.

Gain/Frequency Response
Ref 1kHz:

40 - 125Hz	:	+0.4 -1.0dB
125Hz - 10kHz	:	\pm 0.4dB
10 - 14kHz	:	+0.4 -1.1dB
14 - 15kHz	:	+0.4 -1.8dB

Noise Level : better than -57dBq 0ps
better than -60dBq 0s

Programme-modulated Noise,
at +9dBu, 100Hz : better than -47dBq 0ps

Total Harmonic Distortion:

100Hz at +8dBm	:	less than 0.1%
1kHz at 8dBm	:	less than 0.1%

Crosstalk *:

40Hz	:	better than -80dB
500Hz - 5kHz	:	better than -85dB
15kHz	:	better than -75dB

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Difference in Phase
between Ch A and Ch B *:

40Hz	:	less than 17°
200Hz - 4kHz	:	less than 9°
14kHz	:	less than 17°
15kHz	:	less than 23°

4. LINK DISTORTIONS OCCURRING SINGLY
FOR NEGLIGIBLE DEGRADATION OF SOUND PERFORMANCE

Decoder Input Level	:	+3-6dB
Continuous Random Noise (unweighted)	:	-36dB
Power Supply Hum	:	500mV p-p
Tilt Over Four Lines	:	less than 10%

2T Sin² Pulse Response:

Pulse to Bar	:	100 +30-15%
--------------	---	-------------

Line-time Waveform Distortion:

Bar K **	:	less than 6%
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Chrominance-Luminance Gain Inequality *	:	±24%
--------------------------------------------	---	------

Chrominance-Luminance Delay Inequality *	:	±80ns
---------------------------------------------	---	-------

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STEREO SOUND IN SYNC

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MONITORING

Contents

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3.	MONITOR 1 - SOFTWARE	Sh. 595-3
3.1	What It Does	Sh. 595-3
3.2	How It Does It	Sh. 595-5
3.3	Modifying the Program	Sh. 595-6
3.4	Output Indications	Sh. 595-15
4.	REAR PANEL CONNECTIONS	Sh. 595-16

ILLUSTRATIONS

Fig. 1	Representation of PROCaccessC	Sh. 595-11
Fig. 2	Representation of PROCassessD	Sh. 595-12

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STEREO SOUND IN SYNC

LDM 1903/00/01 (8928 190 30001)

LDM 1904/00/01 (8928 190 40001)

MONITORING

1. INTRODUCTION

Most of the cards in the Stereo Sound in Sync system have fault indication LEDs and fault outputs to the mother board to indicate whether some part of the system has failed. The fault outputs are taken to a monitoring card, Monitor 1 which provides remote fault indications on the basis of the inputs sent to it.

2. MONITOR 1 - HARDWARE

This card is a Z80 processor system with interfacing to the rest of the system. Thus the action of the card depends on the software supplied for it.

24 fault input lines are provided, not all of which are currently used. These are taken to R/S flip-flops which are set by the fault input going active. The outputs of the flip-flops appear as three read-only ports at address 00, 20 and 40 Hex. The flip-flops assigned to each port are reset by the program reading from that port.

Main and secondary fault outputs are provided along with six open-collector outputs. The main fault output is driven from a monostable which has to be regularly triggered by the program to keep the output in the 'system good' state. This is so that, if the program crashes, the monitor will declare a fault. The main and secondary fault outputs and the open-collector outputs are driven from a write-only port at 60 Hex.

The circuit is provided with 16k bytes of RAM, 16k bytes of EPROM which is copied to RAM on switch-on and a 16k byte BBC BASIC interpreter EPROM. A CTC chip is supplied to provide a real-time clock.

There is also an 8-bit data bus, which is not used in this application and various input and output control or timing signals.

A 4-pole switch S3 is set to indicate to the software the circumstances

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in which the card is working. The switch positions have the following significance:

- | | |
|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1. On: Coder | Off: Decoder |
| 2. On: Main facilities | Off: Full facilities,
i.e. in the case of
the Coder, when an
Audio Decoder module
is fitted, in the
case of the Decoder,
when an Audio
Comparator is
fitted. |
| 3. On: Not used | Off: Not used. |
| 4. On: No audio modules | Off: With audio modules. |

The main fault output controls a green 'System Good' LED which protrudes through the front panel and a 2-pole changeover relay whose contacts are connected to the 37-way 'D' type connector on the back panel.

The secondary output controls a red LED behind the front panel and another 2-pole changeover relay connected to the 37-way 'D' connector.

Six other LEDs with corresponding open-collector outputs to the 37-way D connector indicate fault inputs in logical groupings whenever the main fault output comes on. The fault groupings are determined by the software.

Two RS232 ports are provided on the front of the module: one for interactive control or modification of the software via a terminal; the other for loading a program from a microcomputer or sending a program from RAM to a PROM Programmer. In both cases the baud rate is 9600, there must be one or more stop bits, parity is ignored and there is no handshake. The data output to a PROM programmer is in 'Intel Intellec' format. A TERMINAL ENABLE switch and ESCAPE button are provided for use with these facilities. The two RS232 ports are labelled X2 and the connections are as follows (Pin 1 at the top):

1. OV)
)
2. Transmit) Terminal
)
3. Receive)
4. Transmit to PROM PROGRAMMER
5. Receive from BBC microcomputer
6. OV.

A small HELP screen is available by typing '*' on the terminal.

3. MONITOR 1 - SOFTWARE

3.1 What It Does

Most of the software is concerned with controlling the main fault output. On the coder the secondary fault output is used to indicate that the incoming video already carries sound in syncs, so it can be used to drive an external bypass relay. On the decoder it is not used. The six open-collector outputs are currently used to give information about the nature of the fault once the system has been declared faulty.

The software is designed so that brief fault inputs do not cause the main fault output to come on, unless too many occur in a given time. Also the inputs must be fault free for a specified time before the fault output is switched off again.

More precisely, for each input the following variables can be set: TL%, TC%, TTG%, NL%, FP%.

- TL% If an input is continuously faulty for a period of TL% then the main fault output comes on. Note that since the inputs are fed via R/S flip-flops, as long as the input is showing a fault at least once in each program cycle the input will appear to be continuously faulty (e.g. a rapidly pulsing fault input would appear as a continuous fault). If TL% is set to -1 then the input is allowed to go faulty continuously without triggering the main fault output, though intermittent faults can still trigger the fault output (see NL%, FP% below).
- TC% If after being faulty an input is good for a period of less than TC% then that good period is ignored for the purpose of timing the length of the fault, i.e. the input is considered to be continuously faulty with the good period being bad. If TC% is longer than TL% and two short faults occur within a period of TC% (but separated by more than TL%) then the main fault output will come on.
- NL%, FP% These variables control intermittent fault detection. If more than NL% faults occur in a period of FP%, then the main fault output comes on (note that faults separated by less than TC% count as one fault). Counting take place in separate periods so it is possible for more than NL% faults to occur in a period of FP% without triggering the main fault output if, say, half of them occur at the end of one timing period and the other half at the start of the next, with less than or equal to NL% in each period. Once a timing period has completed with less than or equal to NL% faults the next period does not start

until another fault appears. Once more than NL% faults have been detected a new timing period starts immediately and the input is considered intermittently faulty until a timing period expires with less than or equal to NL% faults counted.

TTG% Once the main fault output has come on it will not go off again until each input has been fault free for the preceding period of TTG%. This applies to all inputs, not just to those that caused the main fault output to come on in the first place.

Note: If an intermittent fault has been detected the main output cannot go good until a period of FP% has expired. This may well be longer than TTG%. TTG% applies only to the actual fault input, it does not time from when an intermittent fault clears. If an intermittent fault clears then the main fault output will go off immediately so long as the inputs have already been fault free long enough.

The program's accuracy in timing faults depends on the frequency at which it polls its inputs. This is variable. If all the inputs are static then the period is of the order of 0.1s. If the inputs change, the program then has additional processing to do and this delays the next poll by about 0.7s, though a worst case of between 1 and 1.5s is possible.

The most obvious effect is that short faults appear longer than they really are. Once a fault has been detected the fact that it has been cleared will not be detected for around 0.7s. Therefore there is no point in setting any of TL%, TC%, or TTG% to less than about one or two seconds, unless they are actually set to zero.

On the coder the secondary fault output is used to indicate that the incoming video already carries sound in sync. This is done under the control of a timer so the output does not come on until sound in sync has been detected for a period of BP_{on} and it does not go off until there has been no sound in sync for a period of BP_{off} . The main fault output may or may not be required to come on when sound in sync is detected; the value of TL% pulses should be set to -1 if not.

The two inputs SYNC FAIL and STANDBY ON are treated as special cases on the coder. SYNC FAIL does not cause the main fault output to come on as long as STANDBY ON comes on within the period of the variable TSD (see Sh. 595-7). The main fault output also comes on if Standby is on after a delay of TSD from SYNC FAIL going off. If it is required that SYNC FAIL or STANDBY ON always turn the main fault output on then the DATA table should be altered so that TL% is not set to -1 for these inputs.

The open-collector outputs are all off while the main fault output is off. When the main fault output is on they are controlled by combinational logic applied to the fault inputs. They are intended to give information about the cause of the fault.

3.2 How It Does It

Each time round the main loop a procedure PROCpoll is called which polls the inputs and logs their behaviour.

Variables 'Stable' and 'Marker' are controlled by PROCFaulty and PROCOK to indicate respectively whether the main fault output will have to change state at some time, if the inputs remain in the current state, and if so, when. While the main fault output is off they are updated each time an input or the intermittent fault detector changes state. While the main fault output is on they are only updated once the marker has been reached or passed and an input or the intermittent fault detector has changed state since they were last updated. This is because with the main fault output on, no changes can move Marker earlier, so it is safe to wait until it is reached before updating it. See REM statements for PROCFaulty and PROCOK on Sh. 595-14.

Each time round the loop Stable and Marker are checked to see whether the main output needs to change state.

Each time a new fault appears the intermittent fault detector checks whether the current timing period has expired. If it has the fault count is reset to zero and a new period is started. A new period is also started if the current period has not expired but this is the first fault since it started.

If the fault count exceeds NL% then an intermittent fault is declared, the count is reset and a new timing period is started. If no new faults appear the intermittent fault is considered to have cleared once this period has expired, but note that, as mentioned above, if a new fault does appear then a new timing period starts, which will have to expire before the intermittent fault is considered to have cleared. Thus one fault will delay the clearing of the intermittent fault even if not enough faults occur to retrigger the detector.

The variable InMark stores the earliest time at which any intermittent fault period is due to expire. By the time it is reached it may be incorrect, i.e. the period which was due to expire may have been curtailed and a new one started. In any case once it is reached all the periods for which an intermittent fault is currently declared are checked to see if they have expired and if so the declaration is cancelled. InMark is then reset for the next period that is due to expire.

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3.3 Modifying the Program

The BASIC program held in EPROM is copied to RAM on switch-on and then run. With a terminal connected as mentioned in Para. 2 the program can be modified and the modified version then run. When an EPROM is required containing the modified program, the RAM contents may be sent to a PROM programmer (Para. 2) with the command SAVE.

The modifications that are most likely to be made to the program are alterations to the DATA tables at the end of the program. For convenience the data tables for coder and decoder are shown below, without line numbers but including an explanatory REM statement that is omitted from the EPROM version due to lack of space.

***** Coder DATA *****						
REM	TL%	TC%	NL%	FP%	TT6%	CHECK
DATA	-1,	0,	2,	20,	0,	Sync
DATA	-1,	0,	2,	20,	0,	Standby
DATA	2,	2,	2,	20,	10,	DataADP
DATA	2,	2,	2,	20,	10,	SigFail
DATA	-1,	0,	2,	20,	0,	Fldsync
DATA	5,	2,	2,	20,	10,	Mute
DATA	2,	2,	2,	20,	10,	ClkADP
DATA	2,	2,	2,	20,	10,	Parity
DATA	2,	2,	2,	20,	10,	Pulses
DATA	1,	0,	1,	20,	10,	RQMerr
DATA	2,	2,	2,	20,	10,	Buffov
DATA	1,	0,	1,	20,	10,	RAMerr
DATA	2,	2,	2,	20,	10,	Buffun
DATA	2,	2,	2,	20,	10,	Ctrlerr
DATA	2,	1,	2,	20,	10,	Insert
DATA	-1,	0,	2,	20,	0,	Spare1
DATA	-1,	0,	2,	20,	0,	Spare2
DATA	-1,	0,	2,	20,	0,	Spare3
DATA	-1,	0,	2,	20,	0,	Spare4
DATA	-1,	0,	2,	20,	0,	Spare5
REM	TSD	TTSG				
DATA	3,	10				
REM	Bpon	Bpoff				
DATA	0,	0				

REM DECDATA Stereo Sis Ver 0.2

AUTO9000

REM***** Decoder DATA *****

REM	TL%	TC%	NL%	FP%	TTG%	CHECK
DATA	2,	2,	2,	20,	10,	Sync
DATA	2,	2,	2,	20,	10,	AmpRef
DATA	2,	2,	2,	20,	10,	DataRec
DATA	2,	2,	2,	20,	10,	SigFail
DATA	-1,	0,	2,	10,	10,	Fldsync
DATA	5,	2,	2,	20,	10,	Mute
DATA	2,	2,	2,	20,	10,	ClkBsr
DATA	2,	2,	2,	20,	10,	Parity
DATA	2,	2,	2,	20,	10,	Pulses
DATA	-1,	0,	2,	20,	0,	Spare1
DATA	2,	2,	2,	20,	10,	Buffun
DATA	-1,	0,	2,	20,	0,	Spare2
DATA	2,	2,	2,	20,	10,	Buffov
DATA	2,	2,	2,	20,	10,	Just
DATA	2,	2,	2,	20,	10,	DataFail
DATA	2,	2,	2,	20,	10,	DataLow
DATA	-1,	2,	10,	5,	10,	ASC
DATA	2,	2,	2,	20,	10,	DataHi
DATA	-1,	0,	2,	20,	0,	Spare3
DATA	5,	2,	2,	20,	10,	DACfail

Any other alterations to the behaviour of the main fault output would involve major changes and would probably mean a complete rewrite of the software.

The function of the secondary fault output (currently unused on the decoder) could be altered, though this should only be done by someone who is sure they know what they are doing.

The behaviour of the six open-collector outputs can be modified. They are simply controlled by combinational logic applied to the fault inputs. No timing is involved. If modification to this combinational logic is required the part of the program to be altered is the procedure called PROCassessC (for the Coder) or PROCassessD (for the Decoder). They use the function FN_i(x), which returns the value TRUE if the input x is currently faulty and FALSE if it is not. BASIC variables with names describing each fault input have been set up with the required value of x, e.g. FN_i(Sync) returns TRUE if line sync has failed. Various FN_i(x) functions are ANDed and ORed together to determine the required states of the six open-collector outputs. The outputs are actually controlled by setting or resetting the six least significant bits of the variable OP. This is done by:

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OP = OP OR y to set a bit (LED/output off)

or

OP = OP AND NOT y to reset a bit (LED/output on)

where

y = 1 for bit 0

2 for bit 1

4 for bit 2

8 for bit 3

16 for bit 4

32 for bit 5.

It is vital that the two most significant bits of OP are not altered as these control the main and secondary fault outputs. If there is any doubt about whether they will be altered then the line:

TEMP = OP

should be put immediately after the line DEFPROCassess, and the line

OP = (OP AND &3F) OR (TEMP AND &CO)

immediately before the line ENDPROC. This will ensure that the two most significant bits have the same value when the procedure finishes as when it started.

Conditions such as (SWITCH AND 2) = 2 are included to ensure that apparent faults due to intentionally missing cards are ignored. The positions of Poles 1 to 4 of switch S3 are read into the variable SWITCH (bits 3 to 0 respectively) at the beginning of the program, ON having a bit value 0 and OFF a bit value 1.

For convenience PROCassessC and PROCassessD are listed on Sh. 595-9 and 10, without line numbers but with explanatory REM statements which are omitted from the version supplied in EPROM. Equally useful for implementing changes will be the logic diagram representations of PROCaressC and PROCassessD shown on Sh. 595-11 and 12.

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REM***** PROCassess (Coder) *****
REM Attempts to give some information about the cause of the problem when the system has been declared faulty. This information is given on the LEDs and a/c outputs. Note that if the inputs change this information will change immediately; it is not controlled by timers in the way that the main outputs are. The outputs have the following meanings:
REM output 5 The video input is failing intermittently. Note that a permanent failure is not considered as a fault, as the coder will switch to standby and the sound will be correctly transmitted. Switching to and from standby frequently will however break up the sound.
REM output 4 The incoming video already carries SiS; the video output of this unit will be unusable.
REM output 3 Either, i) Incoming line syncs are at the wrong rate,
REM ii) If using external data the data is not valid NICAM-728 data,
REM iii) If using the internal NICAM-728 coder, it is faulty.
REM output 2 Any of the signals (ie data, data clock, C0, C0 clock) from the source selected by the Clock & I/O module have failed.
REM output 1 The decoded bitstream is not a valid NICAM-728 bitstream, or has a high error rate.
REM output 0 There is a hardware fault.
REM NB hardware faults could of course cause any of the above indications to come on, but the listed faults are those most likely to be the cause of the problem.

DEFPROCassessC
DSPPFail=((SWITCH AND 1)=1) AND (FNi(ROMerr) OR FNi(RAMerr))
NoSig =FNi(SigFail)
BadWire=FNi(DataADP) AND NOT NoSig
NonNic =(FNi(Buffav) OR FNi(Buffun)) AND NOT FNi(DataADP) AND NOT SBF
Coded =FNi(Pulses)
InVideo=INFLT AND (BITMASK%(Sync) OR BITMASK%(F1dsync))
SBfault=SBF OR SBW
InsFail=FNi(Insert) AND NOT NoSig AND NOT NonNic AND NOT Coded AND NOT InVideo

ProcClk=FNi(ClkADP)
BadNic =((FNi(Mute) OR FNi(Parity)) AND ((SWITCH AND 4)=4)) OR (FNi(Ctrlerr) AND ((SWITCH AND 1)=1))

OP=OP OR &3F
IF InVideo THEN OP=OP AND NOT 32
IF Coded THEN OP=OP AND NOT 16
IF NonNic THEN OP=OP AND NOT 8
IF NoSig THEN OP=OP AND NOT 4
IF BadNic THEN OP=OP AND NOT 2
IF SBfault OR DSPPFail OR BadWire OR ProcClk OR InsFail THEN OP=OP AND NOT 1
ENDPROC

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REM***** PROCassess (Decoder) *****
REM Attempts to give some information about the cause of the problem when the system has been declared faulty. This information is given on the LEDs and o/c outputs.
REM Note that if the inputs change this information will change immediately, i.e. it is not controlled by timers in the way that the main outputs are.
REM The outputs have the following meanings:
REM output 5 Incoming field syncs are failing intermittently, probably means that coder is switching between normal and standby.
REM output 4 No incoming video, or SiS pulses are non existent or defective, e.g. wrong amplitude.
REM output 3 The bitstream error rate is high.
REM output 2 Any of the signals (ie data, data clock, C0, CO clock) from the source selected by the Clock & I/O module have failed.
REM output 1 There is an audio decoding fault.
REM output 0 There is a hardware fault.
REM NB hardware faults could of course cause any of the above indications to come on, but the listed faults are those most likely to be the cause of the problem.

DEFPROCassessD
FldSyncInt=(INFLT AND BITMASK%(Fldsync))>0
Novideo=FNi(Sync)
Notcoded=FNi(Pulses) AND NOT Novideo
BadPulses=(FNi(AmpRef) OR FNi(DataLow) OR FNi(DataHi) OR FNi(Just)) AND NOT Novideo AND NOT Notcoded
BadSignal=Novideo OR Notcoded OR BadPulses OR FldSyncInt
NoSig=FNi(SigFail)
NICerrors=((FNi(Buffov) OR FNi(Buffun)) AND NOT BadSignal AND NOT FNi(AGC)) OR (NOT NoSig AND ((FNi(Mute) OR FNi(Parity)) AND ((SWITCH AND 1)=1)))
NoNICdata=NOT BadSignal AND (FNi(DataFail) OR FNi(DataRec))
DACfault=FNi(DACfail) AND ((SWITCH AND 4)=4)
Hardware=NoNICdata OR FNi(AGC) OR (FNi(ClkBSR) AND NOT NICerrors AND NOT BadSignal)

OP=OP OR &3F
IF FldSyncInt THEN OP=OP AND NOT 32
IF Novideo OR Notcoded OR BadPulses THEN OP=OP AND NOT 16
IF NICerrors THEN OP=OP AND NOT 8
IF NoSig THEN OP=OP AND NOT 4
IF DACfault THEN OP=OP AND NOT 2
IF Hardware THEN OP=OP AND NOT 1
ENDPROC

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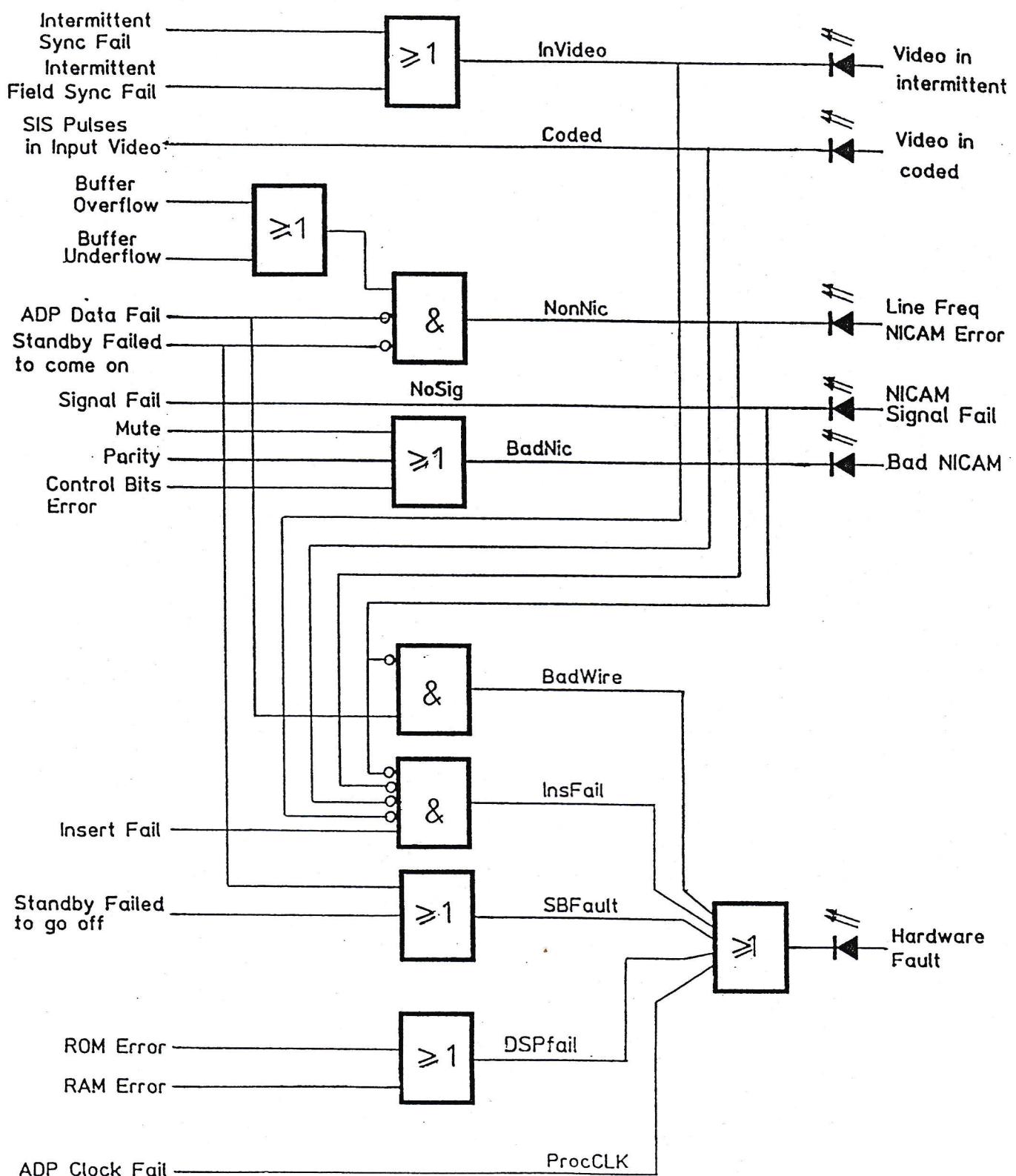


Fig. 1 Representation of PROCassessC

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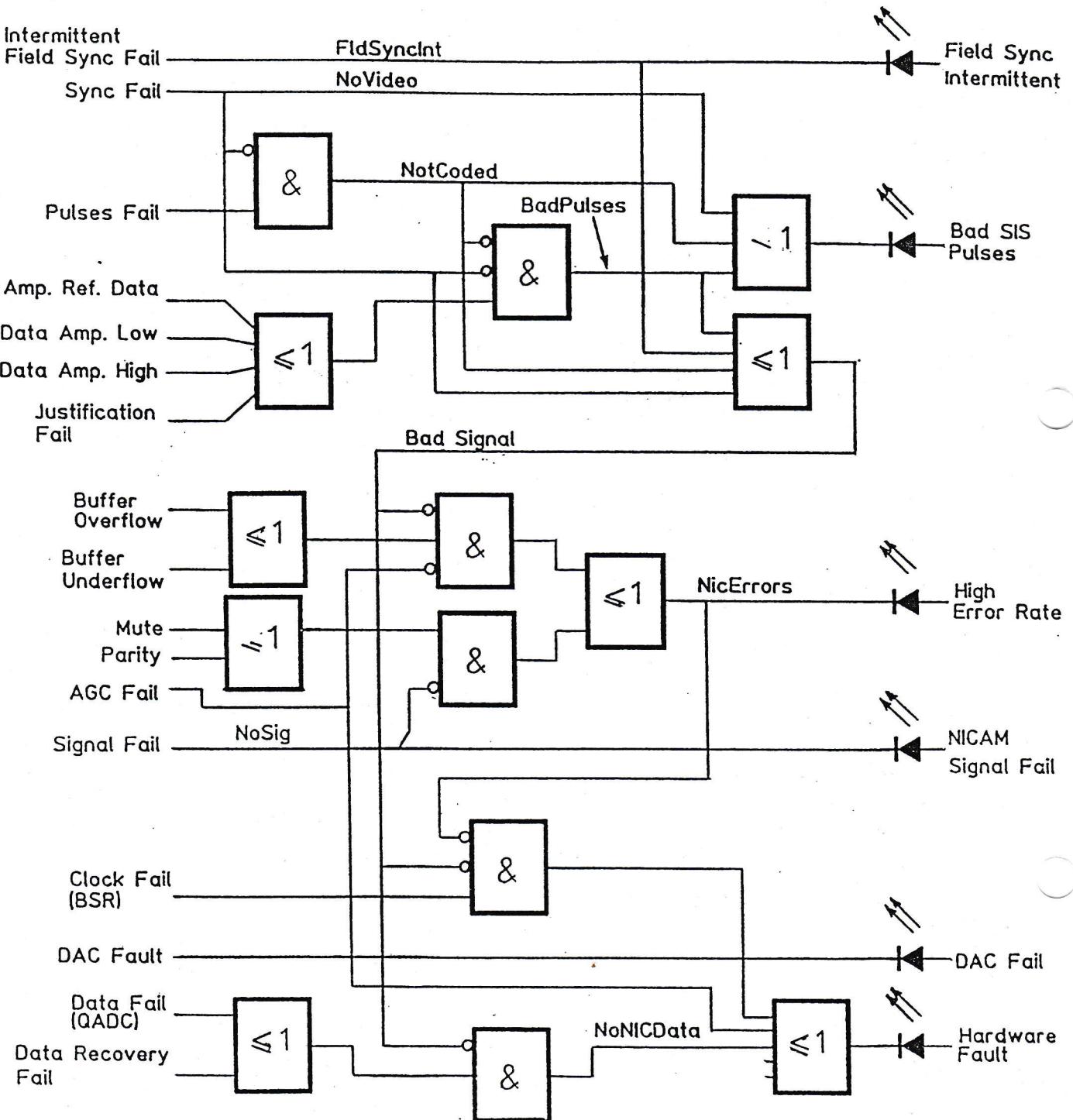


Fig. 2 Representation of PROCassessD

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In several other cases REM statements have been omitted from the version of the program supplied in EPROM, so they are given below to aid understanding of the program.

REM***** MAIN LOOP *****
REM Calls PROCpoll each time round the loop, which reads the inputs and keeps records of their behaviour. Also calls, when required, the procedures which decide whether the system is good or not and the procedures which control the outputs. Exactly which procedures are called depends on the state of various flags and timers.

REM* PROCstate controls the main output.

REM It should only alter bit 7 of OP and leave the other bits unchanged.

REM***** PROCsecondary controls the secondary output.*****
REM It should only alter bit 6 of OP and leave the other bits unchanged.

REM***** PROCind controls the o/c outputs.*****
REM It should only alter bits 0 to 5 of OP and leave bits 6 & 7 unchanged.

REM***** PROCpoll *****
REM Input monitoring procedure.

REM Returns the following information: FAULT contains current state of inputs, ie bit n =1 if input n is declaring a fault.

REM CHANGE indicates which inputs have changed state since PROCpoll was last called, ie bit n =1 if input n has changed.

REM INFLT indicates which inputs are considered to be intermittently faulty.

REM Further information is contained in the arrays TNF%() and TFC%().

REM TNF%(n) gives the time at which a new fault appeared on input n.

REM TFC%(n) gives the time when input n last went good.

REM Definitions:

REM "new fault": an input indicates a fault after being good for at least TC%(n) centiseconds, if the input has been good for less than that length of time the fault is considered to be a continuation of the previous fault.

REM "intermittently faulty": more than NL%(n) new faults have been counted in a period of FP%(n). Note that counting takes place in separate periods, so it is possible for more than NL%(n) faults to occur in a period of FP%(n) if some of them occur at the end of one counting period and some at the start of the next, with less than NL%(n) occurring in each period.

REM***** PROCfaulty *****
REM Should be called whenever an input or the intermittent fault detector
changes state and the system good LED is on.
REM It returns a flag, Stable, which is TRUE if the system is to remain in the
good state indefinitely. Otherwise it also returns, in the variable Marker,
the time at which the system should be declared bad, assuming no other
changes take place before then.

REM***** PROCOK *****
REM When called returns the time, in Marker, at which the system can be declared
good again, assuming no input changes before then. If there is no time at
which the system can be declared good the flag Stable will be set TRUE and
Marker will give the earliest time at which the system could go good
assuming the inputs change as required, i.e. there is no need to call the
procedure again before Marker is reached.

REM***** Time functions *****
REM Note the following conventions: The value of the real time clock is stored
in the variable Tpoll at the time of polling the inputs and Tpoll is used as
the current time throughout the program.
REM The highest two bits of Tpoll are held at zero. The same goes for any other
variable storing a time. This is so that modulo arithmetic can be performed
without risk of overflow.
REM FNtto(T) returns the time till T, which may be in the past or future. NB
due to the modulo nature of TIME events that were in the past will
eventually move into the future, this happens after about two months.

REM***** Input testing function *****
REM FNi(n) is set TRUE if input n is currently showing a fault.

REM***** PROCpowerup *****
REM Provides a delay so that transient fault indications at switch on do not
result in the system being declared bad for a long time; the system good
output does not come on until this delay has expired.

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3.4 Output Indications

Output	Coder	Decoder
Main Secondary	System Fail Video Input Coded	System Fail Not Used
o/c 5	Video Input Intermittent	Field Syncs Intermittent
o/c 4	Video Input Coded	Bad SIS Pulses
o/c 3	Line Freq/NICAM Data Error	High Error Rate
o/c 2	NICAM Signal Fail	NICAM Signal Fail
o/c 1	Bad NICAM	DAC Fail
o/c 0	Hardware Fault	Hardware Fault

Note: Relays are energised (i.e. not 'normal') for system good. Open collector output polarity is ground for system good.

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4. REAR PANEL CONNECTIONS

Coder and Decoder: 37-way D-type plug

Pin No.	Function
20	1 Open collector output 0 2 Open collector output 1
21	2 Open collector output 2 3 Open collector output 3
22	4 Open collector output 4 5 Open collector output 5
23	6 Earth (OV) 7 Earth (OV)
24	8 Main alarm relay - normally closed contact 1 9 Main alarm relay - common contact 1
25	10 Main alarm relay - normally open contact 1 11 Main alarm relay - normally closed contact 2
26	12 Main alarm relay - common contact 2 13 Secondary alarm relay - normally open contact 1
27	14 Secondary alarm relay - normally closed contact 1 15 Secondary alarm relay - common contact 1
28	16 Secondary alarm relay - normally open contact 2 17 Secondary alarm relay - normally closed contact 2
29	18 Secondary alarm relay - common contact 2 19 Secondary alarm relay - normally open contact 2
30	20 OV 21 Parity error flag output (open collector)
31	22 Not used
32	23 Not used
33	24 Not used
34	25 Not used
35	26 Not used
36	27 Not used
37	28 Audio Ch A output red (600 ohms balanced) 29 Audio Ch A output blue (600 ohms balanced)
	30 OV 31 OV
	32 Audio Ch B output red (600 ohms balanced) 33 Audio Ch B output blue (600 ohms balanced)

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SYSTEM SETTING-UP

1. GENERAL

The following procedures are to assist in the testing and setting up of the units being put into service.

The oscillators should be set up using an off-air frequency standard and a good quality counter, and monitoring at buffered test points.

CAUTION: PRINTED CIRCUIT BOARDS SHOULD NOT BE REMOVED OR
INSERTED WITH THE POWER SWITCHED ON, AND BOARDS
SHOULD ONLY BE INSERTED INTO THE CORRECT SLOTS
BY REFERENCE TO THE NAMES ON THE BOARDS AND THE
LEGENDS ON THE FRONT PANEL.

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2. CODER SYSTEM ADJUSTMENTS

2.1 Power Supplies

- (1) With only the Power Supply module connected and the power off, set the voltage selector on the rear panel to the mains voltage in use.
- (2) Insert an extender board in any position in the frame.
- (3) Switch the power on and check the DC voltage rails on the extender board, relative to 0V at Pin 32a or c, as follows:
 - (a) +5V at Pin 28a or c, or 29a or c.
 - (b) +20V at Pin 27a or c.
 - (c) -20V at Pin 30a or c.
- (4) Switch off the power and fit all the printed circuit boards into the frame.
- (5) Connect the positive end of a meter to the top of R75 on the Sync Separator and the negative to the bottom of R72. Access from the front without using the extender board.
- (6) Switch on and check the +5V supply. It should be $5V \pm 0.05V$. If necessary adjust R4 on the PSU module.

2.2 Moveable Link Positions

Switch off and check the following link positions:

Audio Input Filter	:	X17, X18 to N.
Audio ADC	:	X10 to S.
DSP	:	X2, X4 fitted, X3 not fitted.
Clock and I/O	:	X2 to X6 to N.
		X16, see note on circuit diagram; if in doubt, use position A.

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X18 to A (for Tone 2 = silence).
X19 and X20 to C.

Audio Decoder (if fitted) : X4, X16, X17 to ab.
X3, X15, X18 to bc.

Asynchronous Data Proc : All links to N except X18 to
'LS' or 'MS' according to whether
standby sync is required to be
Line Sync only or Mixed Sync.
X16 Fitted.

Sync Separator : X7 to N.

Monitor 1 : X3 to 1; X4 fitted; X9 to A.
S3/1 to COD.
S3/2 To FULL if an Audio Decoder
module is fitted, to MAIN if not.
S3/3 Not applicable.
S3/4 to NO AUDIO, if a DSP module
is not fitted.

2.3 Clock and I/O

Use the switches on the front of the module or Remote Control to select Tone 1 or Tone 2 and Free-running mode. Adjust R14 for 5824kHz $\pm 0.3\text{Hz}$ oscillator frequency at X14. DO NOT ATTEMPT THIS WITHOUT CHECKING THAT THE ACCURACY AND STABILITY OF YOUR FREQUENCY COUNTER IS ADEQUATE FOR THE TASK, i.e. BETTER THAN 1 PART IN 10^8 .

This frequency should be checked after the first year, and less frequently thereafter.

2.4 Digital Signal Processor (DSP)

Probe X5 (A31 Pin 3) and adjust C5 for locking; this will be a compound waveform which repeats after four transitions. Set C5 for mean mark : space ratio of 50 : 50, when the ratio of the times between the four transitions will be approximately 2 : 2 : 1 : 1.

2.5 Audio Decoder (Optional)

- (1) Probe X5 and adjust C31 for a locked signal of 50 : 50
mark : space ratio.

- (2) Probe X7 and adjust C35 for a locked signal of 50 : 50
mark : space ratio.

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- (3) Set the switches on the front of the Clock and I/O module (or use the remote control unit if fitted), to select Tone 1.
- (4) Connect an Audio Level meter with 600 ohms input impedance to the Channel A output pins (35 and 17) on the Monitoring socket on the rear panel. If the intended use of the output of this module is to drive a high-impedance circuit, the input impedance of the meter should be set to HIGH IMPEDANCE. Adjust R17 for the correct output level.

Note: Tone 1 is a digitally generated internal tone of 0dBu at 1kHz to match the UK NICAM 728 specification for audio headroom of 14.8dB for a 0dBu 2kHz signal. Other current specifications for audio headroom are around 12dB for a 0dBu 2kHz signal; to match these, R17 must be adjusted for a correspondingly lower output level.

- (5) Repeat (4) for channel B, connecting to pins 37 and 19 of the Monitoring socket and adjusting R43.

2.6 Sync Separator

Note: The Sync Separator, Asynchronous Data Processor and Video Processor modules need to be set up as a trio (see 2.6(14), 2.7(3) and 2.8(10)).

- (1) Connect the Sync Separator board via the extender board.
- (2) Switch on and apply a 100% colour bar signal to the 'Video' input on the rear panel.
- (3) Connect the oscilloscope probe to test point X5 and adjust R91 so that the clamp pulse occurs 5 to 5.5 μ s after the leading edge of sync at X4. Also check that the clamp pulse is 1.5 to 2.1 μ s wide.
- (4) Monitor X8 and adjust R87 for a pulse width of 4.7 μ s \pm 0.1 μ s.
- (5) Connect a second oscilloscope probe to X6 and adjust R90 so that the clamp pulse at X6 begins 4.8 to 5.0 μ s after the negative-going edge at X8. Check that it is 1.8 \pm 0.3 μ s wide.

- (6) Monitor the clamp guard pulse at X9 and adjust its width by R89 to $3.5\mu s$ less than the repetition period, (ignoring the irregular repetition periods during the field sync sequence).
- (7) Monitor the video input on the rear panel and the line trigger pulse on X1-16a and adjust R69 for a delay of 175ns between the half-amplitude point of the leading edge of line syncs and the negative going edge of the line trigger pulse (up to 200ns is permissible if 175ns cannot be achieved).
- (8) Monitor the Field Trigger + at X1-14c and check that it is between 4 and $6\mu s$ wide.
- (9) Monitor the Mixed Sync output at X1-15a. The line sync width should be 4.8 to $5.0\mu s$ as will be alternate equalising pulses. (For examination of the equalising pulses and broad pulses, trigger the oscilloscope to the Field Trigger pulse at X1-14c).
- (10) Connect the oscilloscope via the probe to Test Point X11 and check that the falling edge occurs less than $3.5\mu s$ after the leading edge of input sync, and that the pulse width is at least $1\mu s$.
- (11) Monitor A13 Pin 6 and adjust C32 for 0V.

Note: This is dependent upon the oscillator being locked to a correct line frequency source.

- (12) Monitor the following outputs from the board:

Clamp + at X1-12c	:	$1.5 - 2.1\mu s$
Sample + at X1-10a	:	five (for 625 lines) or six (for 525 lines) negative-going broad pulses in the vertical interval.

Regenerated Sync at X1-20a

Composite Blanking at X1-12a

Field Blanking at X1-22a

Composite Gate at X1-21a
(Vertically blanked horizontal sync).

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- (13) By applying both normal video and SIS signals to the Coder input and removing either sync or only field sync, check the operation of the failure indicator LEDs H1, H2 and H3.
- (14) THIS ADJUSTMENT SHOULD BE DONE AFTER those of 2.7(3) and 2.8(10) if standard mixed sync is to be used. Set X18 on the Asynchronous Data Processor to MS (Standby Mixed Sync). Remove the input video and monitor the SIS Output from the rear panel. Adjust C45 on the Sync Separator module for 440ns delay from sync leading edge (half-amplitude point) to first digit (marker pulse) leading edge (half-amplitude point).
- (15) Switch off and replace the board.

2.7 Asynchronous Data Processor

Note: The Sync Separator, Asynchronous Data Processor and Video Processor modules need to be set up as a trio (see 2.6(14), 2.7(3) and 2.8(10)).

- (1) Connect the Asynchronous Data Processor board via the extender board, then switch on.
- (2) With no video input, monitor the Clock at X14 and adjust C31 for 5968.75kHz ±5Hz (PAL) or 6010.489kHz ±5Hz (NTSC).
- (3) Connect Video input at the rear panel and monitor the SIS output. Adjust C48 for 440ns delay from sync leading edge (half-amplitude point) to first digit (marker pulse) leading edge (half-amplitude point).

Note: This adjustment should follow the correct adjustment of the Line Trigger delay on the Sync Separator module: see section 2.6(7).

2.8 Video Processor

- (1) Apply a signal to the 'Video' input at the rear panel.

- (2) Connect the Coder Video Processor board via the extender board.
- (3) Switch on and monitor the video output terminated in 75 ohms. At A8 Pin 13, monitor with an oscilloscope and probe and check that the clamp pulse is less than $2.1\mu s$.
- (4) Monitor the video output and adjust:
 - R25 for a video amplitude of 1V p-p.
 - R29 to set black level at 0V.
 - R24 for a quaternary data amplitude of 700mV.
 - R18 to set the base of the quaternary digits at -300mV (PAL) or -286mV (NTSC).
- (5) Remove the video input and adjust R118 to set the position of sync tip of standby sync the same as for video.
- (6) Adjust R57 for sync amplitude of 300mV (PAL) or 286mV (NTSC). Data amplitude should still be 700mV.
- (7) Apply a suitable signal for checking frequency response to the video input and adjust C31 for a flat response.
- (8) Check the other video output for similar performance.
- (9) Monitor the buffered output at X1 Pin 4C and check that it is 1V p-p and sitting at -1V.
- (10) Set X18 on the Asynchronous Data Processor to LS (Standby Line Sync). Remove the input video and monitor the SIS output from the rear panel. Adjust R119 on the Video Processor for 440ns delay from sync leading edge (half-amplitude point) to first digit (marker pulse) leading edge (half-amplitude point).

Note: This adjustment should follow the correct adjustment of normal sync-to-marker timing on the Asynchronous Data Processor (see 2.7(3)).
- (11) Switch off and replace the board.
- (12) Return to section 2.6(14) for adjustment of sync-to-marker timing for Standby Mixed Sync.

2.9

Audio Input Filters

- (1) Remove the Audio ADC board and connect the Audio Input Filters board via the extender board.

Note:

The only adjustment on this module is the gain setting (R25 for channel A, R26 for channel B); if the optional Audio Decoder is fitted, or if a Decoder is available the audio gain of the Coder is best set in conjunction with a Decoder module which has been set up for correct output levels with digitally generated test tones. Then R25 and R26 on the Audio Input Filters module are set for unity gain through Coder and Decoder.

If a Decoder or an Audio Decoder module is not available, proceed as follows.

- (2) Switch on and set the links X17 and X18 to T (Test).

- (3) Feed a balanced audio signal into the 'Audio Input' socket on the rear panel, at:

1kHz and 1,420mV

or 2kHz and 852mV

or 2.15kHz and 775mV.

Notes:

1. These input levels are quoted in mV to avoid errors due to the source equipment displaying output levels in dBm on the assumption that the output is loaded with 600 ohms.
2. These input levels are to achieve a gain setting corresponding to the UK broadcasters' specified audio headroom of 14.8dB for a 0dBm, 2kHz signal; other current specifications are around 12dB headroom for a 0dBm, 2kHz signal, for which the input level has to be reduced accordingly, or the output level in (4) below has to be increased accordingly.

- (4) Connect a high-impedance meter to the monitor jack socket at the front of the unit and adjust the output level to 0dBm by means of R25.

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(5) Repeat (4) for Channel B using R26.

(6) Set the links to N (Normal).

(7) Switch off and replace the board.

2.10 Audio ADC

(1) Connect the ADC board via the extender board.

(2) Remove the audio input.

(3) With an oscilloscope or logic probe sequentially monitor A12 Pins 14 to 11, 9 to 6 and A11 Pins 13 to 11, 9 to 6 and adjust R4 so that there is no change in logic level as the sample and hold switches between channels 1 and 2. Check through the sequence again. (R4 is an offset control which adjusts the DC offset of both channels to be the same but not necessarily zero. Thus, when both channels give out the same offset word, or only the LSB is changing, R4 is correctly adjusted.)

(4) Switch off and replace the board.

2.11 General Notes

The coder setting up is now complete. Proceed to the setting up of the decoder, Para 3.

Specification measurements, signalling and remote functions can now be checked. Setting Link X9 in the Asynchronous Data Processor to 0 removes data from the sync pulses to enable video checks to be made.

3. DECODER SYSTEM ADJUSTMENTS

3.1 Power Supplies

- (1) With only the Power Supply module connected and the power switched off, set the voltage selector on the rear panel to the mains voltage in use.
- (2) Insert an extender board in any position in the frame.
- (3) Switch the power on and check the DC voltage rails on the extender board, relative to OV at Pin 32a or c, as follows:
 - (a) +5V at Pin 28a or c, or 29a or c.
 - (b) +20V at Pin 27a or c.
 - (c) -20V at Pin 30a or c.
- (4) Switch off the power and fit all the printed circuit boards into their positions in the frame.
- (5) Connect the positive end of a meter to the top of R75 and the negative to the bottom of R72 on the Sync Regenerator, gaining access from the front without using an extender board.
- (6) Switch on and check the +5V supply. It should be 5V ±0.05V. If necessary adjust R4 on the PSU module.

3.2 Moveable Link Positions

Switch off and check the following link positions:

Sync Regenerator	:	X7 to 'N' (Normal).
Quaternary ADC	:	X11 fitted; X2, X14 to front; X9 both vertical.
Data Recovery	:	X3 to front.
Bitstream Regenerator	:	X2, X3, X4, X7, X9 to 'N'; X11, X12 fitted.

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Monitor 1 (if fitted) : X3 to '1';
X4 fitted;
X9 to 'A';
S3/1 to DEC
S3/2 to FULL, if a Comparator
board is fitted.
S3/3 Not applicable.
S3/4 to NO AUDIO, if an Audio
Decoder is fitted.

Clock and I/O (Reframer) : X2, X3, X4, X5, X6, X11 to 'N'.
X12-1 to A, B, C, D, E, F, for
Tone 1 as required (see
Installation Section 4.2.2);
X12-2 to G or H for Tone 2 =
silence; X24, X25 to F for Full
Reframing.

Audio Decoder : X4, X16, X17 to 'ab';
X3, X15, X18 to 'bc'.

DAC and Transformers : X3 to 'bc';
(internal mute control off);
X4 to 'ab'.
(internal mute control).

3.3 Sync Regenerator

Note: The Sync Separator and Quaternary ADC modules need to
be set up as a pair.

- (1) Connect the Sync Regenerator board via the extender board;
then switch on.
- (2) Apply a 100% colour bar signal to the SIS input on the
rear panel, and terminate with 75 ohms on the loop-out
socket.
- (3) Monitor Test Point X5 and adjust R91 so that the clamp
occurs 5 to $5.5\mu s$ after the leading edge of syncs at X4.
Also check that it is 1.5 - $2.1\mu s$ wide.
- (4) Monitor X8 and adjust R87 for a pulse width of
 $4.7 \pm 0.1\mu s$.
- (5) Connect a second oscilloscope probe to X6 and adjust R90
so that the clamp pulse at X6 begins 4.8 to $5.0\mu s$ after
the negative-going edge at X8. Also check that its width
is 1.5 - $2.1\mu s$.

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- (6) Monitor the clamp guard pulse at X9 and adjust its width by R89 to $3.5\mu s$ less than the line repetition period (ignoring the irregular repetition periods during the field synchronising sequence).
- (7) Monitor the video input on the rear panel and the line trigger pulse on X1-16a and adjust R69 for a delay of 245ns between the half-amplitude point of the leading edge of line syncs and the negative-going edge of the line trigger pulse (up to 300ns is permissible if 245ns cannot be achieved).

Note: This adjustment affects the Quaternary ADC module (see 3.4(7) and (8)).

- (8) Monitor the Field Trigger + at Pin 14c and Field Trigger - at Pin 14a and check that it is $4 - 6\mu s$ wide.
- (9) Monitor the Mixed Sync output at X1-15a. The Line Sync width should be $4.8 - 5.0\mu s$, as will be alternate equalising pulses. (For examination of the equalising pulses and broad pulses, trigger the oscilloscope from the Field trigger pulses at X1-14c).
- (10) Monitor Test Point X11 and check that the falling edge occurs less than $3.5\mu s$ after the leading edge of input sync and that the overall pulse length is greater than $1\mu s$.
- (11) Monitor A13 Pin 6 and adjust C32 for 0V.

Note: This is dependent upon the oscillator being locked to a correct line frequency source.

- (12) Monitor the following outputs from the board:

Clamp + at X1-12c : $1.5 - 2.1\mu s$

Sample + at X1-10a : five (for 625 lines) or
six (for 525 lines)
negative-going broad
pulses in the vertical
interval.

Regenerated Sync at X1-20a

Composite Blanking at X1-12a

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Field Blanking at X1-22a

Composite Gate at X1-21a
(Vertically blanked horizontal sync).

- (13) By removing and applying normal video, SIS video and video without field component, check the operation of the failure indicators H1, H2 and H3.
- (14) Feed a colour bar SIS signal to the input and adjust C45 so that the timing delay between the input colour bar sync and the output sync is the same as the delay between the input colour bar video and the output colour bar video.

3.4 Quaternary ADC

- (1) Connect a Stereo Sound in Syncs signal to the SIS Input on the back panel and terminate in 75 ohms on the loop-out socket.
- (2) Fit the board via an extender board and connect an oscilloscope via a probe to X7 and OV.
- (3) Switch on and adjust R6 for digits of 1.8V p-p.
- (4) If the board has not been previously tested, preset the delay line (X3) links to Positions 2 and 5 counting from the front to the back.
- (5) Connect the frequency counter to X11 and measure the oscillator frequency; it should be

11.9375MHz \pm 5Hz (PAL) or
12.020978MHz \pm 5Hz (NTSC).

Note that this is dependent on the coder being locked to the Asynchronous Data Processor, which in turn is phase-locked to line sync.

- (6) Check that the oscillator goes out of lock when the SIS input feed to the decoder is removed, and goes back into lock when it is replaced.

- (7) Monitor the marker pulse (the first of the digits in the sync pulse) at X7 and the SAMPLE pulses at X13, and adjust the falling edge of sample pulse to occur 5ns after the centre (peak) of the marker, by adjusting the second half of the delay line (X3) for coarse adjustment, and C29 for fine adjustment. The second half of the delay line is towards the rear of the board.
- (8) Monitor X3 (marker link) and A15 Pin 10 and check that the marker pulse falls 45ns before first rising edge at Pin 10. Adjust the first half of the delay line to achieve this as nearly as possible.

3.5 Bitstream Regenerator

- (1) Fit the Bitstream Regenerator board via an extender board, then switch on.
- (2) Monitor the frequency on X9.
- (3) Remove X11 and X12.
- (4) By applying 0V to X1 Pin 19c and +5V to X1 Pin 20C, then +5V to Pin 19c and 0V to Pin 20c, pump the frequency up and down; the resulting frequency range should be 8.736MHz $\pm 200\text{Hz}$. The range of 400Hz can be set by R48 and the centre frequency by C16. A tolerance of 5Hz is allowed on the low and high frequencies.
- (5) Switch off and replace the board.

3.6 Clock and I/O (Reframer)

Use the switches on the front of the module or a Remote Control unit to select Tone 1 or Tone 2 and free-running mode. Adjust R14 for 5824kHz $\pm 0.3\text{Hz}$ at X14. DO NOT ATTEMPT THIS UNLESS YOU ARE SURE THAT THE ACCURACY AND STABILITY OF YOUR FREQUENCY COUNTER IS ADEQUATE FOR THE TASK, i.e. BETTER THAN 1 PART IN 10^8 .

This frequency should be checked after the first year, and less frequently thereafter.

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3.7 Audio Decoder

- (1) Probe X5 and adjust C31 for a locked signal of 50 : 50 mark : space ratio.
- (2) Probe X7 and adjust C35 for a locked signal of 50 : 50 mark : space ratio.
- (3) Refer to Installation Section 4.2.2 and set Tone 1 for a line up tone suitable for your system, particularly noting the choice between UK headroom tones and EBU headroom tones. Select Tone 1 by means of the switches on the front of the Clock and I/O (Reframer) module or a Remote Control Unit, if connected.
- (4) Connect an Audio Level meter with 600 ohms input impedance to the Channel A output pins (35 and 17) on the Monitoring socket on the rear panel. If the intended use of the output of this module is to drive a high-impedance circuit, the input impedance of the meter should be set to HIGH IMPEDANCE. Adjust R17 for the correct output level according to the tone selected for Tone 1 as in (3) above.
- (5) Repeat (4) for channel B, connecting to pins 37 and 19 of the Monitoring socket and adjusting R43.

3.8 DAC and Transformers

- (1) Set the switches on the front of the Clock and I/O (Reframer) module (or use the remote control unit if fitted), to select Tone 1.
- (2) Connect an Audio Level meter with a high-impedance balanced input, to the Channel A output pins (2 and 3) on the Audio Output (Stereo) socket on the rear panel. Adjust R15 for the correct output level according to the tone selected for Tone 1 in section 3.7 (3) above..

Note: The 600-ohm terminating resistors R27 and R28 are normally fitted on the module. They may be disconnected if external terminations are to be used. The input impedance of the meter should be set accordingly.

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- (3) Repeat (2) for channel B, connecting to pins 4 and 5 of the Audio Output socket and adjusting R26.

3.9 Audio Comparator (if fitted)

Full information to follow.

3.10 Video Processor

- (1) Connect the Video Processor board via the extender board, then switch on.
- (2) Apply a 100% colour bar signal to the video input on the rear panel, and monitor Video Output 1 on the rear panel on an oscilloscope terminated in 75 ohms.
- (3) Monitor A7 Pins 13 and 5 and check that the pulse is 1.7 - 2.1 μ s wide in each case.
- (4) Monitor the video output and adjust:

R8 for a video amplitude of 700mV p-p.

R21 to set video and sync at colour burst blanking level.

R137 for a sync output amplitude of 300mV (625 lines)
or 286mV (525 lines).

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R91 to set the top of sync level with blanking.

R34 to set the output blanking DC level at 0V.

- (5) Monitor the output on a Vectorscope and adjust L1 to correct the phase of the burst with respect to the bars and check that the bars are correctly positioned in the boxes.
- (6) Carefully observe the output and check for correct adjustment of the above controls, readjusting where necessary.
- (7) Apply a suitable signal for checking frequency response to the video input and adjust C50 for a flat response.
- (8) Check the other video output for similar performance.
- (9) Monitor the buffered video output at Pin 4c and check for an output of approximately 1V p-p.
- (10) Switch off and replace the board.

3.11 General Notes

The decoder setting up is now complete. Specification measurements, signalling and remote functions can now be checked.

4. MODULE FAULT INDICATIONS

4.1 Coder

Digital Signal Processor	ROM Error RAM Error Control Error	Indicates failure of self-test on DSP programme ROM. Indicates failure of self-test on DSP internal RAM. Indicates that Control data input via rear panel is for undefined use, or for data or mono + data bitstream.
Clock and I/O	Ext Data Fail Ext Clock Fail Ext C ₀ Clock Fail Ext C ₀ Fail Signal Fail	Indicates no data detected from Auxiliary input on rear panel. Indicates no data clock detected from Auxiliary input on rear panel. Indicates no C ₀ clock detected from Auxiliary input on rear panel. Indicates no C ₀ detected from Auxiliary Input on rear panel. Indicates a request has been made, either locally or remotely, to select or lock to a signal missing according to the above indications.
Audio Decoder	Mute Parity Error	Indicates a mute has been applied to the decoded audio because the frequency of parity errors is too great for acceptable quality of audio. Indicates that the Audio Decoder has detected a parity error.
Monitor 1	Refer to separate section in the Coder or Decoder handbook (see Information Finder).	

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Async Data Processor	Insert Fail	Indicates failure to insert quaternary data into video.
	Buffer U-flow	Indicates underflow of the data buffer, i.e. too little data to maintain correct insertion rate.
	Buffer O-flow	Indicates overflow of the data buffer, i.e. too much data to maintain correct insertion rate.
	Clock Fail	Indicates failure of 728kHz clock from the Clock and I/O module.
	Data Fail	Indicates failure of 728kHz data from the Clock and I/O module.
	Standby	Indicates that standby line syncs are being output, probably due to failure of input video.
Sync Separator	Pulses Present	Indicates the presence of SIS data in the input video.
	Sync Fail	Indicates failure of input sync, i.e. no video.
	No Field Syncs	Indicates failure of input field syncs.

4.2 Decoder

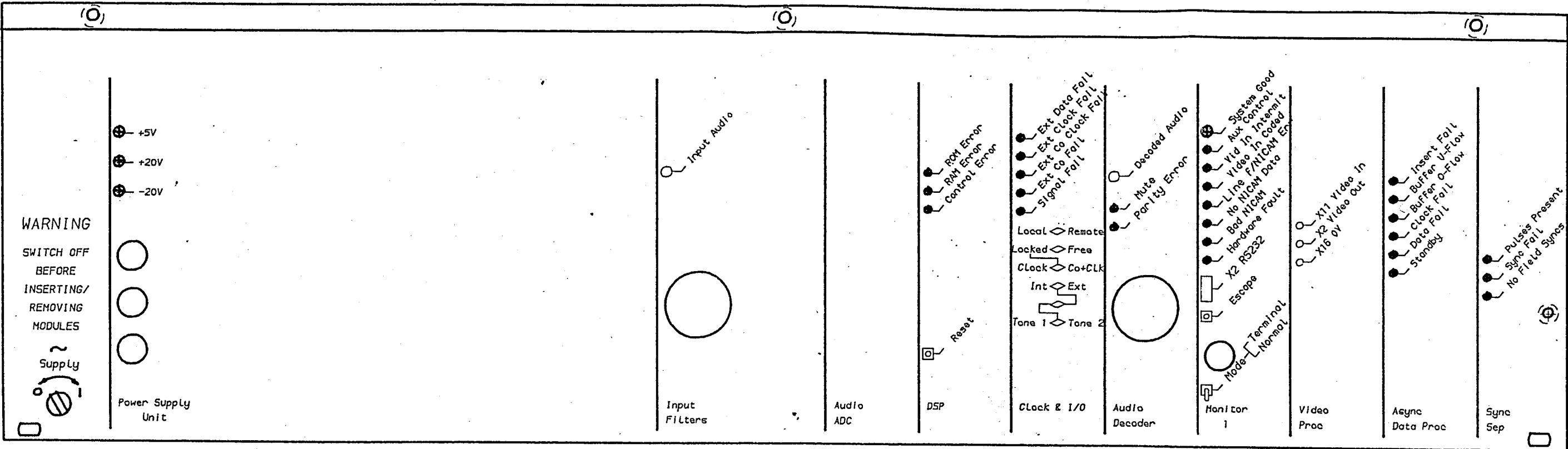
Sync Regenerator	Pulses Missing	Indicates the absence of SIS data in the input video.
	Sync Fail	Indicates failure of input sync, i.e. no video.
	No Field Syncs	Indicates that no field syncs are present on the input.

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Quaternary ADC	Amp Ref Data	Indicates that amplitude reference data is present in the input video, due to a coder fault.
	Data Fail	Indicates that no data is being detected.
	Justification Fail	Indicates that justified data has not been detected.
	Data Amp Low	Indicates that the detected data is 3dB, or more, low in amplitude, possibly due to low video amplitude.
	Data Amp High	Indicates that the detected data is 3dB, or more, high in amplitude, possibly due to high video amplitude.
	AGC Fail	Indicates that the micro-processor AGC system has failed and is being reset.
Data Recovery	Recovery Fail	Indicates a failure to obtain data from the Quaternary ADC.
Bitstream Regenerator	Clock Fail	Indicates failure of 728kHz clock from the module.
	Buffer O-flow	Indicates overflow of the data buffer, i.e. too much data to maintain correct output data rate.
	Buffer U-flow	Indicates underflow of the data buffer, i.e. too little data to maintain correct output data rate.

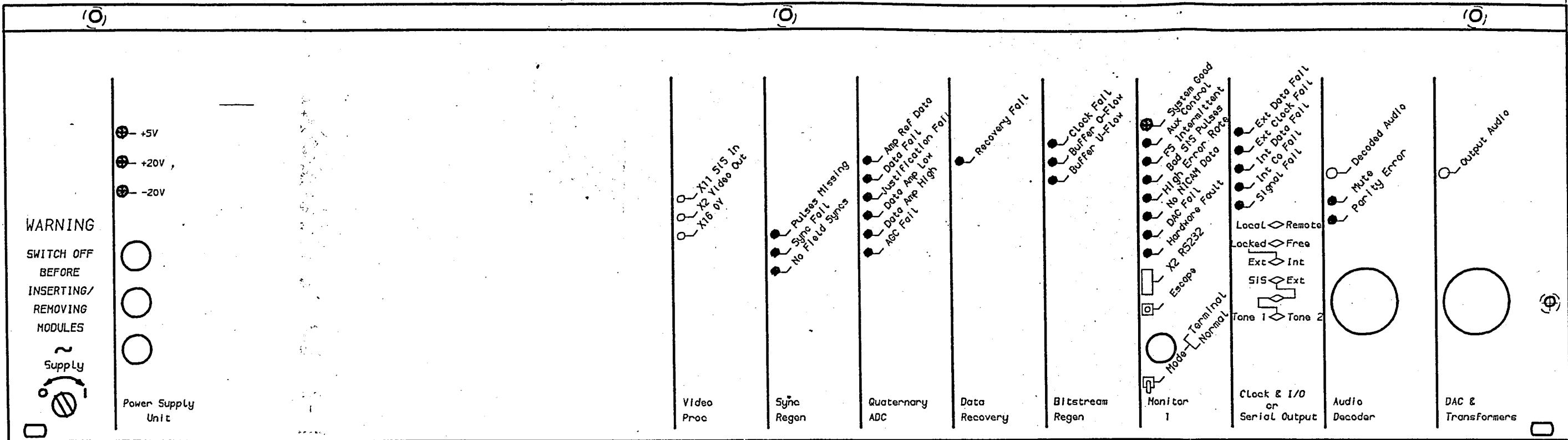
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Monitor 1	Refer to separate section in the Coder or Decoder handbook (see Information Finder).	
Clock and I/O (Reframer)	Ext Data Fail	Indicates no data detected from Auxiliary input on rear panel.
	Ext Clock Fail	Indicates no data clock detected from Auxiliary input on rear panel.
	Int Data Fail	Indicates no data detected from Bitstream Regenerator.
	Int C_0 Fail	Indicates no C_0 detected from Audio Decoder module which may indicate failure of Reframer.
	Signal Fail	Indicates a request has been made, either locally or remotely, to select or lock to a signal missing according to the above indications; or that there is Int C_0 fail.
	Int Tone	Tone 1 or Tone 2 is selected, either deliberately or due to reframing action.
Audio Decoder	Mute	Indicates a mute has been applied to the decoded audio because the frequency of parity errors is too great for acceptable quality of audio.
	Parity Error	Indicates that the Audio Decoder has detected a parity error.



TITLE		MODULE LAYOUT		8928 190 30001			
STEREO SOUND IN SYNC CODER							
ARCHIVE No		2	SH	10	SH	512-2	
DRAWN	N. BROWN	MECH	CHK	ELECT	CHK	APPROVED	
VARIAN T.V.T. LIMITED CAMBRIDGE						© 1989 DATE DRAWN 89-11-28 FORM A3	

D190_30001



TITLE		MODULE LAYOUT			
STEREO SOUND IN SYNC DECODER		8928 190 40001			
ARCHIVE No		2 SH	10 SH	512-2	
DRAWN	N. BROWN	MECH CHK	ELECT CHK	APPROVED	
VARIAN T.V.T. LIMITED CAMBRIDGE					
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