

SERVICE MANUAL

**STEREO SOUND IN SYNC
LDM 1903/1904**

DECODER

3913 985 09364



8928 190 40001

April 1996

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2ND EDITION, 1977 ("SAFETY REQUIREMENTS FOR RADIO
TRANSMITTING EQUIPMENT").

A M E N D M E N T R E C O R D S H E E T

STEREO SOUND IN SYNC DECODER

LDM 1904/00/01 (8928 190 40001)

Publication No. 3913 985 09364

All official amendments issued for this publication should be recorded in the following table.

AL No.	AL Date	Date Incorporated	By Whom	Remarks
1	Dec/90	Dec/90	-	General update incorporated.
2	Jan/91	Dec/91	TVT	New Clock and I/O (Reframer).
3	Aug/93	Aug/93	Harris	Audio Comp Option (BBC).
4	Apr/96	Apr/96	Harris	New ADC and Various.
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STEREO SOUND IN SYNC DECODER

LDM 1904/00/01 (8928 190 40001)

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STEREO SOUND IN SYNC DECODER

LDM 1904/00/01 (8928 190 40001)

GENERAL DESCRIPTION

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STEREO SOUND IN SYNC DECODER

LDM 1904/00/01 (8928 190 40001)

GENERAL DESCRIPTION

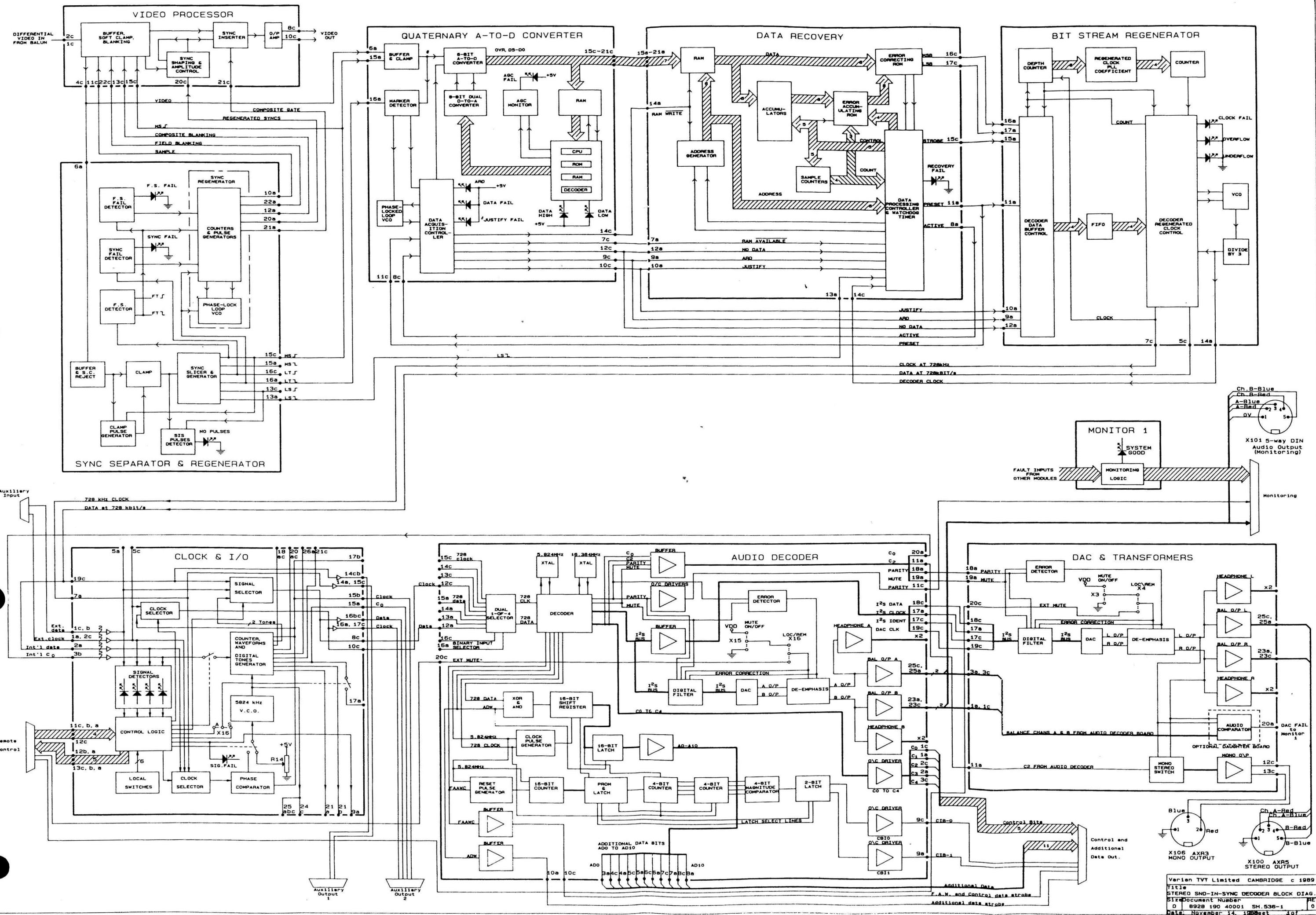
1. INTRODUCTION

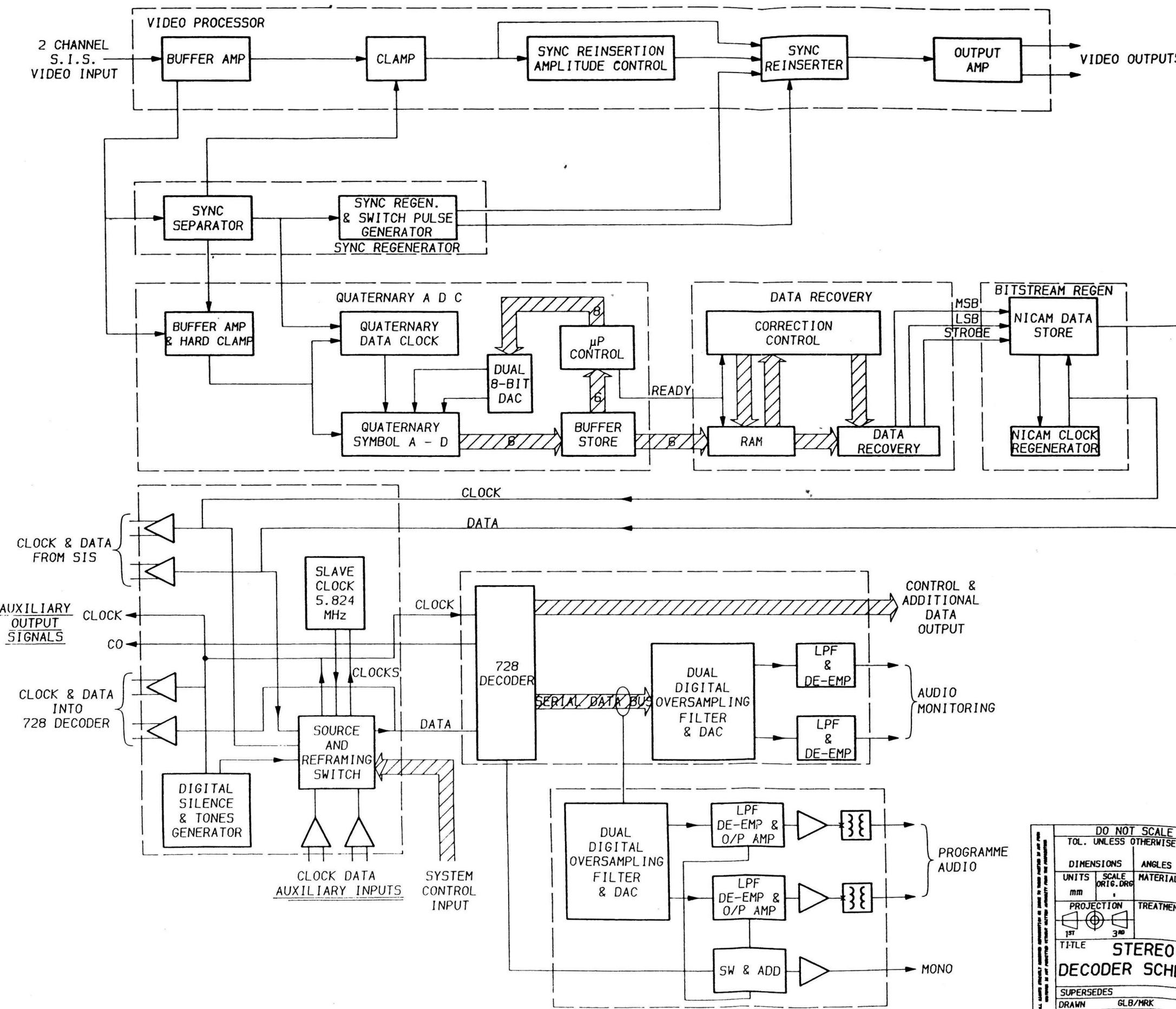
This volume contains detailed information on all the modules that form part of the Decoder. At this stage each section contains:

- (a) Detailed circuit description (FUNCTIONAL DESCRIPTION).
- (b) Circuit diagram.
- (c) Printed circuit board assembly drawing.
- (d) Parts lists.

- Notes:
- (i) In some cases the part numbers on the circuit diagram and the assembly drawing differ from that of the title of the section.
 - (ii) The item numbers appearing on the assembly drawing refer to the item numbers in the parts list.

An outline block diagram of the decoder is shown in Sh. 510-1, and interconnection of the main modules is shown in the functional block diagram, Sh. 536-1.





DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING	
TOL. UNLESS OTHERWISE STATED		SURFACE TEXTURE	1ST USED ON
DIMENSIONS		ANGLES	
UNITS	SCALE	HOLEs	
mm	ORIG.DRG.	MATERIAL	
PROJECTION		TREATMENT	
1st		3rd	
TITLE STEREO SIS DECODER SCHEMATIC B928 190 40001			
SUPERSEDES		1 SH 10 SH 510-1	X 89-05-15 2 91-01-10
DRAWN	GLB/MRK	MECH CHK	ELECT CHK
VARIAN T.V.T. LIMITED CAMBRIDGE © 1989 DATE DRAWN 89-05-15 FORM A2			

D190_40001

PSU MODULE3913 446 74920Contents

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C H A N G E S U M M A R YPSU MODULE3913 446 74920

(Issue 1)

References	Brief Description of Change	Documents Affected
PGV 3322 5.10.87	F2 changed from 1A, 2422 086 01021 to 1.25A, 2422 086 01023. F3 changed from 1A, 2422 086 01021 to 1.25A, 2422 086 01023.	Parts List Circuit Diagram
PGV 3613 02.04.90	C7 to C9, 100nF capacitors, 3913 200 10052 and C10 to C13, 100nF capacitors, 2012 310 00318 added to improve noise immunity.	Parts List Circuit Diagram Assembly Drawing
PGV 3963 06.07.90	R5, 0R51 resistor, 2113 256 02619 added in series with A3 + and R6, 0R51 resistor, 2113 256 02619 added in series with A3 - to reduce surge at switch-on.	Parts List Circuit Diagram Assembly Drawing Text
CA 37652 02.11.90 CA 38858 27.03.92 CA 41507 07.12.92 ECN10389 15.11.94	Mechanical and parts list changes.	Parts List
ECN11210 18.12.95	A3 on parts list should be KBPC602 rectifier 9338 816 50682.	Parts List

PSU MODULE3913 446 74920**1 FUNCTIONAL DESCRIPTION**

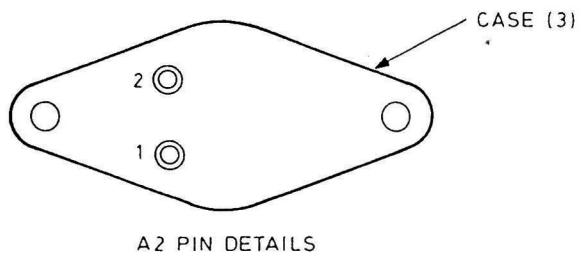
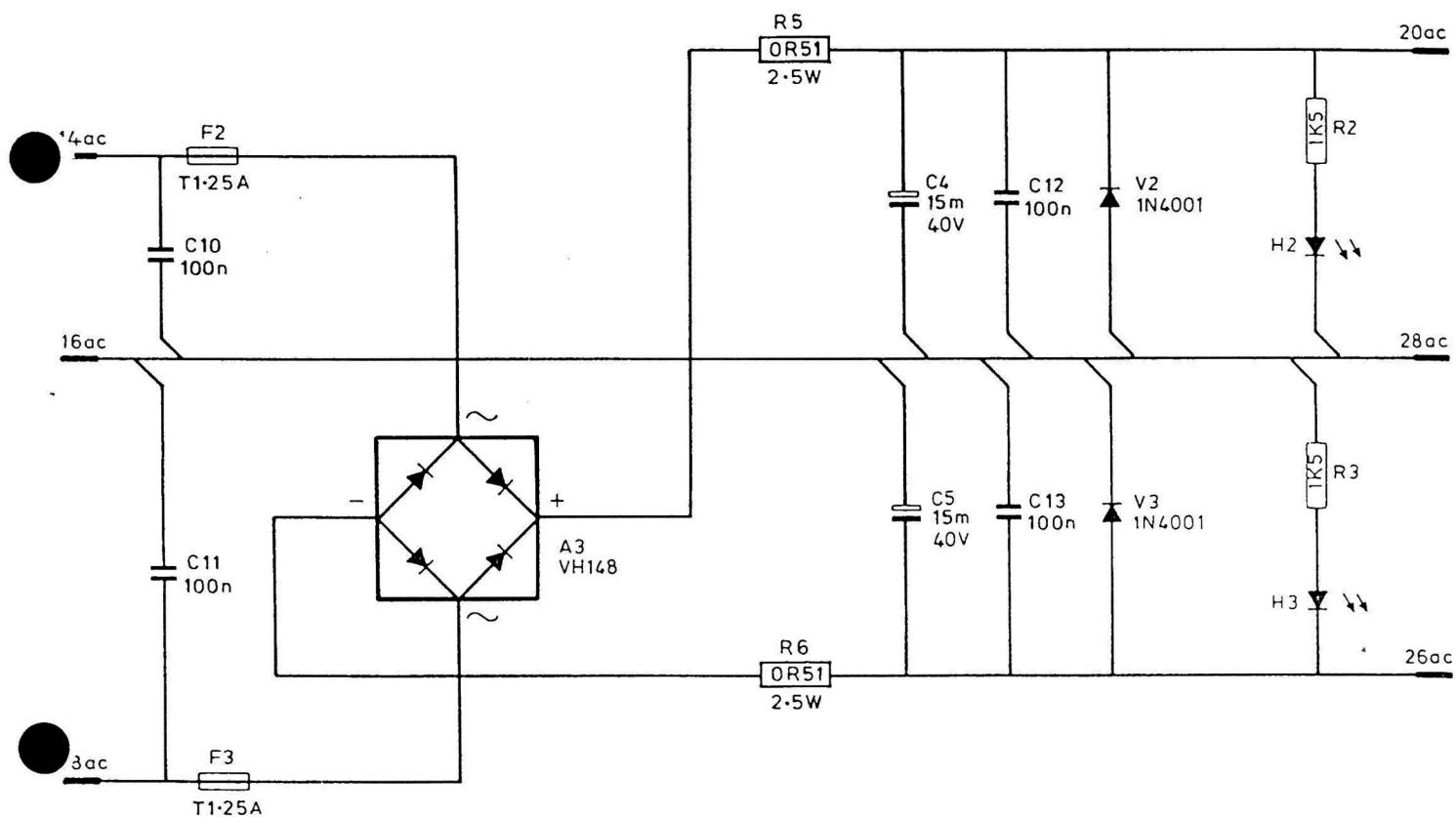
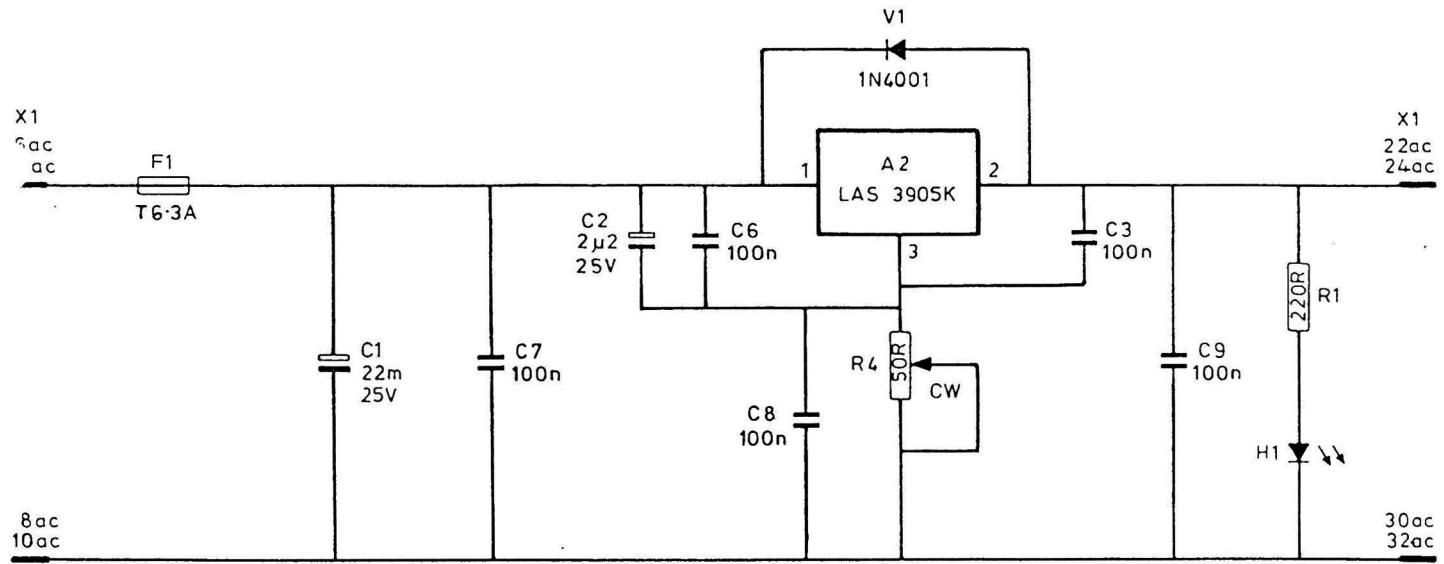
The Power Supply module works in conjunction with the mains transformer and bridge rectifier situated on the back panel of the equipment.

The +5V supply utilises an LAS 3905K regulator IC (A2). It is rated at 8A output and has internal current limiting and thermal shutdown. It is also protected by fuse F1 which, in practice, will normally blow before either the current limit or thermal limit is reached. It is supplied from a 9.1 - 0 - 9.1V centre-tapped secondary of the mains transformer, full-wave rectified by the diode bridge mounted on the back panel. The 5V output voltage is adjusted by R4. Refer to the System Setting-up Instructions in the System Description and User Information Manual.

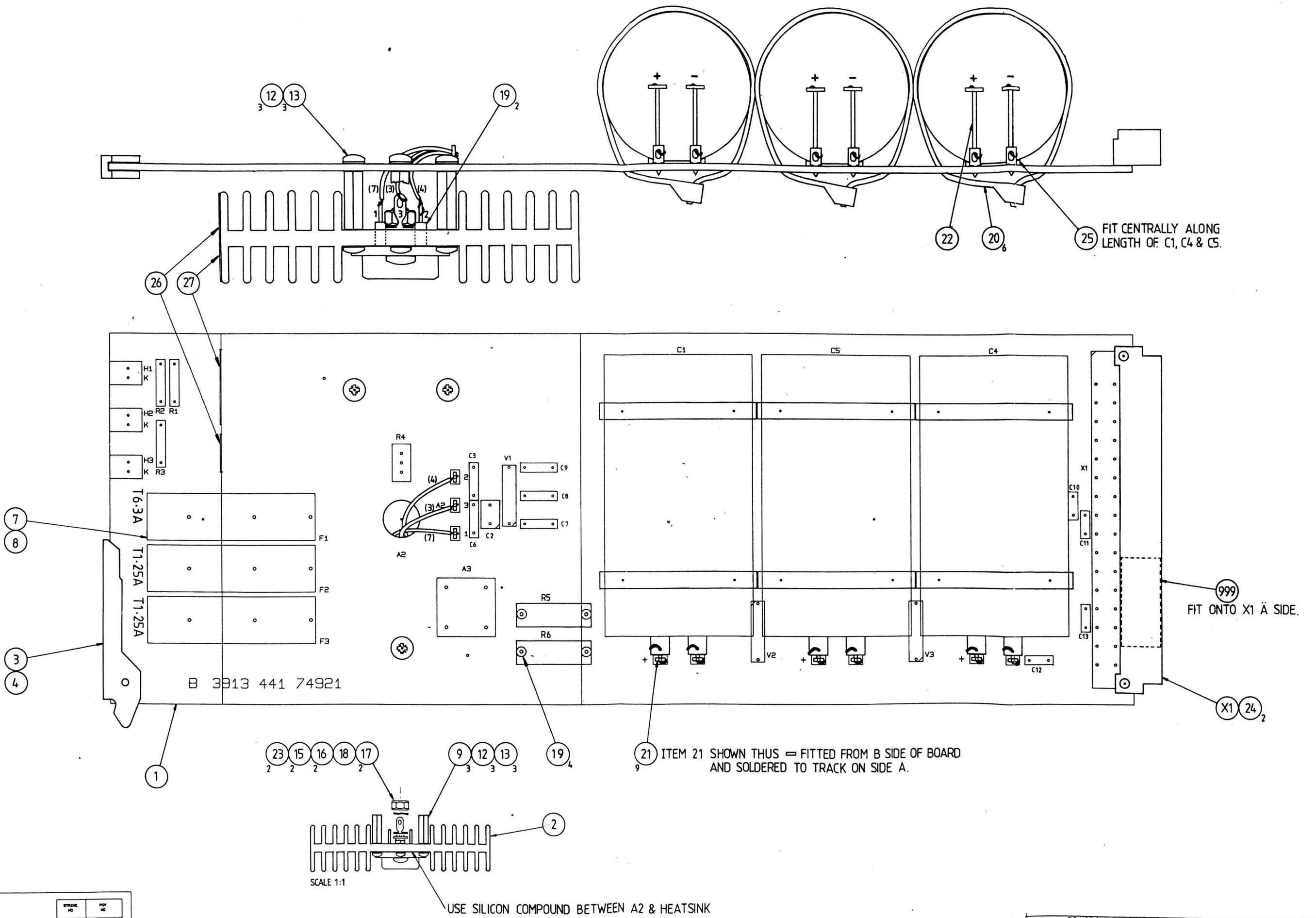
The $\pm 20V$ is unregulated. The full-wave bridge rectifier A3, on this board, is supplied from a 16.3 - 0 - 16.3V centre-tapped secondary of the mains transformer. The loaded output voltages should be within 1V of the nominal 20V, if the mains input voltage is at its nominal value. If either of the fuses F2 or F3 should blow, the surviving one will carry the whole load and also blow almost immediately. R5 and 6 reduce the switch-on surge, thus reducing the likelihood of F2 or 3 blowing unnecessarily.

2 FAULT FINDING

If a single diode of a bridge rectifier should fail, the problem may not be immediately apparent, but will be revealed by checking the frequency of the ripple voltage across C1 or C4/C5, which will be 50Hz instead of 100Hz.



POWER SUPPLY UNIT ASSEMBLY CIRCUIT		3913 446 7492	SH.130-1	880113 3322 1 890330 CA31394 1 890330 3613 1 900709 3963
DRAWN ISI LTD	CHK C.S. Clement	APPROVED		
PYE T.V.T LIMITED CAMBRIDGE © 1987		DATE DRAWN 870127		FORM A3



STRIKE NO	PW NO
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NOTE: STRIKE LEVEL SIGN HERE MUST NOT BE CONFUSED WITH THE LEVEL DATED SIGN ON ASSOCIATED DRAWINGS & PARTS LIST.

1. APPLY STRIKE PLATE NO 3913 441 74921 WITH THIS ASSEMBLY IN POSITION INDICATED

2. STRIKE PLATE TO LEVEL INDICATED IN THIS SET.

DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING	
TOL UNLESS OTHERWISE STATED		SURFACE TEXTURE	
UNITS MM		ANGLES	HOLDS
SCALE	DEGR/DGR		
2:1			
PROJECTION		TREATMENT	
SEE SEPARATE PARTS LIST		SEE 3913 982 90010 CODE C.	
TITLE		3913 446 7492	
SUPERSEDES		1976 10 09	
DRAWN BY DJF		1976 10 12	
MECH CM		ELECT CM	
1976 10 14 PGV 3963		APPROVED	

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3913 446 69530
3913 446 67580

DECODER VIDEO PROCESSOR

3913 446 69530 (PAL)
3913 446 67580 (NTSC)

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C H A N G E S U M M A R YDECODER VIDEO PROCESSOR3913 446 69530 (PAL), 3913 446 67580 (NTSC)

References	Brief Description of Change	Documents Affected
PGV 3250 20.5.87	<u>On PCB 3913 446 74760:</u> R89 changed from 8k2, 2322 156 18202 to 6k2, 2322 156 16202 to change A7a pulse width from nominal 2.54µs to 1.9µs (test limits to be 1.7µs to 2.1µs). Connection to V3 base changed from R7/V4c to 4Ve/R12/C2. Test Point X12 added at A7 Pin 13. Test Point X13 added at A7 Pin 5.	Parts List Circuit Diagram Assembly Drawing Text
PGV 3283 28.9.87	<u>On PCB 3913 446 74760:</u> C71 changed from 82p, 100V ceramic to 39p, 100V, ceramic, 2222 683 34399. C91, 100p, 100V, ceramic, 2222 683 34101 added between V35/V36 negative and V37/V38 positive.	Parts List Circuit Diagram Assembly Drawing
PGV 3335 PGV 3341 5.11.87	<u>On PCB 3913 446 74760:</u> C90 changed from 100p, 2222 683 34101 to 1000p, 2222 630 19102. R15 changed from 10R, 2322 156 11009 to 56R, 2322 156 15609.	Parts List Circuit Diagram
PGV 3719 10.08.89	<u>On PCB Assembly 3913 466 74760:</u> L/C combination L7/R145/C91 inserted between the junction of V29 base and R59 and the junction of R60/C50.	Circuit Diagram Parts List Assembly Drawing
PGV 3766 16.10.89	R52 and R53, 74R1, changed from 2322 163 47419 to 2113 112 03105.	Parts List
CA 32992 28.02.90	R9 on circuit diagram changed from 1k to correct value of 360R.	Circuit Diagram
	<u>Correction:</u> On PGV 3719 above, C91 incorporated correctly as C92.	Circuit Diagram Assembly Drawing Parts List
PGV 4392 18.04.91	L1 changed to 3913 449 51400.	Parts List
CA 36470 30.03.90	CA 36323 PGV 4514 CA 41507 11.06.91 06.09.91 07.12.92	Various mechanical changes. Parts List
PGV 4845 07.05.92	Potentiometers replaced with different type.	Parts List
CA 41531 14.04.93	C9 replaced with higher voltage type.	Parts List

DECODER VIDEO PROCESSOR

3913 446 69530 (PAL)
3913 446 67580 (NTSC)

1. FUNCTIONAL DESCRIPTION

Sound-in-Sync video input to the module is via the differential input stage comprising A1 and its associated components, which provides a high degree of common-mode rejection for the incoming video signal. V46 provides a buffered output immediately after A1 to supply video to the Sync Regenerator (3913 446 67370) and Quaternary ADC (3913 446 74810) modules. The output of A1 also passes to a variable-gain stage consisting of V1 and V2, the gain being adjusted by R8. The output from this stage goes to a monitoring point on the front of the board, and to the video clamp circuit comprising V3, V4, the clamp capacitors C2 and C3 and the clamp transistor, FET V5. This clamp stage works by the clamping voltage being set on C3 by the clamp pulse, and C2 then gradually reaching this voltage during the line period, via R14. This means that no steps or spikes are introduced onto the video signal by the clamp pulse. The incoming sound-in-sync video, having been clamped, passes to a two transistor buffer stage comprising V10 and V11, and then to a blanking stage and a reinserted sync amplitude control circuit.

Clamp pulses for V5 (and also for the regenerated sync clamp transistor V20 - see below) are generated by A7 and A8, which themselves are fed by positive-going mixed sync and field blanking from the sync regenerator module. During normal video time (i.e. not field blanking), line sync trailing edges trigger A7a. This has a time constant such that its output is high until after the start of the colour subcarrier reference burst following the line sync, and when its output once again goes low, A7b is triggered to produce a clamp pulse of approximately $1.9\mu s$ width, clamping black level video during the latter half of the burst to a DC level set by R21 (nominally 0V). Clamping occurs during the end of burst because the effect of link distortions can be to cause line-by-line black level changes immediately following the sync. These, however, should be minimal by the time video is clamped. During field blanking, the output of A7a is prevented from reaching the input of A7b; instead, A7b is triggered directly by sync trailing edges. Clamp pulses are fed to the appropriate clamp transistor by V8/V9 and V23/V24, which provide level shifting to drive the FET gates.

Regenerated mixed sync for insertion into the video to replace the quaternary data is generated by the Sync Regenerator, buffered by A12c and V16, and passed through a 1.5MHz Gaussian filter Z1, which provides sync shaping. V17 provides a low-impedance drive to the sync amplitude adjustment FET, V18. This FET acts as a voltage-controlled resistor,

and so a potential divider across the regenerated sync path is formed by R82 and V18, control of V18 being via A6 (see below). V19 buffers the sync for clamping by V20 and the clamp capacitor C26, the clamp pulses for V20 being as previously described. After passing through the cascode stage A5, the syncs are ready for insertion into the video by A4, and they also pass to V25 for sync amplitude control.

Sync amplitude control is provided by comparing the amplitude of incoming and regenerated sync, and adjusting the regenerated sync amplitude until they match. V25 (negatively) charges C30 every line to the sync tip voltage of the regenerated sync, and R72 provides a discharge path for this capacitor, with a time constant chosen to give no significant charge decay during line time. Since incoming video at this point contains quaternary data, comparisons for means of adjusting sync amplitude can only be carried out during the field interval, when only a small section of each broad sync carries data. This is achieved using V40, under control of the Sync Regenerator, via A12a. During the periods when quaternary data is present in sync, V40 is switched on, holding the base of V26 to OV. During broad pulses in the field interval, V40 is switched off, allowing the broad pulse tips to negatively charge C31. The charge is then held until the next field interval. The voltages on C30 and C31 are compared by the comparator A6, and the resultant output voltage from A6 used to control the resistance of V18.

To remove the line-by-line black level changes caused by link distortions mentioned earlier, incoming video must be blanked before the new sync is inserted. Blanking is achieved using the diode bridge V35 to V38, switched by V12 and V13 under control of the Sync Regenerator, via A12b. Anti-phase signals at the junctions of V35/V36 and V37/V38 make the junction of V35/V38 OV during line blanking, effectively grounding the video signal and giving black level a stable DC value. Quaternary data is also partially blanked, and to prevent blanking of the burst, L1 and C9 (with C62 for NTSC) in parallel form a subcarrier reject network. However, since this network causes unacceptable losses when blanking is not taking place, V41 is normally on to short circuit the network, except during blanking. L1 is adjustable, and must be tuned for correct burst-to-active-line subcarrier phase.

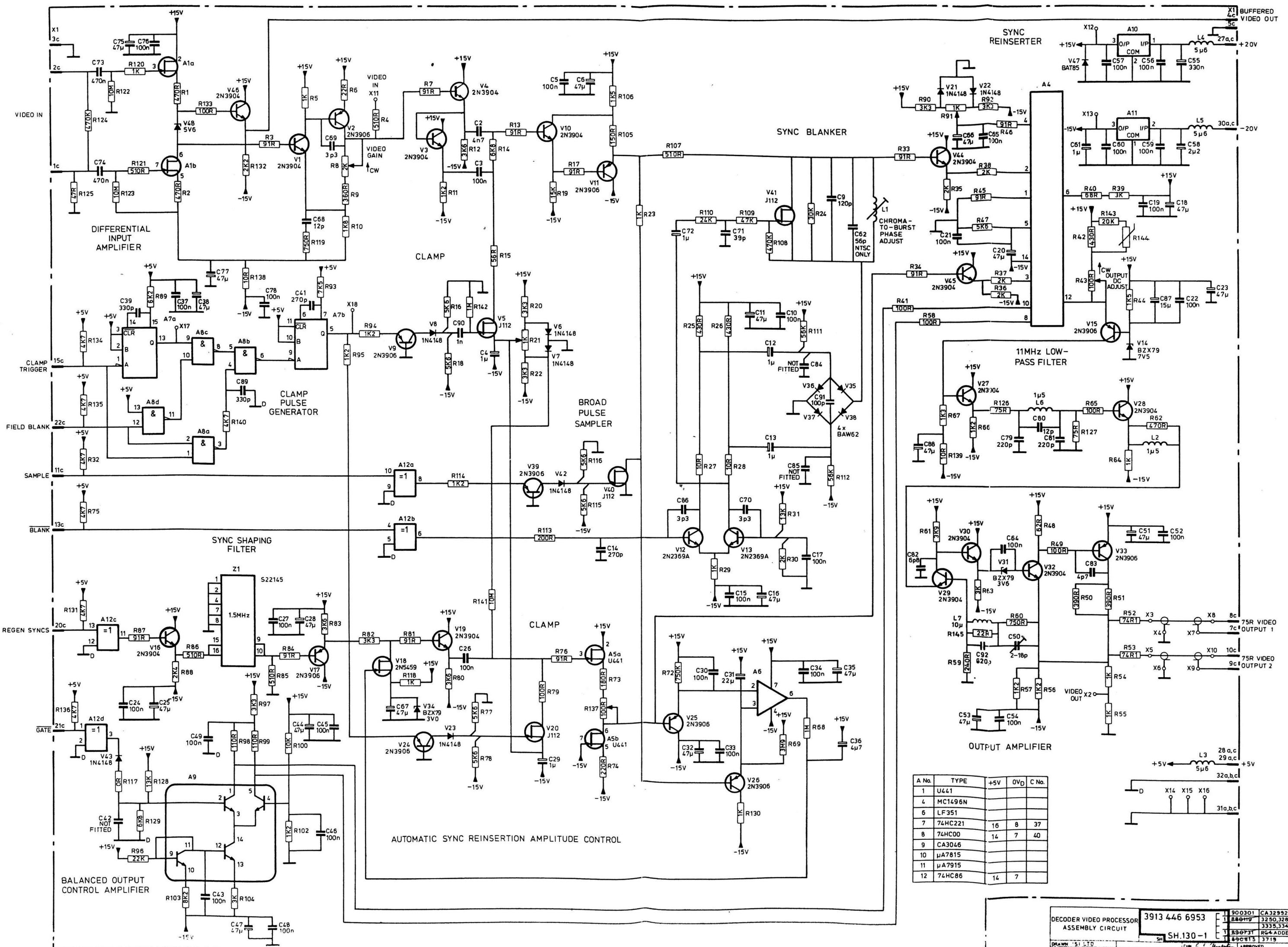
The blanked sound-in-sync video and regenerated sync are fed into the balanced modulator A4 by V44 and V45 respectively. The switching of A4 is controlled by an INSERT command from the Sync Regenerator (low to insert sync). A9 is connected as a long-tailed pair of transistors to give differential switching signals to switch A4, which inserts the regenerated sync to replace the quaternary data in the sound-in-sync video. As the base of V15 is held at a constant voltage by V14, pin 6 of A4 is also at a constant voltage, and so a constant current flows through R42 and R43. This current is divided at A4 pin 6, part of the current flowing into A4 and the rest, representing the video signal, flowing down through V15 and developing a voltage across R67.

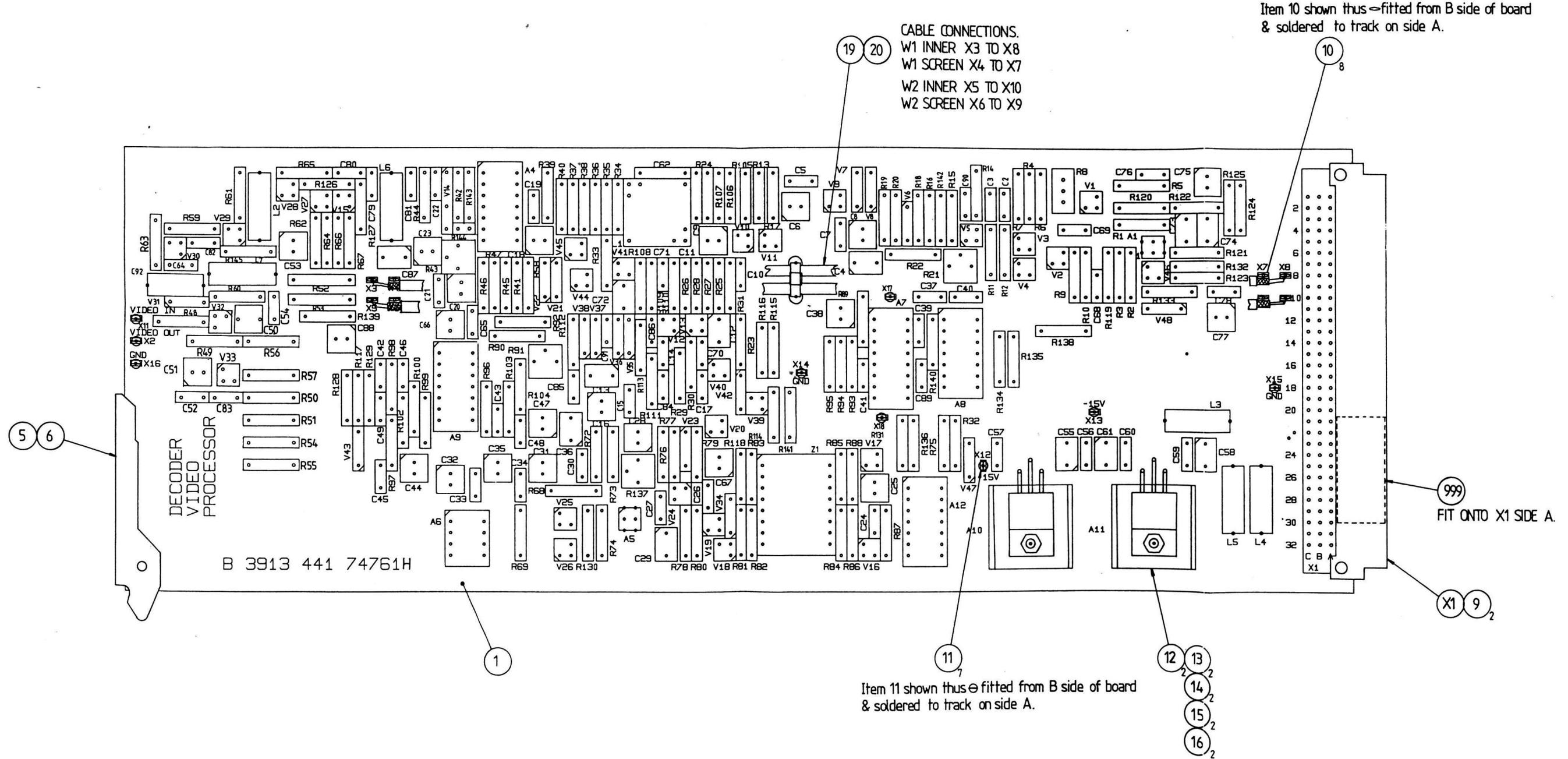
The now normal video is driven into an 11MHz filter by V27, and then into the base of V28, which is the non-inverting input of the video output amplifier. The complete amplifier consists of V28 to V33 and their associated components. V33 is a current booster for V32 to provide two 75-ohm outputs. The stage gain is fixed by R59 and R60 to give 1V p-p video outputs, and the frequency response is set by C50, R60 and C50

3913 446 69530
3913 446 67580

being a negative feedback path to the inverting input of the amplifier.

Power to the digital sections of circuitry (+5V) is provided from the main rack power supply. +15V and -15V is provided from regulators A10 and A11, which are fed from +20V and -20V, smoothed but unregulated, once again from the rack power supply.





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DIMENSIONS		ANGLES	HOLDS
UNITS	SCALE	MM	INCH
2-1		SEE SEPARATE PARTS LIST.	
		SEE 3913 982 90010 CODE C.	
PROJECTION		TREATMENT	
W 3rd		SEE 3913 982 90010 CODE C.	
DECODER VIDEO		3913 441 7476	11-18704-02
PROCESSOR ASSY DRG		11-18705-18	11-18707-30
SUPERSEDED		11-18708-29	11-18709-29
DRAWN BY		TP	MACH CHG
REVISED BY			ELECT CHG
APR-1967			APR-1967

3913 446 67330
3913 446 67340

SYNC SEPARATOR AND REGENERATOR

3913 446 67330 (PAL)
3913 446 67340 (NTSC)

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1.5 Clamp Pulse Generation	Sh. 595-2
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SYNC SEPARATOR AND REGENERATOR

3913 446 67330 (PAL), 3913 446 67340 (NTSC)

References	Brief Description of Change	Documents Affected
PGV 3244 6.5.87	<u>On PCB 3913 446 74770:</u> C15 changed from 100n, Polyester to 10n, ceramic, 2222 629 19102. C56, 150p, 2222 683 34151 added. R91, potentiometer, 10k, 2111 369 00085 added. R92, 27k added. R24 changed from 56k to 47k. R25 changed from 36k to 27k. R88 changed from 56k to 47k.	Parts List Circuit Diagram Assembly Drawing
PGV 3260 27.5.87 *	<u>On Sync Regenerator (Basic) 3913 446 67370:</u> C58, 39p added between A15 Pins 3 and 5. C59, 100p added between A15 Pin 5 and OV, but not fitted; on circuit diagram C59 reads '100p - NOT NORMALLY FITTED'. * Change applicable to BBC contract.	Parts List Circuit Diagram Assembly Drawing
PGV 3240 16.11.87	<u>On Sync Regenerator (Basic) 3913 446 67370:</u> Order of contents of the FPLS A18 changed; A18 changed from 3913 036 60200 to 3913 036 60210.	Parts List Circuit Diagram
PGV 3361 8.1.88	<u>On PCB 3913 446 74770:</u> R95, 4k7, 2322 156 14702 added in series with A3 Pin 3. C60, 5p6, 2222 683 09568 added between A5 Pins 3 and 4.	Parts List Circuit Diagram Assembly Drawing
PGV 3405 4.3.88 *	<u>On PCB 3913 446 74770:</u> C16 and C17 changed from 180p, 2222 683 58181 to 820p, 2222 630 19821. C24 changed from 120p, 2222 683 34121 to 1n2, 2222 630 19122. R31 and R33 changed from 10k, 2322 156 11003 to 2k2, 2322 156 12202. R45 changed from 39k, 2322 156 11903 to 3k9, 2322 156 13902. A16 Pins 3 and 11 disconnected from +5V and connected to A16 Pin 2. * Applies to assemblies with Issue 1C printed boards.	Circuit Diagram Parts List
PGV 3396 89.01.31	<u>On PCB 3913 446 74770:</u> C60, 5p6 deleted from the parts list. R95, 4k7 deleted from the parts list. C15, 10n deleted; C15 4n7 added. R29 changed from 330k to 1M, 2322 156 11005. (This countermands PGV 3361).	Parts List Circuit Diagram Assembly Drawing

C H A N G E S U M M A R Y

SYNC SEPARATOR AND REGENERATOR

3913 446 67330 (PAL), 3913 446 67340 (NTSC)

References	Brief Description of Change	Documents Affected
PGV 3553 (Issue 3) 89.01.31	C60 removed from 3913 446 74770 and added to 3913 446 67330 and 67340 (see PGV 3396). <u>On PCB 3913 446 74770:</u> C60 changed from 5p6 to 100p, 2222 683 34101 <u>On Sync Regenerator (basic) 3913 446 67370:</u> C27 changed from 82p to 150p, 2222 683 34151.	Circuit Diagrams Parts Lists
PGV 3611 89.02.07	<u>On PCB 3913 446 74770:</u> R96, 300R, 2322 156 13001 added between A14 Pin 6 and X1 Pin 15a. This makes 3913 446 67330 Issue 6 and 3913 446 67340 Issue 4.	Circuit Diagram Parts Lists Assembly Drawing
PGV 3754 89.10.05	C45 changed from 4-40pF to 5-57pF, 2222 809 08003.	Circuit Diagram Parts List
PGV 3764 89.10.12	V14, transistor 2N2369A, 9330 295 71112 added. V15 and V16, transistors 2N3906, 9330 791 70702 added. V23, diode MV2109, 9332 795 10702 added. V24, diode IN4148, 9330 839 90112 added.	Circuit Diagram Assembly Drawing Parts List.
PGV 3782 89.11.27	A18 is re-programmed to 3913 036 60580 with new PLS105 program. A6 Pin 5 disconnected from existing network and connected to A18 Pin 17. R101 deleted. R24 changed from 47k to 33k, 2322 156 13303. A6a pulse width is set to 42 $\pm 5\mu s$ by means of R87.	Circuit Diagram Assembly Drawing Parts List Text
PGV 3782 Issue 2 08.01.90	A18 reprogrammed to 3913 036 60570.	Parts List
PGV 3864 30.03.90	R30, 10k, 2322 156 11003 changed to 1k, 2322 156 11002 to improve reliability of circuit operation with attenuated input signals.	Circuit Diagram Parts List
PGV 3855 30.03.90	A14 pin 1 disconnected from X8/A6 pins 7 and 11. V27, V28 and V29 diodes BAW62, 9331 012 20112 added: anodes connected to A14 pin 1. Cathodes: V27 to A5 pin 11; V28 to A6 pin 5/ A18 pin 17; V29 to A5 pin 8/A6 pin 9. R112, 39k connected between A14 pin 1 and +5V.	Circuit Diagram Assembly Diagram Parts List

C H A N G E S U M M A R Y

SYNC SEPARATOR AND REGENERATOR

3913 446 67330 (PAL), 3913 446 67340 (NTSC)

References	Brief Description of Change	Documents Affected
PGV 3944 01.05.90	R30, 1k, 2322 156 11002 changed to 4.7k, 2322 156 14702. R112, 39k, 2322 156 13903 changed to 10k, 2322 156 11003.	Circuit Diagram Assembly Drawing Parts List
PGV 3961 02.05.90	V30, A23, R113, R122, C70 to C73 added as redesigned Sync Fail Detector: V30, transistor BC559, 9331 977 60112; A23, LM311, 9332 233 10682; R113, 470k, 2322 156 14704; R115, R117, 82R, 2322 156 18209; R116, 3k, 2322 156 13002; R114, R118, R119, 10R, 2322 156 11009; R120, 9.1k, 2322 156 19102; R121, 1k, 2322 156 11002; R122, 22k, 2322 156 12203; C70, 10nF, 2222 629 19103; C71, C72, C73, 100nF, 2012 310 00318. Capacitors C74 to C80, 100nF, 2012 310 00318 added between +5V and 0V supply pins of A5, A7, A9, A14, A19, A20 and A21. OV test point, 2413 015 02201 added near A4,5. R97 replaced by X13, 1x2 Berg Header, 3913 445 50110. Socket 2-way, 2422 549 26016 added (X13). <u>The above changes are incorporated in new PCB 3913 446 75480 that replaces 3913 446 74770.</u>	Circuit Diagram Assembly Drawing Parts List
PGV 3990 08.06.90	R35, 100k, 2322 156 11004 changed to 1M, 2322 156 11005. R117, 82R, 2322 156 18209 changed to 330R, 2322 156 13301. R115, 82R, 2322 156 18209 changed to 56R, 2322 156 15609. C44, 47pF, 2222 683 34479 changed to 68pF, 2222 683 34689.	Circuit Diagram Parts List
PGV 4053 16.07.90	C18, 330nF, 2012 310 00322 changed to 330nF, 2012 310 03124. C34, 47nF, 2012 310 00316 changed to 47nF, 2012 310 03122.	Parts List

C H A N G E S U M M A R Y

SYNC SEPARATOR AND REGENERATOR

3913 446 67330 (PAL), 3913 446 67340 (NTSC)

References	Brief Description of Change	Documents Affected
PGV 4104 21.08.90	C27 reduced from 150pF to 120pF.	Circuit Diagram Parts List
PGV 4159 05.10.90	C44 increased from 68pF to 150pF.	Circuit Diagram Parts List
PGV 4327 04.02.91	R9 changed from 1M8 to 1M0.	Circuit Diagram Parts List
PGV 4845 07.05.92	Potentiometers replaced with different type.	Parts List
CA 41507 07.12.92	Mechanical changes.	Parts List
PGV 5055 05.03.93	R115 changed from 56R to 27R. R117 changed from 330R to 180R.	Circuit Diagram Parts List
ECN10573 01.03.95	Mechanical change.	-
ECN11051 22.09.95	Correction to setting up procedure in System Manual.	System Manual

3913 446 67330
3913 446 67340

SYNC SEPARATOR AND REGENERATOR

3913 446 67330 (PAL)
3913 446 67340 (NTSC)

1. FUNCTIONAL DESCRIPTION

1.1 General

The same printed circuit board is used for both of the above assemblies; differences between PAL and NTSC are small. The Sync Regenerator (for Decoders) uses the circuitry of the Sync Separator (Coders) plus additional circuitry to generate syncs in synchronism with the incoming video or sound-in-sync signal.

1.2 Input Buffer and Subcarrier Rejection

The video or sound-in-sync input signal is AC coupled into A3. R4 and R3 set the gain to about 3. C6 provides high frequency roll-off. L2 and C9 (+ C8 for NTSC) give rejection of colour subcarrier, necessary to prevent false triggering of the sync detector on low luminance, high chrominance signals. R5 dampens the tuned circuit to reduce ringing on luminance steps.

1.3 Clamping Circuit

Transistor V1 provides a low impedance source before the clamp capacitor C10. Clamping of black level to OV is achieved during the back porch with FETs V2 (soft clamp) and V5 (hard). Generation of the clamp pulses is described in Para 1.5.

1.4 Sync Pulse Generation

The two matched FETs of A4, connected in cascode, buffer the clamped video signal without changing the DC level. The output of the Sync Slicer A5 changes state as the video signal on pin 3 passes through the sync half-amplitude voltage, which is supplied to pin 4. The sync tip voltage is first detected by V10 (aided by V26), stored (with V_{be} offset) on C18, further smoothed by R36/C19, corrected for V_{be} offset by V11 (aided by V30) and halved by R38 and R21.

A6a is triggered by the output of A5 and in turn triggers A6b. The $5\mu s$ pulses fed back from A6b to A5 prevent A5 responding to sound in sync digits if they are present in the input signal. The other input to A6a is from A18, and is a pulse which remains low from shortly after a leading edge of line sync is detected to within $1\mu s$ of the time that the next leading edge is due. Thus A6a cannot respond to mid-line equalising and broad pulse edges nor to spurious sub-black during active line time. Thus A6a and A6b generate line trigger and line sync pulses undisturbed by the field sequence or by spurious sub-black pulses. The mixed sync pulses at A5 Pin 9 and at Pin 15a of the board connector have alternate equalising pulses widened to $5\mu s$ by the feedback from A6b, and so are non-standard in this respect. The negative-going line trigger pulses on Pin 16a of the board connector are delayed by R69 and C44 so that the LTedge is delayed by 245 - 300ns relative to the leading edge of sync in the incoming video. C60 is fitted at the input to A5 to reduce the effects of noise.

1.5 Clamp Pulse Generation

The video from the subcarrier rejection circuit is passed to the emitter follower V8 with a little additional filtering by R26 and C14. V9 is a simple sync pulse detector which triggers the non-retriggerable monostable A8a to produce a $1.8\mu s$ clamp pulse from the trailing edge of sync. During start-up conditions these clamp pulses are fed to V2 via A7c and V4. This clamps the video adequately for the sync slicer to start to work, whereupon the Normal Clamp Pulse Generator A8b operates. The Clamp Pulse Changeover Control A9a is a retriggerable monostable, triggered via A7d when the Start-up and Normal clamp pulses occur at the same time. Then Normal clamp pulses from A8b are fed to both soft and hard clamps, through A9a's control of A7a, A7b and A7c. When the video input fails, A9a is no longer triggered, its outputs change state after $670\mu s$ and clamping falls back to the Start-up Clamp Pulse Generator. A8b is triggered by the trailing edge of the sync slicer output, via A22b. A22b is a non-retriggerable monostable which is set to give a $62\mu s$ pulse, and therefore prevents the production of a clamp pulse from spurious sub-black during picture time. During the field sequence when there are half line pulses, A22b can still only trigger once per line, so maintaining a steady clamp efficiency apart from slipping nearly half a line at the beginning of the broad pulses and just over half a line at the end of the field sequence. In order to check the $670\mu s$ pulse length of A9a, X7 is provided with 'Normal' and 'Test' positions; in 'Test' A9a receives field trigger pulses so that it is not retriggered before the end of its natural pulse length.

1.6 Sync Fail Detector

The Sync Fail Detector A23 is a voltage comparator which takes the detected Sync Tip voltage on V11e and compares it with a fixed voltage produced by the potential divider consisting of R115 and R116. R120 and R117 provide hysteresis so that it will change state decisively. Its output controls the Sync Fail indicator LED H2, and provides outputs to other modules.

1.7 Field Trigger Generation

The Mixed sync pulses from A5 are fed to the 'Field Sync Detector' via A14d. Between sync pulses, C22 is kept discharged by V12. When a pulse is present V12 is turned off and C22 starts being charged by current through R42. If the pulse is short i.e. a line sync or equalising pulse, C22 will not have time to charge to the turn-on voltage of V13. If the pulse is a broad field pulse, V13 will be turned on and monostables A10a and A10b will be triggered. The pulse width ($350\mu s$) of A10a masks the second and following broad pulses. A10b provides the desired pulse width of $4.5\mu s$.

1.8 Field Sync Fail Detector

The field sync pulses are passed to monostable A9b and continuously retrigger it, keeping its \overline{Q} output low. If these pulses stop, \overline{Q} will go high after 55ms and LED H3 will light to indicate the fault.

1.9 Sound Pulses Present Detector

A21 is to detect the presence of sound in sync pulses in the incoming video. It is fed with the same clamped video as A5, but its reference voltage on pin 4 is 0V (between quaternary levels 1 and 2). A16a gives a 100ns pulse triggered from the leading edge of sync. The trailing edge of this 100ns pulse triggers A16b to give a $1.6\mu s$ pulse to gate the output of A21 (pin 9). This output therefore goes low only if the clamped video on A21 pin 3 is above 0V during a period from $0.1\mu s$ to $1.7\mu s$ after leading edge of sync; such an occurrence implies that sound in sync pulses are present and A20a is repeatedly retriggered to indicate the fact. R77 is fitted so that the LED H1 is lit and the Fault output on pin 19c of the board connector is high for the unexpected situation, i.e. pulses not present.

1.10 Sync Regeneration

Integrated circuits A17 and A18 are Field Programmable Logic Sequencers (FPLS), of the Signetics Integrated Fuse Logic (IFL) family. They are clocked by the output from an oscillator running at a multiple of TV line frequency. At each clock pulse the outputs change state according to:

- (a) Their previous states.
- (b) The previous states of internal registers.
- (c) The input states.
- (d) How the devices have been programmed.

1.10.1 Power-on Reset

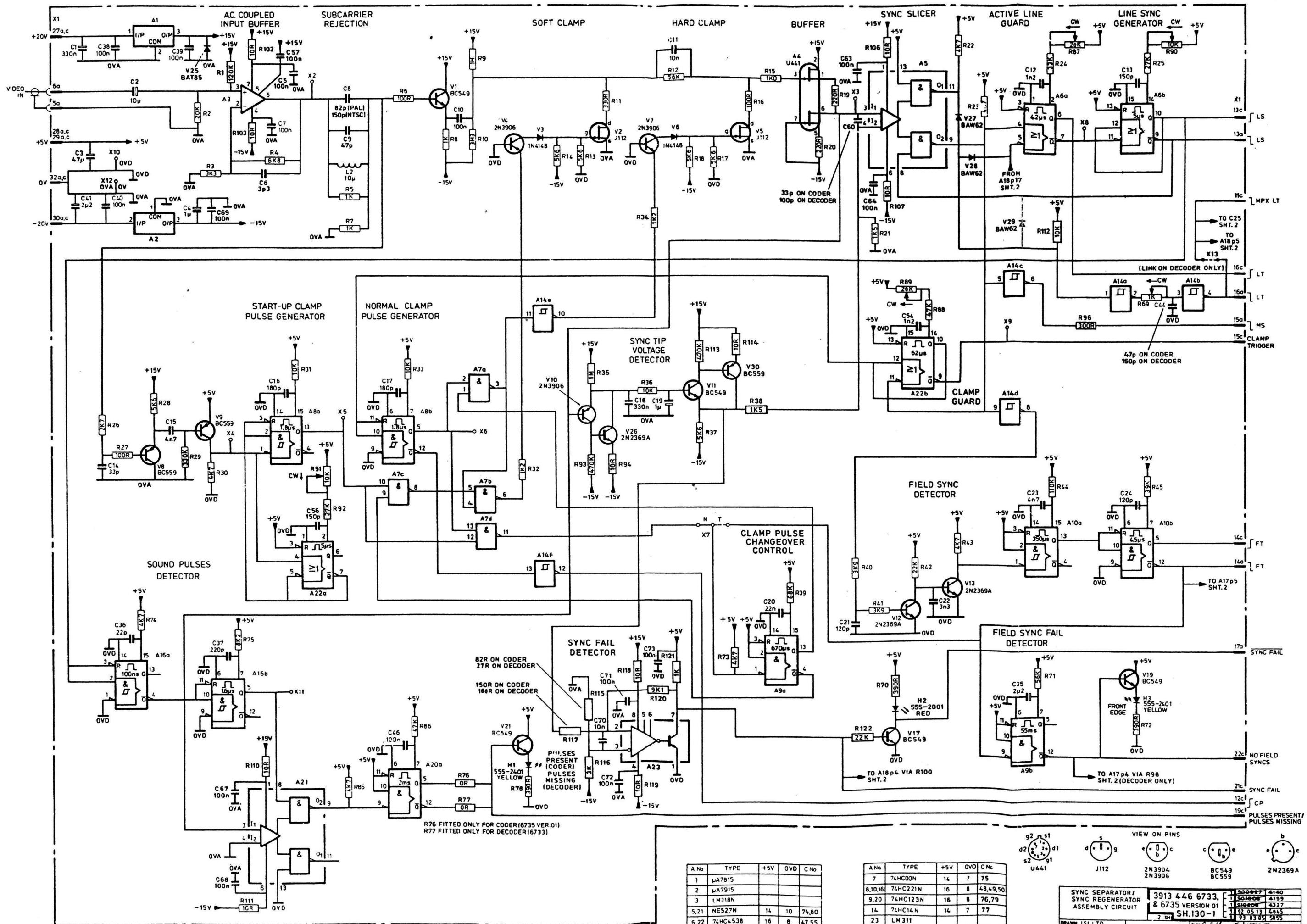
A short time after switch-on, the rising voltage on C42 triggers monostable A20b which in turn provides a reset pulse to the two IFLs.

1.10.2 Voltage-controlled Oscillator

The oscillator frequency is 328 times line frequency. FPLS A18 (Decoder Line Sync Generator, DLSG) in conjunction with counter A19 produces a phase reference pulse every 328 clock cycles. The filter consisting of L3, L4 and the associated components shapes the phase reference pulse into a voltage ramp which is sampled by the transconductance amplifier A11 at the moment the leading edge of the line trigger pulse occurs. The sampling pulse on Pin 5 of A11 is produced by V14, its short duration being due to the time constant of R53 and C25. The output of A11 is a pulse of current to add to or subtract from the charge on C28 according to the ramp voltage at the moment of sampling. The voltage on C28 is buffered by A12 and fed to A13 which is connected as an integrating amplifier. The output of A13 is used to control the capacitance of the varicap diode V23. This acts as fine tuning to the crystal oscillator and thus keeps a constant phase relationship between Line Trigger and Phase Reference. Trimmer capacitor C32 across the varicap diode should be set so that the output from A13 is 0V when the system is locked. Trimmer C45 in the ramp generating filter is used to match the timing of reinserted sync to that of incoming sync (allowing for overall delay through the video processor).

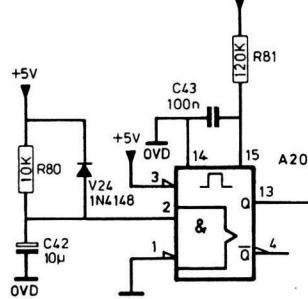
1.10.3 Line and Field Sync Generator

As well as providing a phase reference pulse for the line-locked oscillator, A18 provides half-line repetition rate pulses 2FL for the Decoder Field Sync Generator (DFSG) A17 which counts through a 625 (or 525) half-line sequence to determine the correct times for equalising pulses and broad pulses. Under the control of outputs from A17, A18 produces the full sequence of Regenerated Sync, Composite Blanking, Composite Gate (for control of reinsertion of regenerated sync) and Sample (for control of sampling of input broad pulse amplitude). To ensure that the whole sequence is in phase with the incoming signal, DLSG has a Line Trigger input and DFSG has a Field Trigger input.

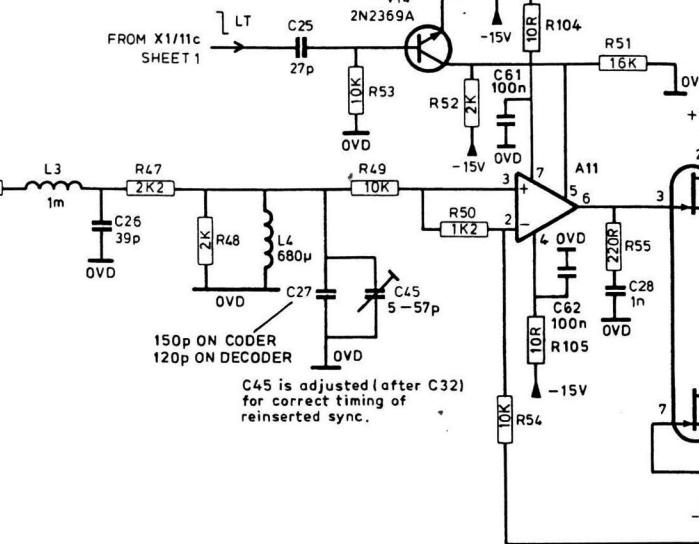


A No	TYPE	+5V	OVD	C No
11	CA3080E			
15	MC10109	1,16	8	53
17,18	N825105N	28	14	51,52
19	74HC163	16	8	78
20	74HC123	16	8	SEE SH.1
13	LF351			

POWER ON RESET
PULSE GENERATOR



GATE PULSE GENERATOR



RAMP GENERATING FILTER

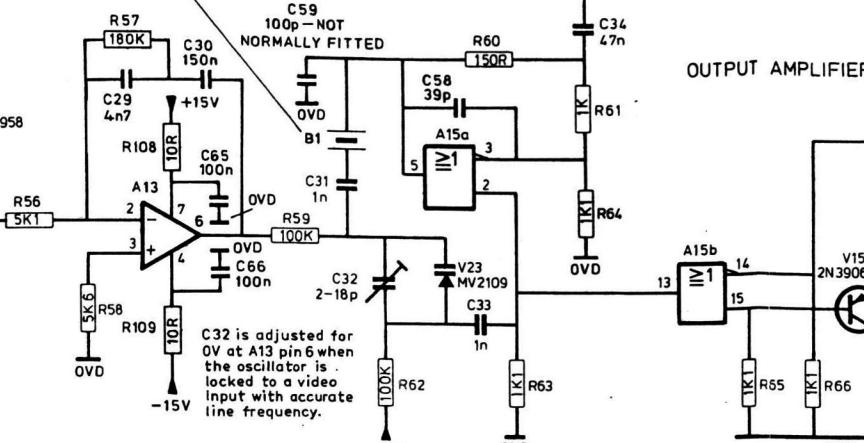
GATED COMPARATOR

INTEGRATOR

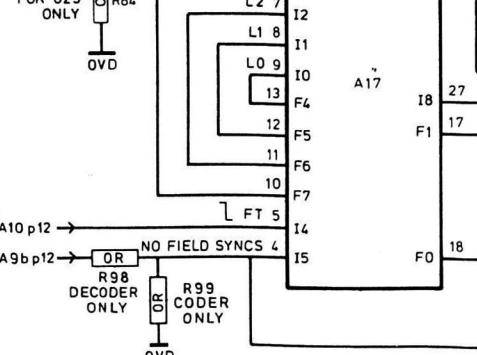
VOLTAGE CONTROLLED OSCILLATOR

B1 FREQ: 625 LINES: 5.125MHz
525 LINES: 5.160835MHz

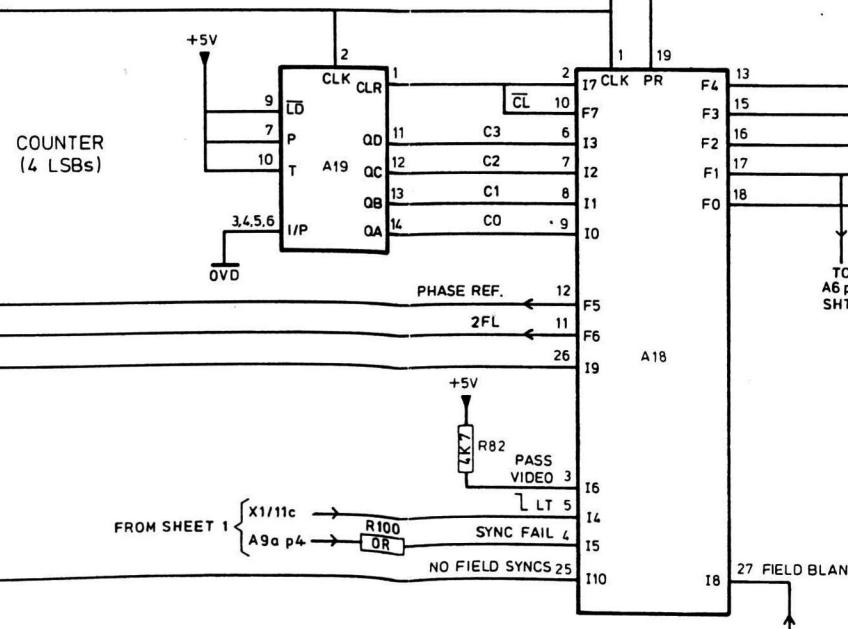
C59 100p-NOT
NORMALLY FITTED



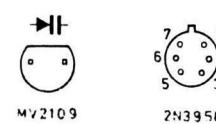
OUTPUT AMPLIFIER



÷ 625 (OR 525) COUNTER
AND FIELD SEQUENCE
CONTROLLER

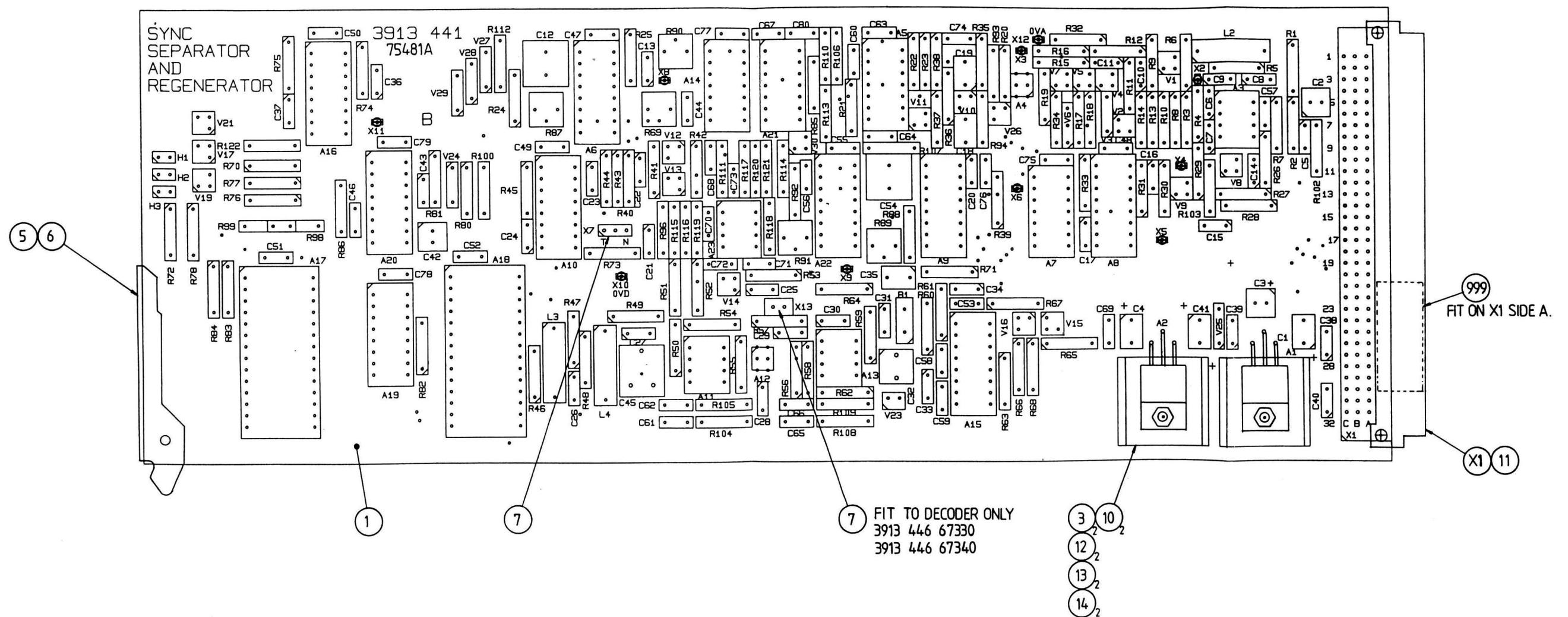


÷ 328 COUNTER
AND COMPOSITE SYNC.
GENERATOR



89-207	3782
90-0521	CA32993
90-0615	3961
90-0616	3990
89-0726	3754

3913 446 6733,
& 6735 VERSION 01
SH.130-2
DRAWN BY: J. W. G. APPROVED



STROKE NO	POV NO
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

NOTE: THE STROKE LEVEL SHOWN HERE MUST NOT BE CONFUSED WITH THE STROKE LEVELS SHOWN IN ASSOCIATED DRAWINGS & PARTS LIST.

1 APPEND STROKE NO ONLY FOR BASE INDICATED WITH THIS ASSEMBLY IN POSITION INDICATED

DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING	
TOL. UNLESS OTHERWISE STATED		SURFACE TEXTURE	LIT USED ON
UNITS	SCALE	ANGLES	HOLE
MM	2:1	SEE SEPARATE PARTS LIST.	
		SEE 3913 982 90010 CODE C.	
TITLE: SYNC SEP & REGENERATOR PCB.		3913 446 7548	
APPROVED:		DATE: 1990-04-30	
DESIGNER: J. HAN		ELECT. DRAFTER: J. HAN	
APPROVED:		APPROVED:	

QUATERNARY ADC3913 446 69760 (NICAM-728)Contents

CHANGE SUMMARY	Sh. 508-1	
1. FUNCTIONAL DESCRIPTION	Sh. 595-1	
2. USE OF RS-232 INTERFACE	Sh. 595-4	
ILLUSTRATIONS		
Circuit Diagram	3913 446 67310	Sh. 130-1 and 2
Assembly Drawing	3913 446 74810	Sh. 110-1
PARTS LIST		

C H A N G E S U M M A R Y

QUATERNARY ADC

3913 446 69760

References	Brief Description of Change	Documents Affected
PGV 3605 06.02.89	<p><u>On PCB Assembly 3913 446 74810:</u> C29 changed from 4p37 to 5p57. Contents of the parts list transferred to Parts List 3913 446 67310.</p> <p><u>3913 446 67320:</u> New circuit diagram created from 3913 446 67310, with C29 change incorporated. B1 frequency table removed from circuit diagram.</p> <p><u>Note:</u> This makes 3913 446 67320 Issue 3.</p> <p><u>On PCB Assembly 3913 446 74810:</u> A15 changed from 3913 036 60070 to DDAK - K, 3913 036 60360. A25 changed from 3913 036 55630 to Forth program ROM DC SIS9, 3913 036 60420. Contents of the parts list transferred to Lists 3913 446 67310 and 69510. New Parts Lists 3913 036 60360 and 60420 created.</p>	Circuit Diagrams Parts Lists
	<p><u>3913 446 67310:</u> Circuit diagram amended as follows: (a) B1 frequency table added: NICAM 3, 625 11.00MHz NICAM 3, 525 11.076922MHz NICAM 728, 625 11.9375MHz NICAM 728, 525 12.020978MHz (b) R68 circuit label changed to "NICAM 728 ONLY". R69 circuit label changed to "NICAM 3 ONLY". A15 circuit label changed to "676/728 ONLY". This circuit diagram now holds for versions 3913 446 67310, 69510 and 69760.</p> <p><u>3913 446 69760:</u> New parts list created by the transfer of contents of Parts List 3913 446 74810, with the following alterations: B1, crystal 11.9375MHz, 3913 074 50760 - Version 1 NICAM 728,625. B1, crystal 12.020978MHz, 3913 074 50770 - Version 2 NICAM 728,525. R68, 2k2, 2322 156 12202 Versions 1 and 2. R69 not fitted. This makes 3913 446 69760 Issue 1.</p>	

C H A N G E S U M M A R Y

QUATERNARY ADC

3913 446 69760

References	Brief Description of Change	Documents Affected
PGV 3713 04.08.89	On the edge connector X1, Pins 31a, b and c are linked to Pins 32a, b and c.	Circuit Diagram Assembly Drawing
PGV 3716 09.08.89	R9 changed from 1k6 to 1k5, 2322 156 11502. Two solder tags added.	Circuit Diagram Assembly Drawing Parts List
PGV 3840 17.01.90	V13, diode BAW62, 9331 012 20112 added between pins 4 and 5 of A4, + to pin 4. Note added to circuit diagram: <u>Caution with A1 and A4:</u> Shorting between adjacent pins 5 and 6 or 10 and 11 will result in Immediate destruction of the device.	Circuit Diagram Assembly Drawing Parts List
PGV 3848 18.01.90	A16, AM25LS2539, 9337 893 20662 changed to PAL 16L8-4CN programmed as Dual 2-4 Decoder 3913 036 55730. New base fitted.	Circuit Diagram Assembly Diagram Parts List
PGV 3853 19.01.90	A2, 74CHT123, 9336 699 10112 changed to 74HC123, 3913 935 12015.	Circuit Diagram Parts List
CA 35544 06.02.90 CA 36470 30.03.90 CA 41312 08.10.92 CA 41507 07.12.92 ECN10573 01.03.95 ECN10790 30.05.95	Various mechanical and parts lists changes.	Parts List

QUATERNARY ADC3913 446 69760 (NICAM-728)1. FUNCTIONAL DESCRIPTION

Sound-in-syncs video is AC coupled into A1 from the Decoder Video Processor module (3913 446 69530). A1 is configured as a non-inverting amplifier with a nominal gain of 2.6, adjustable by R6. The output of A1 drives an 11MHz low-pass filter, formed around L1, which removes any high frequency noise present on the video. The output from this filter goes to the video clamp circuit comprising V1, V2, the clamp capacitors C7 and C8 and the clamp transistor, FET V3. This clamp stage works by the clamping voltage being set on C8 by the clamp pulse, and C7 then gradually reaching this voltage during the line period, via R18. This means that no steps or spikes are introduced onto the video signal by the clamp pulse. Clamp pulses for V3 are $1.9\mu s$ wide pulses following the sync trailing edge, and are obtained from A2a, which is itself triggered by positive going mixed syncs from the Sync Regenerator module (3913 446 67330). R9, R10 and V5 set the black level DC which is 1.9V (measured at X7). Clamped sound-in-syncs video then passes to A3 and A4, which are configured as a non-inverting amplifier with a fixed gain of 2. At X7, the quaternary data amplitude should be 1.8V, with 0dB video input. At this point, the video passes into A6, a 6-bit flash A-to-D converter, and also the negative input of A5, a differential comparator with strobed outputs.

The function of A5 is to produce a timing reference from the marker pulse that occurs at the start of each burst of quaternary data, and it detects this marker pulse by comparing the video presented at its negative input to the average of the positive and negative reference voltages to A6. These references are optimised for the quaternary data amplitude at the input to A6 (see below). With the output of A8a normally low, A5 positive output is inhibited, until a line trigger edge from the Sync Regenerator, coinciding with the sync leading edge, sets A8a output high. The next rising edge (i.e. the marker pulse) on the negative input to A5 produces a falling edge on its positive output, which resets A8a via A9, inhibiting A5 again, and goes to produce a system timing reference via A8b. A8b behaves in the same way as A8a; the negative edge on its clock input produces a negative edge on its inverted output, which is reset 650ns later after its output has passed through D1 and D2. By means of the tapping point X3 on D1, precise system phasing can be established.

One of the outputs from X3 passes to a Phase-locked Loop (PLL), for synchronisation to data of the clock for A15, the Decoder Data Acquisition Controller. The first stage of this PLL is the filter formed by L3 and C25. This produces an 'S'-shaped curve from the falling marker

edge, and the delay of this curve, and hence fine phasing of the system clock, is adjusted using C29. This S-curve then passes into the gated op-amp A10, the gating pulse being derived from a sampling edge generated by A15, and passed through C38, V9 and then to A10. The sampled S-curve from the output of A10 is buffered by the dual FET A11 into A12, which is connected as an integrator, the PLL time constant being set by the integrator time constant. The output of A12 controls the varicap diode V6, which is part of an oscillator loop consisting of crystal B1, A13a, and their associated components. The output of A13a feeds A13b, which provides a differential signal to drive V7 and V8, the final clock drive being taken from the collector of V8. This is then used to clock A15, the clock frequency being twice the quaternary data rate, which is itself a multiple of video line frequency.

The other output of the marker pulse from X3 goes directly into A15, to control storage of quaternary data samples. When A15 receives a line trigger edge, it sends sample pulses, via A18a, to A6 and also to the 5-bit counter, A14. Although A6 has begun to sample the video, the samples obtained are not stored until a marker pulse is detected, and similarly, sampling continues for a short time after the end of quaternary data, but the samples are ignored. Since A6 produces 8V data, the 7-bit quaternary data samples obtained (6 bits plus over-range) are divided down to 5V logic levels by R30 and R31, and buffered and inverted by A7. They are then stored in RAM on the Data Recovery module (3913 446 69770), and also in A19, its addresses being set up by the counter A20, which is in turn clocked by A15. By working with A14 during quaternary data bursts, and from the relative timing of the marker pulse, A15 is able to detect justified data, Amplitude Reference Data (ARD), or an absence of data, and so can produce error indications for ARD, Data Fail, and, if A2b is not retriggered before it times out, Justification Fail.

The AGC acts by varying the positive and negative reference voltages into A6, so that the incoming quaternary data lies within the best 'window' for sampling by A6, and is based around A21, a 6500 series microprocessor with a built-in Forth interpreter, with its program held in the 8K x 8 PROM A25. The AGC operates by analysing 20 lines worth of quaternary data, which is stored in the 2K x 8 RAM, A24. Following the line sync period, when one burst of quaternary data samples have been stored in A19, these samples are transferred to A24, the address counter A20 now being clocked by A21 via A26. The data is analysed by counting the number of times that each 6-bit quaternary data value occurs. Since the data being sampled is quaternary, there will be four groups of occurrences across the 64-level range, and from the position of these occurrences, particularly those representing the bottom and top levels, the optimum reference voltages can be calculated and passed to the dual 8-bit D-to-A converter, A27. The two reference voltages produced by A27 are buffered by the two halves of A28 and fed to A6. Hence, the 6-bit (64-step) sampling window for the quaternary data can be moved up and down and adjusted in size over an 8-bit (256-step) range. By comparing the calculated reference values with ideal values, the AGC system produces Data Amplitude High and Data Amplitude Low warnings for +3dB and -3dB data levels respectively. The busses between A21, A24, A25, and A27 are tri-state, with data sharing part of the address bus, so the octal latch A23 provides address and data busses for A24 and A25, and the 256 x 8 PROM A26 performs address decoding of control lines for A24, A25, and A27.

A29, together with A30 and A9c form a 'watchdog' and power-on reset circuit for the AGC system. A29 is a 24-stage frequency divider, clocked at half the A21 clock frequency. If A29 reaches half count, i.e. Q(24) goes high, Q(18) clocks this into A30a, which provides a low reset for A21, and also sets A30b, giving an AGC Fail indication. However, in normal operation, A29 and A30b will be continually reset by the AGC system (A29 via A9c and A18d), and no reset or fault indication will be produced. On power-on, C59 will charge up slowly via R63, causing A29 to be reset and A30a to be set, this latter condition resetting A21. As C59 charges up towards 5V, A30a set is released, and the reset on A21 is released when Q(18) on A29 goes high.

Power to the digital sections of circuitry (+5V) is provided from the main rack power supply. +15V and -15V is provided from regulators A31 and A32, which are fed from +20V and -20V, smoothed but unregulated, once again from the rack power supply. +8V for A6 is supplied by A33, which takes its input from the +15V regulated supply from A31.

2. USE OF RS-232 INTERFACE

The Quaternary ADC microprocessor software includes provision for using an RS-232 interface to aid in testing and fault diagnosis. This allows certain functions of the AGC system that would normally be under the control of the microprocessor to be controlled manually from a terminal. The data format is as follows:

Transmit/Receive speed - 1200 baud.

Bit format - 8 data bits, 1 start bit, 1 or 2 stop bits, no parity.

Connections - 2 line (RxD, TxD), no handshake required.

Data are transmitted from the module on edge connector Pin 22a and Test Point X6 (near A21), and received by the module on edge connector Pin 23a and Test Point X5. The data at these points are at TTL levels, so an external level shifter must be provided for full RS-232 interfacing.

In order to use the terminal facility, Link X2 must be set to the test (T) position (towards the edge connector) and the board then switched on. Changing the position of X2 without switching off will have no effect. Switching on the module in test mode should produce the following terminal display:

2-Channel SIS Test Mode Menu

- 1 RESET
- 2 CLARAM
- 3 ADDSAMPLE
- 4 DACRAMP continuous until key pressed
- 5 AQRCYCLE
- 6 REPORT
- 7 SETHREF
- 8 SETLREF
- 9 TESTSIS continuous until key pressed
- 0 MENU
- / NORMAL MODE reset necessary for further tests.

The AGC system will not actually be working at this point; the microprocessor will have loaded initial high and low reference values for the 6-bit ADC which assume that the Decoded is receiving 0dB video and that the module is correctly set up for digits 1.8V high, black level clamped to 1.9V, at X7. However, providing that these conditions are met, sound should be correctly decoded. The AGC system can now be controlled manually from the terminal by entering the appropriate character, as indicated on the menu (no "return" required). The meaning of each function is as follows:

RESET	This reset the ADC references to their initial values.
-------	--

CLARAM This clears the RAM that is used to store the occurrences of quaternary levels for calculation of the ADC reference values.

ADDSAMPLE This causes one burst of data to be acquired and added into the histogram for calculation of the ADC reference voltages. However, no calculation is done at this point. It will also return a value of DBSTAT, which indicates the status of the data burst. The possible values of DBSTAT and their meanings are as follows:

- True Status DBSTAT 0 - normal data
- True Status DBSTAT 1 - justified data
- True Status DBSTAT 2 - amplitude reference data
- True Status DBSTAT 3 - no data
- False Status DBSTAT 255 - no video

DACRAMP This causes the two ADC reference voltages from the DAC to be continually ramped up and down over a period of about 0.5s.

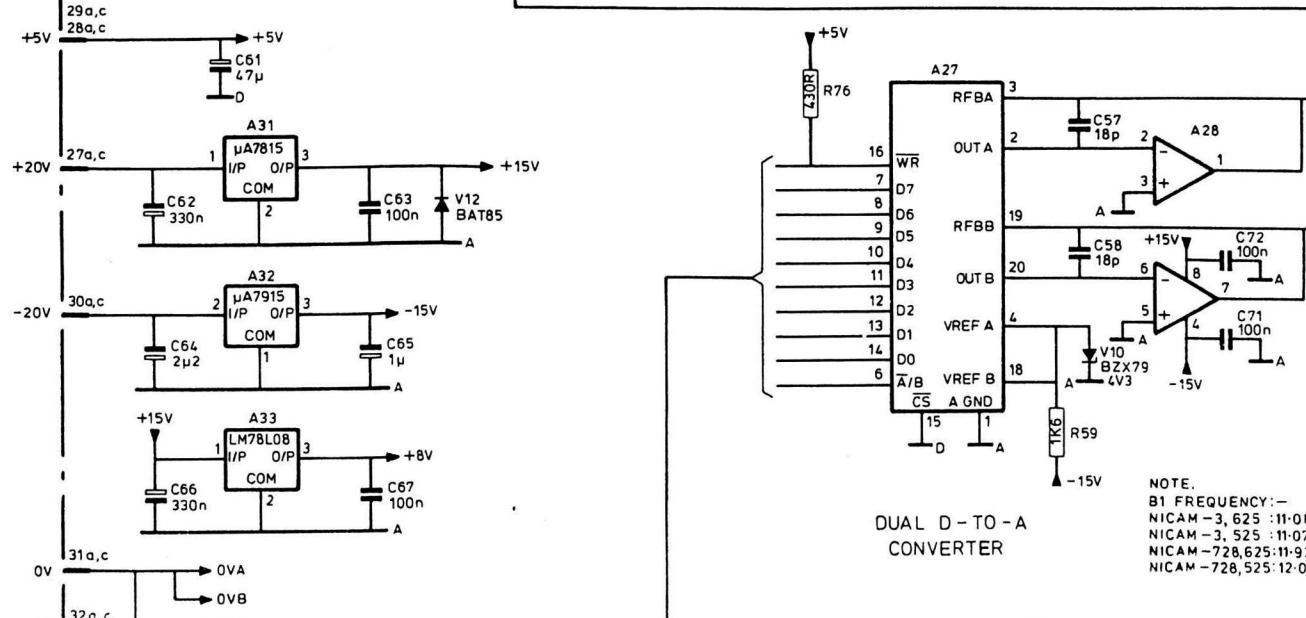
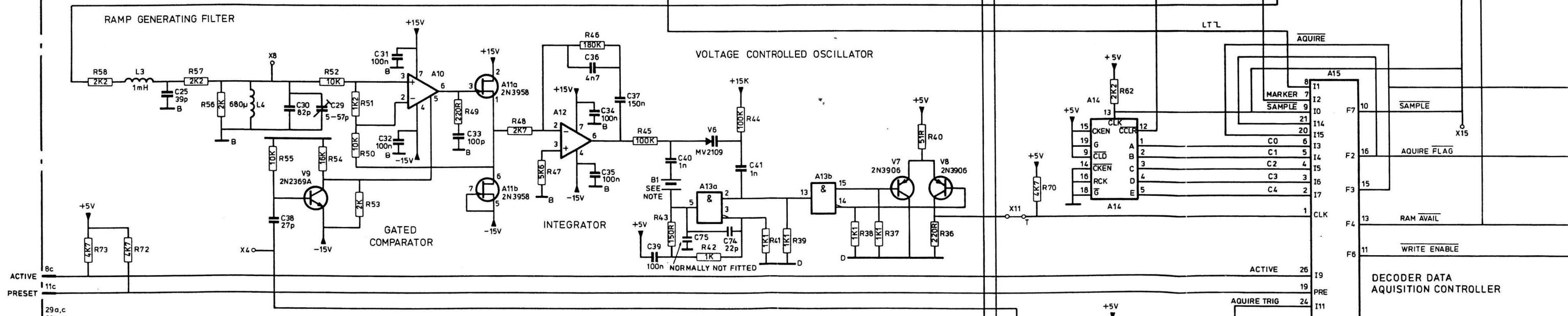
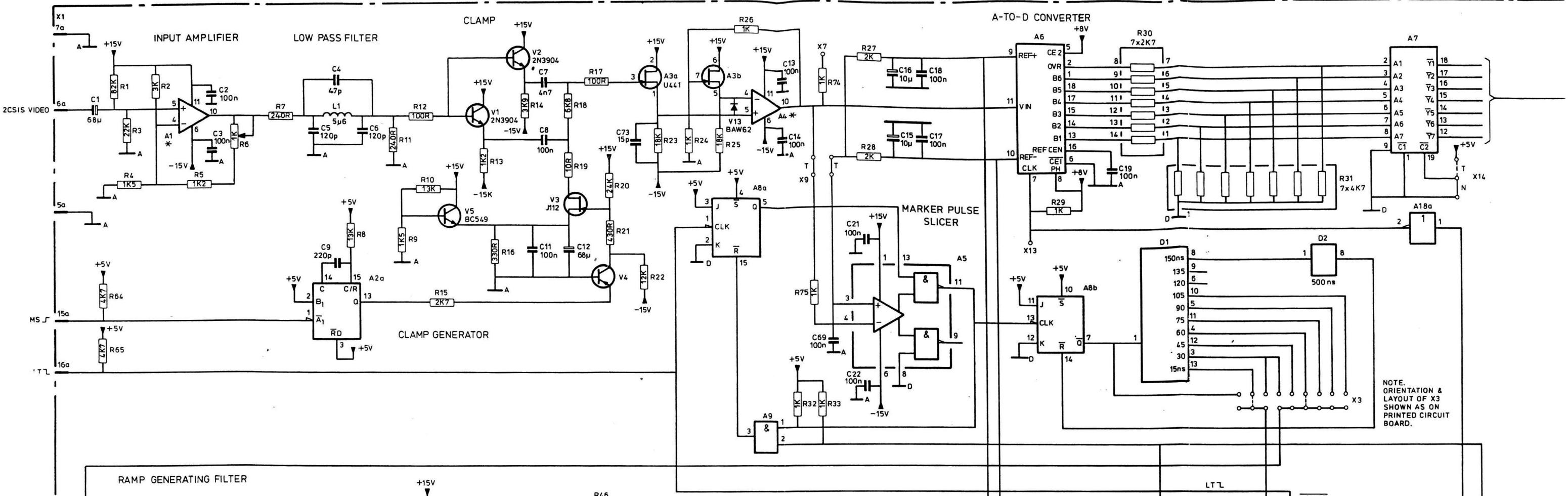
AQRCYCLE This causes the micro to acquire 20 lines worth of data, construct a histogram of occurrences of quaternary levels in RAM, and calculate new ADC reference voltages on the basis of the histogram.

REPORT This causes the sample histogram table to be printed on the terminal together with variables calculated from the data, as follows:

- HAVG - average high sample value from ADC (0-63)
- LAVG - average low sample value from ADC (0-63)
- CREF - mean of the new high and low ADC references from DAC (0-255)
- RREF - difference between the high and low ADC references (0-255)
- GA - gain adjustment required to give optimum sampling next time
- HREF - new value of high ADC reference from DAC (0-255)
- LREF - new value of low ADC reference from DAC (0-255)

The AGC system adjusts HREF and LREF to attempt to obtain values for HAVG of 52.5 and LAVG of 10.5, and GA gives the gain adjustment required for a difference of 42 between HAVG and LAVG.

SETHREF	Allows the value of the high ADC reference to be entered from the terminal. The value entered must lie in the range 0 to 255.
SETLREF	Allows the value of the low ADC reference to be entered from the terminal. The value entered must lie in the range 0 to 255.
TESTSIS	This causes the AGC system to operate normally with data being continually acquired and the ADC reference voltages being recalculated. The process may be stopped at any time by pressing any key on the terminal.
MENU	This causes the test menu to be printed on the terminal.
NORMAL MODE	Typing "/" puts the AGC system into its normal operation mode. Any further commands from the terminal will be ignored, and the test mode can only be regained by turning the module off and on again.



A No.	TYPE	+8V	+5V	0V	C No.	A No.	TYPE	+8V	+5V	0V	C No.
1,4 *	H1-5195-5					17,30	74HCT74				
2	74HC123	16	8	10	18	7406		14	7	46	
5	NFS27N	14	10		19	82S09		14	7	47	
6	CA3300D	12	3		21	R65F11		28	14	48	
7	74HC540	20	10	20	23	74HCT573		20	10	51	
8	74HC112	16	8	23	24	HM6116LP-4		24	12	52	
9	74HCT08	14	7	50	25	2764		28	14	53	
10	CA3080E				26	TBP2BL22		20	10	54	
12	LF351				27	AD7528		17	5	55	
13	MC10109P	1,16	8	42	28	MC1458					
14,20	74LS593	20	10	43,49	29	MC14521B		5,16	3,8	60	
15	PLS105	28	14	44	01	3814 100 150		14	7	24	
16	PA16L8-4CN	20	10	45	02	3814 100 500		14	7	24	

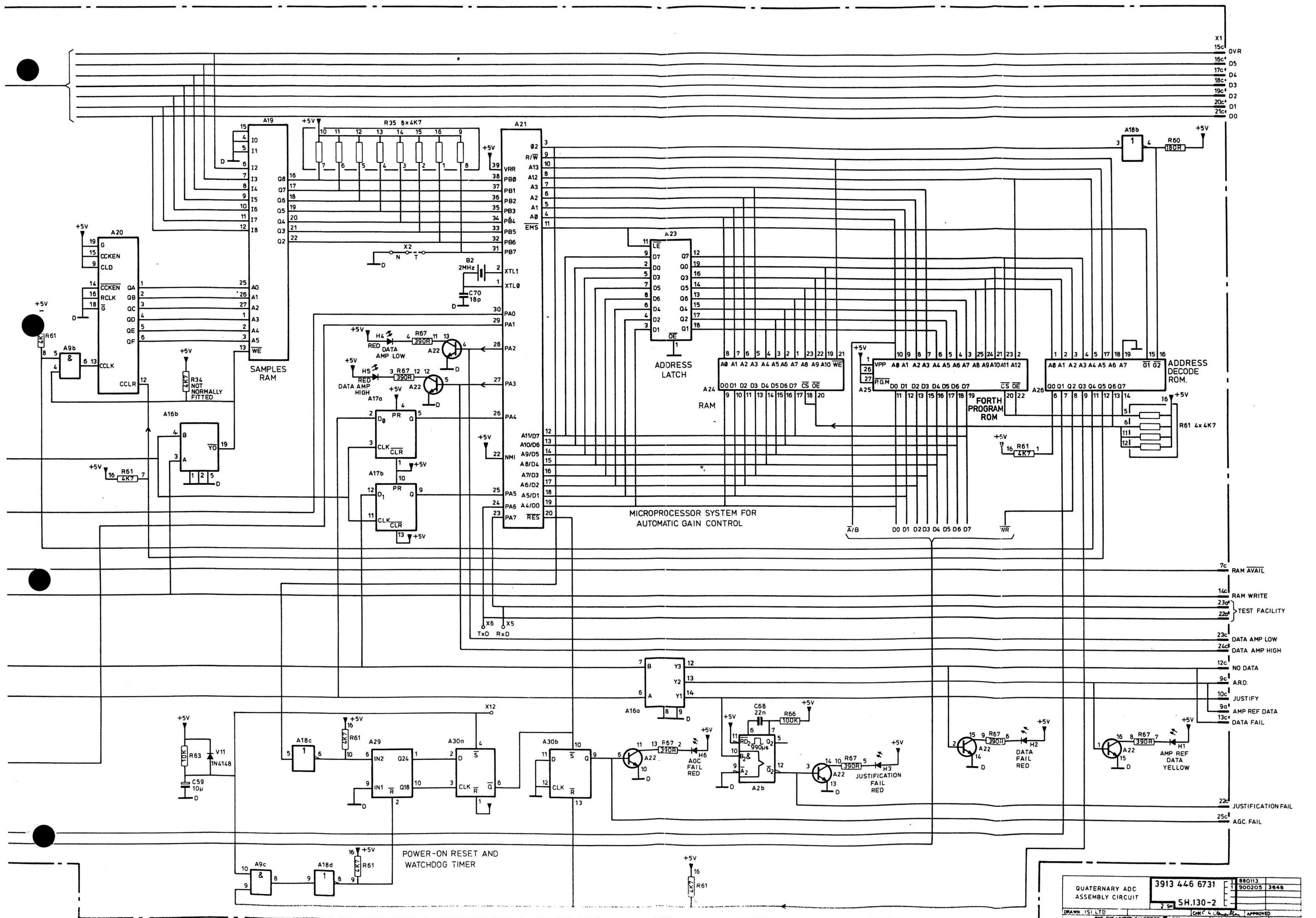
* CAUTION WITH A1 & A4:-
SHORTING BETWEEN
ADJACENT PINS 5 & 6 OR
10 & 11 WILL RESULT IN
IMMEDIATE DESTRUCTION
OF THE DEVICE.

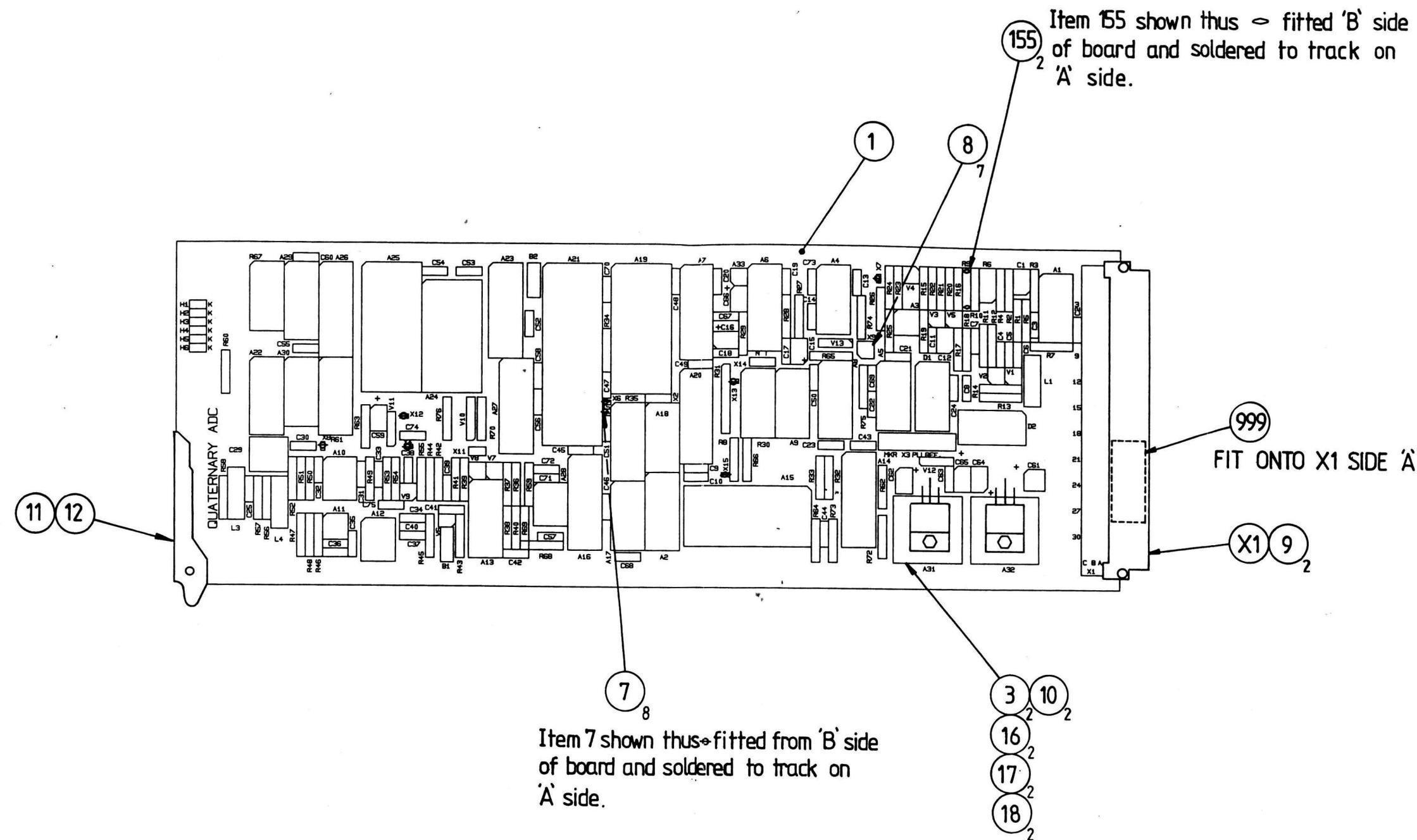
QUATERNARY ADC
ASSEMBLY CIRCUIT

3913 446 6731	1 890 914 3716
1 900 205 3640 4,6,3853	1 890 914 3554
1 890 914 3554	1 890 915 3605

SH.130-1

DRAWN BY: T. APPENSON





FIT IC BASE ITEM 5 AT A16 AND A26
 FIT IC BASE ITEM 13 AT A24
 FIT IC BASE ITEM 4 AT A15 A19 AND A25
 FIT IC BASE ITEM 14 AT A21
 FIT IC BASE ITEM 15 AT A6

DO NOT SCALE THIS PRINT				DIMENSIONS ARE SHOWN AFTER PLATING	
TOL UNLESS OTHERWISE STATED				SURFACE TEXTURE	1st USED ON
DIMENSIONS	SCALE	ANGLES	HOLEs		
UNITS	MM	1:1			
ORG DRG	1.1				
PROJECTION	3rd				
SEE SEPARATE PARTS LIST					
SEE 3913 982 90010 CODE C					
1G 21 02 90					
QUATERNARYADC PCB ASSY DRG 3913 446 7481					
SUPERSEDES		SH	SH		
DRAWN	POLYTEC	MECH. CHK.	ELECT. CHK.	APPROVED	
PYE TTV LIMITED CAMBRIDGE © 19 DATE DRAWN FORM A2					

DATA RECOVERY3913 446 69770 (NICAM 728)Contents

CHANGE SUMMARY	Sh. 508-1
1. FUNCTIONAL DESCRIPTION	Sh. 595-1
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Circuit Diagram ..	3913 446 69490
	Sh. 130-1 and 2
Assembly Drawing ..	3913 446 74820
	Sh. 110-1
PARTS LIST	

C H A N G E S U M M A R Y

DATA RECOVERY

3913 446 69770

(Issue 2)

References	Brief Description of Change	Documents Affected
PGV 3219 13.5.87	<u>On PCB 3913 446 74820:</u> A2 Pin 17 connected to +5V. Track added for +5V and OV links.	Circuit Diagram
PGV 3220 25.2.87	<u>On PCB 3913 446 74820:</u> A9 Pin 26 connected to OV.	Circuit Diagram
PGV 3242 27.4.87	<u>On PCB 3913 446 74820:</u> A3 and A4 changed from 9337 572 80112 to 3913 935 12058. A9 (3913 036 54720) changed from 3913 935 20038 to 3913 935 20091. A12 (3913 036 54730) changed from 9337 627 20682 to 3913 935 20091.	Parts List Circuit Diagram
PGV 3246 14.5.87	Order of four pins of X4 changed to agree with the circuit diagram.	Assembly Drawing
PGV 3274 19.6.87	<u>On PCB 3913 446 74820:</u> A7 and A8 changed from 3913 935 35009 to 9333 243 30602.	Parts List Circuit Diagram
PGV 3347 30.11.87	<u>On PCB 3913 446 74820:</u> A13 changed from 3913 036 60170 to 3913 036 60250.	Parts List Circuit Diagram
PGV 3619 13.02.89	<u>3913 446 69520 (A-LAW):</u> Contents of Parts List 3913 446 74820 transferred to this parts list. New circuit diagram created from 3913 446 69490. <u>3913 446 69490 (NICAM 3):</u> Contents of Parts List 3913 446 74820 transferred to this parts list. A13 changed from 3913 036 60250 to DDPC - K, 3913 036 60370. New Parts List 3913 036 60370 created. Circuit diagram amended as follows: (a) A13 change as above. (b) R3 labelled "NOT FITTED FOR NICAM 3" (c) R9 labelled "NOT FITTED FOR NICAM 728" (d) A13 Pin 2 connection labelled "676/728" This circuit diagram then holds for versions	Circuit Diagrams Parts Lists

C H A N G E S U M M A R Y

DATA RECOVERY

3913 446 69770

(Issue 2)

References	Brief Description of Change	Documents Affected
PGV 3619 (cont'd)	3913 446 69490 and 69770. <u>3913 446 69770 (NICAM 728):</u> Contents of Parts List 3913 446 74820 transferred to this parts list, with the following items versionised: R9 Component not fitted Version 1 NICAM 728 R3 4k7, 2322 156 14702 Version 1 NICAM 728.	
CA 36470 30.03.90 CA 41507 07.12.92	Mechanical changes.	Parts List
PGV 4774 31.03.92	EPROM changed from 9336 523 70862 to 9338 827 53682.	Parts List Circuit Diagram

DATA RECOVERY3913 446 69770 (NICAM 728)1. FUNCTIONAL DESCRIPTION

One line's worth of quints (24 or 22) in the form of 6-bit values from the Quaternary ADC board are clocked into a RAM (A1) by a 6-bit address generator (A2 = 6-bit counter) in the first $4.7\mu s$ (= length of sync pulse of the $64\mu s$ line period).

Two 4-bit adders (A3, A4) and two 9-bit latches (A5, A6) are connected so as to form a pair of accumulators under the control of the Decoder Data Processing Controller (DDPC) FPLS (A13). The address generator now clocks the data out of the RAM and one accumulator is used to sum the values which the DDPC decides correspond to quaternary level 0, and the other to sum the values the DDPC decides correspond to level 3. Using the two pairs of sums and counts a PROM (A9) calculates average error values for Levels 0 and 3 from the ideal values. These are fed to another PROM (A12) which selects a corresponding look-up correction table from the 256 it has stored. This occurs within about the next $20\mu s$ of the line period.

In the remaining $40\mu s$ (approximately) of the $64\mu s$ the data is clocked out of the RAM (again), this time into A12 (PROM) which uses the selected correction table to convert the 6-bit values to the four quaternary levels which it outputs as 2-bit values (LSB, MSB), accompanied by a Data Available STROBE from the DDPC.

The largest proportion of the $64\mu s$ available is devoted to data O/P to spread the data out as much as possible time-wise in order to minimise line rate jitter of the data to the Bitstream Regenerator.

The ARD (Amplitude Reference Data) and NO DATA inputs indicate invalid data, in which case the DDPC does not do any processing but waits for the next data.

The JUSTIFY I/P is necessary so the DDPC knows whether to expect 22 or 20 quints.

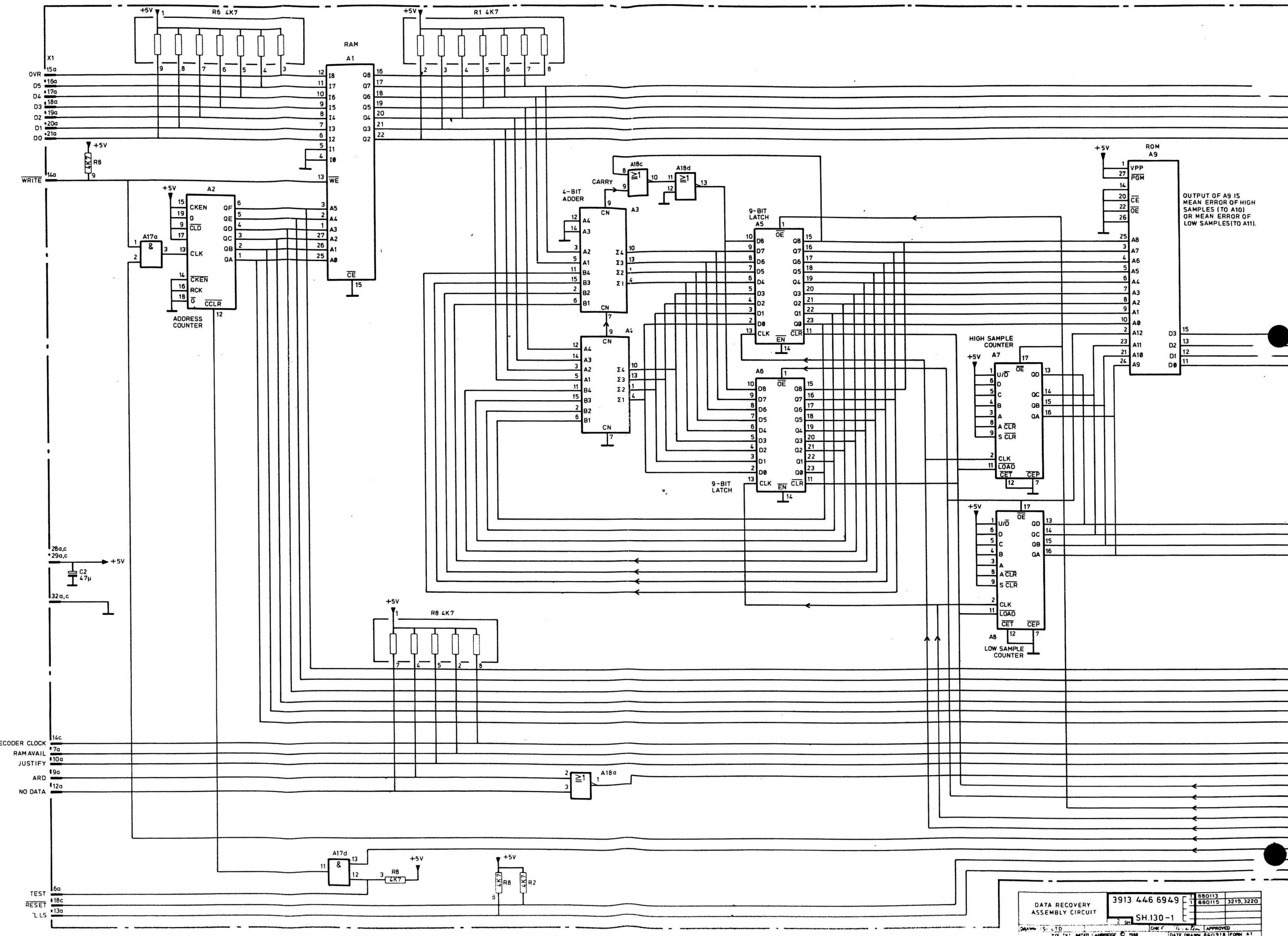
The DECODER CLOCK I/P (2.912MHz from the Bitstream Regenerator board) is used to provide the board clock.

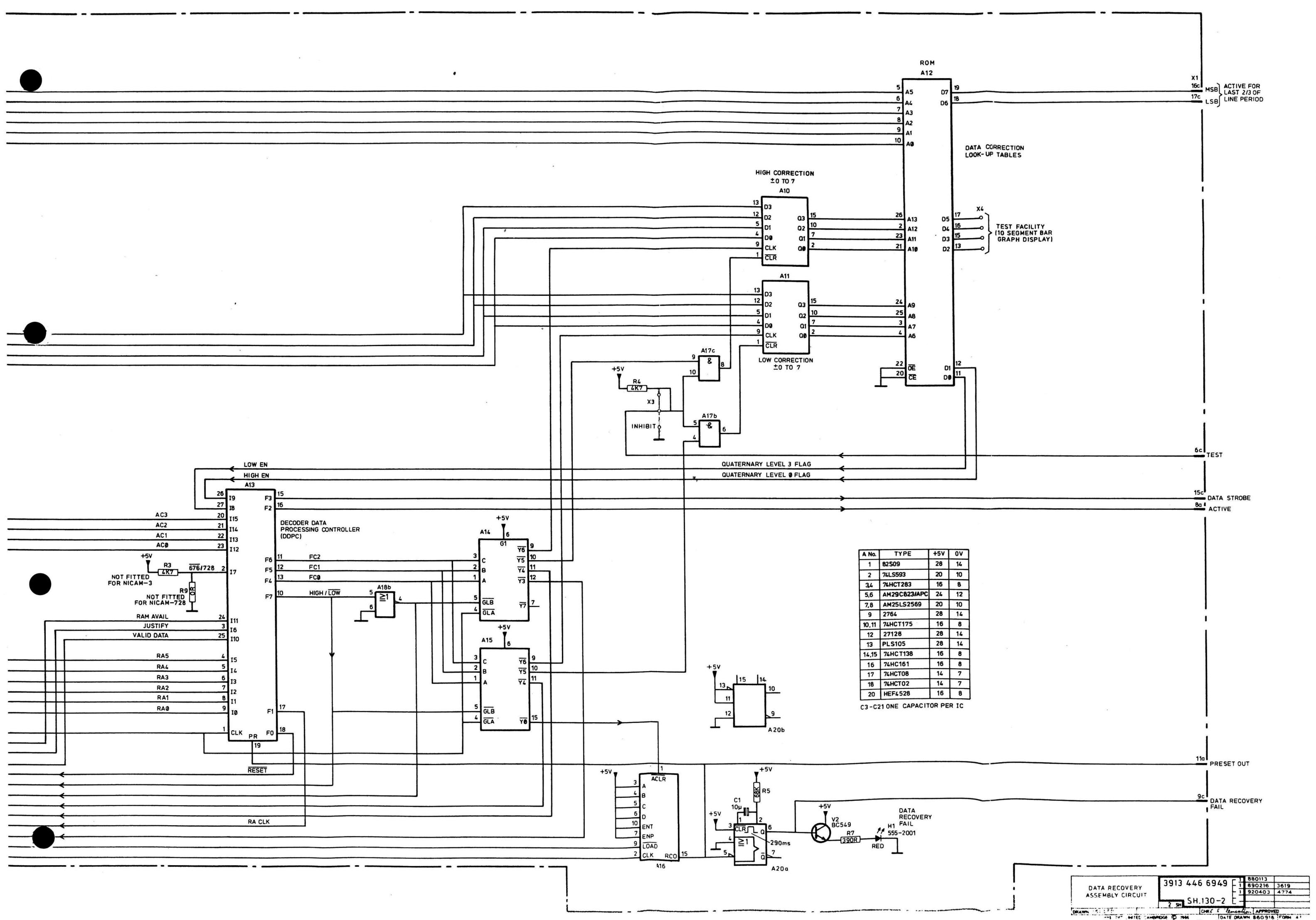
The DDPC disables the (data available) STROBE O/P to prevent the marker being interpreted as data.

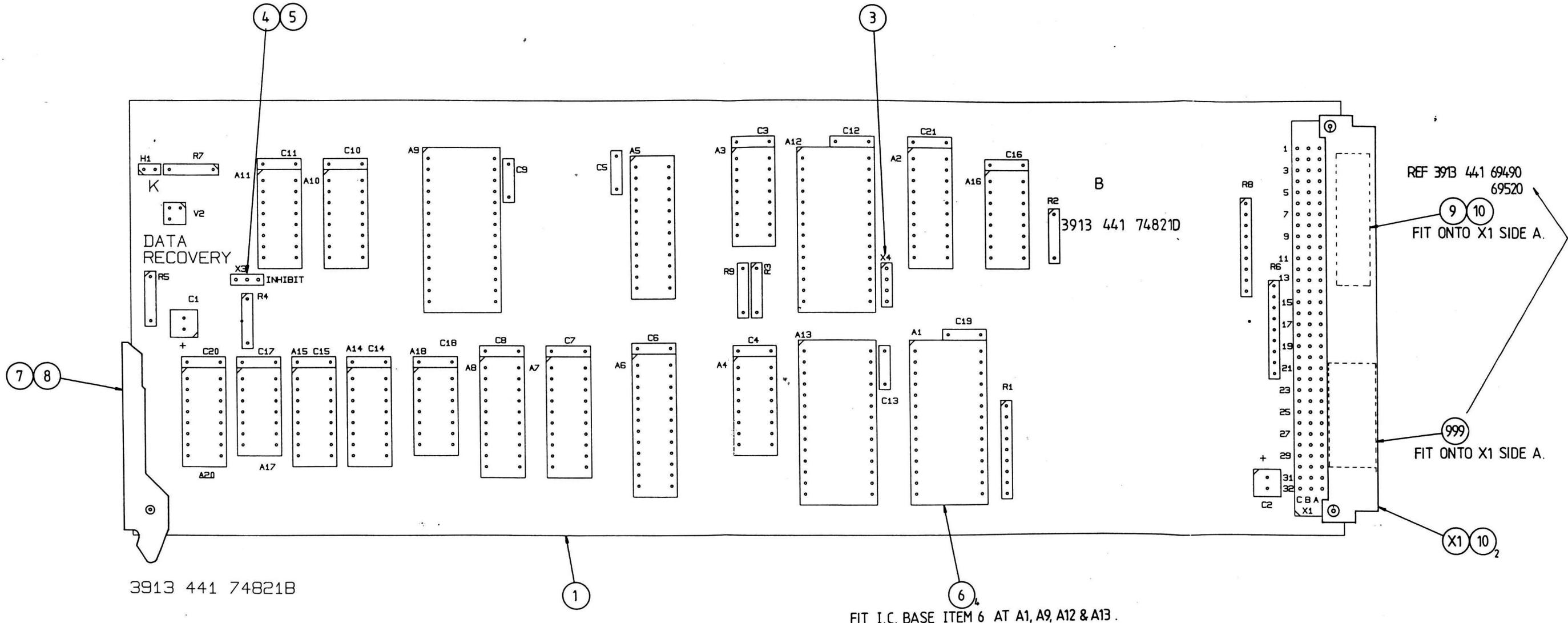
A watchdog timer (A16 = 4-bit counter) counts line syncs from the LS I/P. If there is a RAM contention the DDPC will not reset the watchdog timer; after counting 16 sync pulses it will generate the PRESET signal and the PRESET O/P (to the Quaternary ADC and the Bitstream Regenerator) and the DATA RECOVERY FAIL fault O/P.

Initialisation:

On a PRESET signal the DDPC clears the address generator. The Decoder Data Acquisition Controller (DDAC) on the Quaternary ADC board takes control of the RAM with the RAM AVAIL I/P and sends data into the RAM with the WRITE I/P. On completion of this operation the DDPC assumes control of the RAM, asserts the ACTIVE O/P and initialises the address generator (again), the accumulators and the counters with the RESET signal.







NO. STROKE PLATE INSTRUCTION	
1 APPEND STROKE PLATE NO 3913 982 90010 ISSUED WITH THIS ASSEMBLY IN POSITION INDICATED	
2 STROKE OFF NUMBERS ON PLATE TO LEVEL INDICATED IN THIS DETAIL	
NOTE THE STROKE LEVEL SHOWN HERE MUST NOT BE CONFUSED WITH THE ISSUE DATES SHOWN ON ASSOCIATED DRAWINGS & PARTS LIST	
STROKE NO	POV NO
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

DO NOT SCALE THIS PRINT				DIMENSIONS ARE SHOWN AFTER PLATING	
TOL UNLESS OTHERWISE STATED		SURFACE TEXTURE		IN USED ON	
DIMENSIONS	SCALE	UNITS	ANGLE	HOLES	
MM	ORG ORG	MM			
SEE SEPARATE PARTS LIST					
PROJECTION TREATMENT					
SEE 3913 982 90010 CODE C.					
TITLE		3913 446 7482.		15186 09 11	
DATA RECOVERY PCB ASSY.				10187 03 02	
SUPERSEDES				10187 05 28	
DRAWN D.J.F.		MEC CHK		ELECT CHK	
APPROVED					
PYLE T.V.T LIMITED CAMBRIDGE (TRANSMITTER DIV.) © 1986 DATE DRAWN 16/09/11 FORM A					

BITSTREAM REGENERATOR3913 446 67600 (Version 2, NICAM 728)Contents

CHANGE SUMMARY	Sh. 508-1
1. FUNCTIONAL DESCRIPTION	Sh. 595-1
ILLUSTRATIONS	
Circuit Diagram	Sh. 130-1
Assembly Drawing	Sh. 110-1
3913 446 75390	
PARTS LIST	

C H A N G E S U M M A R Y

BITSTREAM REGENERATOR

3913 446 67600

References	Brief Description of Change	Documents Affected
PGV 3238 13.5.87	<p><u>On PCB 3913 446 74790:</u></p> <p><u>On existing modules:</u></p> <p>R43 becomes 'value selected on test' (actual test limits: top limit 8112120 to 8112200Hz bottom limit 8111800 to 8111880Hz).</p> <p><u>On new layout modules:</u></p> <p>R42, 5k1 and R43, 10k replaced by R48, 10k potentiometer, 2111 369 00085. R48 connected as follows: End (a) to OV Slider (b) to X8/R16 End (c) to A16 Pins 2, 6. X11 added in series with A6 Pin 11. X12 added in series with A6 Pin 10.</p>	Parts List Circuit Diagram Assembly Drawing
PGV 3274 19.6.87	<p><u>On PCB 3913 446 74790:</u></p> <p>A7 and A8 changed from 3913 935 35009 to 9333 243 30602</p>	Parts List Circuit Diagram
PGV 3280 17.11.87	<p><u>On PCB 3913 446 74790:</u></p> <p>C36, 27p, 2222 683 34279 added between A15 Pins 3 and 5. Provision to be made on printed board for C37, 9999 999 00071/Q between A15 Pin 5 and OV; circuit diagram to read 'NOT NORMALLY FITTED'.</p>	Parts List Circuit Diagram Assembly Drawing
PGV 3348 28.11.87	<p><u>On PCB 3913 446 74790:</u></p> <p>A3 changed from 3913 036 60180 to 3913 036 60280. A6 changed from 3913 036 60190 to 3913 036 60290.</p>	Parts List Circuit Diagram
PGV 3620 16.02.89	<p><u>3913 446 67590 (NICAM 3):</u></p> <p>A3 changed from 3913 036 60280 to DDRC-E, 3913 036 60430. Parts List 3913 036 60430 created. This makes 3913 446 67590 Issue 4.</p> <p><u>3913 446 67600 (A-LAW):</u></p> <p>Contents of Parts List 3913 446 74790 transferred to Parts List 67590; contents of 67590 added to this parts list. Two versions created: Version 1 (A-LAW) and Version 2 (NICAM 728), with the following differences: Version 1: A3 3913 036 60280, B1 3913 074 50660 Version 2: A3 3913 036 60430, B1 3913 074 50780</p>	

C H A N G E S U M M A R Y

BITSTREAM REGENERATOR

3913 446 67600

References	Brief Description of Change	Documents Affected
PGV 3536 02.08.89	Parts List 3913 446 74790 discontinued and its contents integrated into Parts List 3913 466 67590 (see PGV 3620 above).	Parts Lists
CA35518 20.10.89	Parts List 3913 446 67600 corrected.	Parts List
PGV 3861 02.04.90	A11, 3913 036 06230 changed to 3913 036 06540. R48 frequency range adjustment changed from 80kHz to 400kHz. R9 and 10, 6k8, 2322 156 16802 changed to 15k, 2322 156 11503.	Parts List
PGV 4053 16.07.90	C18, 47nF, 2012 310 00316 changed to 47nF, 2012 310 03122.	Parts List
PGV 4078 08.08.90	C38, 1nF, 2222 630 19102 and R49, 470k, 2322 156 14704 added to A7a to avoid excessive bitstream frequency change after a signal interrupt at coder video input. A3, 3913 036 60430 reprogrammed to 3913 036 60610. A6, 3913 036 60380 reprogrammed to 3913 036 60620. A11, 3913 036 06230 reprogrammed to 3913 036 06550.	Circuit Diagram Assembly Drawing Parts List
PGV 4845 07.05.92	Potentiometers changed to different type.	Parts List
CA 41507 07.12.92 ECN10564 28.02.95 ECN10887 14.07.95	Various mechanical changes.	Parts List

BITSTREAM REGENERATOR3913 446 67600 (Version 2, NICAM 728)1. FUNCTIONAL DESCRIPTION

The arrival of data (LSB, MSB) at the Decoder Data Buffer Controller (DDBC) FPLS (A3) from the Data Recovery board is signalled by a (data available) STROBE (from the same board). The Gray coding (implemented in the coder) is decoded (in A3) and the data is de-multiplexed to two pairs of bits into a 4×32 FIFO buffer (A4, A5). The data is multiplexed to a serial data stream with its accompanying 728kHz data clock by the Decoder Regenerated Clock Controller (DRCC) FPLS (A6). The DRCC provides 728kHz by a divide by 4 of the 2.912MHz board clock which is provided by a divide by 3 (4-bit) counter (A14).

The board clock frequency is controlled by a negative feedback system.

The depth (fullness) of the FIFO is monitored by a buffer depth (2×4 -bit) counter (A9, A10) which counts up SHIFT INs and counts down SHIFT OUTs (i. e. it counts nibbles). The counter cycle is 16 (board) clock cycles long -corresponding to shifting one set of 4 bits out of the FIFO. The count direction (UP/DOWN) is alternated by the data clock. COUNT (enable)s are the result of a SHIFT OUT coinciding with DOWN or a SHIFT IN coinciding with UP. SHIFT OUTs are synchronous with DOWNs (= data clock lo) but SHIFT INs can occur at any time and so are four (board) clock cycles long to ensure they coincide with an UP (= data clock hi).

Once every counter cycle (16 board clock cycles) a SHIFT OUT is used to latch out the depth counter O/P into the Regenerated Clock PLL Coefficients (RCPLLC) PROM (A11) which loads a (4-bit) counter (A12) with a corresponding value. (The depth counter is preloaded by the DRCC at initialisation such that its MSB corresponds to a 'more than half full' signal, HIGH DEPTH). This signal and the countdown of the counter (A12), fed via the DRCC, control the pumping direction, and the length of time the pump is enabled, respectively, of the VCO pump. This pump (based on a PLL) either increases (pumps up) or decreases (pumps down) the oscillator frequency.

On initialisation, caused by:

- (a) A fault - an on board fault
 - an off board fault I/P.

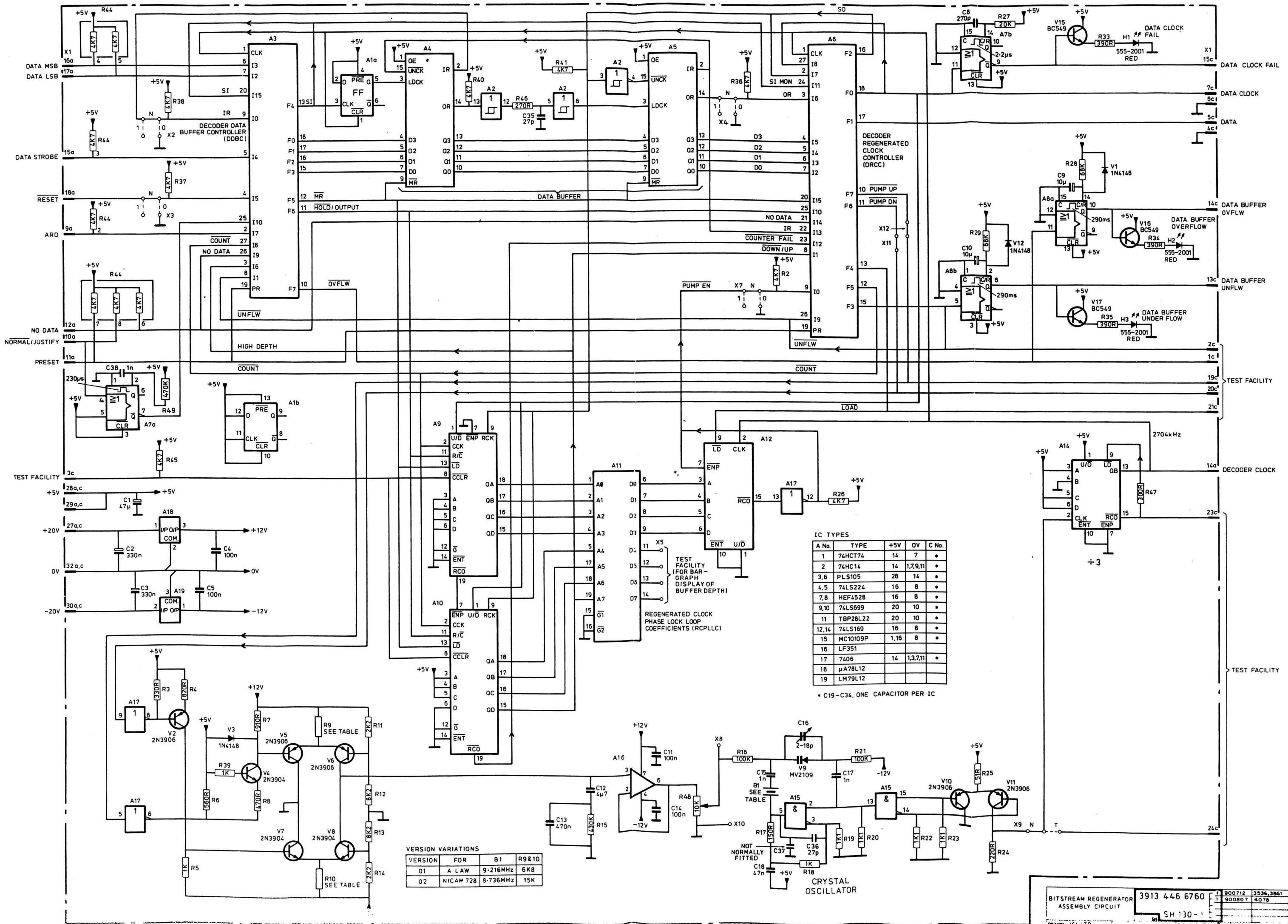
ARD (Amplitude Reference Data)
DATA FAIL.

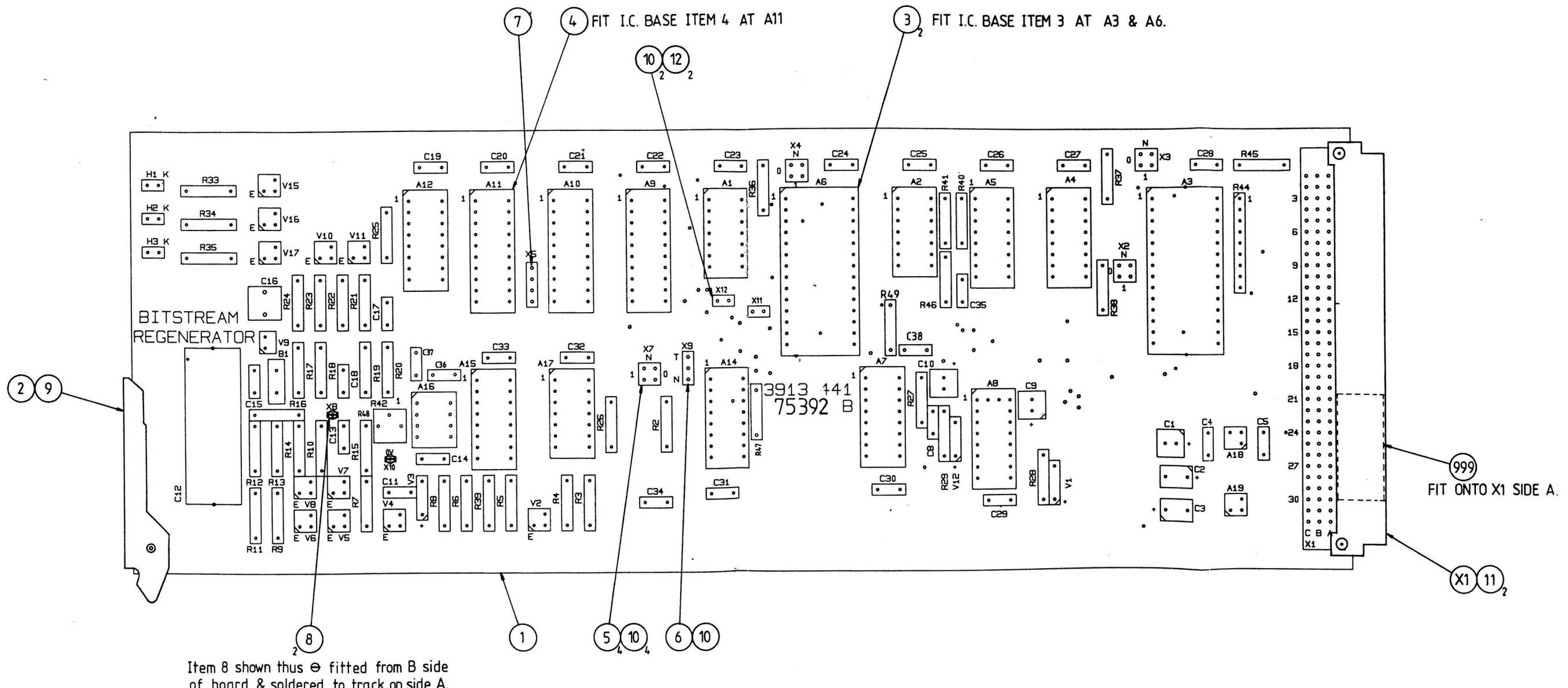
(b) Start up - a PRESET I/P

The DDBC resets the FIFO, checks the DRCC has preset the buffer depth counter and enables the DRCC with the HOLD/OUTPUT signal when the HIGH DEPTH signal indicates that the buffer is half full. Thus HOLD/OUTPUT must also switch the depth counter O/Ps from unlatched to latched.

The fault O/Ps from the board are:

CLOCK FAIL (board clock fail).
OVERFLOW (FIFO buffer overflow).
UNDERFLOW (FIFO buffer underflow).





STROKE NO	PGV NO
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

NOTE: THE STROKE LEVEL SHOWN HERE MUST NOT BE CONFUSED WITH THE ZEROLEVEL SHOWN ON ASSOCIATED DRAWINGS & PARTS LIST

DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING	
TOL UNLESS OTHERWISE STATED		SURFACE TEXTURE	AS USED ON
DIMENSIONS		ANGLES	HOLE
UNITS	SCALE	MATERIAL	
MM	INCHES	PROJECTION	ASSEMBLY NO.
	Z:1	TREATMENT	PATTERN NO.
SEE SEPARATE PARTS LIST			
SEE 3913 982 90010 CODE C.			
TITLE: BITSTREAM PCB		PCB	11/04
REGENERATOR ASSY		3913 446 7539	2/90 08 21 PGV4078

MONITOR 13913 446 69880Contents

CHANGE SUMMARY	Sh. 508-1
1. GENERAL DESCRIPTION	Sh. 595-1
2. FUNCTIONAL DESCRIPTION	Sh. 595-1
2.1 CPU and Memory	Sh. 595-1
2.2 Fault Inputs	Sh. 595-1
2.3 Fault Outputs	Sh. 595-2
2.4 Input/Output Ports	Sh. 595-2
2.5 Power Supplies	Sh. 595-2

ILLUSTRATIONS

Circuit Diagram	Sh. 130-1 and 2
PCB Assembly Drawing ..	3913 446 74930
	Sh. 110-1

PARTS LISTS

C H A N G E S U M M A R Y

MONITOR 1

3913 446 69880

References	Brief Description of Change						Documents Affected					
CA 35542 30.01.90	3913 036 55420 should be described as a PAL not an EPROM (A26, 27, 28).						Parts List					
CA 36470 02.04.90	PGV 4053 16.07.90	CA 38816 19.08.91	CA 40576 09.06.92	CA 40862 26.06.92	CA 38837 25.08.92							
CA 41507 07.12.92	ECN10294 18.10.94	ECN10736 09.05.95	ECN10964 01.08.95	ECN10972 28.09.95								
Various parts list and mechanical changes.												

MONITOR 13913 446 698801. GENERAL DESCRIPTION

The Monitor 1 module is a Z80-based processor system which, under the control of its software, monitors the fault outputs from the other modules in a Stereo Sound in Sync coder or decoder and declares faults when appropriate. For more information on the actual monitoring process, refer to the section on Monitoring in the associated system handbook (see Information Finder).

2. FUNCTIONAL DESCRIPTION2.1 CPU and Memory

The Z80 CPU, A5, runs at a clock rate of 4MHz. This is produced by the 8MHz oscillator around B1/V1, the D-type flip-flop A2a used as a divide-by-2, and the active pull-up, V2, which ensures fast rise and fall times for the clock edges. 32K of ROM and 16K of RAM are provided for the system. 16K of ROM, A6, contains a BBC BASIC interpreter, and a further 16K of ROM, A7, contains the software. On switching on, the contents of A7 are loaded into A8 and A9, two 8K RAMs, and the software is run from the RAM. By fitting R24 instead of R25, a 32K ROM may be fitted for A6. Memory decoding is provided by A3, A10a and parts of A11 and A16. A real-time clock facility is provided by the CTC device, A25.

2.2 Fault Inputs

24 fault input lines are provided, not all of which are used. These are taken to A26, A27 and A28, programmable logic devices programmed as octal R/S flip-flops, which are set by the fault input going active. The outputs of the flip-flops appear as three read-only ports at address 00, 20 and 40 Hex. The flip-flops assigned to each port are reset by the program reading from that port.

2.3 Fault Outputs

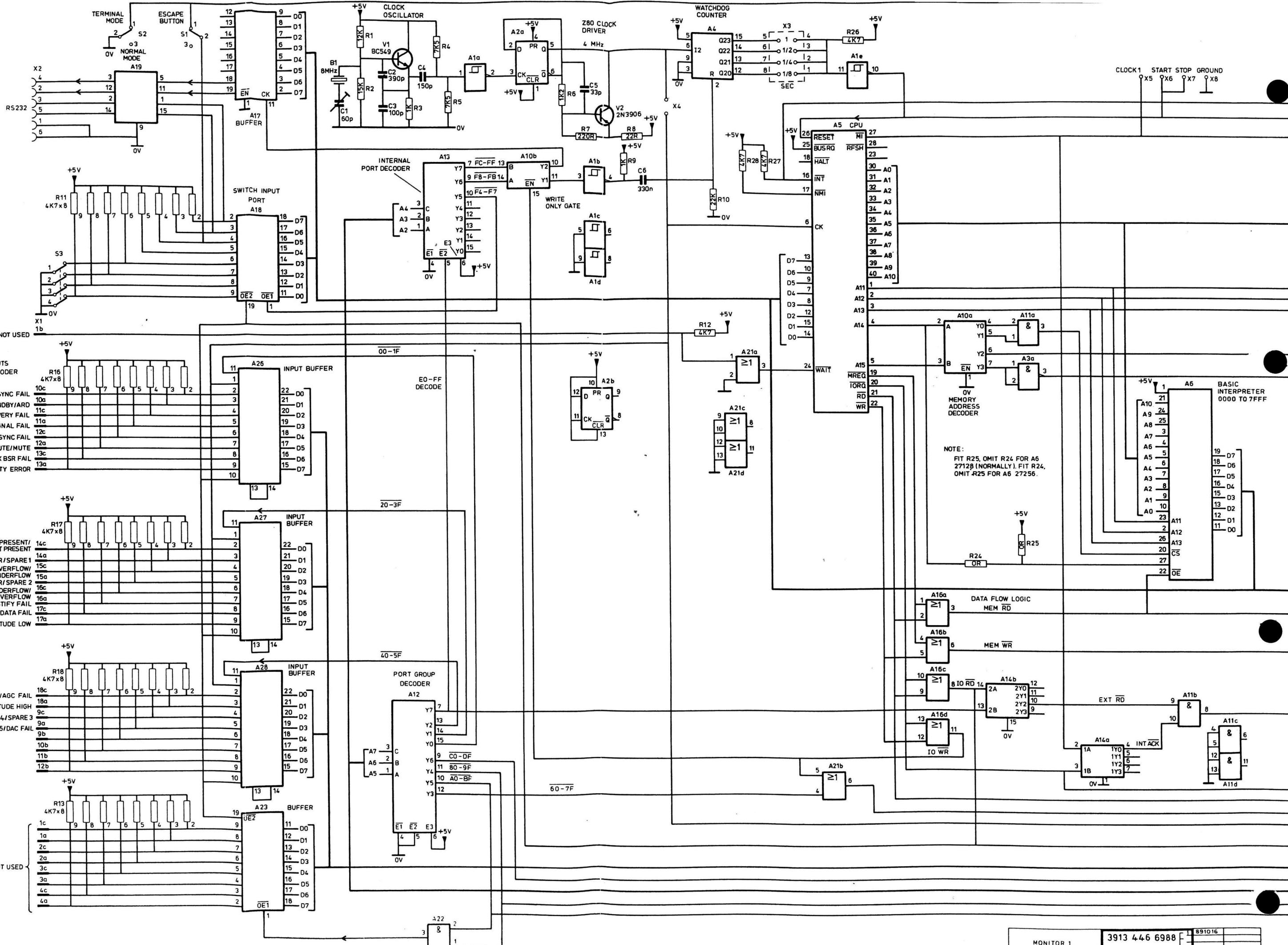
A main fault output (Green LED H1 and relay K1, driven by V4), and a secondary fault output (relay K2, driven by V5) are provided along with six open-collector outputs, A30, mimicked by red LEDs H2 to H8. All the fault outputs, except the main, are latched by A29, which also provides sufficient sink current to drive H2 to H8. The main fault output is driven from a monostable which has to be regularly triggered by the program to keep the output in the 'system good' state. This is so that, if the program crashes, the monitor will declare a fault. The main and secondary fault outputs and the open-collector outputs are driven from a write-only port at 60 Hex. The open-collector outputs are provided with an associated return path to OV.

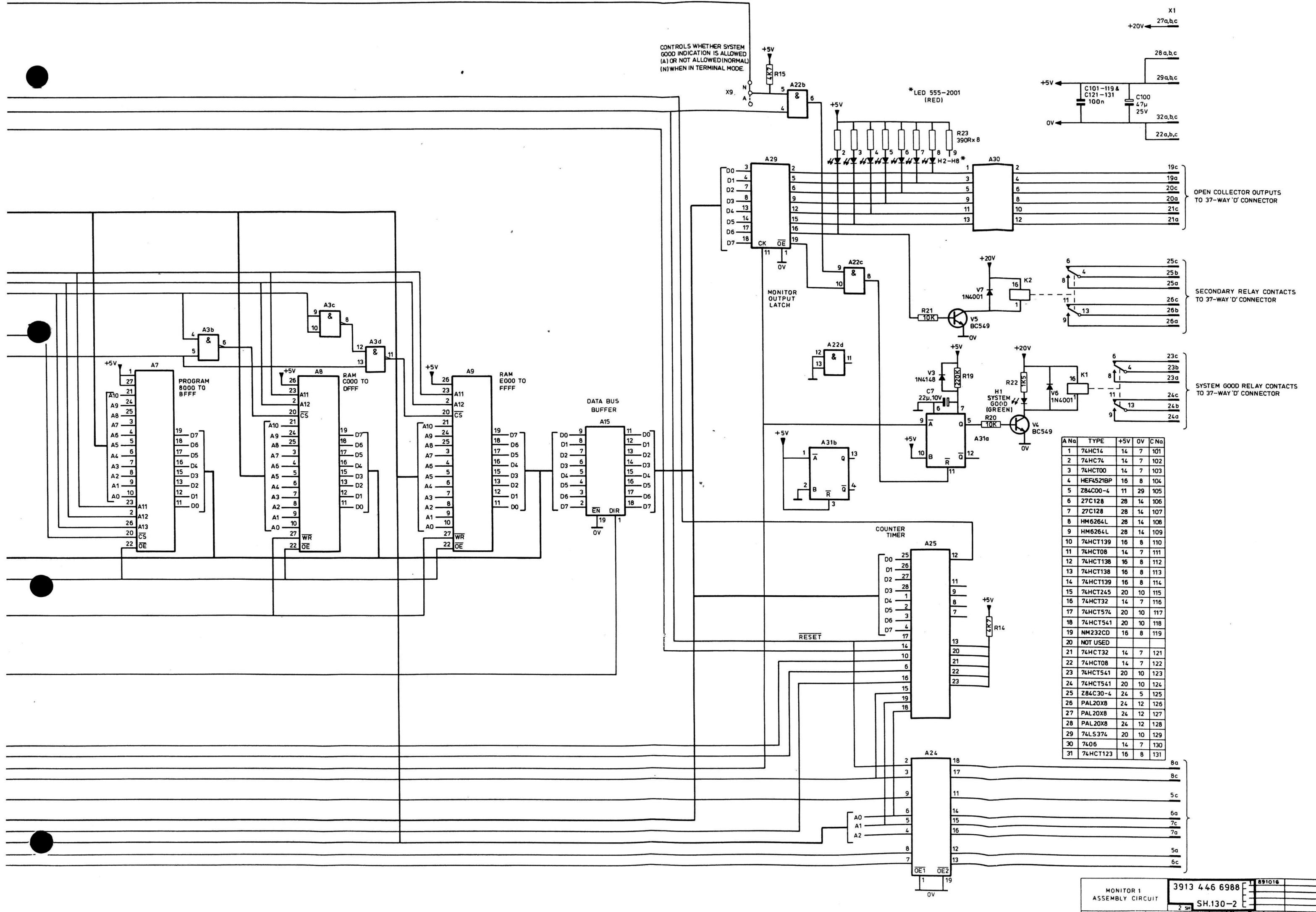
2.4 Input/Output Ports

A18 acts as an input port onto the data bus, buffering S3 and two RS232 input lines. S3 is set to indicate to the software the circumstances in which the card is working: as coder or decoder, with or without audio modules, and with or without audio comparison (Decoder only). A17 provides an output port for two RS232 output lines. The two RS232 ports are taken to X2 on the front of the module via A19, an RS232 driver. One is used for interactive control or modification of the software via a terminal; the other for loading a program from a microcomputer or sending a program from RAM to a PROM Programmer. For information on connections and data formats, refer to the Monitoring section in the associated system handbook. A TERMINAL ENABLE switch and ESCAPE button, S2 and S1, are provided for use with these facilities. A24 provides an 8-bit output bus, though this is not used. Port decoding and READ and WRITE signals are produced by A12, A13 and parts of A16, with A14 and A11b controlling the direction of the bi-directional data bus buffer, A15.

2.5 Power Supplies

+5V for the majority of the circuitry is obtained from the main rack power supply. The SYSTEM GOOD LED, H1 and the relays K1 and K2 are powered from the +20V supply in the rack, which is smoothed but not regulated. Hence, this may have up to 1V of ripple on it, but this does not affect the LED or relay operation.





CLOCK AND I/O (REFRAMER)3913 446 75490Contents

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2.2 Signal Selection and Routing	Sh. 595-2
2.3 Locking and Synchronisation	Sh. 595-2
2.4 Signal Selection and Synchronisation	Sh. 595-3
2.5 Tally-Backs and LED Indicators	Sh. 595-4
2.6 Reframing	Sh. 595-4
3. REFRAMING TIMES	Sh. 595-7
4. ADJUSTMENT AND TESTS	Sh. 595-8

ILLUSTRATIONS

Circuit Diagram	Sh. 130-1 and 2
Assembly Drawing	Sh. 110-1

PARTS LISTS

C H A N G E S U M M A R Y

CLOCK AND I/O (REFRAMER)

3913 446 75490

References	Brief Description of Change	Documents Affected
PGV 4245 26.11.90	The following parts added to Parts List: 2712 028 00877 Pin St St. 2522 178 15059 Pan head screw M3X8. 2513 712 02004 Washer M3. 2522 401 60008 Nut M3. 2500 622 00002 Rivet. 3913 081 67890 Mod Label. 3913 081 66640 Label, EPROM window.	Parts List
PGV 4255 04.12.90	A36, EPROM changed from 3913 935 20091 to 3913 935 20093.	Parts List
PGV 4279 17.12.90	A4, PROM changed from 3913 036 60530 to 3913 036 60660.	Parts List
CA 41507 07.12.92 ECN10270 06.10.94 ECN10283 12.10.94	Mechanical and parts list changes.	Parts List

CLOCK AND I/O (REFRAMER)

3913 446 75490

1. GENERAL DESCRIPTION

The primary functions of the module are:

- (a) To select data and clock signals for routing between other modules and the rear panel, and for locking of the internal timing reference oscillator and counter.
- (b) To provide digitally generated test tone data as an alternative to programme sound.
- (c) To hide discontinuities in the NICAM 728 bit-stream coming from the Bitstream Regenerator module or from the Auxiliary input, or when the module itself is asked to switch between these two sources.
- (d) To provide clock and framing signals for synchronising coders.

2. FUNCTIONAL DESCRIPTION

2.1 Master Oscillator

A5 is a 5824kHz oscillator on which depends the accuracy of the frequency of the 728 kbit/s bit-stream for the test tones generated by the Decoder, when in free-run mode. Its free-running frequency, which is set by R14, has a stability within ± 0.5 ppm over the temperature range, and with time should vary less than 0.5 ppm per year (less in later years).

2.2 Signal Selection and Routing

The normal signal routing through the module is data and clock in from the Bitstream Regenerator and out to the Audio Decoder module.

Alternatively, External Data and Clock applied via the Auxiliary Input on the Rear Panel to A1A inputs can be routed to the Audio Decoder module, or one of the tones generated in A36 can be selected. Signal selection is made by the lower three switches of S1, or by remote control lines A2 and A3 provided the top switch of S1 is set to Remote. X12 enables Tone 1 or Tone 2 to be selected from one of eight tones in A36. Tone 1 is intended as a line-up or test tone. Tone 2 is the fall-back tone in the event of signal failure, and the signal used by the reframer circuitry during reframing; Tone 2 is normally silence, though an alternative could be selected for test purposes. The format of Tone 1 or Tone 2 is automatically selected as Stereo or Mono according to the format of the last-used incoming signal, though this can be overridden by a link setting (X11). The standard tones available from A36 are listed in the System Description and User Information Manual, Installation, para 4.2.2.

Auxiliary Output 1 allows rear panel access to data and clock from the Bitstream Regenerator. Auxiliary Output 2 allows rear panel access to whatever signal is being sent to the Audio Decoder module, and to the relevant clock. C₀ is also available from Auxiliary Output 2 as the internal clock and counter are always synchronised to the Data being sent to the Audio Decoder module. (C₀ is the Application Control bit which is low for 8 frames and high for 8 frames, thus defining a 16-frame sequence; at this output it goes high as the first bit of frame 1 is output, and low as the first bit of frame 9 is output.)

2.3 Locking and Synchronisation

The Auxiliary Input is for Ext Data and its associated clock input, to which the internal oscillator may or may not be locked when a test tone is selected for decoding. When Ext Data is selected for decoding, the internal oscillator is locked to Ext Clock. When data extracted from syncs is selected, the internal oscillator is locked to the clock regenerated on the Bitstream Regenerator module. Any clock selected for locking is routed through the analogue demultiplexer A8 (section X) to the Signal In (SIN) pin of the Phase Locked Loop (PLL) controller A6.

The output of A6 is routed through A8 (section Y) to the frequency control pin of the oscillator. PLL control filtering is provided by R13, R12, C55 and C56. R11 provides the correct source impedance for the required frequency range of A5. The clock being used for locking is also fed to A7A. A7A controls one section of A8, such that if the clock should fail, the output from A6 is prevented from reaching A5 before it can send the oscillator frequency to one end of its range.

For two coders to code audio in synchronism with each other, not only must their clocks be synchronous, but their frame sequences must also be synchronous. This is achieved by C_0 locking. C_0 may be input at the coder's Auxiliary input, with related clock. A decoder may be used as a source of C_0 and related clock. C_0 is obtained from the Read Address Counter and fed to Auxiliary Output 2.

2.4 Signal Selection and Synchronisation

Switches (S1) on the front of the module provide local control of signal selection and synchronisation mode. Their functions are indicated on the circuit diagram and on the inside of the front panel of the equipment. When the top switch is set for 'Remote', the input lines A3, A2, A1, and A0 become effective for remotely controlling these selections. They may be either 5V logic or pull-downs to indicate a zero, and open circuit to indicate a '1'. The presence of External input signals is monitored by retriggerable monostable ICs (A2 and A3). The lack of any such signals is indicated by LEDs H1 - 4, and fed to A4. A4 also receives the logic signals from the remote control inputs and the local control switches, and controls other ICs involved in synchronisation and signal selection.

2.4.1 Locking and Remote/Local

While SIS is selected, the local oscillator is locked to the clock regenerated from SIS, and generates the 728 clock for the counters in the reframer section.

While Ext Data is selected, the local oscillator is locked to Ext Clock. If Ext Clock fails, the local oscillator is free-running and Signal Fail (H5) is indicated.

While Tone 1 or Tone 2 is selected remotely, the local oscillator is locked or free-running as follows:

<u>A3</u>	<u>A2</u>
-----------	-----------

1 1 Local control of signal selection and lock mode.

1 0 Locked to Clock regenerated from SIS. If data from SIS fails, it free-runs; Signal Fail is indicated.

0 1 Locked to Ext Clock. If Ext Clock fails, it free-runs; Signal Fail is indicated.

0 0 Free-run.

While Tone 1 or Tone 2 is selected locally, the local oscillator is locked or free-running according to the switch settings on the front of the module. The effects of signal failure are equivalent to those listed above for remote control.

2.4.2 Signal Selection for Decoding

Remote signal selection for decoding depends upon control lines A1 and A0 as follows:

A1 A0

1	1	From SIS. If data fails, Tone 2; Signal Fail indicated.
1	0	Ext Data. If data fails, Tone 2; Signal Fail indicated.
0	1	Tone 1.
0	0	Tone 2.

Local Signal Selection is according to switch settings on the front of the module. The effects of signal failure are equivalent to those listed above for remote control.

2.5 Tally-Backs and LED Indicators

B0 to B3 tally-backs follow the coding of A0 to A3, indicating fall-back conditions due to signal failure when relevant, rather than requested conditions. If Local Control is selected either locally or remotely B3 and B2 are '1', to indicate 'local' and they do not indicate the lock condition selected. B4 is a remote Signal Fail indication. H5 is the on-board Signal Fail indicator. H6 indicates selection of Tone 1 or 2 for whatever reason, including momentary use of Tone 2 during reframing. H1 - 4 are described in para 2.4.

2.6 Reframing

2.6.1 NICAM 728 Bit-stream Format

The bit-stream consists of 1ms 'frames' each consisting of 728 bits; there is also a 16-frame sequence. Each frame begins with an 8-bit Frame Alignment Word (FAW) followed by four Application Control bits. The first of these, C₀, is '1' for eight consecutive frames, and then '0' for eight consecutive frames, thus identifying the 16-frame sequence. C₁, C₂, and C₃ indicate whether the data format is Stereophonic, Monophonic, Data or shared. For the purpose of operation of the Reframer, any format

which is not Stereo is regarded as Mono. The significant difference between Stereo and Mono formats is that the data for two channels in Stereo are interleaved within each frame, while for Mono the data for the two signals are interleaved frame by frame. Any change in format should occur only on the first frame of a 16-frame sequence, and should be signalled 16 frames in advance.

2.6.2 Reframer Operation

The Reframer module has two modes of operation:

- (a) FULL reframing, in which the 16-frame sequence is maintained, and the data may be delayed for up to 17ms.
- (b) MINimum delay reframing, in which the maximum delay of data is 2ms for a Stereo Signal, or 3ms for a Mono signal, but the 16-frame sequence is not maintained.

FULL or MIN mode is selected by two moveable links, X24 and X25.

2.6.2.1 FULL Reframing

Incoming data is written into a 32-frame memory (RAM) A30 and, while all is well, read out at least 1ms later. The FAW is checked each frame, as it is written into the memory. If it is wrong, a continuous search for a FAW is begun and, after the end of the frame currently being read out, data is read from a Read Only Memory (ROM) A36, containing data equivalent to silence. The FAW check is performed by the Field Programmable Logic Sequencer A18 which also controls the reading of data from RAM or ROM and resets their associated Write and Read Address Counters A26 - 29 and A31 - 35 when necessary. Since the reading of data from RAM is at least one frame behind the data being written, the frame being read can safely be continued to its end without reaching the error detected. The data read from ROM continue the 16-frame sequence without interruption, and are selected from Stereo or Mono format areas of ROM according to the format read from the last good frame of incoming data.

When the continuous search of incoming data yields a FAW, the refraher checks whether the FAW also occurs 728 bits later. If it does not, the refraher reverts to its continuous search mode again; if it does, C_0 is also checked. If C_0 does not change within 8 frames, the FAW is regarded as spurious, and a continuous search for another FAW begins. If C_0 does change, the RAM write address counter is reset so that data for the new frame is stored in RAM starting at address zero. (Conceptually zero, not literally zero, because there are 296 unused RAM locations at the beginning of each block of 1024 to suit the address counter configuration.) If or when the C_0 change is from 0 to 1 (indicating frame 1) the output data can be read from RAM after one more frame. How much after, depends upon where the Read Address Counter is in its 16-frame sequence, for the switch from ROM back to RAM is made only at the beginning of a 16-frame sequence. At this point the Read Address Counter is reset in case it was about to read from the second half of the 32-

frame store. Additionally, before the switch to RAM is made, the format of the incoming bit-stream is checked to be the same as the silence being read from ROM. If it is not, the forthcoming change in format is signalled by reading data from the other half of the ROM and, provided no errors are found in the meanwhile, the switch to RAM is made 16 frames later.

After the C_0 change from 0 to 1 has been found, the incoming C_0 is checked every frame. If the correct sequence is broken, the reframer reverts to searching for a C_0 change and, if it has already switched to RAM for its source of output data, it switches back to ROM. If more than 8 frames pass without a C_0 change, or if the FAW check fails, the reframer reverts to continuous FAW search mode.

2.6.2.2 MINimum Delay Reframing

The operation in MIN mode is as described above for FULL mode up to the point when a C_0 change from 0 to 1 is found. Again, at least one more frame is necessary before the output can be read from RAM. Then if the detected incoming signal format is Stereo the switch to RAM takes place at the beginning of the next frame to be read. If the format is Mono the switch to RAM takes place at the beginning of the next odd frame to be read ('odd' when the frames in a 16-frame sequence are numbered 1 to 16). As this switching takes place the Read Address Counter is reset, so there may be a discontinuity in the 16-frame sequence.

In MIN mode C_0 is checked only during the reframing process up to the point when the change from 0 to 1 is found. Any subsequent errors in the C_0 sequence without errors in FAW, will pass through the reframer undetected.

Additionally, in MIN mode there is no format check before the output source is switched to RAM, so a change between mono and stereo at a discontinuity will not be signalled 16 frames in advance.

2.6.3 Response of Decoders

In FULL reframing mode, decoders should detect no errors.

In MIN reframing mode, decoders should detect no errors on a sample by sample basis, but should detect any change in the C_0 sequence. How they respond to this will vary from decoder to decoder. The preservation of correct samples should prevent unpleasant noises associated with unsynchronised switching, but muting is likely as the decoder locks onto the new C_0 sequence. In the case of the decoder 'chip' used in the Stereo Sound in Syncs equipment, the reaction to the change in C_0 sequence depends upon exactly what change occurs. If the sequence jumps from frame 7, 8 or 9 to frame 1, the decoder mutes momentarily within 10 or 20 milliseconds and indicates parity errors, though it should not have found any. If the jump to frame 1 occurs at any other point in the frame sequence, the decoder chip carries on for about 500ms before muting, in this case not indicating parity errors. In neither case are there unpleasant noises as would be associated with genuinely incorrect data.

3. REFRAMING TIMES

The histograms below show measured FULL reframing times when switching between two stereo signals both with random frame timing relative to the Read Address Counter. Similar results would be expected if both signals were dual monophonic. If one signal were stereo format and one were mono, the reframing times would be expected to be greater by 16ms. In MIN reframing mode, the times would be expected to be shorter by between 0 and 15ms for a Stereo signal and by between 0 and 14ms for a Mono signal.

FULL REFRAMING - STEREO

MUSIC	250Hz	ANALOGUE SILENCE	DIGITAL SILENCE
1	1	1	1
2	2	2	2
3	3	3	3-
4	4	4	4
5	5	5	5
6	6	6	6
7	7-	7	7-
8	8	8	8
9	9--	9	9-
10	10-	10	10
11	11--	11	11
12	12-	12	12
13	13---	13	13-
14	14----+	14	14-
15	15----+-	15	15
16----	16----+	16--	16
17---	17---	17-----+---+-	17--
18----+	18---	18-----+	18
19----+-	19---	19----+	19
20----+-	20----+-	20-----+	20--
21--	21----+	21-----+	21-
22----+-	22---	22----	22--
23----+---+	23----+--	23----+	23-
24----+	24----+--	24----+	24----
25----+	25--	25--	25--
26----+-	26---	26-----+	26-----+-
27--	27----	27-----+	27----
28----+	28---	28-----+	28----
29----+---	29--	29----	29-
30----	30	30----+--	30----
31----+---+-	31--	31----+---+	31----+--
32--	32--	32	32----
33	33--	33-	33----+
34	34-	34-	34-----
35	35-	35	35----+
36	36	36	36---
37	37	37	37----
38	38	38-	38----
39	39	39-	39----+--
40	40	40	40--
41	41	41--	41--
42	42	42--	42-
43	43	43-	43-
44	44	44--	44----
45	45	45	45----+--
46	46	46	46-
47	47	47	47-
48	48	48-	48----
49	49	49	49
50	50	50	50--
51	51	51	51
52	52	52	52
53	53	53	53
54	54	54	54
55	55	55	55-
56	56	56	56-
57	57	57	57
58	58	58	58
59	59	59	59
60	60	60	60
61	61	61	61
62	62	62	62-
ms	ms	ms	ms

4. ADJUSTMENT AND TESTS

The following adjustment and checks may be made as necessary:

(1) Oscillator Frequency

Set R14 for the correct free-running frequency of the 5.824MHz oscillator. The oscillator frequency is slightly affected by a probe on its output, therefore check for 2912000Hz at X26 (A23 pin 14). Required accuracy is ± 0.1 ppm - beware of inadequate frequency counters!

A quicker method, if an adequately accurate NICAM 728 signal is available, is to input the accurate source, select Tone 1 or 2 and Free-run. Then compare the two waveforms at X22 and X10, and adjust R14 for zero slip.

(2) A7A Timing

Check for a pulse on X7 every Clock period ($1.3\mu s$); its width should be approximately $0.7\mu s$, but is not critical.

Now mount the module on an extender in a Decoder, fed with a Stereo Sound in Syncs signal from a Coder.

(3) Clock Locking and Phasing

Use Switches S1 or Remote Control to lock the oscillator to the clock from Ext or SIS. Check that the 728kHz squarewaves at X10 and X22 are locked and in phase (within one tenth of a cycle).

The following tests can be done only as far as Remote Control panel and Auxiliary Input facilities are available.

(4) Local Signal Selection

Set S1-1 to Local; check signal selection by S1-4,5,6.

(5) Local Synchronisation

With Tone 1 or 2 selected, check locking to SIS, Ext or free-run according to S1-2,3.

(6) Remote Signal Selection and Synchronisation

Set S1-1 to Remote. Check signal selection and locking according to Remote control keys.

(7) Fall-back (Local or Remote)

Check correct fall-back of signal source and locking with signal fail and/or clock fail as detailed in the module description, by disconnecting the SIS input at the back panel, and using any other facilities available.

At the same time check that LEDs H1 - 5 correctly indicate missing inputs. H4 (C_0 from Decoder module failed) should not normally light while the reframer is functioning properly, but can be checked by selecting Tone 2 and momentarily removing the Tone 2 selection link.

(8) Local Priority

Check that 'Local' on either S1-1 or on the Remote Control Panel overrides 'Remote' on the other.

(9) Stereo/Mono Detection

Monitor X11 (set to N = Normal); check that it is '0' when a Stereo signal is received and '1' when a Mono signal is received. It may be useful to select Tone 1D - refer to the information on the Tones EPROM in the System Description and User Information Manual, Installation, para 4.2.2.

(10) Write-Read Delay

- (a) Monitor X22 and X10 with an oscilloscope triggered from X22.
- (b) With X24 and X25 set for FULL reframing, check that the delay between the squarewaves at X22 and X10 is always between 1ms and 17ms. The system should be reset randomly several times by momentarily removing link X6. The result should always be 1 to 17ms.
- (c) With X24 and X25 set for MINimum delay reframing and receiving a Stereo signal, check that the delay range is 1 to 2ms.
- (d) With X24 and X25 set for MINimum delay reframing and receiving a Mono signal, check that the delay range is 1 to 3ms.

(11) Reframing Time

If facilities are available for switching between two

unsynchronised data sources (e.g. a Stereo Sound in Syncs Coder and another data source connected to the Auxiliary Input of the Coder or Decoder), the reframing action and time can be checked.

With FULL reframing, when the data source is switched, there should be no indications of parity errors or mute from the Audio Decoder module and no unpleasant sounds from the audio output of the Decoder (compared with audio from the Coder's Decoder module, if the source switching is being done at the Coder).

For MIN reframing, see 2.6.3, 'Response of Decoders'. While switching between the two signals monitor X15 with an oscilloscope set to Single sweep, positive trigger, 10ms/cm, in order to check that the reframing time is in the range indicated by the histograms given in section 3.

The reframing check could be repeated several times for different random timings of the two signal sources for:

- (a) FULL reframing, Stereo to Stereo or Mono to Mono,
- (b) FULL reframing, Stereo to Mono and Mono to Stereo,
- (c) MIN reframing, Stereo to Stereo,
- (d) MIN reframing, Mono to Mono,

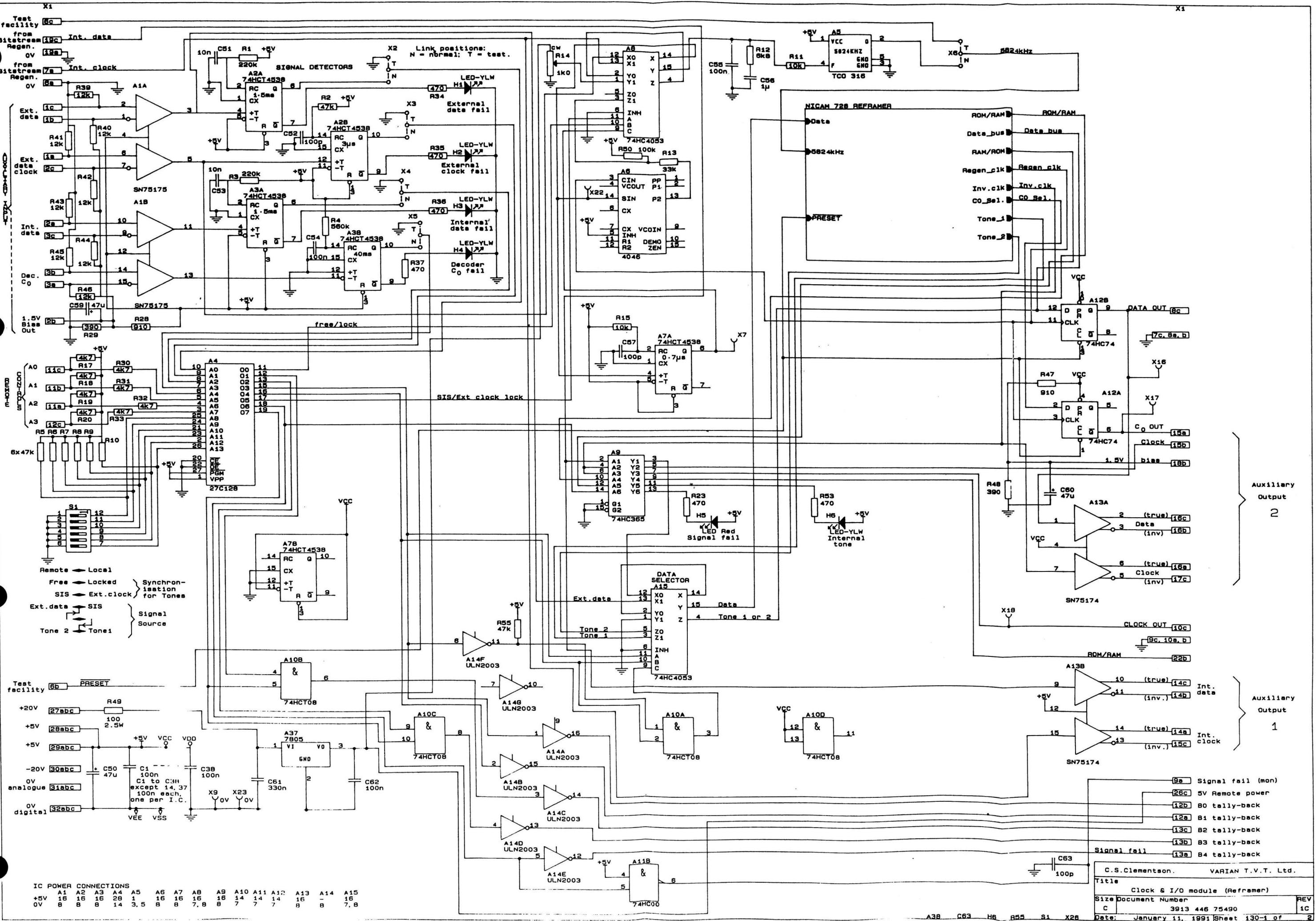
and may include frame-repetitive (e.g. silence or 1kHz digitally generated tones) and non frame-repetitive signals (e.g. music or tones below 1kHz). Note that the internal timing of a Coder or Decoder can be changed randomly by momentary removal of link X6 on the Clock and I/O module.

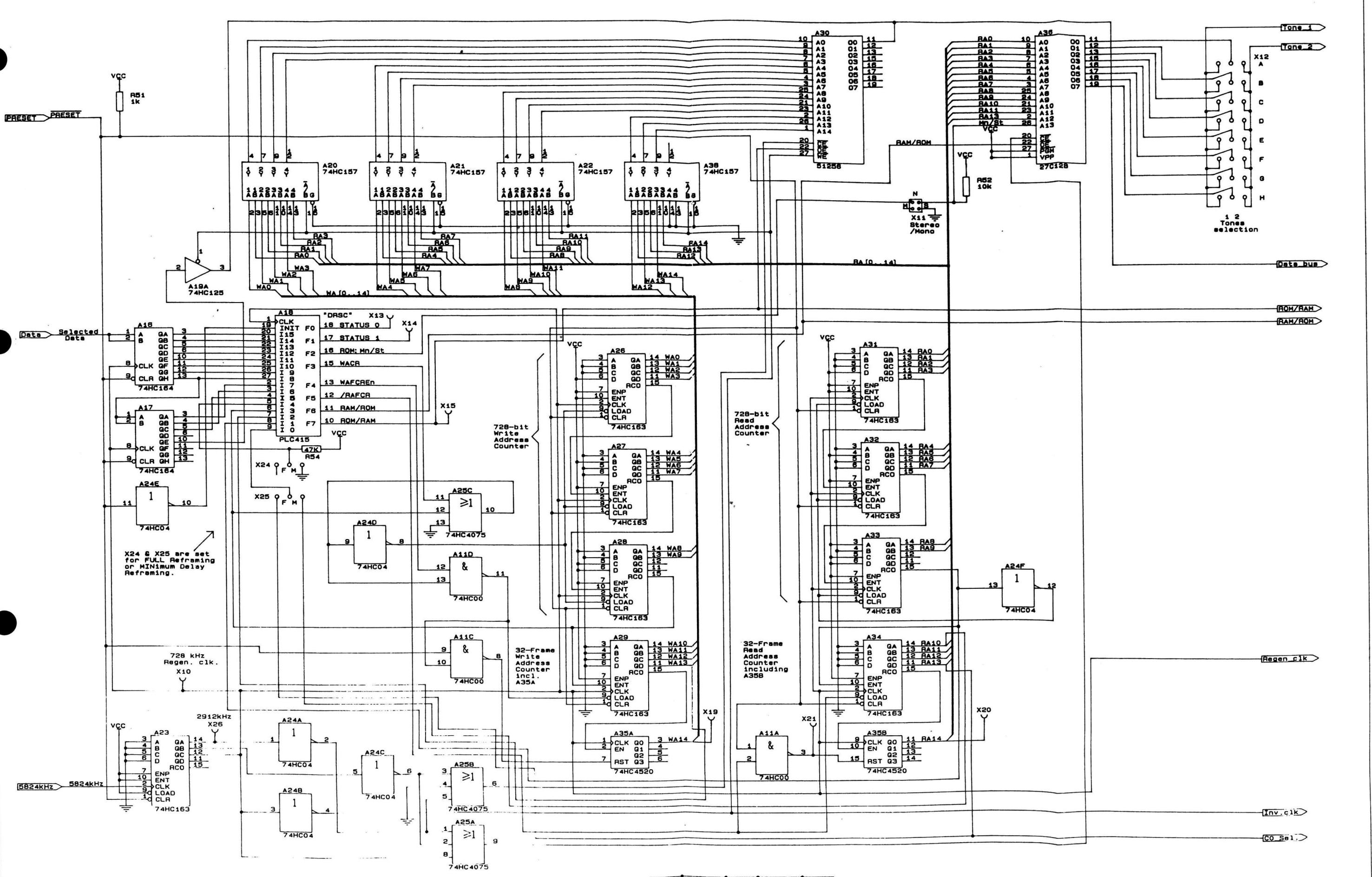
(12) Bias Outputs

Check that there is a +1.5V bias output at X1-2b and X1-18b.

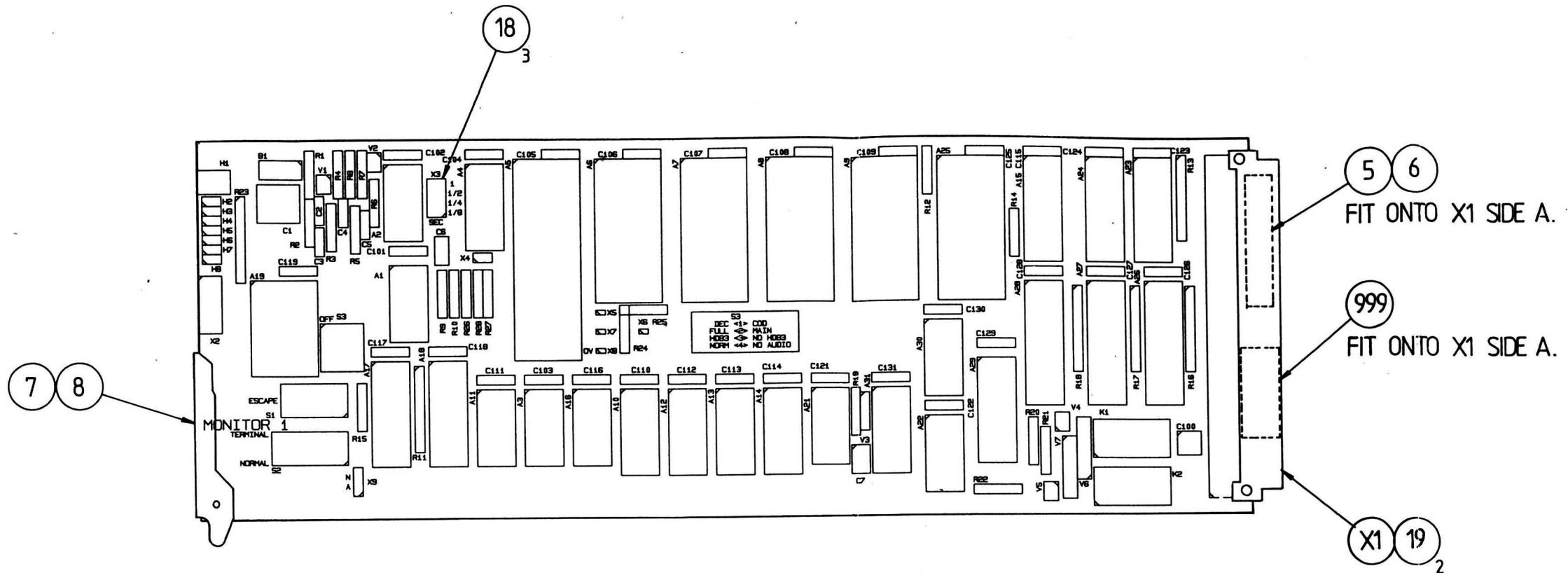
(13) Auxiliary Outputs

Check that there are true and inverse outputs for Data and Clock for Auxiliary Output 1 and for Auxiliary Output 2.





Varian TTV Ltd., CAMBRIDGE, ENGLAND.
Design Engineer: C.S.Clementson.
Title: NICAM 728 REFRAMER.
Size Document Number: C 3913 446 75490
REV 1B Date: January 11, 1991 Sheet 130-2 of 2



FIT IC BASE ITEM 15 AT A6,A7,A8,A9,A25.

FIT IC BASE ITEM 16 AT A5.

FIT IC BASE ITEM 17 AT A26,A27,A28.

MOD. LEVEL STRIKE PLATE INSTRUCTIONS

1 AFFIX STRIKE PLATE No. 3913 081 66620, ISSUED WITH THIS ASSEMBLY, IN POSITION INDICATED

2 STRIKE OFF NUMBERS ON PLATE TO LEVEL INDICATED IN THIS DETAIL

THE STRIKE LEVEL SHOWN HERE MUST NOT BE CONFUSED WITH THE ISSUE DATES SHOWN ON ASSOCIATED DRAWINGS & PARTS LISTS.

STRIKE No	P G V. No
1	
2	3342
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

DO NOT SCALE THIS PRINT				DIMENSIONS ARE SHOWN AFTER PLATING		
DIMENSIONS		TOL UNLESS OTHERWISE STATED		SURFACE TEXTURE		1st USED ON
UNITS	SCALE	ORIG. DRG.	MATERIAL	ANGLES	HOLDS	
MM						
PROJECTION		SEE SEPARATE PARTS LIST.		TREATMENT		
1st		SEE 3913 982 90010 CODE C.		3rd		
THE MONITOR 1 PCB ASSY DRG.				3913 446 7493		1B 1870320 1 187 11 13 PGV 3342
SUPERSEDES		1 SH 10 SH 10-1				
DRAWN T.P.		MECH CHK		ELECT CHK		APPROVED
PYE TVT LIMITED CAMBRIDGE (TRANSMITTER DIV.) © 1987						DATE DRAWN 870320 FORM A 2

3913 446 75460

SERIAL OUTPUT

3913 446 75460

NOT SUPPLIED

Jan/90

AUDIO DECODER3913 446 7544001VERSION 1 - AUDIO AND DIGITAL MONITORINGContents

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3.1 General	Sh. 595-4
3.2 Procedure	Sh. 595-4

ILLUSTRATIONS

Circuit Diagram	Sh. 130-1
Assembly Drawing	Sh. 110-1

PARTS LISTS

C H A N G E S U M M A R YAUDIO DECODER3913 446 7544001

References	Brief Description of Change	Documents Affected
PGV 3739 89.09.22	R13 and R51, potentiometers, 10k, 2113 391 00577 added.	Circuit Diagram Assembly Drawing Parts List
PGV 3749 89.09.28	R73, 39R, 2.5W, 2113 256 02292 added between the output of A2 and the input of A30.	Circuit Diagram Assembly Drawing Parts List
PGV 3799 89.11.16	Parts List up-dated. On the circuit diagram R73, 39R re-numbered R74. C11 changed from 10μ to 47μ F. A30, 5V regulator, changed from 9332 110 51742 to 7805, 3913 935 00001. Potentiometers R13 and R51 deleted. Socket DIL, 24-way x 0.6 deleted. Minor mechanical changes.	Circuit Diagram Parts List
PGV 4222 12.11.90	R72, 3k9, 2322 156 13902 changed to 5k1, 2322 156 15102 and made adjustable on test. Two solder tags, 2413 015 14168 added.	Circuit Diagram Assembly Drawing Parts List Text
CA 41598 08.11.93	Crystal Insulator fitted to B2.	Assembly Drawing Parts Lists
CA 38426 22.03.91	CA 32796 CA 39314 CA 40516 CA 41164 CA 41598 21.08.91 05.11.91 06.04.92 12.01.93 08.11.93 Various mechanical and parts list changes.	Parts List
ECN10283 12.10.94	Parts list amended.	Parts List
ECN10383 14.11.94	R72 AOT resistor changed from 5K1 to 4K7.	Circuit Diagram Parts List
ECN10704 28.04.95	A22 replaced by different type.	Parts List

AUDIO DECODER3913 446 7544001VERSION 1 - AUDIO AND DIGITAL MONITORING1. GENERAL DESCRIPTION

This board is based around the Texas CF70123 NICAM decoder chip and provides latched and buffered outputs for the control bits C0 to C4, the additional data bits AD0 to AD10 and the two Nordic data bits CBI0 and CBI1.

The input to the decoder board is made via a dual one-of-four data selector which is controllable externally. Audio output from the board is in the form of balanced 600-ohm lines plus a headphone socket. The output from the decoder chip is in an I²S bus format. This is fed to a digital filter chip which also performs four-fold oversampling and error interpolation on the signal.

The output from the digital filter is then fed to the DAC still in the I²S bus format. De-emphasis and the remaining filtering of the audio signal are performed in a multiple operational amplifier (A22) which also provides a headphone output. A pair of low-noise dual operational amplifiers is then used to provide a balanced, though not isolated, line output signal to the outside world.

To find the Nordic data bits, seven bits of data in a block are taken from the interleaved 728-bit bitstream. They are then EOR-ed together and the result counted for each of five blocks of data. The decision for a 1 or a 0 is arrived at by comparing the count to 2 and then setting the appropriate latch.

- Notes:
- 1. The control and data bits are latched at the end of the additional data by the falling edge of ADW.
 - 2. The two Nordic data bits are latched during the last clock cycle of the frame and the first clock cycle in the next frame.

2. FUNCTIONAL DESCRIPTION

NICAM 728 clock and data are brought into the board via A29 which is a dual one-of-four data selector; the two control lines are normally held high but can be controlled via the remote control socket.

The selected clock and data are then fed to the decoder chip via a buffer (A6). Reconstituted 728kHz clock and 8.192MHz clock are produced from two phase-locked crystal-controlled oscillators of 5.824MHz and 16.384MHz respectively. Along with two control lines the 728 clock and data are fed to the digital decoding part of the board. The two control lines are FAAWC which goes high from the start of the frame alignment word to the start of the additional data bits and ADW which goes high for the duration of the additional data bits.

Clock for the shift register is generated by three gates, A26D, A28B and A27D, which delay the 728kHz clock by half of one 5.824MHz clock cycle. This ensures that the data on the input to the shift register is stable.

The 728 data are fed to a 16-bit shift register, A18, A19 via an exclusive OR gate, A26A. Control of the EOR gate is from the inverted ADW line via an AND gate (A27A, A25E), this disables the feedback from the output of the shift register during the data bit period. These data bits are then latched into two latches, A20, A21 on the falling edge of ADW.

During the interleaved data part of the frame the feedback around the shift registers is enabled via A27A, A25E. Data are fed into the shift register and EOR-ed in A26A with the bit that was 16 bits before it; this has the effect of finding the parity on these two bits.

As the interleaved NICAM data are fed into the shift registers the Nordic data bit decoding is controlled by the PROM A12, which is clocked at 1.456MHz from the 16-bit counter A13, A14. A negative-going reset pulse of half a 5.824MHz clock cycle for the counters is generated by A28A and A27B on the rising edge of FAAWC. This ensures that the prom will always be in step with the incoming data. The output from the PROM is latched into A8 which is clocked from an inverted 2.912MHz clock. This PROM controls the clearing of the shift registers at various points and also counts the result into either of two counters, A15, A16. At the end of the frame the count from A16 is compared with '2' in A17, a 4-bit magnitude comparator, the result (CIB0) is then latched into the top half of A10. The output from A15 is then loaded into A16, compared with '2' and the result latched into the bottom half of A10 as CBI1.

A7, A8 and A9 are open collector drivers which are used to buffer all outputs. Control bits C0 to C4 are fed from A4 to the rear connector via the open-collector buffers in A8.

If the incoming signal has more than 1 in 100 parity errors and the MUTEEN pin is low then the decoder chip will provided a mute signal which is fed to the digital filter chip A3. When the MUTEEN pin is taken high this mute is disabled allowing signals with fewer than 1 in 100 errors to be output.

A low on C4EN will provide a mute signal if control bit C4 is low,

indicating that the FM transmission and the stereo signal are different. A high on C4EN will unmute the decoder allowing test transmissions to proceed.

Output from the decoder chip to the digital filter chip is in I²S bus format. This I²S bus is also buffered in A6 and fed to the edge connector this is so that a good isolated and balanced output can be obtained from another board. Error LEDs H1 (MUTE) and H2 (PARITY) are also fed from this point, with the feed to H2 being via V5, R65, R66 and C42 which stretches the parity pulse so that it is long enough to be seen.

Remote control of the mute feed into the digital filter is achieved via the AND gate made up of A27C, A26C and the control links MUTESEL and LOC/REM.

The digital filter chip digitally filters the audio signal and provides an effective four-fold oversampled output to the DAC A5. If an erroneous signal is sent to the digital filter chip it will interpolate between the last good signal and the next good signal to provide a click-free signal to the DAC. In the event of a mute error the digital filter will step down to zero using a raised cosine function in 32 steps.

Still in the I²S bus format the signal is then passed to the dual 16-bit DAC. Biasing of the outputs on the DAC is performed partly by its own internal biasing and partly by R7, R8, R9 and C18. DC blocking is provided by C37 and C38, while R6 and R10 provide bias for the first operational amplifier in A22.

The various operational amplifiers in A22 are used to provide the de-emphasis and anti-aliasing filtering for the audio signal. A22 also provides the headphone feed and a feed to a pair of low-noise operational amplifiers, A23, A24. These operational amplifiers are arranged to produce a balanced 600-ohm line signal which is fed to the rear connector. Both the headphone and the line output levels are adjustable independently of each other.

Due to the method by which the decoder chip generates its mute there is a delay during which time a lot of erroneous signals can be produced. In order to prevent this breaking through an additional mute signal is produced by D3, D4, R67, R68, R69 and C43. This signal is fed through a buffer in A7 to the mute pin of A22 which, with C14, normally provides a mute at switch-on.

3. SETTING-UP PROCEDURE3.1 General

This procedure assumes an untested and brand new board.

Test equipment required:

Voltmeter, e.g. Fluke or AVO.

20MHz bandwidth oscilloscope.

x10 oscilloscope probes.

Accurate NICAM 728 clock and data generator with presetable Control, Additional and Nordic data bits.

Power supplies:

+20V and -20V at 500mA

+5V at 1A, i.e. Coder or Decoder Rack Frame Assembly and extender card.

Audio distortion/noise meter.

3.2 Procedure

(1) Set the links to the following positions:

X3	Low
X4	High
X15	High
X16	Local
X17	Low
X18	High.

(2) Connect all the power supplies and check that the following voltages exist between OV (X12) and the following points:

A4	Pin 1 or Pin 21	+5V
A22	Pin 26	-12V
A22	Pin 28	+12V
A22	Pin 1	+5V.

All the above voltages should be within 5%.

(3) Check that Pins 2 and 14 of A29 are held high; if not and

you are using a Coder or Decoder Rack Frame, check the input select on the Clock and I/O module.

- (4) Connect NICAM 728 data to X1 Pin 12a and NICAM 728 clock to X1 Pin 12c. Set the NICAM generator to stereo silence with all control, additional and Nordic data bits off. Check that the voltage between A5 Pin 6 and OV (X12) and A5 Pin 5 and OV (X12) is +2.5V +0.5V, -0.3V. If not select a value for R72 to achieve this.
- (5) Using the oscilloscope and a x10 probe look on Pin 7 of A29 and check that NICAM 728 data is present. NICAM 728 clock should be present on Pin 9 of A29.
- (6) Connect the oscilloscope probe to X5 and adjust C31 for a stable even mark/space square wave. Check on X6 for a 5.824MHz square wave of approximately 5V p-p.
- (7) When this condition is obtained repeat (6) for X7 and X8 but at a frequency of 16.384MHz, using C35.
- (8) Check on Pin 40 of A4 for a clock signal of 8.192MHz.
- (9) Compare the waveforms present on Pins 3, 4 and 33 of A4 to those in Figure 1 and ensure that they are the same. The same signals should also appear on Pins 2, 1 and 3 of A5.

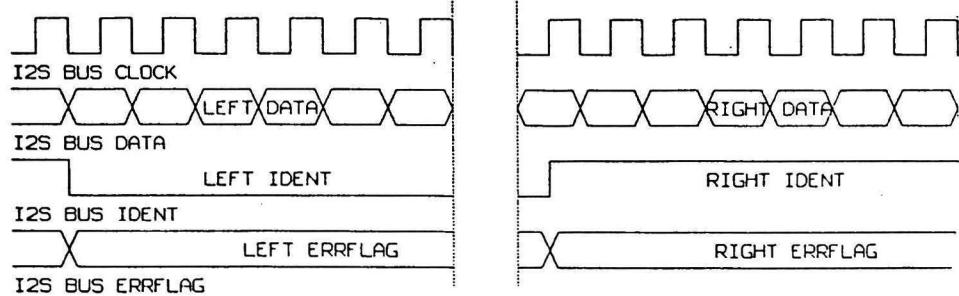
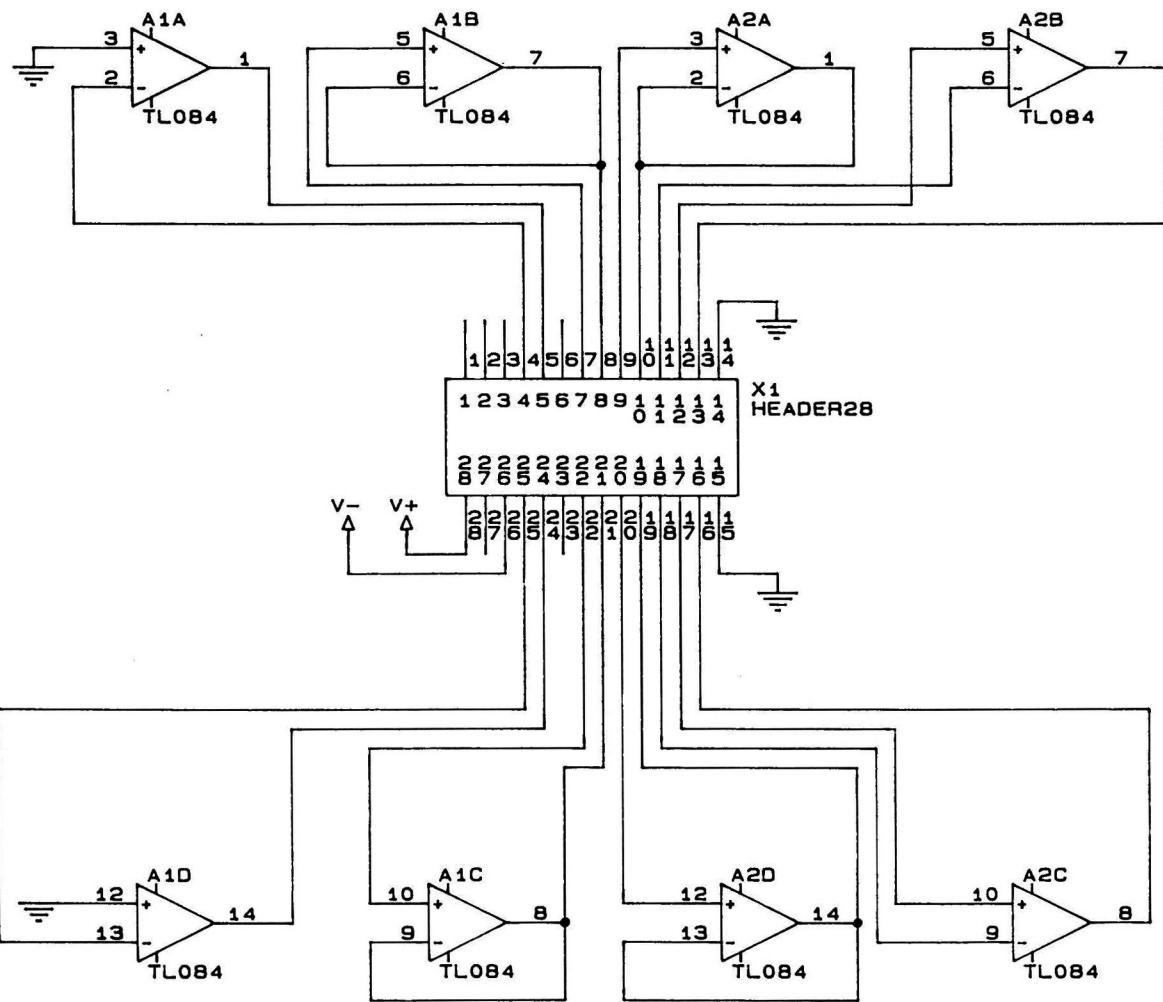


Figure 1 - I²S Bus Waveforms

- (10) Connect a 600-ohm audio level and distortion measurement set to X1 Pins 23a and 23c (Channel A) and set the NICAM generator for 14.7dBu at 2kHz. Adjust R17 for 14.7dBu on the output.
- (11) Move the audio test measurement set to X1 Pins 25c and 25a and repeat (10) for Channel B using R43 to adjust the level.

- (12) Check that the distortion, frequency response, crosstalk and noise meet specification on both channels.
- (13) Insert a pair of 600-ohm headphones into the jack socket X2. Using tones and/or program, check that the signal is clean and that there are no spurious noises.
- (14) Control bits C0: Look on A8 Pin 1 and check that there is a square wave of 16ms repetition rate with an even mark/space ratio.
- (15) Control bits C1 to C4: Look in turn on A8 Pins 2 to 5 and toggle the respective control bit on the NICAM generator; the relevant pin should echo the NICAM generator.
- (16) Additional data bits: The additional data bits appear on A8 Pins 6 to 8 (AD0 to AD2) and A9 Pins 1 to 8 (AD3 to AD10). Toggling the additional data bits on the NICAM generator will cause the relevant pin to echo this action.
- (17) Nordic data bits: Put the oscilloscope probe onto A7 Pin 1 and toggle CIB0 on the NICAM generator. The pin should follow the action of CBI0. Repeat the above for A7 Pin 2 (CBI1).
- (18) Muting: Set C3 on the NICAM generator to on; H1 (MUTE) LED should come on and all audio outputs should be muted. Set X3 to high; the mute LED should go out and the audio output should be distorted. Set X3 and X4 to low, and C3 to 0 on the NICAM generator; the output should be muted and H1 will be on. Turn on C4 on the NICAM generator; H1 should be extinguished and the audio should be clear and unmuted. Set X4 to high and C4 on the NICAM generator to OFF. Set X16 to REMOTE and check that short-circuiting X1 Pin 20c to OV causes the audio to be muted and the MUTE LED H1 to come on.
- (19) Restore all links and control bits to their initial conditions.

The unit is now ready to be used.



TDA1542 SUBSTITUTE BOARD.
USED ON AUDIO MONITORING
PCB NICAM AND SIS

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(992 9333 001)

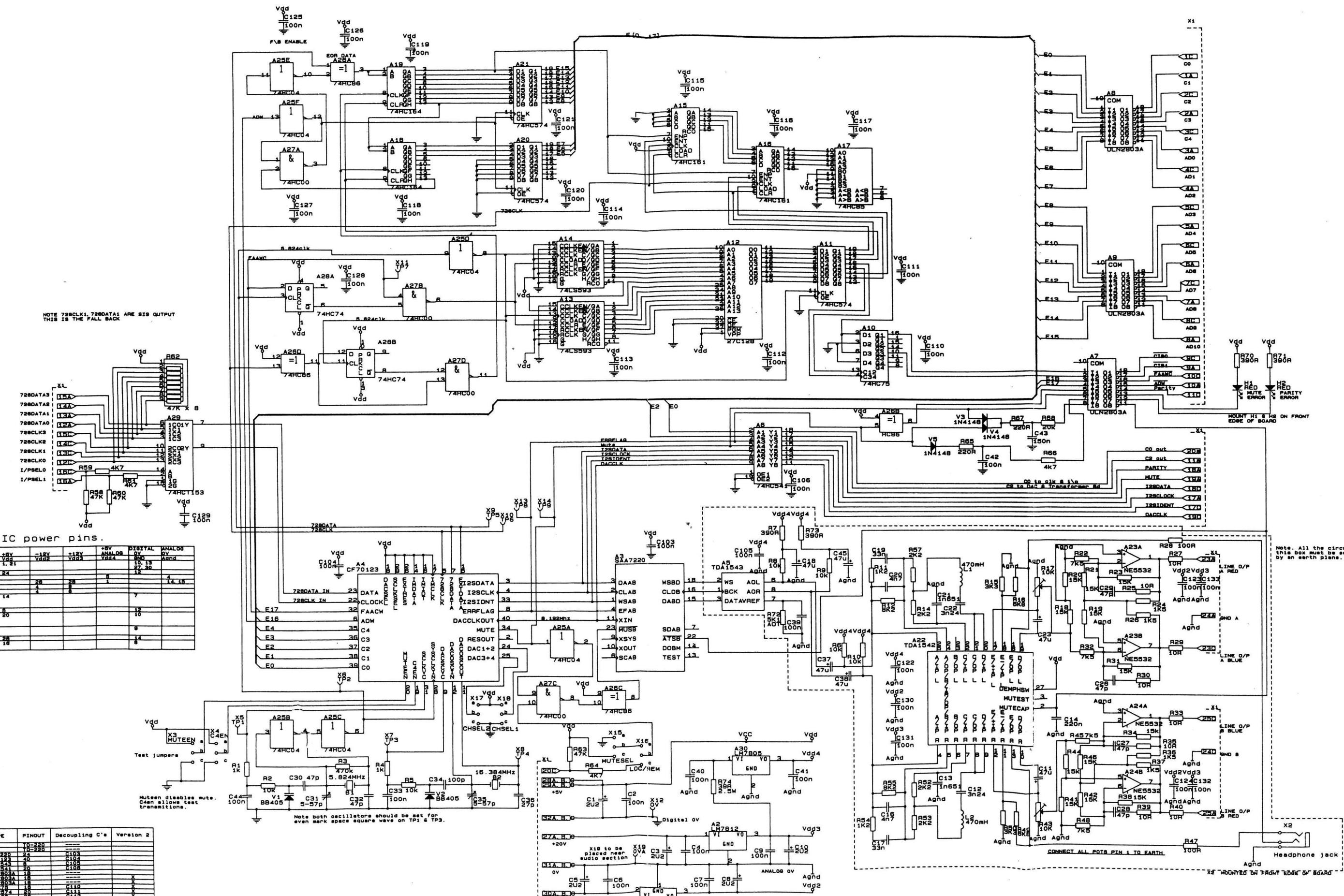
ISSUE A SIZE A4

DAN D HAMMOND

CHK

DATE 26/4/95

SH 1/1

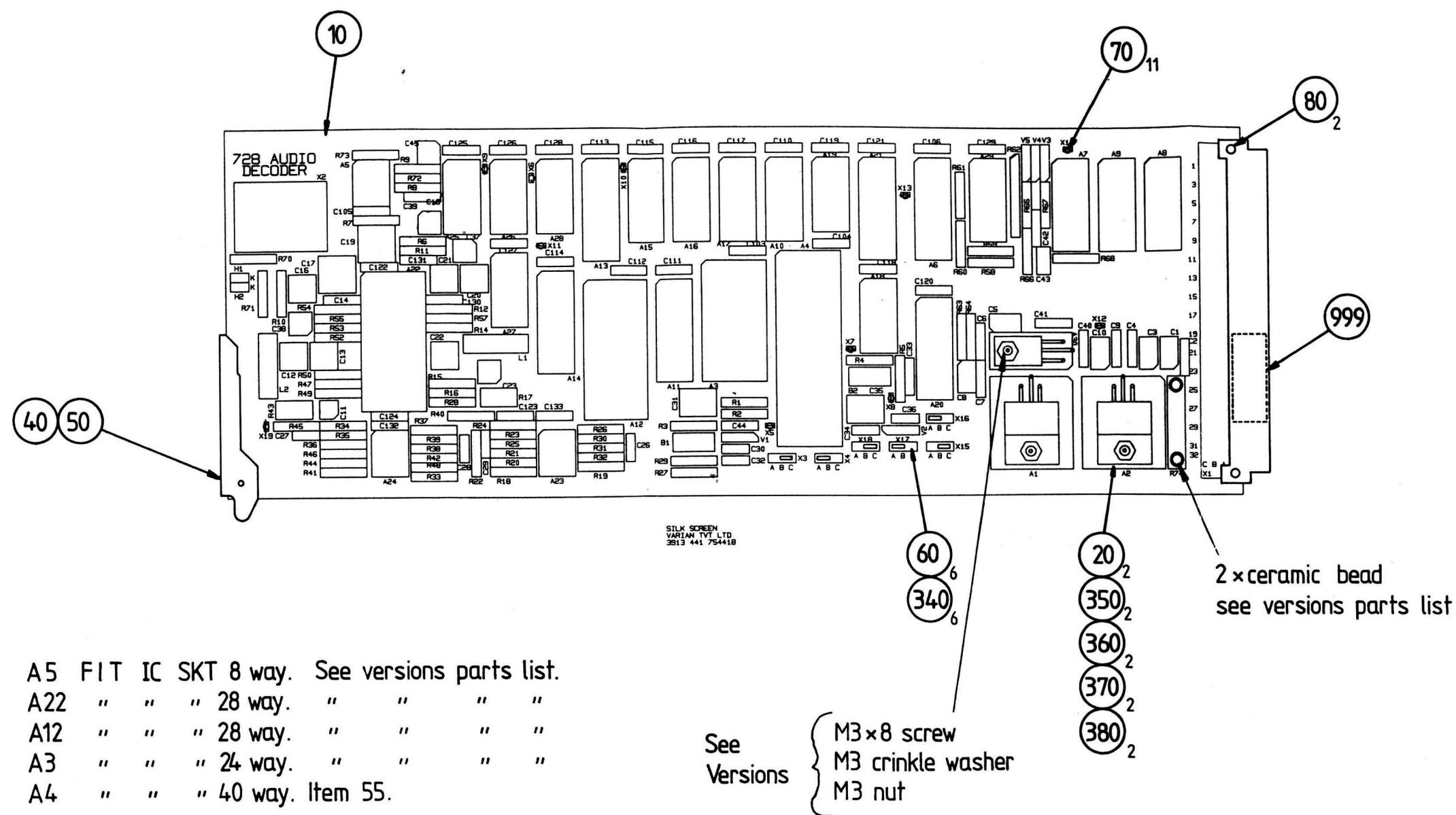


IC No	Type	Pinout	Decoupling C's	Version 2
A1	74HC154	10-22	---	
A2	74HC120	24	C103	
A3	74HC104	20		
A4	74HC148	28	C105	
A5	74HC244	20	C108	
A6	74HC243	20	C108	
A7	74HC220	20	C108	
A8	U12603A	18	---	
A9	U12603A	18	---	
A10	U12603A	18	---	
A11	74HC4042	20	C110	
A12	74HC4042	20	C111	
A13	74HC158	28	C112	
A14	74HC93	20	C114	
A15	74HC541	18	C116	
A16	74HC548	18	C117	
A17	74HC541	18	C118	
A18	74HC548	18	C119	
A19	74HC161	20	C120	
A20	74HC161	20	C121	
A21	74HC154	20	C122	
A22	74HC154	20	C123	
A23	74HC154	20	C124	
A24	74HC154	20	C125	
A25	74HC154	20	C126	
A26	74HC154	20	C127	
A27	74HC154	20	C128	
A28	74HC154	20	C129	
A29	74HC154	20	C130	
A30	74HC154	20	C131	
A31	74HC154	20	C132	
A32	74HC154	20	C133	
A33	74HC154	20	C134	
A34	74HC154	20	C135	
A35	74HC154	20	C136	
A36	74HC154	20	C137	
A37	74HC154	20	C138	
A38	74HC154	20	C139	
A39	74HC154	20	C140	
A40	74HC154	20	C141	
A41	74HC154	20	C142	
A42	74HC154	20	C143	
A43	74HC154	20	C144	
A44	74HC154	20	C145	
A45	74HC154	20	C146	
A46	74HC154	20	C147	
A47	74HC154	20	C148	
A48	74HC154	20	C149	
A49	74HC154	20	C150	X

NOTE: All components are fitted for version 1.
ICs & their decoupling capacitors marked with X are not fitted for version 2.

VERSION 0: AS SHOWN
VERSION 02: SEE TABLE FOR COMPONENTS NOT FITTED

Varian TTV Limited CAMBRIDGE © 1989
Title: AUDIO DECODER PCB ASSEMBLY CIRCUIT
Site: Document Number: REV
D: 3813 446 78440 SH 130-1 103
Date: May 1989 13. Imprint 137



DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING		
TOL. UNLESS OTHERWISE STATED		SURFACE TEXTURE		
DIMENSIONS		ANGLES	HOLEs	1ST USED ON
UNITS	SCALE ORIG. DRG	MATERIAL		
MM	1:1	SEE SEPARATE PARTS LIST.		
PROJECTION		TREATMENT		
1ST	2ND	SEE 3913 982 90010 CODE C		
TITLE		12-10-89		
AUDIO DECODER 728		3913 446 7544		
PCB ASSY DRG		SUPERSEDES		
		1	SH.	SH. 110-1
DRAWN	HECH. CHK.	ELECT. CHK.	APPROVED	
VARIAN TTV LTD CAMBRIDGE (c) 1989 DATE DRAWN 12-10-89 FORM				

DAC AND TRANSFORMERS3913 446 75450Contents

CHANGE SUMMARY	Sh. 508-1
1. GENERAL DESCRIPTION	Sh. 595-1
2. FUNCTIONAL DESCRIPTION	Sh. 595-2
3. SETTING-UP PROCEDURE	Sh. 595-3
3.1 General	Sh. 595-3
3.2 Procedure	Sh. 595-3

ILLUSTRATIONS

Circuit Diagram	Sh. 130-1
Assembly Drawing	Sh. 110-1

PARTS LISTS

C H A N G E S U M M A R YDAC AND TRANSFORMERS3913 446 75450

References	Brief Description of Change	Documents Affected
PGV 3746 28.09.89	C52, 330p, 2222 683 58331 added between Pins 16 and 17 of A3. Parts List up-dated with corrections. Minor mechanical modifications.	Circuit Diagram Assembly Drawing Parts List
PGV 3804 16.11.89	Track re-routed from X1 Pins 17a and 17c to R32 and A1 Pins 3 and 4.	Assembly Drawing
PGV 3805 17.11.89 Issue 2	R50 changed from 20k to 10k, 2322 156 11003. R50 changed from 10k to 15k, 2322 156 11503.	Circuit Diagram Parts List.
PGV 3851 09.01.90	Track changes on PCB to eliminate IF crosstalk.	
PGV 3928 03.04.90	Legends a, b and c added to PCB at X3 and X4.	Assembly Drawing
CA 41614 19.07.93	Optional connection between Audio Comparator Board 3913 446 75470 and junction of R42/R43/R57 added for facilitating 19kHz monitoring tone (BBC only).	Circuit Diagram
ECN10388 15.11.94	Mechanical change.	Parts List
ECN10878 12.07.95	Note removed from circuit diagram and connections X8 pins 3 and 4 shown.	Circuit Diagram
ECN10999 25.08.95	Capacitor 2222 036 24471 changed to 16V type 2222 037 54471.	Parts List

DAC AND TRANSFORMERS3913 446 754501. GENERAL DESCRIPTION

This board accepts 16-bit stereo samples and provides balanced and isolated outputs via transformers to the rear connector. It also provides a balanced, though not isolated, mono output for monitoring purposes.

Decoded NICAM 728 is input to the board in I²S bus format from the Audio Decoder board. The I²S bus is then buffered and fed to a digital filter chip which also performs four-fold oversampling, mute and parity error correction.

Still in the I²S bus format the signal is passed to a dual 16-bit DAC which has current source outputs. These outputs are fed into a virtual earth amplifier which also forms part of the anti-aliasing filtering. After filtering the signal is de-emphasised according to the CCITT J17 curve. It is at this point that additional muting is performed by a FET switch.

After passing through a variable-gain amplifier the audio signal is passed to three types of output. The first output is through a transformer and this provides a 600-ohm isolated program output. A second output is in the form of a balanced, though not isolated, 600-ohm MONO output, the third is a stereo headphone socket mounted on the front of the board.

2. FUNCTIONAL DESCRIPTION

The input to the board is in the I²S bus format and is buffered in A1; also fed into this input buffer is the remote Mute Enable line which is then fed via selecting links to one input of A10b. After the buffer the mute is inverted in A10a and then fed to the digital filter chip via the AND gate formed by A10b and A10c.

Buffered I²S bus signals are then fed to the digital filter chip A2; this chip performs the first part of the audio filtering required and also works out the interpolation required to perform four-fold oversampling. This obviates the need for expensive analogue audio filters on the output. The digital filter chip is also used to correct parity errors and to mute the signal when the quality of the decoded audio degenerates beyond a certain point.

After digital filtering the signal, still in the I²S bus format, is fed to A3, a dual 16-bit DAC which converts the digital signal to an analogue current. As the output from the B channel is identical only the A will be described. This analogue signal is fed into a virtual earth amplifier A7a, which along with A7b forms part of a 3-pole low-pass Bessel filter, used to perform the anti-imaging filtering.

De-emphasis is performed by A8a to the CCITT J17 de-emphasis curve. A4 is a variable-gain amplifier which then drives the output transformers, a feed to the headphone amplifier A9a and another feed to the mono output amplifier A15a,b via the solid state switches in A16. The solid state switch is controlled from Bit C2 in the NICAM bitstream and comes from the decoder board. Thus when C2 is low, indicating mono only, one of the channels (A) is fed to the output amplifier. This amplifier takes a feed from both channels and adds them together to produce a balanced mono output. Output selection of MONO, STEREO or DUAL LANGUAGE takes place on the decoder board and is not selectable on this board.

Due to the time taken on the decoder board to produce a mute signal an extra mute circuit has been implemented to avoid erroneous signals being output at this time. The mute and parity lines are diode OR-ed by V1, V2 and fed to the retriggerable monostable A14a via a filter which is used to filter out single parity errors. However, when multiple parity errors occur the monostable is triggered and the audio signal is muted by the Q output of A14a and then fed through a level shifter to FET V8. The NOT Q output of A14a is used to control the attenuation pin of the digital filter; this also reduces the amount of erroneous signal breakthrough.

3. SETTING-UP PROCEDURE

3.1 General

This procedure assumes an untested and brand new board.

Test equipment required:

Voltmeter, e.g. Fluke or AVO.

20MHz bandwidth oscilloscope.

x10 oscilloscope probes.

I²S bus data generator, Decoder Rack Frame Assembly.

Power supplies:

+12V and -12V, at 500mA;
+5V at 1A.

(Decoder Rack Frame Assembly and extender board).

Audio distortion/noise meter.

3.2 Procedure

(1) Set Link X3 to Position 'High' and X4 to Position 'Local'.

(2) Connect all the power supplies and check that the following voltages exist between OV (X12) and the following points:

A2 Pin 24	+5V
A3 Pin 26	-5V
A7 Pin 4	-15V
A7 Pin 7	+5V.

All the above voltages should be within 5%.

(3) Connect the six I²S bus lines to X1 Pins 17a to 19c and X1 Pin 11a to OV. Compare the waveforms present on Pins 1, 2

and 3 of A3 to those in Figure 1 and ensure that they are the same.

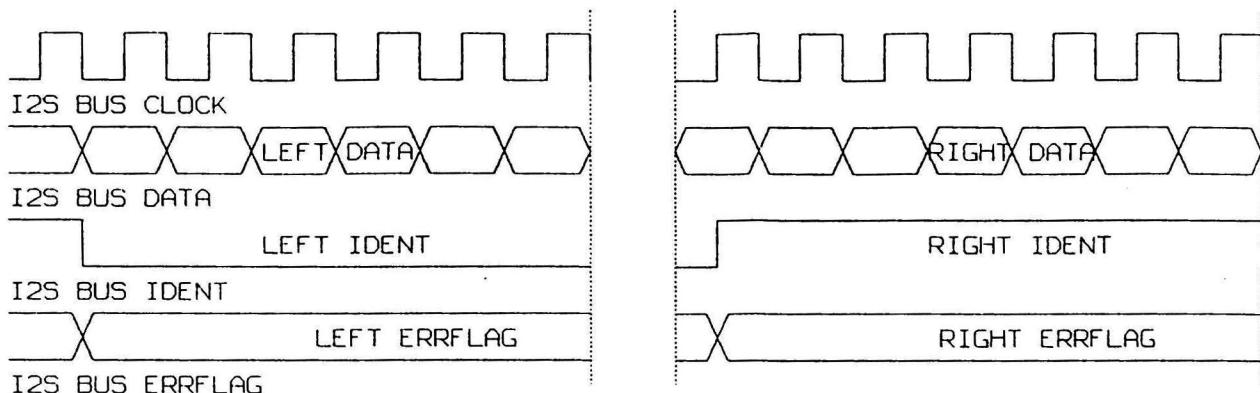


Figure 1 - I²S Bus Waveforms

- (4) Check that R27 and R28 are not fitted.
- (5) Connect a 600-ohm audio level and distortion measurement set to X1 Pins 23a and 23c (Channel A) and set the I²S bus generator for 14.7dBu at 2Khz. Adjust R15 for 14.7dBu at the output.
- (6) Move the distortion measurement set to X1 Pins 25c and 25a, and repeat (5) for Channel B, using R26 to adjust the level.
- (7) Connect the audio test set to X1 Pins 13c and 12c and set the I²S bus generator for 0dB at 400Hz in both channels. Check that the gain stays the same when X1 Pin 11a is taken high. Turn off the tone in Channel B and ensure that the gain does not change. Return X1 Pin 11a to low.
- (8) Check that the distortion, frequency response, crosstalk and noise meet specification on both channels.
- (9) Insert a pair of 600-ohm headphones into the jack socket X2. Using tones and/or program, check that the signal is clean and that there are no spurious noises.
- (10) Set the I²S bus generator to produce a tone in both channels. Inject a square wave of approximately 10Hz at 5V p-p to the junction of V1, V2 and R33. Check that on A14 Pin 13 there is a pulse produced on each rising and falling edge of the waveform on Pin 1.

- (11) Connect the oscilloscope probe to X16 and check that whilst the output from A14 is high the audio signal is muted by at least 30dB.
- (12) Repeat (10) for X10.
- (13) Set X16 to remote and check that short-circuiting X1 Pin 20c to 0V causes the audio to be muted. Restore all links to their initial conditions.

The unit is now ready to be used.

AUDIO DAC

MISSING

CCT

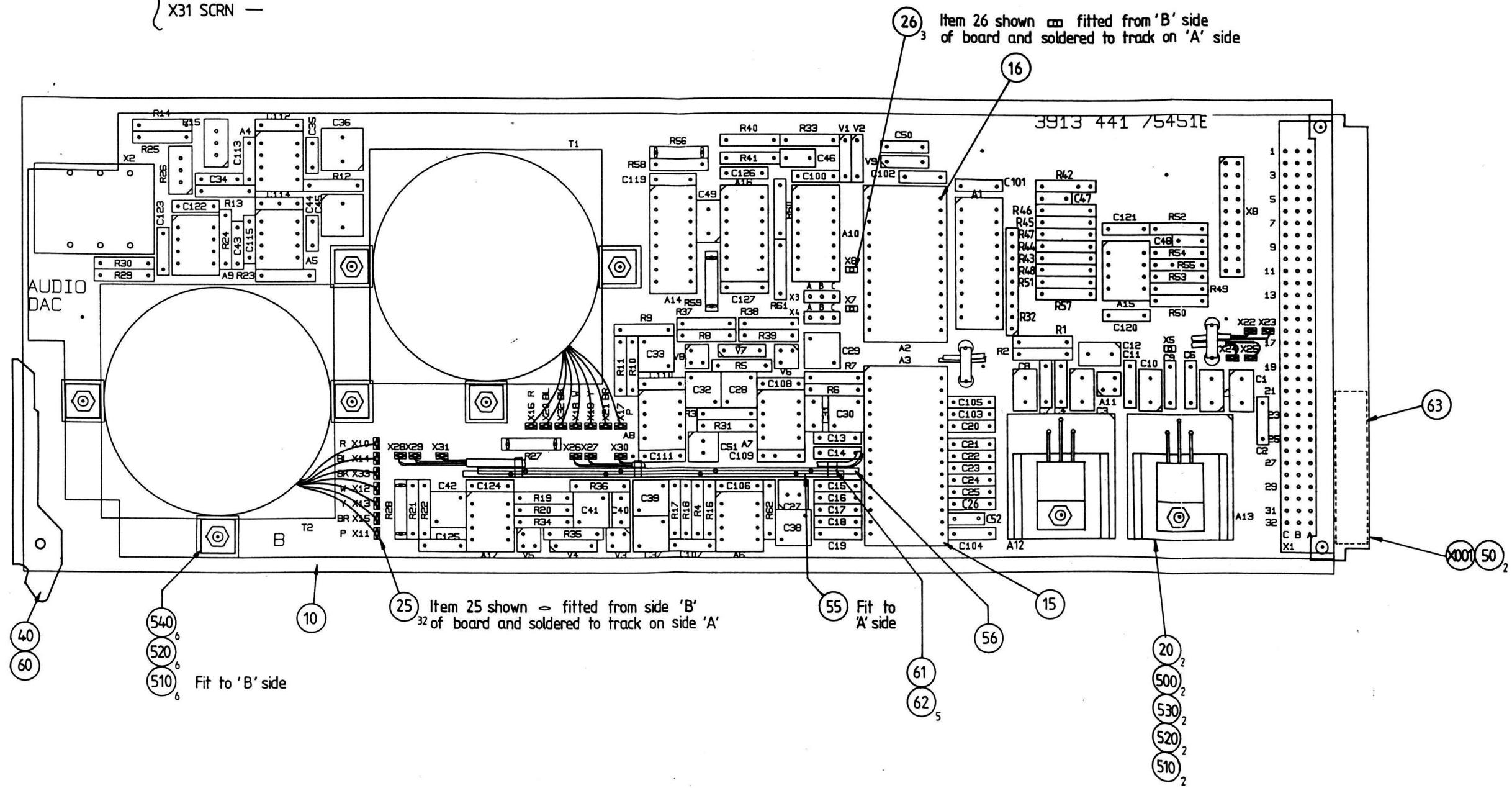
DIAGRAM



CABLE CONNECTIONS

W1 { X27 RED X23
X26 BLUE X22
X30 SCRN —

W2 { X29 RED X25
X28 BLUE X24
X31 SCRN —



NOTE: STRIKE PLATE INSTRUCTION

1. APPLY STRIKE PLATE NO. 5000 ON BOARD INDICATED WITH THIS ASSEMBLY IN POSITION INDICATED

2. STRIKE PLATE IS TO LEVEL INDICATED IN THIS DATA

NOTE: THE STRIKE PLATE EPOXY MUST NOT BE CONFUSED WITH THE EPOXY USED ON ASSOCIATED DRAWINGS OR PARTS LIST

STRIKE NO	P/N NO
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DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING		
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MM	2:1			
SEE SEPARATE PARTS LIST				
SEE 3913 982 90010 CODE C.				
TITLE: AUDIO DAC & TRANSFORMER PCB.		3913 446 7545		
DRAWN BY: J. J. H. DATE: 10/10/87		VERIFIED BY: J. J. H. APPROVED BY: J. J. H.		
DESIGNED BY: J. J. H. CHECKED BY: J. J. H. APPROVED BY: J. J. H.		PRINTED BY: VARTAN LTD CAMBRIDGE		

DECODER RACK FRAME ASSEMBLY3913 446 69820Contents

CHANGE SUMMARY	Sh. 508-1
1. GENERAL DESCRIPTION	Sh. 595-1
ILLUSTRATIONS	
Motherboard - Circuit Diagram	Sh. 130-1
Power Transformer Wiring - Circuit Diagram	Sh. 130-2
Decoder Ribbon Cables	Sh. 130-3
Rear Panel Layout .. 8928 190 40001	Sh. 512-1
Motherboard PCB Assembly	3913 446 75430
Motherboard PCB Assembly	3913 446 75430

PARTS LISTS

C H A N G E S U M M A R Y

DECODER RACK FRAME ASSEMBLY

3913 446 69820

References	Brief Description of Change	Documents Affected
CA 32991 15.11.89	<u>On Motherboard PCB 3913 446 75430:</u> X10 Pin 25a is connected to X43. X10 Pin 25c is connected to X42. (Error on circuit diagram).	Circuit Diagram
PGV 3839 19.01.90	<u>On Motherboard PCB 3913 446 75430:</u> Earth connection removed at X8 Pin 12b. Connection of X18 Pin 12b to X122 Pin 5 changed to X18 Pin 12b to X122 Pin 6. X122 Pin 5 remains connected to earth. (Circuit Diagram is correct.)	Assembly Drawing
PGV 3929 03.04.90	End piece 2712 028 00816 changed to 2700 028 01087.	Parts List
PGV 3810 Issue 2	Label containing BBC patent GB2116403 information placed on rear panel.	
PGV 3980 22.05.90	Specification of Mains Toroidal Transformer 3913 449 51380 updated.	
PGV 4002 08.06.90	Lockwasher 2522 616 04140 added between transformer and rear panel.	Parts List
PGV 4033 21.06.90	Specification of Mains Toroidal Transformer 3913 449 51380 further updated.	
PGV 4059 23.07.90	Neoprene gasket, supplied as part of transformer 3913 449 51380, fitted between transformer and rear panel in place of 'Tesmol' tape 1222 100 15056 and lockwasher 2522 616 04140.	Parts List Assembly Drawing
ECN10194 02.09.94 ECN10509 06.02.95	New type voltage selector.	Parts List
ECN10385 14.11.94 ECN11055 22.09.95	Mechanical and parts list changes.	Parts List

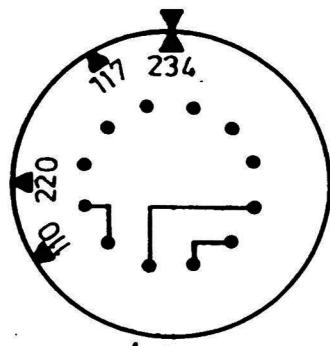
DECODER RACK FRAME ASSEMBLY

3913 446 69820

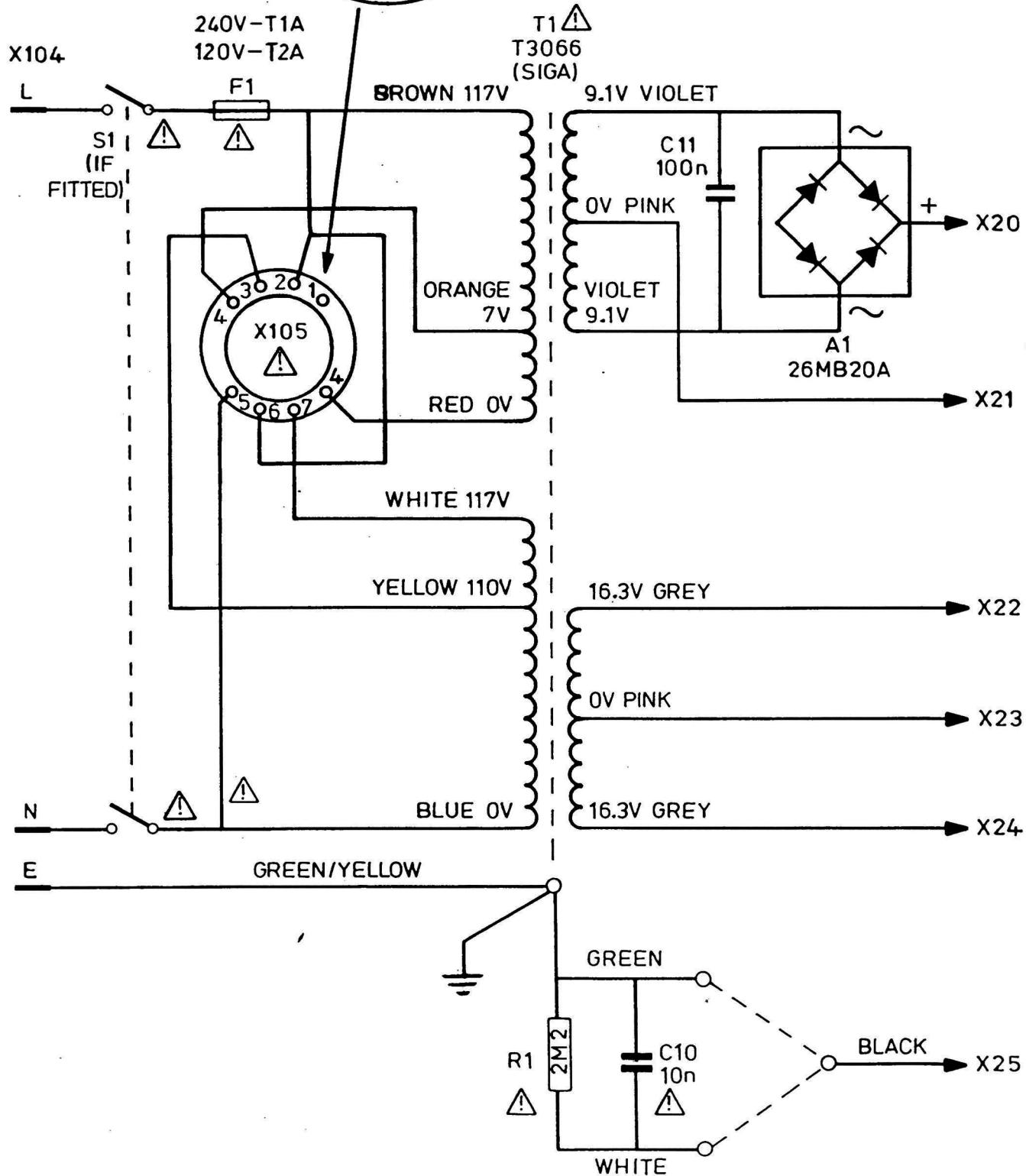
1. GENERAL DESCRIPTION

This unit comprises:

- (a) A motherboard assembly, containing the sockets which the various modules are plugged into, the internal wiring between modules and the connectors for the ribbon cables that take the interface connection to and from the rear panel.
- (b) Module runners.
- (c) Rear panel assembly, supporting the following components:
 - (i) Mains transformer and rectifier to provide the module supplies.
 - (ii) Mains voltage selector and power wiring.
 - (iii) SIS input balun.
 - (iv) All input and output connectors.
- (d) Front panel providing access to audio sockets and certain operational indicators.
- (e) Side panels.



ROTATABLE
CONTACTS OF
MAINS VOLTAGE
SELECTOR



STEREO SIS POWER
TRANSFORMER WIRING

3913 446 6979
& 6982
SH 130-2

1 891016

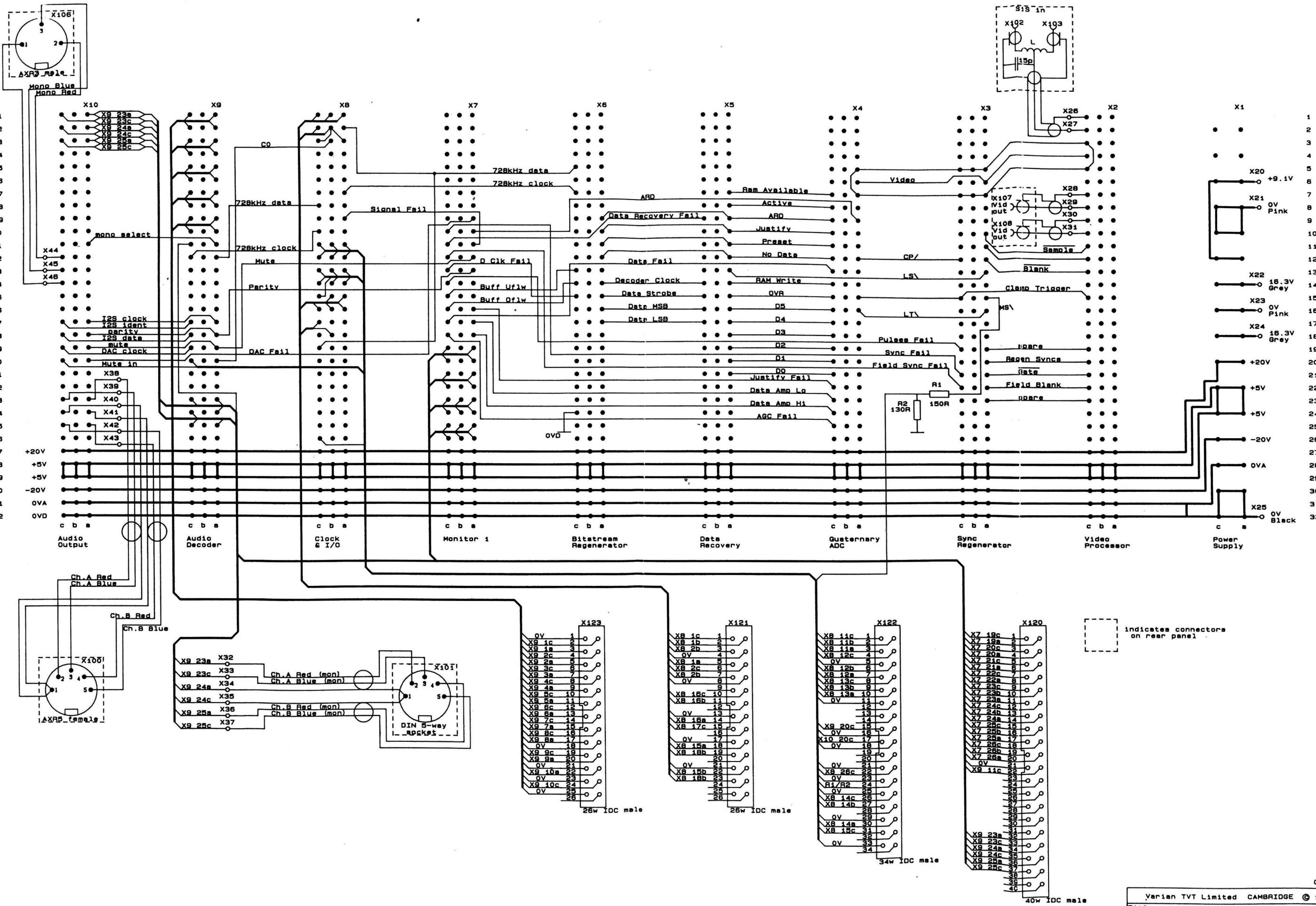
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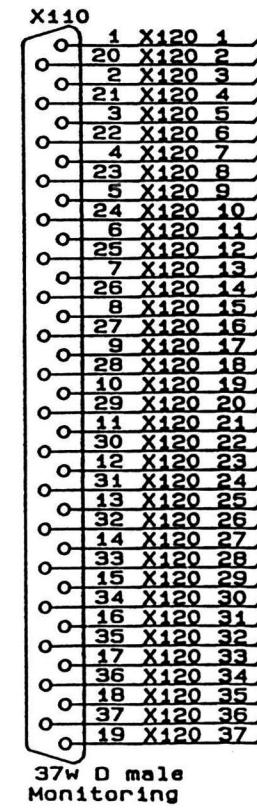
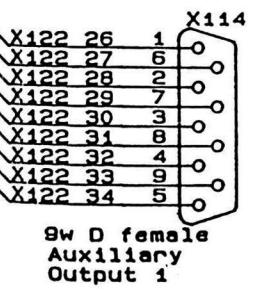
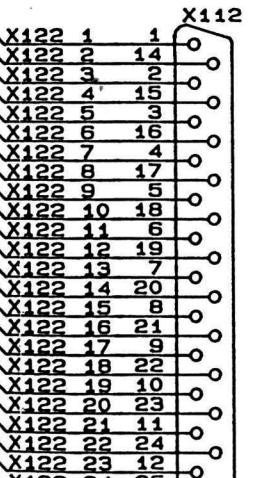
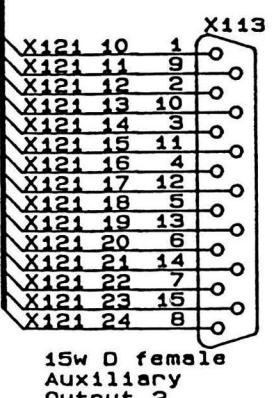
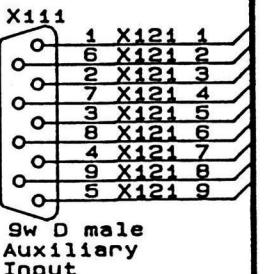
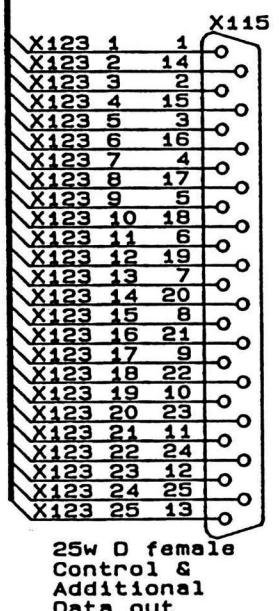
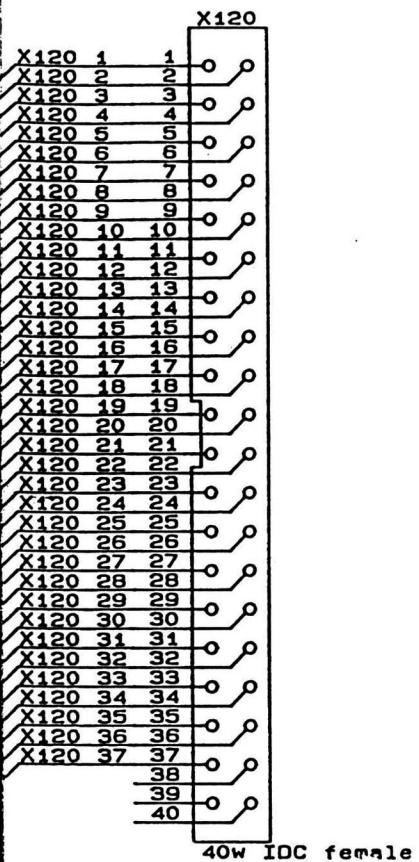
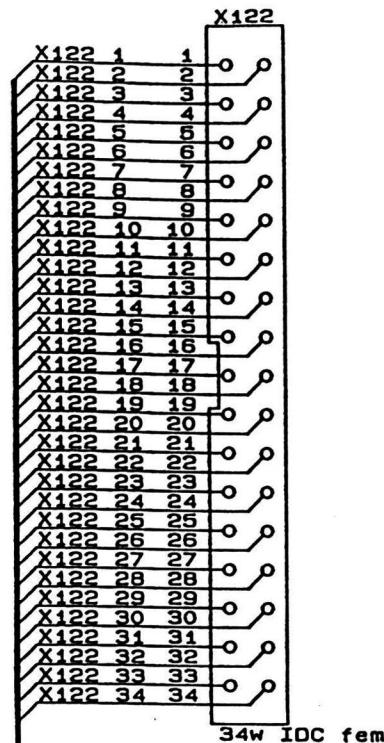
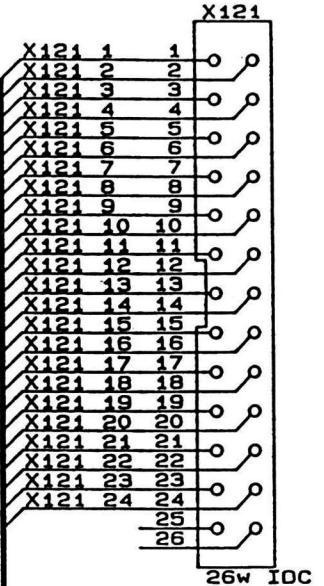
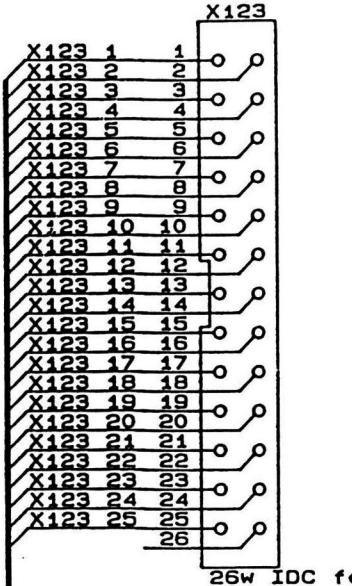
VARIAN TTV LTD CAMBRIDGE © 1989

CHK. C.S. Clementson APPROVED

3 SH

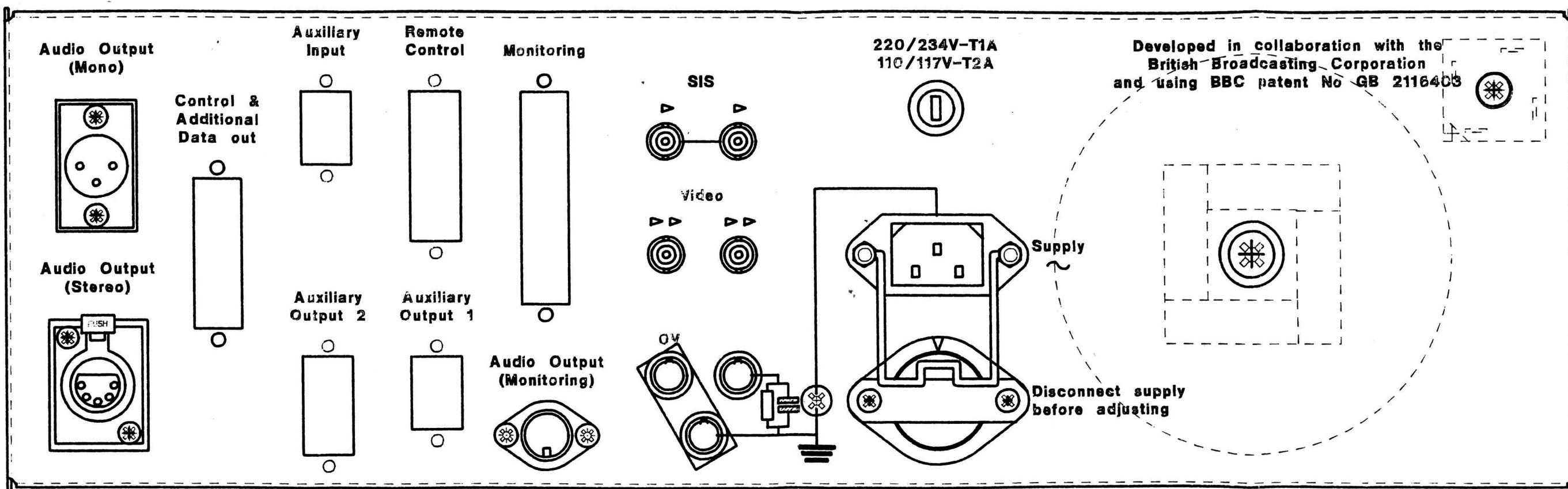
DATE DRAWN 891016 FORM A 4





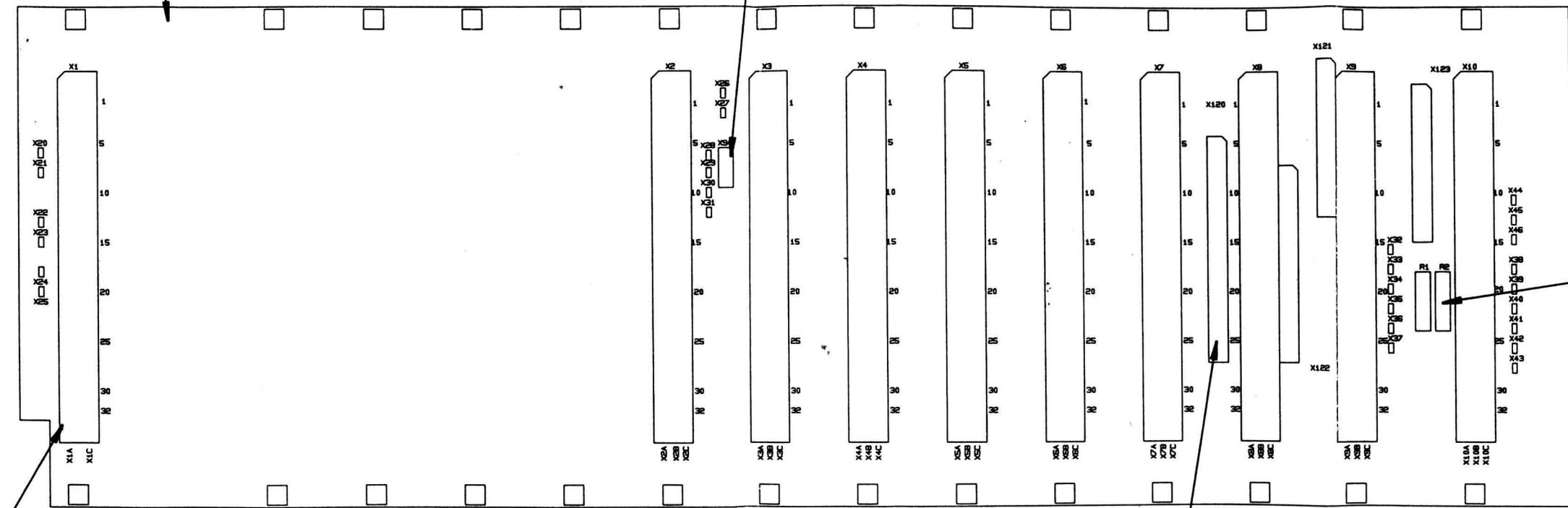
Varian TVT Limited CAMBRIDGE © 1989	
Title	
STEREO SIS DECODER RIBBON CABLES CONNECTIONS	
Size Document Number REV	
B	3913 446 69820 SH.130-3 00
Date: January 4, 1990 Sheet 3 of 3	

View on
Rear Panel



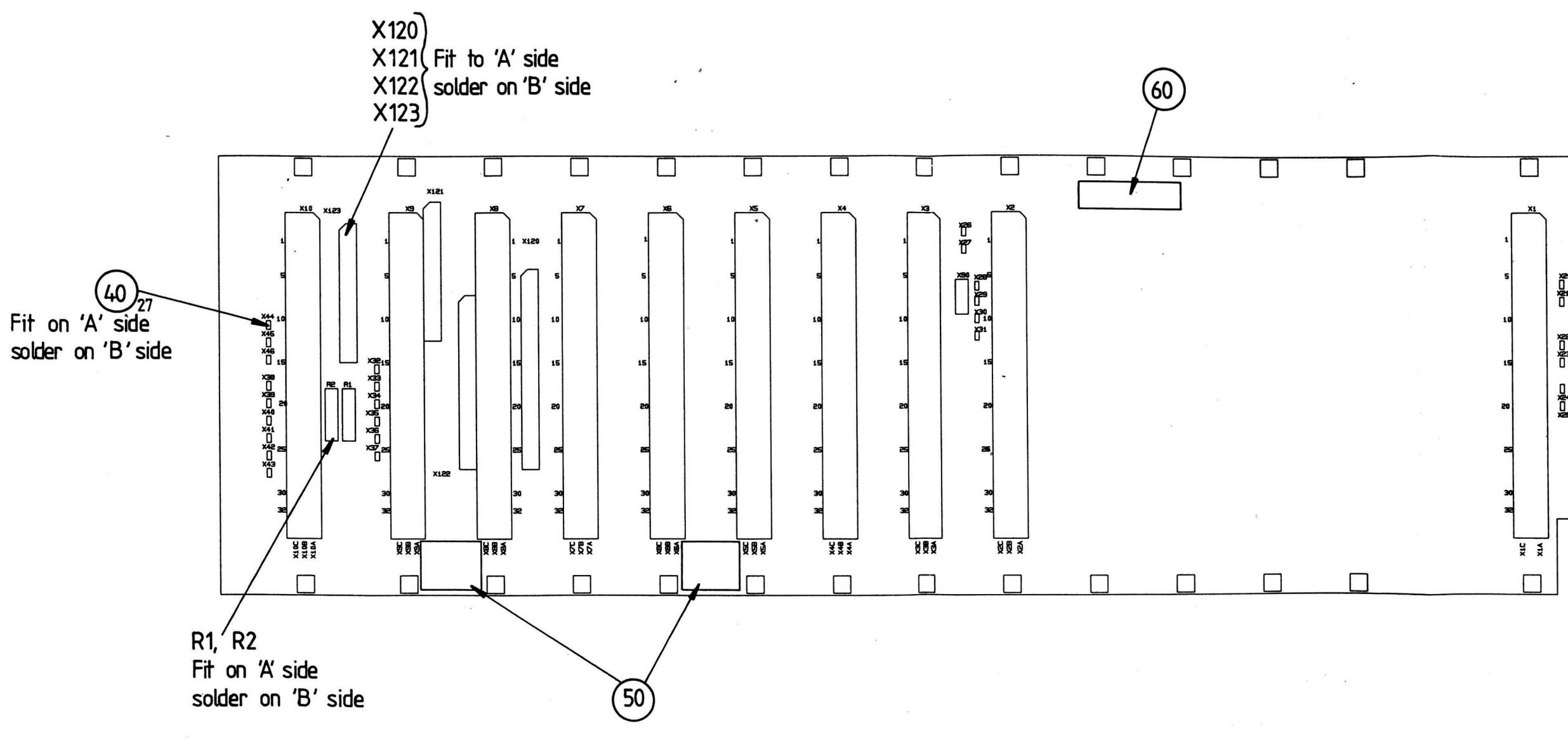
TITLE REAR PANEL LAYOUT		8928 190 40001		89-11-29			
STEREO SOUND IN SYNC DECODER		1	SH	1C	SH	512-1	
ARCHIVE NO.				ELECT CHK		APPROVED	
DRAWN	N. BROWN	MECH CHK					
VARIAN T.V.T LIMITED CAMBRIDGE		© 1968		DATE DRAWN 89-11-29		FORM	

D190_40001



SIDE B

DO NOT SCALE THIS PRINT		DIMENSIONS ARE SHOWN AFTER PLATING	
DIMENSIONS	ANGLES	HOLDS	
UNITS MM	SCALE 1:1	MATERIAL	
SEE SEPARATE PARTS LIST			
PROJECTION		TREATMENT	
1ST		3RD	
TITLE		CODE	
728 SIS DECODER MOTHER BOARD		3913 446 7543	
SUPERSEDES		2 SH. 110-1	
DRAWN		MECH. C.H.	
		ELECT. C.H.	
		APPROVED	
VARIAN T.V.T LTD CAMBRIDGE (C) 1989 DATE DRAWN 12-10-89 FORM			



SIDE A

DIMENSIONS			ANGLES		SURFACE TEXTURE		1ST USED ON		
UNITS	SCALE	ORIG.DRG.	MATERIAL:	HOLEs					
MM	1:1		SEE SEPARATE PARTS LIST						
PROJECTION			TREATMENT:						
1ST			3RD						
SEE 3913 982 90010 CODE C									
TITLE 728 SIS DECODER MOTHER BOARD			3913 446 7543						
SUPERSEDES			12-10-89						
DRAWN			07-02-90						
MACH.CHR.			ELECT.CHR.						
APPROVED									
VARIAN T.V.T LTD CAMBRIDGE (c) 1989 DATE DRAWN 12-10-89 FORM									