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System Setting-up

STEREO SOUND IN SYNC

LDM 1903/00/01 (8928 190 30001)

LDM 1904/00/01 (8928 190 40001)

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1. GENERAL

The following procedures are to assist in the testing and setting up of the units being put into service.

The oscillators should be set up using an off-air frequency standard and a good quality counter, and monitoring at buffered test points.

CAUTION: PRINTED CIRCUIT BOARDS SHOULD NOT BE REMOVED OR
INSERTED WITH THE POWER SWITCHED ON, AND BOARDS
SHOULD ONLY BE INSERTED INTO THE CORRECT SLOTS
BY REFERENCE TO THE NAMES ON THE BOARDS AND THE
LEGENDS ON THE FRONT PANEL.

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2. CODER SYSTEM ADJUSTMENTS

2.1 Power Supplies

- (1) With only the Power Supply module connected and the power off, set the voltage selector on the rear panel to the mains voltage in use.
- (2) Insert an extender board in any position in the frame.
- (3) Switch the power on and check the DC voltage rails on the extender board, relative to 0V at Pin 32a or c, as follows:
 - (a) +5V at Pin 28a or c, or 29a or c.
 - (b) +20V at Pin 27a or c.
 - (c) -20V at Pin 30a or c.
- (4) Switch off the power and fit all the printed circuit boards into the frame.
- (5) Connect the positive end of a meter to the top of R75 on the Sync Separator and the negative to the bottom of R72. Access from the front without using the extender board.
- (6) Switch on and check the +5V supply. It should be $5V \pm 0.05V$. If necessary adjust R4 on the PSU module.

2.2 Moveable Link Positions

Switch off and check the following link positions:

Audio Input Filter	:	X17, X18 to N.
Audio ADC	:	X10 to S.
DSP	:	X2, X4 fitted, X3 not fitted.
Clock and I/O	:	X2 to X6 to N.
		X16, see note on circuit diagram; if in doubt, use position A.

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X18 to A (for Tone 2 = silence).
X19 and X20 to C.

Audio Decoder (if fitted) : X4, X16, X17 to ab.
X3, X15, X18 to bc.

Asynchronous Data Proc : All links to N except X18 to
'LS' or 'MS' according to whether
standby sync is required to be
Line Sync only or Mixed Sync.
X16 Fitted.

Sync Separator : X7 to N.

Monitor 1 : X3 to 1; X4 fitted; X9 to A.
S3/1 to COD.
S3/2 To FULL if an Audio Decoder
module is fitted, to MAIN if not.
S3/3 Not applicable.
S3/4 to NO AUDIO, if a DSP module
is not fitted.

2.3 Clock and I/O

Use the switches on the front of the module or Remote Control to select Tone 1 or Tone 2 and Free-running mode. Adjust R14 for 5824kHz $\pm 0.3\text{Hz}$ oscillator frequency at X14. DO NOT ATTEMPT THIS WITHOUT CHECKING THAT THE ACCURACY AND STABILITY OF YOUR FREQUENCY COUNTER IS ADEQUATE FOR THE TASK, i.e. BETTER THAN 1 PART IN 10^8 .

This frequency should be checked after the first year, and less frequently thereafter.

2.4 Digital Signal Processor (DSP)

Probe X5 (A31 Pin 3) and adjust C5 for locking; this will be a compound waveform which repeats after four transitions. Set C5 for mean mark : space ratio of 50 : 50, when the ratio of the times between the four transitions will be approximately 2 : 2 : 1 : 1.

2.5 Audio Decoder (Optional)

- (1) Probe X5 and adjust C31 for a locked signal of 50 : 50
mark : space ratio.

- (2) Probe X7 and adjust C35 for a locked signal of 50 : 50
mark : space ratio.

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- (3) Set the switches on the front of the Clock and I/O module (or use the remote control unit if fitted), to select Tone 1.
- (4) Connect an Audio Level meter with 600 ohms input impedance to the Channel A output pins (35 and 17) on the Monitoring socket on the rear panel. If the intended use of the output of this module is to drive a high-impedance circuit, the input impedance of the meter should be set to HIGH IMPEDANCE. Adjust R17 for the correct output level.

Note: Tone 1 is a digitally generated internal tone of 0dBu at 1kHz to match the UK NICAM 728 specification for audio headroom of 14.8dB for a 0dBu 2kHz signal. Other current specifications for audio headroom are around 12dB for a 0dBu 2kHz signal; to match these, R17 must be adjusted for a correspondingly lower output level.

- (5) Repeat (4) for channel B, connecting to pins 37 and 19 of the Monitoring socket and adjusting R43.

2.6 Sync Separator

Note: The Sync Separator, Asynchronous Data Processor and Video Processor modules need to be set up as a trio (see 2.6(14), 2.7(3) and 2.8(10)).

- (1) Connect the Sync Separator board via the extender board.
- (2) Switch on and apply a 100% colour bar signal to the 'Video' input on the rear panel.
- (3) Connect the oscilloscope probe to test point X5 and adjust R91 so that the clamp pulse occurs 5 to 5.5 μ s after the leading edge of sync at X4. Also check that the clamp pulse is 1.5 to 2.1 μ s wide.
- (4) Monitor X8 and adjust R87 for a pulse width of 4.7 μ s \pm 0.1 μ s.
- (5) Connect a second oscilloscope probe to X6 and adjust R90 so that the clamp pulse at X6 begins 4.8 to 5.0 μ s after the negative-going edge at X8. Check that it is 1.8 \pm 0.3 μ s wide.

- (6) Monitor the clamp guard pulse at X9 and adjust its width by R89 to $3.5\mu s$ less than the repetition period, (ignoring the irregular repetition periods during the field sync sequence).
- (7) Monitor the video input on the rear panel and the line trigger pulse on X1-16a and adjust R69 for a delay of 175ns between the half-amplitude point of the leading edge of line syncs and the negative going edge of the line trigger pulse (up to 200ns is permissible if 175ns cannot be achieved).
- (8) Monitor the Field Trigger + at X1-14c and check that it is between 4 and $6\mu s$ wide.
- (9) Monitor the Mixed Sync output at X1-15a. The line sync width should be 4.8 to $5.0\mu s$ as will be alternate equalising pulses. (For examination of the equalising pulses and broad pulses, trigger the oscilloscope to the Field Trigger pulse at X1-14c).
- (10) Connect the oscilloscope via the probe to Test Point X11 and check that the falling edge occurs less than $3.5\mu s$ after the leading edge of input sync, and that the pulse width is at least $1\mu s$.
- (11) Monitor A13 Pin 6 and adjust C32 for 0V.

Note: This is dependent upon the oscillator being locked to a correct line frequency source.

- (12) Monitor the following outputs from the board:

Clamp + at X1-12c	:	1.5 - $2.1\mu s$
Sample + at X1-10a	:	five (for 625 lines) or six (for 525 lines) negative-going broad pulses in the vertical interval.

Regenerated Sync at X1-20a

Composite Blanking at X1-12a

Field Blanking at X1-22a

Composite Gate at X1-21a
(Vertically blanked horizontal sync).

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- (13) By applying both normal video and SIS signals to the Coder input and removing either sync or only field sync, check the operation of the failure indicator LEDs H1, H2 and H3.
- (14) THIS ADJUSTMENT SHOULD BE DONE AFTER those of 2.7(3) and 2.8(10) if standard mixed sync is to be used. Set X18 on the Asynchronous Data Processor to MS (Standby Mixed Sync). Remove the input video and monitor the SIS Output from the rear panel. Adjust C45 on the Sync Separator module for 440ns delay from sync leading edge (half-amplitude point) to first digit (marker pulse) leading edge (half-amplitude point).
- (15) Switch off and replace the board.

2.7 Asynchronous Data Processor

Note: The Sync Separator, Asynchronous Data Processor and Video Processor modules need to be set up as a trio (see 2.6(14), 2.7(3) and 2.8(10)).

- (1) Connect the Asynchronous Data Processor board via the extender board, then switch on.
- (2) With no video input, monitor the Clock at X14 and adjust C31 for 5968.75kHz ± 5 Hz (PAL) or 6010.489kHz ± 5 Hz (NTSC).
- (3) Connect Video input at the rear panel and monitor the SIS output. Adjust C48 for 440ns delay from sync leading edge (half-amplitude point) to first digit (marker pulse) leading edge (half-amplitude point).

Note: This adjustment should follow the correct adjustment of the Line Trigger delay on the Sync Separator module: see section 2.6(7).

2.8 Video Processor

- (1) Apply a signal to the 'Video' input at the rear panel.

- (2) Connect the Coder Video Processor board via the extender board.
- (3) Switch on and monitor the video output terminated in 75 ohms. At A8 Pin 13, monitor with an oscilloscope and probe and check that the clamp pulse is less than $2.1\mu s$.
- (4) Monitor the video output and adjust:
 - R25 for a video amplitude of 1V p-p.
 - R29 to set black level at 0V.
 - R24 for a quaternary data amplitude of 700mV.
 - R18 to set the base of the quaternary digits at -300mV (PAL) or -286mV (NTSC).
- (5) Remove the video input and adjust R118 to set the position of sync tip of standby sync the same as for video.
- (6) Adjust R57 for sync amplitude of 300mV (PAL) or 286mV (NTSC). Data amplitude should still be 700mV.
- (7) Apply a suitable signal for checking frequency response to the video input and adjust C31 for a flat response.
- (8) Check the other video output for similar performance.
- (9) Monitor the buffered output at X1 Pin 4C and check that it is 1V p-p and sitting at -1V.
- (10) Set X18 on the Asynchronous Data Processor to LS (Standby Line Sync). Remove the input video and monitor the SIS output from the rear panel. Adjust R119 on the Video Processor for 440ns delay from sync leading edge (half-amplitude point) to first digit (marker pulse) leading edge (half-amplitude point).

Note: This adjustment should follow the correct adjustment of normal sync-to-marker timing on the Asynchronous Data Processor (see 2.7(3)).
- (11) Switch off and replace the board.
- (12) Return to section 2.6(14) for adjustment of sync-to-marker timing for Standby Mixed Sync.

2.9

Audio Input Filters

- (1) Remove the Audio ADC board and connect the Audio Input Filters board via the extender board.

Note:

The only adjustment on this module is the gain setting (R25 for channel A, R26 for channel B); if the optional Audio Decoder is fitted, or if a Decoder is available the audio gain of the Coder is best set in conjunction with a Decoder module which has been set up for correct output levels with digitally generated test tones. Then R25 and R26 on the Audio Input Filters module are set for unity gain through Coder and Decoder.

If a Decoder or an Audio Decoder module is not available, proceed as follows.

- (2) Switch on and set the links X17 and X18 to T (Test).

- (3) Feed a balanced audio signal into the 'Audio Input' socket on the rear panel, at:

1kHz and 1,420mV

or 2kHz and 852mV

or 2.15kHz and 775mV.

Notes:

1. These input levels are quoted in mV to avoid errors due to the source equipment displaying output levels in dBm on the assumption that the output is loaded with 600 ohms.
2. These input levels are to achieve a gain setting corresponding to the UK broadcasters' specified audio headroom of 14.8dB for a 0dBm, 2kHz signal; other current specifications are around 12dB headroom for a 0dBm, 2kHz signal, for which the input level has to be reduced accordingly, or the output level in (4) below has to be increased accordingly.

- (4) Connect a high-impedance meter to the monitor jack socket at the front of the unit and adjust the output level to 0dBm by means of R25.

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(5) Repeat (4) for Channel B using R26.

(6) Set the links to N (Normal).

(7) Switch off and replace the board.

2.10 Audio ADC

(1) Connect the ADC board via the extender board.

(2) Remove the audio input.

(3) With an oscilloscope or logic probe sequentially monitor A12 Pins 14 to 11, 9 to 6 and A11 Pins 13 to 11, 9 to 6 and adjust R4 so that there is no change in logic level as the sample and hold switches between channels 1 and 2. Check through the sequence again. (R4 is an offset control which adjusts the DC offset of both channels to be the same but not necessarily zero. Thus, when both channels give out the same offset word, or only the LSB is changing, R4 is correctly adjusted.)

(4) Switch off and replace the board.

2.11 General Notes

The coder setting up is now complete. Proceed to the setting up of the decoder, Para 3.

Specification measurements, signalling and remote functions can now be checked. Setting Link X9 in the Asynchronous Data Processor to 0 removes data from the sync pulses to enable video checks to be made.

3. DECODER SYSTEM ADJUSTMENTS

3.1 Power Supplies

- (1) With only the Power Supply module connected and the power switched off, set the voltage selector on the rear panel to the mains voltage in use.
- (2) Insert an extender board in any position in the frame.
- (3) Switch the power on and check the DC voltage rails on the extender board, relative to OV at Pin 32a or c, as follows:
 - (a) +5V at Pin 28a or c, or 29a or c.
 - (b) +20V at Pin 27a or c.
 - (c) -20V at Pin 30a or c.
- (4) Switch off the power and fit all the printed circuit boards into their positions in the frame.
- (5) Connect the positive end of a meter to the top of R75 and the negative to the bottom of R72 on the Sync Regenerator, gaining access from the front without using an extender board.
- (6) Switch on and check the +5V supply. It should be 5V $\pm 0.05V$. If necessary adjust R4 on the PSU module.

3.2 Moveable Link Positions

Switch off and check the following link positions:

Sync Regenerator	:	X7 to 'N' (Normal).
Quaternary ADC	:	X11 fitted; X2, X14 to front; X9 both vertical.
Data Recovery	:	X3 to front.
Bitstream Regenerator	:	X2, X3, X4, X7, X9 to 'N'; X11, X12 fitted.

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Monitor 1 (if fitted) : X3 to '1';
X4 fitted;
X9 to 'A';
S3/1 to DEC
S3/2 to FULL, if a Comparator
board is fitted.
S3/3 Not applicable.
S3/4 to NO AUDIO, if an Audio
Decoder is fitted.

Clock and I/O (Reframer) : X2, X3, X4, X5, X6, X11 to 'N'.
X12-1 to A, B, C, D, E, F, for
Tone 1 as required (see
Installation Section 4.2.2);
X12-2 to G or H for Tone 2 =
silence; X24, X25 to F for Full
Reframing.

Audio Decoder : X4, X16, X17 to 'ab';
X3, X15, X18 to 'bc'.

DAC and Transformers : X3 to 'bc';
(internal mute control off);
X4 to 'ab'.
(internal mute control).

3.3 Sync Regenerator

Note: The Sync Separator and Quaternary ADC modules need to
be set up as a pair.

- (1) Connect the Sync Regenerator board via the extender board;
then switch on.
- (2) Apply a 100% colour bar signal to the SIS input on the
rear panel, and terminate with 75 ohms on the loop-out
socket.
- (3) Monitor Test Point X5 and adjust R91 so that the clamp
occurs 5 to $5.5\mu s$ after the leading edge of syncs at X4.
Also check that it is 1.5 - $2.1\mu s$ wide.
- (4) Monitor X8 and adjust R87 for a pulse width of
 $4.7 \pm 0.1\mu s$.
- (5) Connect a second oscilloscope probe to X6 and adjust R90
so that the clamp pulse at X6 begins 4.8 to $5.0\mu s$ after
the negative-going edge at X8. Also check that its width
is 1.5 - $2.1\mu s$.

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- (6) Monitor the clamp guard pulse at X9 and adjust its width by R89 to $3.5\mu s$ less than the line repetition period (ignoring the irregular repetition periods during the field synchronising sequence).
- (7) Monitor the video input on the rear panel and the line trigger pulse on X1-16a and adjust R69 for a delay of 245ns between the half-amplitude point of the leading edge of line syncs and the negative-going edge of the line trigger pulse (up to 300ns is permissible if 245ns cannot be achieved).

Note: This adjustment affects the Quaternary ADC module (see 3.4(7) and (8)).

- (8) Monitor the Field Trigger + at Pin 14c and Field Trigger - at Pin 14a and check that it is $4 - 6\mu s$ wide.
- (9) Monitor the Mixed Sync output at X1-15a. The Line Sync width should be $4.8 - 5.0\mu s$, as will be alternate equalising pulses. (For examination of the equalising pulses and broad pulses, trigger the oscilloscope from the Field trigger pulses at X1-14c).
- (10) Monitor Test Point X11 and check that the falling edge occurs less than $3.5\mu s$ after the leading edge of input sync and that the overall pulse length is greater than $1\mu s$.
- (11) Monitor A13 Pin 6 and adjust C32 for 0V.

Note: This is dependent upon the oscillator being locked to a correct line frequency source.

- (12) Monitor the following outputs from the board:

Clamp + at X1-12c : $1.5 - 2.1\mu s$

Sample + at X1-10a : five (for 625 lines) or
six (for 525 lines)
negative-going broad
pulses in the vertical
interval.

Regenerated Sync at X1-20a

Composite Blanking at X1-12a

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Field Blanking at X1-22a

Composite Gate at X1-21a
(Vertically blanked horizontal sync).

- (13) By removing and applying normal video, SIS video and video without field component, check the operation of the failure indicators H1, H2 and H3.
- (14) Feed a colour bar SIS signal to the input and adjust C45 so that the timing delay between the input colour bar sync and the output sync is the same as the delay between the input colour bar video and the output colour bar video.

3.4 Quaternary ADC

- (1) Connect a Stereo Sound in Syncs signal to the SIS Input on the back panel and terminate in 75 ohms on the loop-out socket.
- (2) Fit the board via an extender board and connect an oscilloscope via a probe to X7 and OV.
- (3) Switch on and adjust R6 for digits of 1.8V p-p.
- (4) If the board has not been previously tested, preset the delay line (X3) links to Positions 2 and 5 counting from the front to the back.
- (5) Connect the frequency counter to X11 and measure the oscillator frequency; it should be

11.9375MHz \pm 5Hz (PAL) or
12.020978MHz \pm 5Hz (NTSC).

Note that this is dependent on the coder being locked to the Asynchronous Data Processor, which in turn is phase-locked to line sync.

- (6) Check that the oscillator goes out of lock when the SIS input feed to the decoder is removed, and goes back into lock when it is replaced.

- (7) Monitor the marker pulse (the first of the digits in the sync pulse) at X7 and the SAMPLE pulses at X13, and adjust the falling edge of sample pulse to occur 5ns after the centre (peak) of the marker, by adjusting the second half of the delay line (X3) for coarse adjustment, and C29 for fine adjustment. The second half of the delay line is towards the rear of the board.
- (8) Monitor X3 (marker link) and A15 Pin 10 and check that the marker pulse falls 45ns before first rising edge at Pin 10. Adjust the first half of the delay line to achieve this as nearly as possible.

3.5 Bitstream Regenerator

- (1) Fit the Bitstream Regenerator board via an extender board, then switch on.
- (2) Monitor the frequency on X9.
- (3) Remove X11 and X12.
- (4) By applying 0V to X1 Pin 19c and +5V to X1 Pin 20C, then +5V to Pin 19c and 0V to Pin 20c, pump the frequency up and down; the resulting frequency range should be 8.736MHz $\pm 200\text{Hz}$. The range of 400Hz can be set by R48 and the centre frequency by C16. A tolerance of 5Hz is allowed on the low and high frequencies.
- (5) Switch off and replace the board.

3.6 Clock and I/O (Reframer)

Use the switches on the front of the module or a Remote Control unit to select Tone 1 or Tone 2 and free-running mode. Adjust R14 for 5824kHz $\pm 0.3\text{Hz}$ at X14. DO NOT ATTEMPT THIS UNLESS YOU ARE SURE THAT THE ACCURACY AND STABILITY OF YOUR FREQUENCY COUNTER IS ADEQUATE FOR THE TASK, i.e. BETTER THAN 1 PART IN 10^8 .

This frequency should be checked after the first year, and less frequently thereafter.

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3.7 Audio Decoder

- (1) Probe X5 and adjust C31 for a locked signal of 50 : 50 mark : space ratio.
- (2) Probe X7 and adjust C35 for a locked signal of 50 : 50 mark : space ratio.
- (3) Refer to Installation Section 4.2.2 and set Tone 1 for a line up tone suitable for your system, particularly noting the choice between UK headroom tones and EBU headroom tones. Select Tone 1 by means of the switches on the front of the Clock and I/O (Reframer) module or a Remote Control Unit, if connected.
- (4) Connect an Audio Level meter with 600 ohms input impedance to the Channel A output pins (35 and 17) on the Monitoring socket on the rear panel. If the intended use of the output of this module is to drive a high-impedance circuit, the input impedance of the meter should be set to HIGH IMPEDANCE. Adjust R17 for the correct output level according to the tone selected for Tone 1 as in (3) above.
- (5) Repeat (4) for channel B, connecting to pins 37 and 19 of the Monitoring socket and adjusting R43.

3.8 DAC and Transformers

- (1) Set the switches on the front of the Clock and I/O (Reframer) module (or use the remote control unit if fitted), to select Tone 1.
- (2) Connect an Audio Level meter with a high-impedance balanced input, to the Channel A output pins (2 and 3) on the Audio Output (Stereo) socket on the rear panel. Adjust R15 for the correct output level according to the tone selected for Tone 1 in section 3.7 (3) above..

Note: The 600-ohm terminating resistors R27 and R28 are normally fitted on the module. They may be disconnected if external terminations are to be used. The input impedance of the meter should be set accordingly.

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- (3) Repeat (2) for channel B, connecting to pins 4 and 5 of the Audio Output socket and adjusting R26.

3.9 Audio Comparator (if fitted)

Full information to follow.

3.10 Video Processor

- (1) Connect the Video Processor board via the extender board, then switch on.
- (2) Apply a 100% colour bar signal to the video input on the rear panel, and monitor Video Output 1 on the rear panel on an oscilloscope terminated in 75 ohms.
- (3) Monitor A7 Pins 13 and 5 and check that the pulse is 1.7 - 2.1 μ s wide in each case.
- (4) Monitor the video output and adjust:

R8 for a video amplitude of 700mV p-p.

R21 to set video and sync at colour burst blanking level.

R137 for a sync output amplitude of 300mV (625 lines)
or 286mV (525 lines).

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R91 to set the top of sync level with blanking.

R34 to set the output blanking DC level at 0V.

- (5) Monitor the output on a Vectorscope and adjust L1 to correct the phase of the burst with respect to the bars and check that the bars are correctly positioned in the boxes.
- (6) Carefully observe the output and check for correct adjustment of the above controls, readjusting where necessary.
- (7) Apply a suitable signal for checking frequency response to the video input and adjust C50 for a flat response.
- (8) Check the other video output for similar performance.
- (9) Monitor the buffered video output at Pin 4c and check for an output of approximately 1V p-p.
- (10) Switch off and replace the board.

3.11 General Notes

The decoder setting up is now complete. Specification measurements, signalling and remote functions can now be checked.

4. MODULE FAULT INDICATIONS

4.1 Coder

Digital Signal Processor	ROM Error RAM Error Control Error	Indicates failure of self-test on DSP programme ROM. Indicates failure of self-test on DSP internal RAM. Indicates that Control data input via rear panel is for undefined use, or for data or mono + data bitstream.
Clock and I/O	Ext Data Fail Ext Clock Fail Ext C ₀ Clock Fail Ext C ₀ Fail Signal Fail	Indicates no data detected from Auxiliary input on rear panel. Indicates no data clock detected from Auxiliary input on rear panel. Indicates no C ₀ clock detected from Auxiliary input on rear panel. Indicates no C ₀ detected from Auxiliary Input on rear panel. Indicates a request has been made, either locally or remotely, to select or lock to a signal missing according to the above indications.
Audio Decoder	Mute Parity Error	Indicates a mute has been applied to the decoded audio because the frequency of parity errors is too great for acceptable quality of audio. Indicates that the Audio Decoder has detected a parity error.
Monitor 1	Refer to separate section in the Coder or Decoder handbook (see Information Finder).	

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Async Data Processor	Insert Fail	Indicates failure to insert quaternary data into video.
	Buffer U-flow	Indicates underflow of the data buffer, i.e. too little data to maintain correct insertion rate.
	Buffer O-flow	Indicates overflow of the data buffer, i.e. too much data to maintain correct insertion rate.
	Clock Fail	Indicates failure of 728kHz clock from the Clock and I/O module.
	Data Fail	Indicates failure of 728kHz data from the Clock and I/O module.
	Standby	Indicates that standby line syncs are being output, probably due to failure of input video.
Sync Separator	Pulses Present	Indicates the presence of SIS data in the input video.
	Sync Fail	Indicates failure of input sync, i.e. no video.
	No Field Syncs	Indicates failure of input field syncs.

4.2 Decoder

Sync Regenerator	Pulses Missing	Indicates the absence of SIS data in the input video.
	Sync Fail	Indicates failure of input sync, i.e. no video.
	No Field Syncs	Indicates that no field syncs are present on the input.

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Quaternary ADC	Amp Ref Data	Indicates that amplitude reference data is present in the input video, due to a coder fault.
	Data Fail	Indicates that no data is being detected.
	Justification Fail	Indicates that justified data has not been detected.
	Data Amp Low	Indicates that the detected data is 3dB, or more, low in amplitude, possibly due to low video amplitude.
	Data Amp High	Indicates that the detected data is 3dB, or more, high in amplitude, possibly due to high video amplitude.
	AGC Fail	Indicates that the micro-processor AGC system has failed and is being reset.
Data Recovery	Recovery Fail	Indicates a failure to obtain data from the Quaternary ADC.
Bitstream Regenerator	Clock Fail	Indicates failure of 728kHz clock from the module.
	Buffer O-flow	Indicates overflow of the data buffer, i.e. too much data to maintain correct output data rate.
	Buffer U-flow	Indicates underflow of the data buffer, i.e. too little data to maintain correct output data rate.

Monitor 1	Refer to separate section in the Coder or Decoder handbook (see Information Finder).	
Clock and I/O (Reframer)	Ext Data Fail	Indicates no data detected from Auxiliary input on rear panel.
	Ext Clock Fail	Indicates no data clock detected from Auxiliary input on rear panel.
	Int Data Fail	Indicates no data detected from Bitstream Regenerator.
	Int C_0 Fail	Indicates no C_0 detected from Audio Decoder module which may indicate failure of Reframer.
	Signal Fail	Indicates a request has been made, either locally or remotely, to select or lock to a signal missing according to the above indications; or that there is Int C_0 fail.
	Int Tone	Tone 1 or Tone 2 is selected, either deliberately or due to reframing action.
Audio Decoder	Mute	Indicates a mute has been applied to the decoded audio because the frequency of parity errors is too great for acceptable quality of audio.
	Parity Error	Indicates that the Audio Decoder has detected a parity error.