

8928 190 30001
8928 190 40001
General Description

STEREO SOUND IN SYNC

LDM 1903/00/01 (8928 190 30001)

LDM 1904/00/01 (8928 190 40001)

GENERAL DESCRIPTION

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1. INTRODUCTION

SOUND IN SYNC is a system in which a video link, for example between studio centres, is used for transmission of broadcast quality sound together with the video signal.

At the sending end of the link the audio signal is inserted in digitally coded form in the line synchronising periods of the composite video signal. At the receiving end the decoder converts the received digital information into the original audio signal and restores the video signal to normal.

This system is a development of the Two-channel Sound in Sync system which used the NICAM-3 bitstream. This system uses the NICAM 728 bitstream. It is suitable for either stereophonic or dual-language transmissions. It consists of a Coder Type LDM 1903 and a Decoder Type LDM 1904.

A number of versions of the system are available. These are detailed in the table in Para. 3.

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2. PRINCIPLES OF OPERATION

Refer to the outline block diagrams (Sheets 510-1) and the functional block diagrams (Sheets 536-1).

2.1 Audio Digitisation

Each audio channel is pre-emphasised, band-limited to 15kHz and sampled at 32kHz. The two channels are sampled simultaneously and digitised in a 14-bit A-to-D Converter.

2.2 Compression and Bit Stream Generation

The digitised samples from the two audio channels are dealt with separately by a process of near instantaneous compression in a NICAM 728 compander system; this compresses the samples from 14 to 10 bits. Each set of 32 samples is coded into one of five gain ranges, each range being determined by the greatest magnitude found in the set. The digital coding format used for the samples is 2's complement, but for ease of explanation and understanding the following description of the compression process assumes sign-plus-magnitude coding.

For each sample, the sign bit is sent,

As many of the four most significant magnitude bits (MSBs) as are zeros in all the samples are dropped; the following nine bits are sent. Note that in the example in Fig. 1 there are three leading zeros; the 9-bit block would be shifted to the left or the right if there were two or four leading zeros.

Sample 1	+	0	0	0	1	1	1	0	1	0	1	1	0	1
2	+	0	0	0	0	1	1	0	1	1	1	0	0	1
3	-	0	0	0	1	0	0	1	0	1	0	1	0	1
4	-	0	0	0	0	0	1	1	1	0	0	1	0	0
		All zeros.												
Sample 32	+	0	0	0	1	1	0	1	1	0	0	1	0	1

Fig. 1

A range code sent with each set of samples tells the decoder how many

zeros to re-insert after the sign bit. Thus the signals of highest amplitude are encoded to 10-bit accuracy, while for the low-level signals the full 14-bit accuracy is retained.

For 2's complement coding, which is actually used, the most significant bit (MSB) can be regarded as the sign bit in the above description, and the next most significant bits which are the same as the MSB can be regarded as leading magnitude bits of value zero.

For each 10-bit compressed sample word, a parity bit is added, based upon the six most significant bits. The parity is even. The range codes for each 1ms block of samples are conveyed by two 3-bit scale factors (one for each channel) 'hidden' in the parity bits; the 64 parity bits are divided into six groups of nine (with 10 over), each group being allotted to one scale factor bit; if the scale factor bit is a zero, the parity bits are unchanged; if the scale factor bit is a 1, the parity bits are complemented, i.e. the parity becomes odd. In the decoder, majority decision logic is used to extract the scale factor bits and reveal genuine parity errors. Some countries intend using the remaining 10 parity bits in two groups of five for transmission of two extra data bits, sometimes called Binary Control Information or CIBs.

If the two channels comprise a stereo signal, the bits for the two channels are interleaved on a sample basis, i.e. 11 bits (including parity) for a sample of channel A are followed by the corresponding 11 bits for channel B. If the bitstream is for one or two monophonic signals, the bits for the two channels are interleaved on a frame basis, i.e. a 1ms frame containing samples for 2ms of channel M1 audio is followed by a 1ms frame containing samples for 2ms of channel M2 audio. The frame boundaries correspond to the compression block boundaries. This is followed by a process of bit interleaving within each frame (whether stereo or mono) such that adjacent bits from a sample word occur at least 16 bits apart in the bitstream. Each 1ms frame has an 8-bit frame alignment word at the beginning, followed by five Application Control bits, 11 Additional Data bits and then the 704 (= 64 x 11) sound data bits, making a total of 728 bits per frame. All but the frame alignment word bits are 'scrambled' for energy dispersal, i.e. the bits are complemented or not according to a defined pseudo-random sequence.

2.3 Conversion to Quaternary Form

To insert the digitised audio information in the line sync period of the video signal, pairs of bits are combined to form quaternary (4-level) digits ('quits'). This process enables data at an instantaneous rate of about 12 Mbits/second to appear at 6 Mquits/second, which is well within the bandwidth limits of video circuits.

Quit Level 0 is at peak sync level and Level 3 is 700mV more positive (Fig. 2).

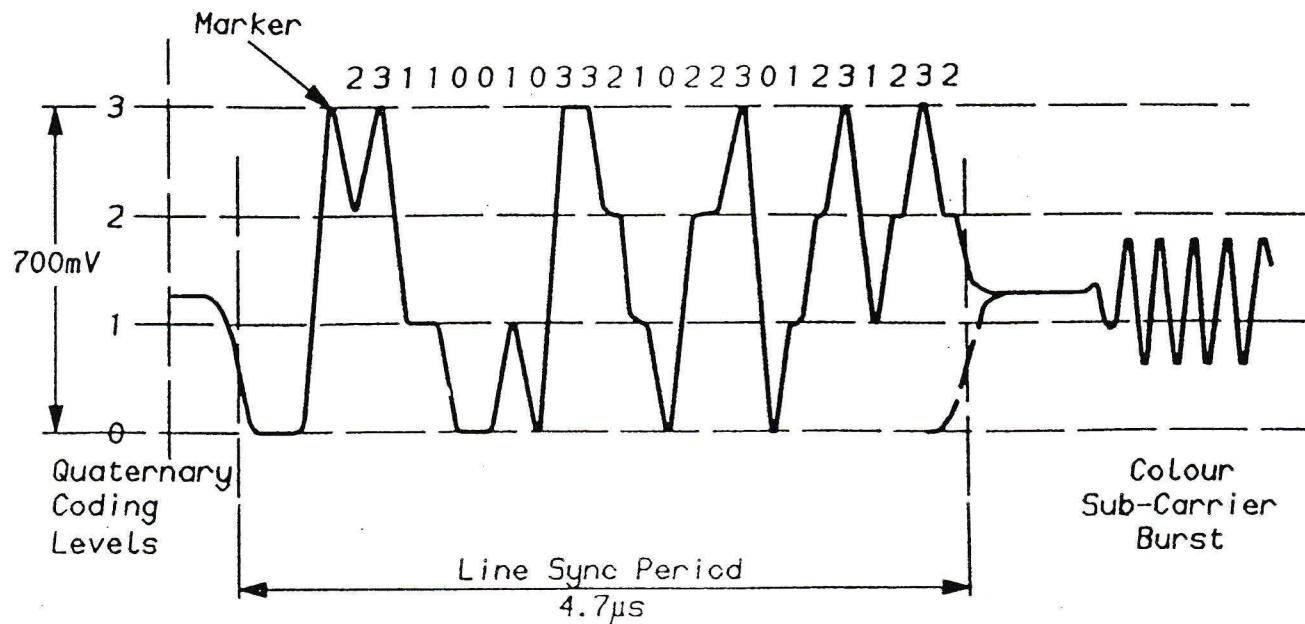


Fig. 2

Since the data rate and the TV line rate are not interrelated the insertion process has to be asynchronous: most sync pulses contain a marker pulse plus 24 quits, but every two or three lines a marker and only 22 quits. The marker and following digits start late, rather than end early. The marker is a Level 3 quit which serves as a timing reference for the following data.

The two bits taken to form each quaternary digit are taken from adjacent bits in the bitstream (Fig. 3). The conversion from bits to quits is done on the basis of the Gray code, i.e. only one bit changes between adjacent quit levels, so that if the decoder detects a quit value incorrectly by one level, only one bit error is produced.

The Gray coding scheme is inverted after the first, third, fifth, etc quit in each sync pulse. This inversion is necessary for a NICAM-3 bitstream and is retained for NICAM 728 although the reason does not apply.

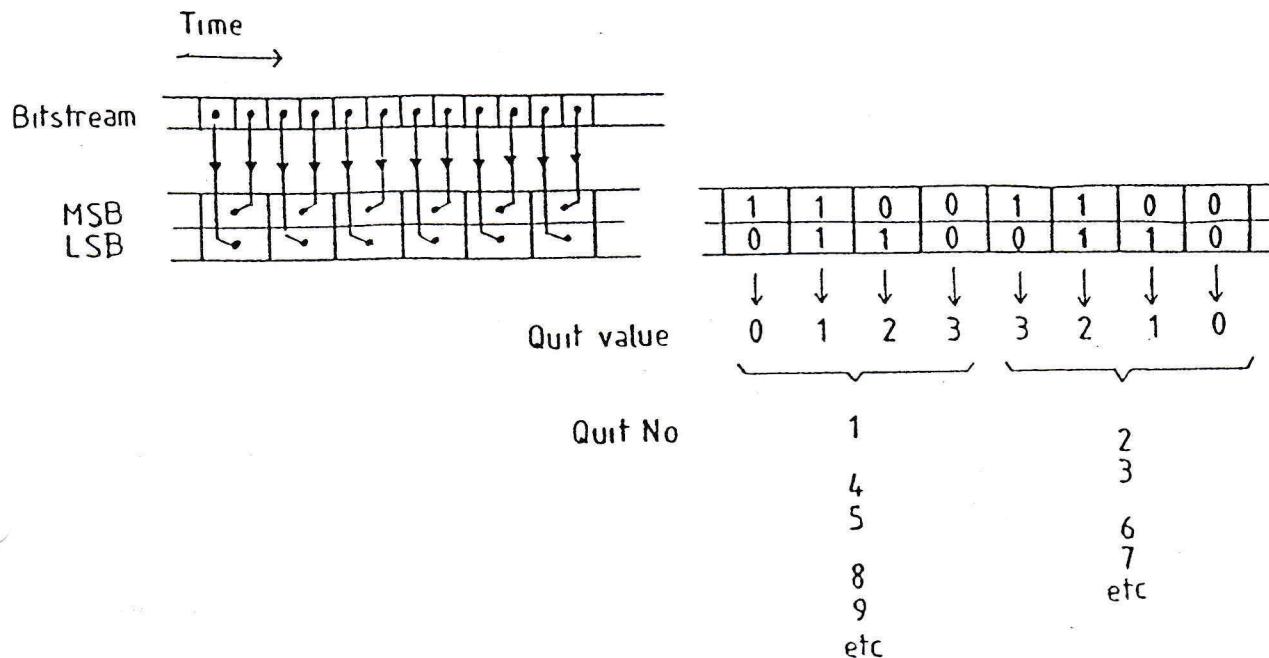


Fig. 3

The asynchronous data insertion is controlled by four Field Programmable Logic Sequencer (FPLS) ICs which monitor the depth of data in a FIFO memory and provide standby sync pulses if the video source should fail. These standby sync pulses may be line sync only or composite sync; the selection is made by the 2-position link X18 on the Asynchronous Data Processor module. Data insertion itself is done in analogue circuitry of mainly discrete components which introduces minimal distortion of the video signal.

2.4 Data Recovery

In the decoder the quits are decoded by a process which is designed to achieve reliable results even after moderate distortion of the signal during transmission. Each quit is sampled and converted to a 6-bit number by a fast ADC: by examining the range of numbers produced, a microprocessor determines the reference voltages to be used by the ADC, thus compensating for any loss or gain in the transmission path. The program for the microprocessor is written in FORTH and stored in an 8kbyte EPROM. The microprocessor has a built-in FORTH interpreter.

The reference voltages to be used by the 6-bit ADC are produced by an 8-bit DAC. Timing is controlled by another FPLS which determines, from the position of the marker pulse after the sync leading edge, whether there are 24 or 22 following quits.

As the microprocessor takes time to respond to changes in quit amplitude, further immediate processing is done on each set of 24 or 22 6-bit quit values: each value within the range expected for a Quit Level 0 or 3 is used to produce an error value which is averaged for each of levels 0 and 3 throughout the set. The two error values (for Levels 0 and 3) are used to select one of 256 look-up tables for correction of the whole set of 6-bit values as they are converted to the original pairs of bits they represent.

2.5 Bit Stream Regeneration

Each pair of bits recovered is fed into a FIFO memory, and the contents of the memory are fed out at a constant rate as a 728kbit/second bit stream equivalent to that in the coder. The bit stream clock regeneration is under the control of a programmed FPLS which maintains a steady clock rate in spite of the erratic rate of arrival of the recovered data.

2.6 Reframing

Any discontinuity in the bit stream will cause the audio decoder to receive spurious data, which may result in unpleasant noises followed by a mute as the decoder circuitry re-locks to the framing data in the bit stream. To avoid the worst effects of any such discontinuity, reframing circuitry is included in the Clock and I/O module.

The reframer stores the incoming data in a memory and reads it out between 1 and 17ms later. As it is stored, the bit stream is checked for the Frame Alignment Word (FAW) which should occur every millisecond (every 728 bits). If the FAW is missing, then the source of data being read out is switched to a bit stream representing silence, held in ROM (Read Only Memory), before the suspect frame has been read out. When the framing of incoming data has been found again and confirmed, reading of data is switched back to RAM. The effect is a short period of silence, typically 30ms, which for much programme material will be unnoticed. The reframer also checks the 16-frame sequence (defined by the C_0 bit immediately following the FAW), again switching to ROM if necessary. At a discontinuity it also checks for a change between stereo and mono and signals the format change 16 frames in advance as required by the NICAM 728 specification.

For situations where a 17ms delay is considered detrimental, the reframer may be set to a mode in which the maximum delay is 2ms for a Stereo signal and 3ms for a Mono signal; but in this case the 16-frame sequence is not maintained though the structure within each frame is maintained.

2.7 Bit Stream Decoding

Decoding the bit stream is done with an Integrated Circuit developed for use in television receivers, followed by a Digital Oversampling Filter

and other ICs as used in Compact Disc players. The oversampling filter reduces considerably the complexity of the filtering which is needed after D-to-A conversion. It increases the effective sampling rate four-fold, by interpolating between samples, while band-limiting the audio to 15kHz. It also applies $\sin x/x$ correction suitable for the following D-to-A converter. A simple analogue active filter following the ADC suppresses the unwanted lobes around the multiples of 128kHz in the spectrum of the DAC's output, while another filter applies de-emphasis before the output amplifier. Circuitry has been added to extract the Additional Data bits and the CIBs mentioned in connection with the coding process.

2.8 Restoration of Video

Blanking the data in the line sync pulse period is not sufficient to restore the video to normal: apart from the fact that the data encroach on the trailing edge of sync pulses, they also overrun alternate equalising pulses which consequently have been widened from $2.3\mu s$ to about $4.7\mu s$. Composite sync therefore has to be fully regenerated and switched into the video waveform in place of the syncs with sound data. An oscillator, in a phase-locked loop controlled by incoming line sync edges, clocks an FPLS, producing line sync, equalising pulses and broad pulses, while another FPLS selects these in turn to form the correct field sequence. A broad pulse detector ensures that the regenerated field sequence occurs at the same time as the incoming field sequence and triggers a sync amplitude sampling circuit which automatically adjusts the amplitude of regenerated syncs.

2.9 Digital Input and Output, and Synchronisation

Facilities are provided for input of Control and Additional Data and CIBs to a Coder and their output from a Decoder.

Facilities are also provided for input and output of 728 kbit/s bit streams and clocks, so that an externally derived bit stream may be inserted in the sync pulses in a Coder, and/or the internally derived NICAM 728 bit stream may be fed out. The interfaces are to the RS-422 standard. Additionally, there are clock and C_0 inputs and outputs which allow two coders to be synchronised in their bit stream generation and in their insertion of quots into the sync pulses, so that switching a decoder between two coders may be accomplished without the decoder losing lock. (C_0 is a NICAM 728 control bit which is alternately 1 for 8 frames and 0 for 8 frames, thus defining a 16-frame sequence).

Similarly, a decoder provides a 728 kbit/s bit stream output as well as audio outputs, and the option of decoding an external bit stream instead of the bit stream extracted from the sync pulses. An external bitstream, if selected, is passed through the reframer circuitry before being decoded.

Both coder and decoder include built-in digital tone generators which may be selected remotely or by switches behind the front panel. One of these

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tones is selected automatically as a 'fall back' source if the signal being used should fail. The fall-back tone is usually set to silence, especially in the decoder, which uses the fall-back tone in the reframing process.

The Decoders provide a C_0 output as well as clock and data, so increasing the possibility of synchronising various signal sources.

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3. SYSTEM VERSIONS

3.1 Stereo Sound in Sync Module Requirements

All modules are 3913 446 xxxx0 version vxx as follows (except for Audio ADC, which is 3913 466 xxxx0):

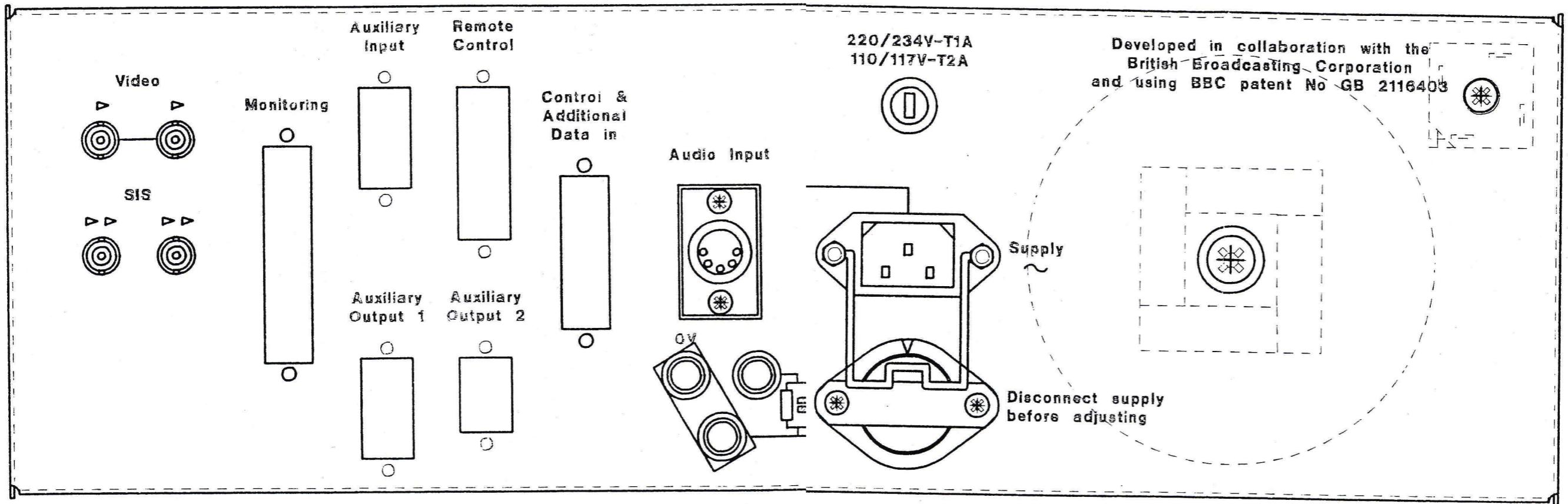
<u>Coder LDM 1903</u>	<u>/12</u>	<u>/14</u>
Power Supply Module	7492	v00
Audio Input Filters	7486	v00
Audio ADC	7890	v00
Digital Signal Processor	7540	v01
Clock and I/O	7541	v01
Audio Decoder	7544	---
Monitor 1	6988	v01
Coder Video Processor	6987	v00
Async Data Processor	6975	v01
Sync Separator PAL	6735	v01
NTSC	6736	---
Rack Frame Assembly	6979	v00

<u>Decoder LDM 1904</u>	<u>/12</u>	<u>---</u>
Power Supply Module	7492	v00
Dec Video Processor PAL	6953	v00
NTSC	6758	---
Sync Sep and Regen PAL	6733	v00
NTSC	6734	---
Quaternary ADC	6976	v01
Data Recovery	6977	v01
Bitsream Regenerator	6760	v02
Monitor 1	6988	v01
Clock and I/O (Reframer)	7549	v00
Audio Decoder	7544	v01
DAC and Transformers	7545	v00
Rack Frame Assembly	6982	v00

3.2 Version Differences

/12 PAL/625 & NICAM-728, system monitoring
/14 PAL/625 & NICAM-728, system and audio monitoring

/80 Listed Customer Variants
/90 Listed Customer Variants



TITLE		REAR PANEL LAYOUT			
STEREO SOUND IN SYNC CODER		8928 190 30001		89-11-29	
ARCHIVE No		1	SP	10	SH 512-1
PAWN N. BROWN		MECH CHK		ELECT CHK	
APPROVED					