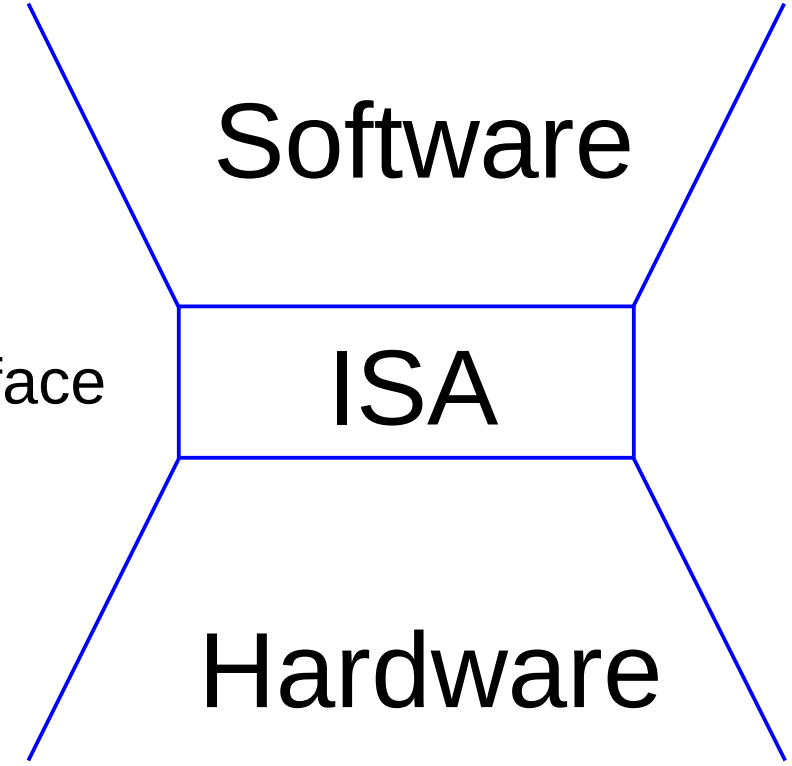
The software / hardware interface



SW only assumes
a fixed ISA

SW / HW interface

Instruction Set Architecture

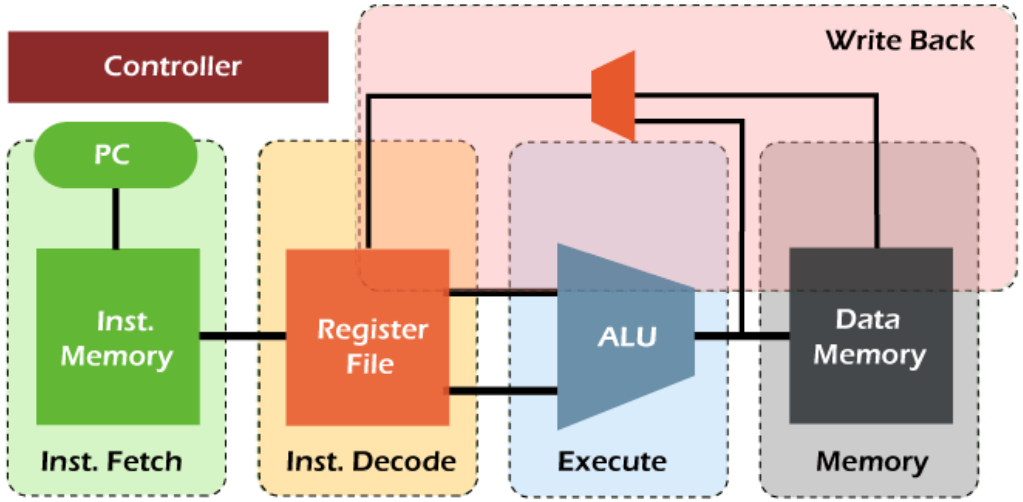
HW may be
implemented in
different ways
for optimal
speed, power, cost

Abstraction levels of software (2)

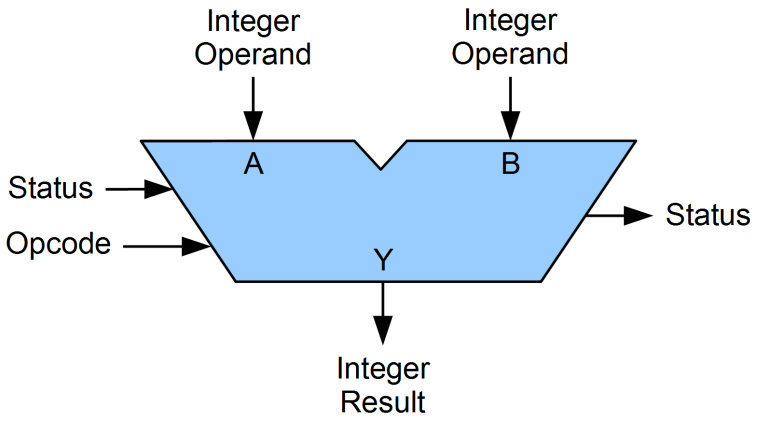
Level	Example	File extension
C-program	C = A+B;	.c
Assembly language	add x3,x1,x2	.asm
Machine language (modules)	0000000 00010 00001 000 00011 0110011 (Format: funct7 rs2 rs1 funct3 rd Opcode. Grouped result: 0 2 1 0 3 0x33)	.obj
Executable machine language	0000000 00010 00001 000 00011 0110011 (Only jumps to targets outside a module are different)	.exe

Abstraction levels of hardware (1)

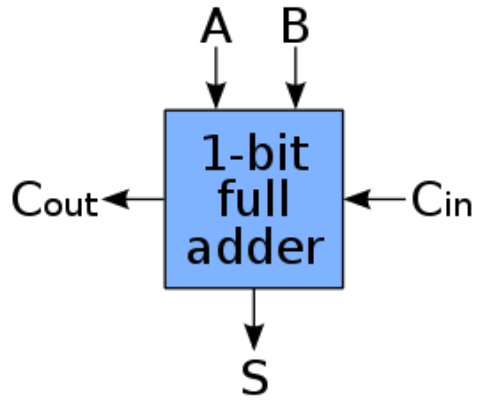
Simple RISC-V processor



64-bit Arithmetic Logic Unit (ALU)



1-bit adder



[Execution, Stages and Throughput in Pipeline – javatpoint]

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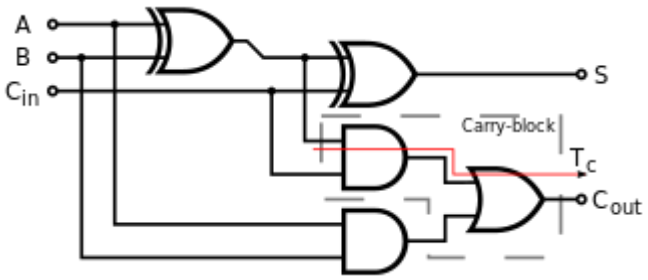
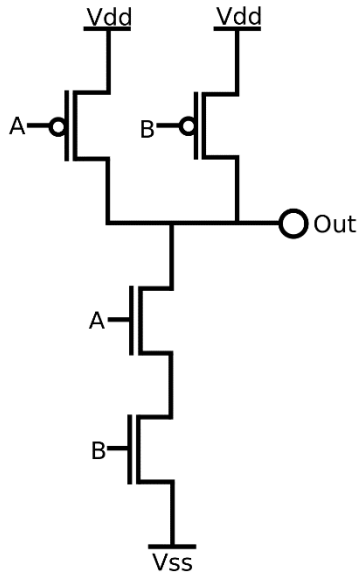
By en:User:Cburnett - Own work, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=1477628

Abstraction levels of hardware (2)

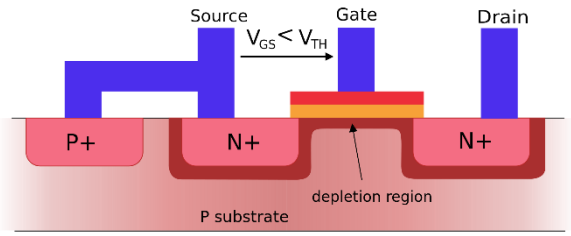
1-bit adder
implemented with gates



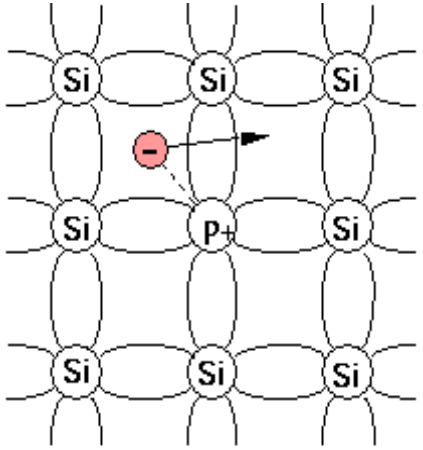
NAND-gate



N-type MOSFET



N-type silicon



1-bit adder: By Inductiveload - Own work, Public Domain, https://commons.wikimedia.org/w/index.php?curid=1023334

NAND_gate: By JustinForce - Own work, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=2593317

N-mosfet: By derivative work: Biezl (talk)MOSFET_functioning.svg: Olivier Deleage and Peter Scott – MOSFET_functioning.svg, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=4504996

N-type silicon: Donor_in_Si_lattice.png (208×209) (wikimedia.org)