4-Bit Carry Look-Ahead Adder using CMOS Mirror Logic

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***Abstract*- This paper presents a transistor-level implementation of a 4-bit carry look-ahead (CLA) adder using CMOS mirror logic. CLA adder design overcomes the delay issue in conventional RCA adder by eliminating the cascading effect of the carry bits. The sum and carry terms are processed at once in the CLA adder. CMOS mirror logic results in reduced transistor count compared to Static CMOS logic. Further, it uses the same transistor topology for NMOS and PMOS networks which leads to a symmetric layout. Spice simulation results of proposed CLA adder confirms 4-bit binary addition.**

I. Reference Circuit Details

Proposed 4-Bit Carry Look-Ahead Adder is implemented using CMOS Mirror Logic. CLA first calculates the values of generate G_i and propagate P_i terms [1]. Then, they are used to calculate carry bits $C_{i+1} = G_i + P_iC_i$. This means every carry bit can be found from generate and propagate terms. Next, sum bits are evaluated using $S_i = P_i \oplus C_i$ for every bit. This avoids the need to ripple the carry bits serially down the chain [2]. Carry and sum terms are implemented using CMOS mirror logic as shown in Fig. 1 and Fig. 3. Generate and propagate terms are implemented using Static CMOS logic as shown in Fig. 2

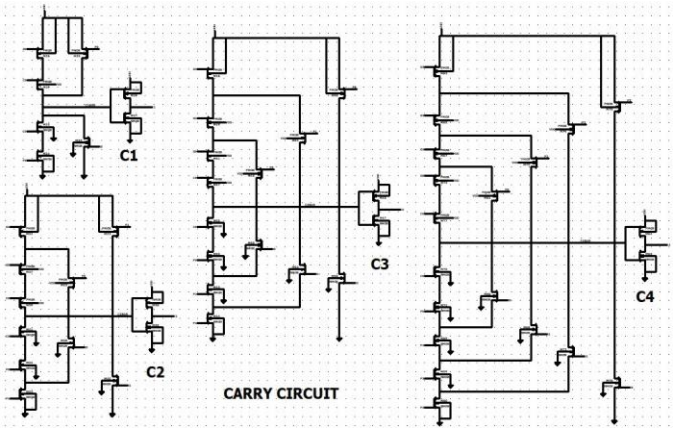

Fig. 1 Carry circuit of 4 bit CLA adder

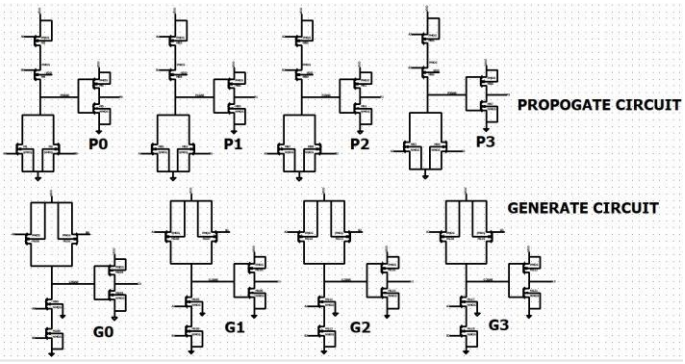

Fig. 2 Generate and Propagate circuit of 4 bit CLA adder

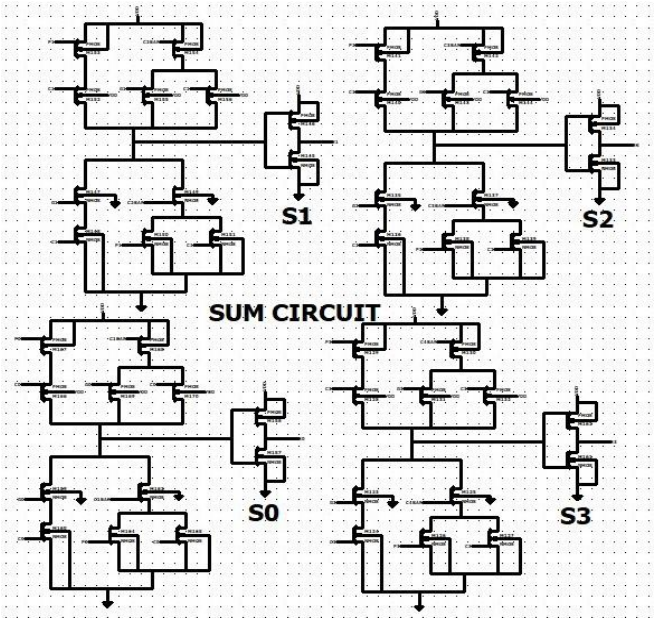

Fig. 3 Sum circuit of 4 bit CLA adder

II. Reference Circuit Waveforms

Simulation of 4 bit CLA adder circuit is done in LTspice. Fig. 4 depicts timings diagrams showing the addition of two 4 bit binary numbers thus validating the functionality of 4 bit CLA adder.

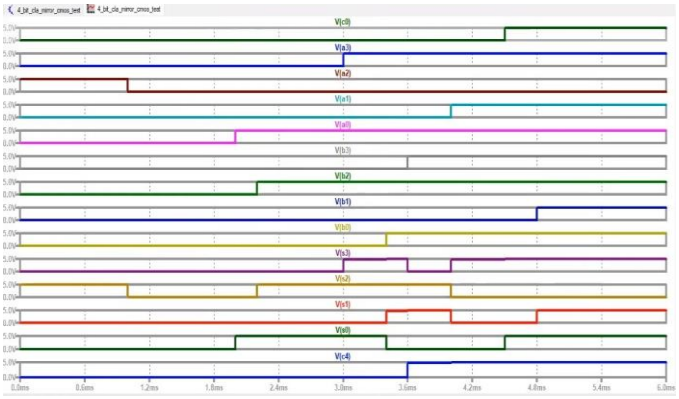

Fig. 4 Reference timing diagram showing addition of two 4 bit binary numbers

References

[1] M. S. Hossain and F. Arifin, "A Proposed Design of Conventional 4-Bit Carry Look-Ahead Adder Improving Performance," 2020 Advanced Computing and Communication Technologies for High Performance Applications (ACCTHPA), 2020, pp. 89-93, doi: 10.1109/ACCTHPA49271.2020.9213227.

[2] Uyemura, J., 2002. Introduction to VLSI circuits and systems. 1st ed. New York: Wiley.