HDL Generator Documentation

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1 Project Introduction

1.1 Purpose

The purpose of this project is to be able to easily describe a Moore state machine and turn it into a hardware description language (HDL). The HDL can then be used with FPGA's.

1.2 System Architecture

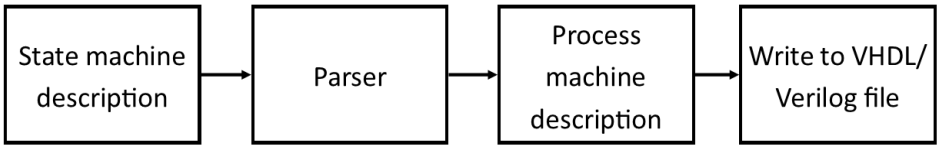

Figure 1.1: System Architecture

2 Language Structure

This section defines how you express a state machine or system of state machines. A Moore machine can be defined using a set of six items. These are:

- Finite set of states (S)
- Initial state (S_0)
- Finite input alphabet (Σ)
- Finite ouitput alphabet (Λ)
- Transition function ($T : S \times \Sigma \rightarrow S$)
- Output function ($G : S \rightarrow \Lambda$)

Graphically this is shown below in Figure 2.1.

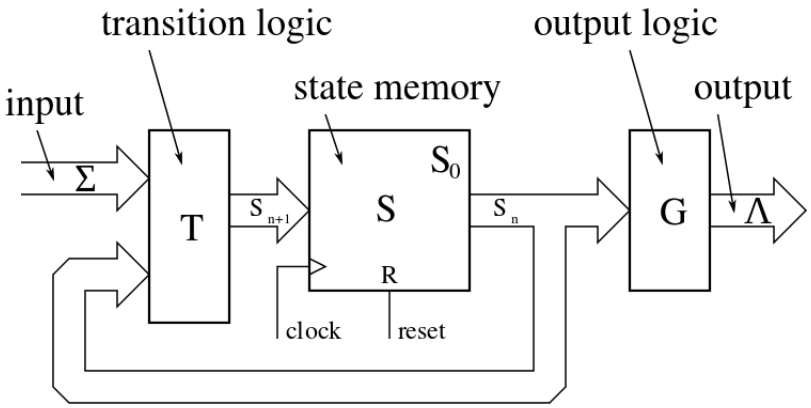

Figure 2.1: Moore Machine
Taken from::://commons.wikimedia.org/wiki/File:Moore-Automat-en.svg

2.1 State Machine Syntax

tTesetign asdfjaslk f alsdkfj fd dkfdfjk fd jd fkjdfjk djkd j j dkjf d

2.2 System Syntax