Lab 3

Logic Design

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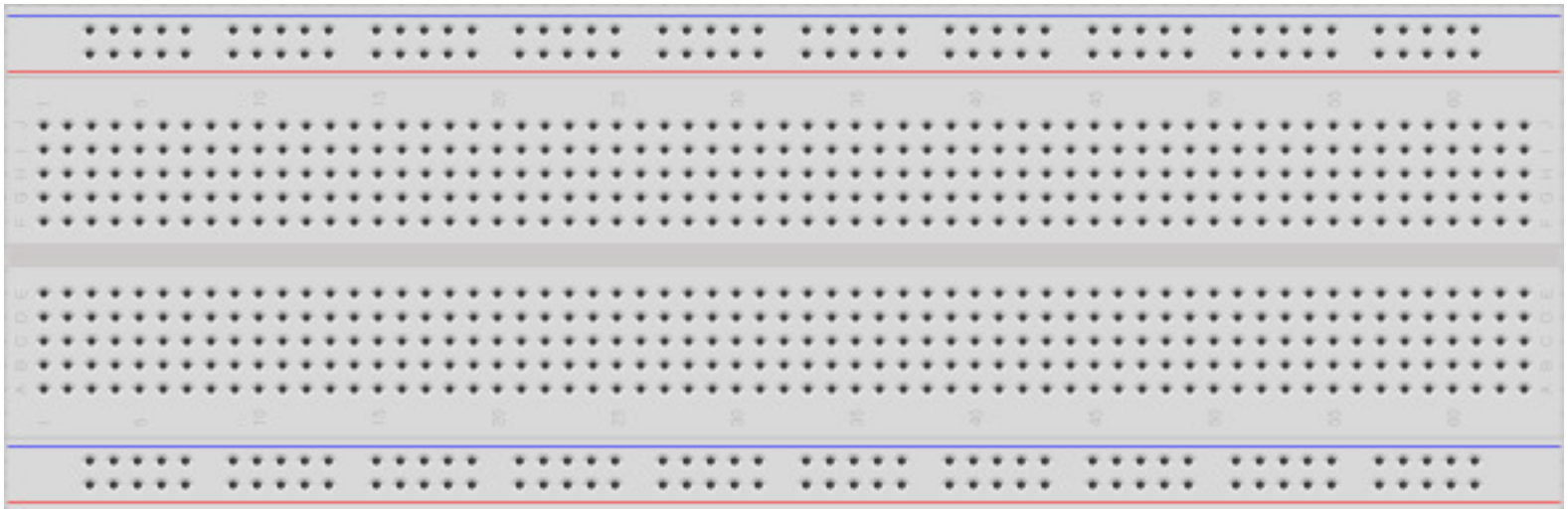
Overview

- **Bread board**
- **2-bit comparator**

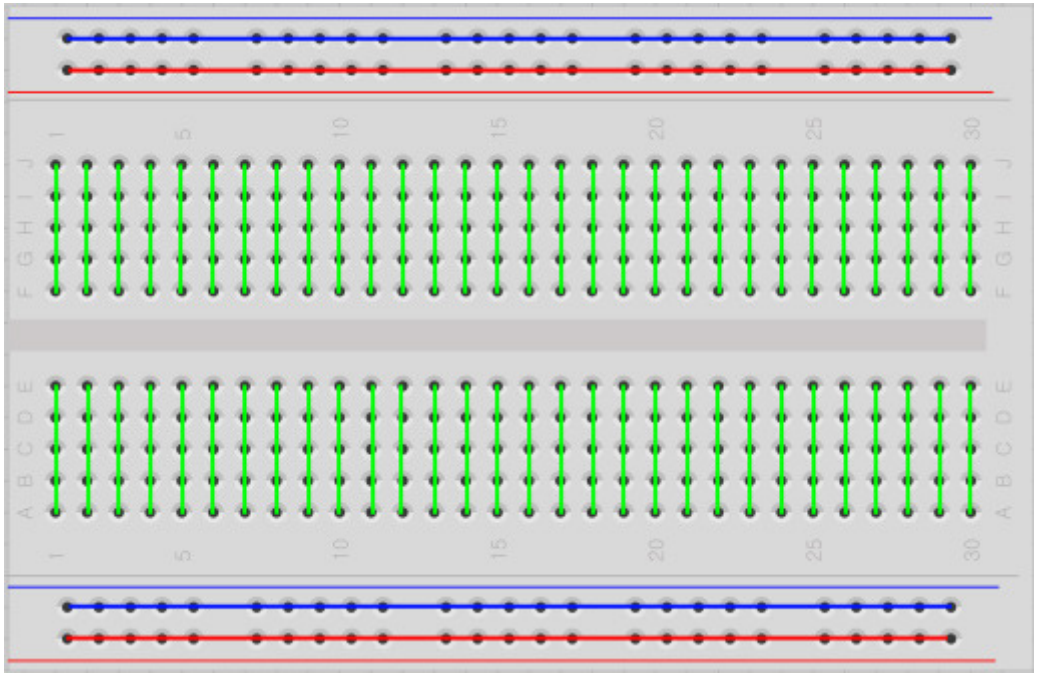
Breadboard

- **브레드보드**
  - 속칭 빵판, 빵틀
  - 재사용 가능한 무땜납 장치
  - 납땜 없이도 회로를 테스트 할 수 있고, 회로 수정이 용이



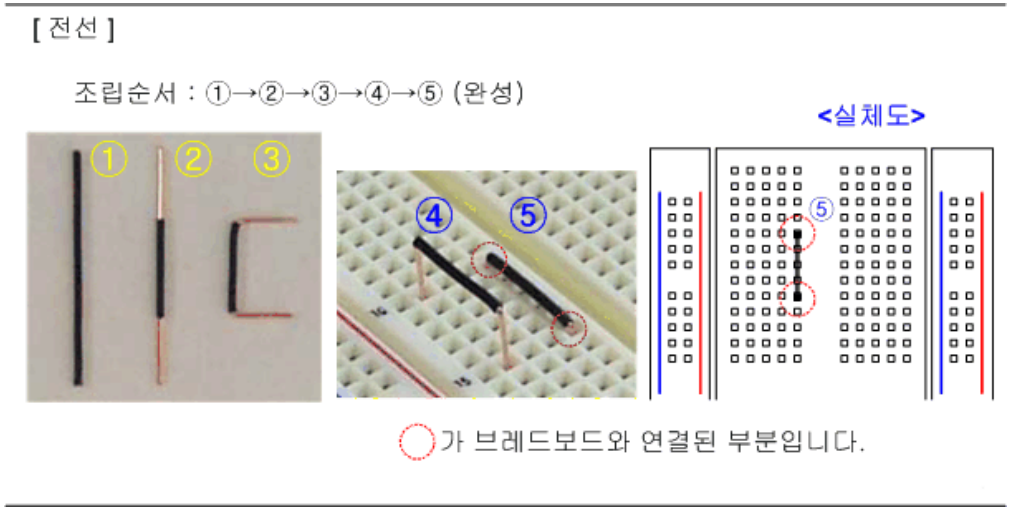
Breadboard

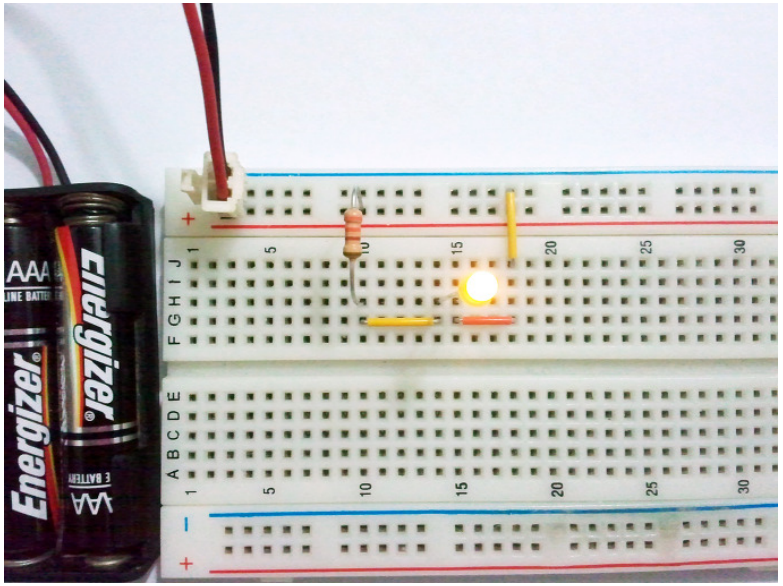
- **브레드보드 내부 연결**
  - 빨간선(+), 파란선(-)은 버스로 VCC, GND 연결에 사용한다.
  - 세로 다섯줄은 IC/부품 영역으로, 부품을 꽂는 부분이다.
  - 줄로 연결된 브레드보드 내부는 스트립(금속)으로 연결되어 있음



Breadboard

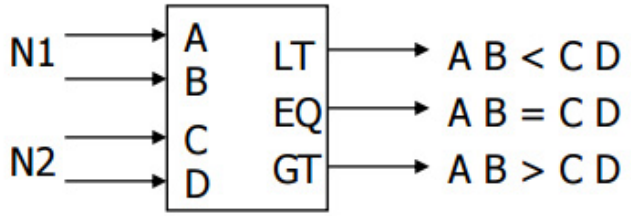
- **브레드보드에 부품 조립하기**
  - 내부에서 합선이 되지 않도록 주의해서 연결하자
  - VCC와 GND 버스라인을 따와서 LED, 칩셋 등의 부품에 연결할 수 있다

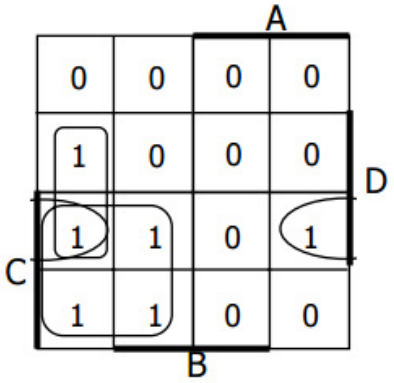




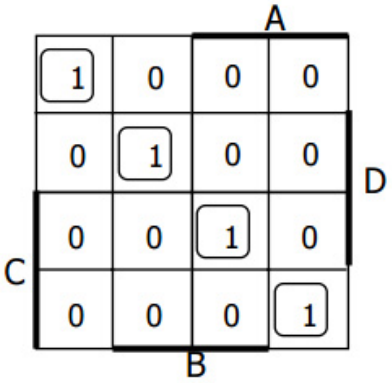
2-bit comparator

- **Block diagram and K-map**

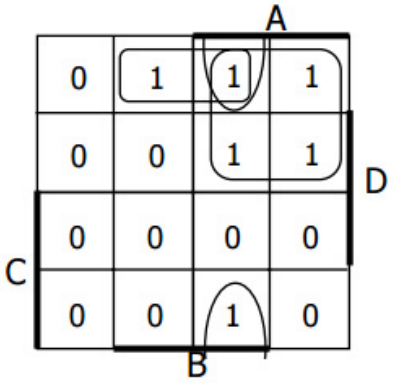




K-map for LT



K-map for EQ



K-map for GT

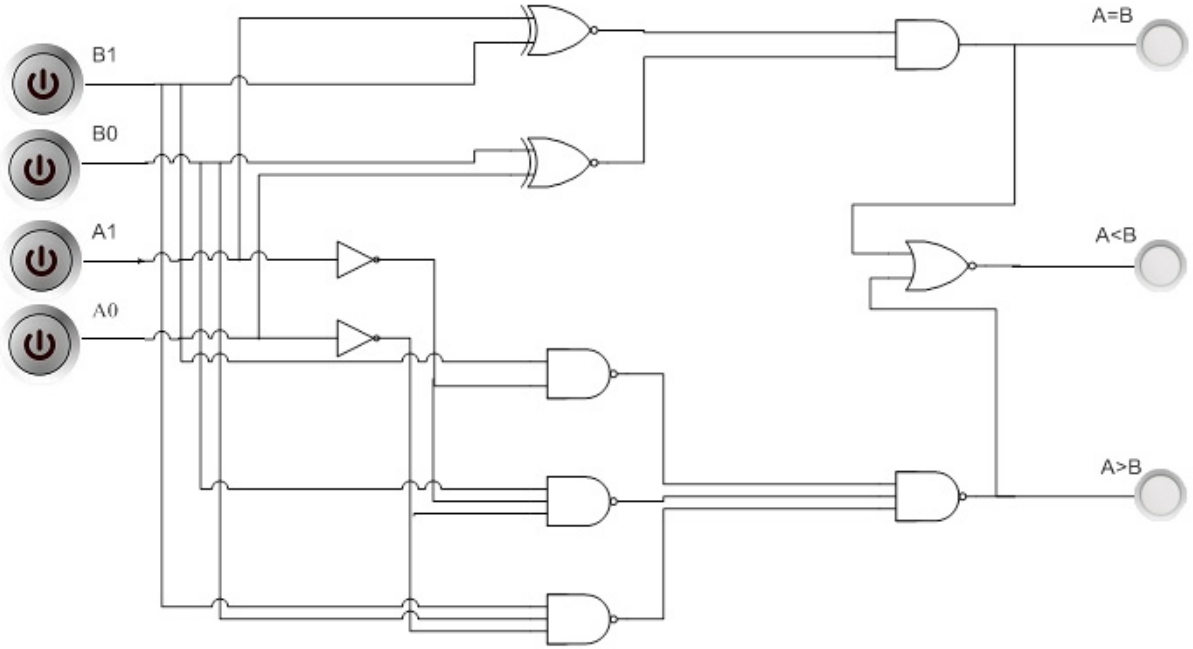
LT = A' B' D + A' C + B' C D

EQ = A' B' C' D' + A' B C' D + A B C D + A B' C D' = (A xnor C) • (B xnor D)

GT = B C' D' + A C' + A B D'

2-bit comparator

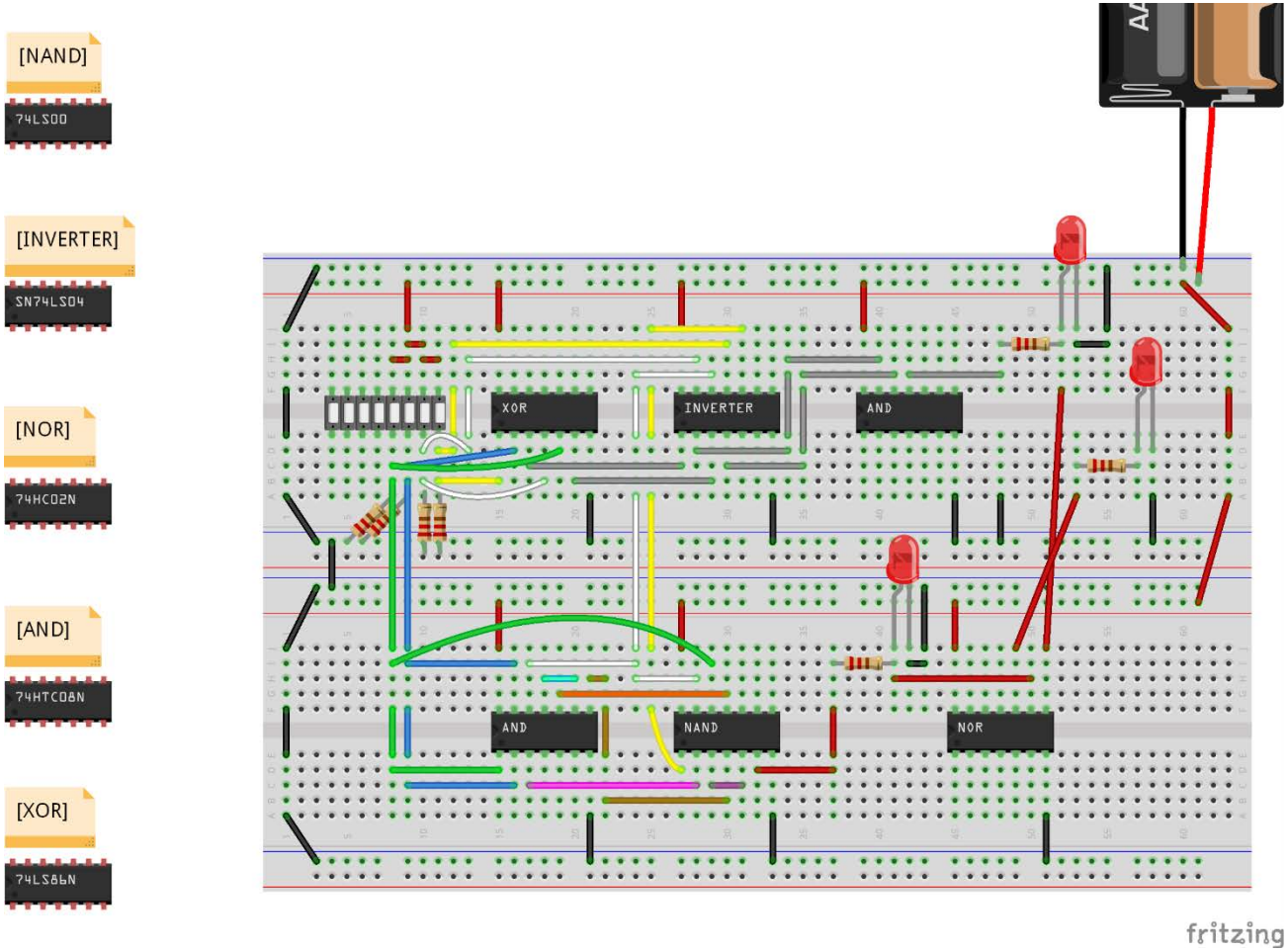
- **Logic design**



A1	A0	B1	B0	Y1 A>B	Y2 A=B	Y3 A<B	
0	0	0	0	0	1	0	
0	0	0	1	0	0	1	
0	0	1	0	0	0	1	
0	0	1	1	0	0	1	
0	1	0	0	1	0	0	
0	1	0	1	0	1	0	
0	1	1	0	0	0	1	
0	1	1	1	0	0	1	
1	0	0	0	1	0	0	
1	0	0	1	1	0	0	
1	0	1	0	0	1	0	
1	0	1	1	0	0	1	
1	1	0	0	1	0	0	
1	1	0	1	1	0	0	
1	1	1	0	1	0	0	
1	1	1	1	0	1	0	

2-bit comparator

- **Breadboard**



저항부분의 구현이 바뀌었으니 확인해 보세요.

디지털 멀티미터로 플로팅을 확인한 후 발생한 곳에 적절한 용량의 저항을 넣어 전압을 감소시켜 보세요.

3-input NAND gate 부분 구현이 수정되었습니다. 참고해주세요

Report (1/2)

- **Requirements**
  - No page limit
  - Attach a video file (which shows result of practice)
    - Submit a packed file (report + video; .zip .tar .tar.gz .. etc.)
  - **Due: March, 30th**

- **Practice**
  - Base contents (procedure, result, role allocation)

Report (2/2)

- **Preparation**
  - BCD
  - 7-Segment display
    - Datasheet
    - Common anode
    - Common cathode **(we will use this type)**
  - Decoder
  - BCD to 7-Segment decoder
    - Concept
    - Truth table + K-map optimization
    - Logic diagram (Schematic)
    - Circuit wiring diagram
  - **Cont'd in detail (next slide)**

Supplement Slides (1/3)

- **Truth table**
  - Input: 4-bit
    - 0000~1001, corresponding to the decimal numbers
    - 1010~1111, don't cares
  - Output: 7-bit
    - A, B, C, D, E, F, G, will be connected to the 7- segment display
    - You **MUST** follow below figure for the output bit selection

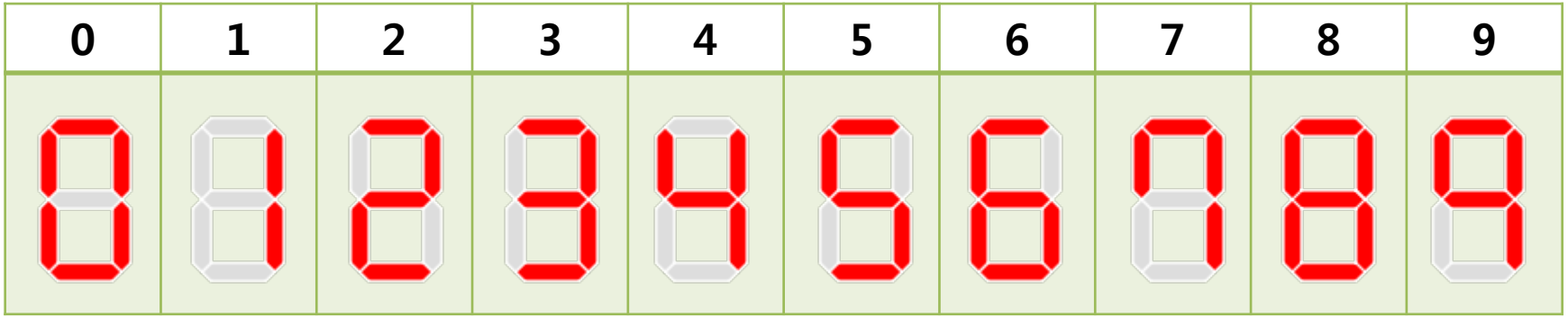


Fig.1 7-segment display

Supplement Slides (2/3)

- **Logic diagram**
  - Draw a schematic using the truth table with K-map method
  - Use AND, OR, NAND, NOR, and NOT gates
    - 3 or more fan-in are allowed for your convenience

Supplement Slides (3/3)

- **Circuit wiring diagram**
  - Draw a circuit wiring diagram of below boolean expressions
  - Use TTL chips, maximum
    - Two 7486 (XOR)
    - Two 7408 (AND)
    - Three 7432 (OR)
    - Three 7404 (NOT)

A	$I3 + I1 + \overline{I2 \oplus I0}$
B	$\bar{I}2 + \overline{I1 \oplus I0}$
C	$I2 + \bar{I}1 + I0$
D	$\bar{I}2\bar{I}0 + (I2 \oplus I0) \oplus \bar{I}1 + (I2 \oplus I0)I1$
E	$(\bar{I}2 + I1)\bar{I}0$
F	$I3 + I2 + \bar{I}1\bar{I}0$
G	$I3 + (I2 \oplus I1) + I1\bar{I}0$

7-segment decoder