DON'T MISS THIS UNIQUE OPPORTUNITY >>> **REGISTER NOW!**

The main objective of this workshop is to provide the details of developing efficient embedded systems design using soft core and hard-core processors with Intel SoC FPGAs. The Nios® soft processors are designed specifically for Intel® FPGAs. The soft processor series is suitable for a wide range of embedded computing applications, from digital signal processing (DSP) to system-control. Nios® V processors are the next generation of soft processors for Intel® FPGA based on the open-source RISC-V Instruction Set Architecture. The Nios® II processors are versatile and deliver unprecedented flexibility for cost-sensitive, real-time, safety-critical and applications processing needs. Cyclone® V SoC FPGA has lower total power compared with the previous generation, efficient logic integration capabilities, integrated transceiver variants, and SoC FPGA variants with an ARM*-based hard processor system (HPS). The product family is recommended for Intel Edge-Centric

applications and designs

KEYNOTE SPEAKER

Sourashtra Joined Intel as RCG and is currently structural design lead in Discrete Graphics SoC within GTCHE org. He has been part of Intel for 15 years and played key leadership roles in convergence of several Big Core IPs and complex SoCs across multiple cross-site organizations. His work in the areas of floorplan and layout convergence has translated to significant die-size/cost savings for many designs and SoC's. Mostly recently he is working on Floorplan and SD convergence of Next Gen Discrete Graphics Base die SoC. Sourashtra relishes in working with different verticals like Floorplan/Layout/Timing and SD convergence/Signoff and Tape-in activities.

Sourashtra is regarded as the Discrete Graphics expert in the area of floorplan/physical integration aspects of die-disaggregation. Sourashtra holds a MS Degree in Electrical Engineering from Wright State University, Ohio

TRAINER

Padmanaban is the Software Enabling and Optimization Engineer in Customer Experience Group at Intel PSG. He has a post graduate degree in Applied Electronics from Anna University, Chennai and Bachelors in EEE from GCT, Coimbatore. He has 16+ years of experience in digital design for both FPGA and ASIC. Prior to joining Intel, he worked as a Chief Faculty in Sandeepani School of VLSI design (Training division of CoreEL Technologies, Bangalore) for 8 years and as an Assistant Professor and Project Coordinator in Ramaiah University of Applied sciences (RUAS) Bangalore for 5 years.

The workshop is **exclusively for students and faculty of institutions that are part of the Intel® Unnati Community**, who are **from the CS, IT and EC streams**, and have a **basic understanding/ knowledge of Digital Logic Design, Verilog/VHDL Programming, and C/C++.**

If you qualify, **all you need to do is Register Now. Please ensure that you give your full name and College ID at the time of registration.** You will receive a join-in link one day before the session. You can join the session by using the Email ID that you register with at 9:30 am IST on May 24, 2023.

At the end of the training, you will be able to:

- Develop efficient embedded system design using Intel FPGAs and SoC FPGAs
- Explore the features and applications of Intel NIOS II and NIOS V Soft-Core Processor.
- Learn to use the Platform Designer system integration tool to develop & configure Nios II processor-based hardware systems.

You will also receive a Participation Certificate from Intel using your full name as given at the time of Registration.

Essential Software

- **Participants need to install Intel® Quartus® Prime – Lite Edition (18.0 or 18.1 on software on their respective computers before the training**.

  It is available for download **here**.

Here are a few tips for you to get the most out of the session:

- Please make sure that you've got the time blocked in your calendar.
- Once you join the session, please make sure that you mute your microphone.
- Please submit your questions to the Presenter(s) by using the **"Ask a Question"** button.

We look forward to seeing you during the session.

Intel Unnati Team