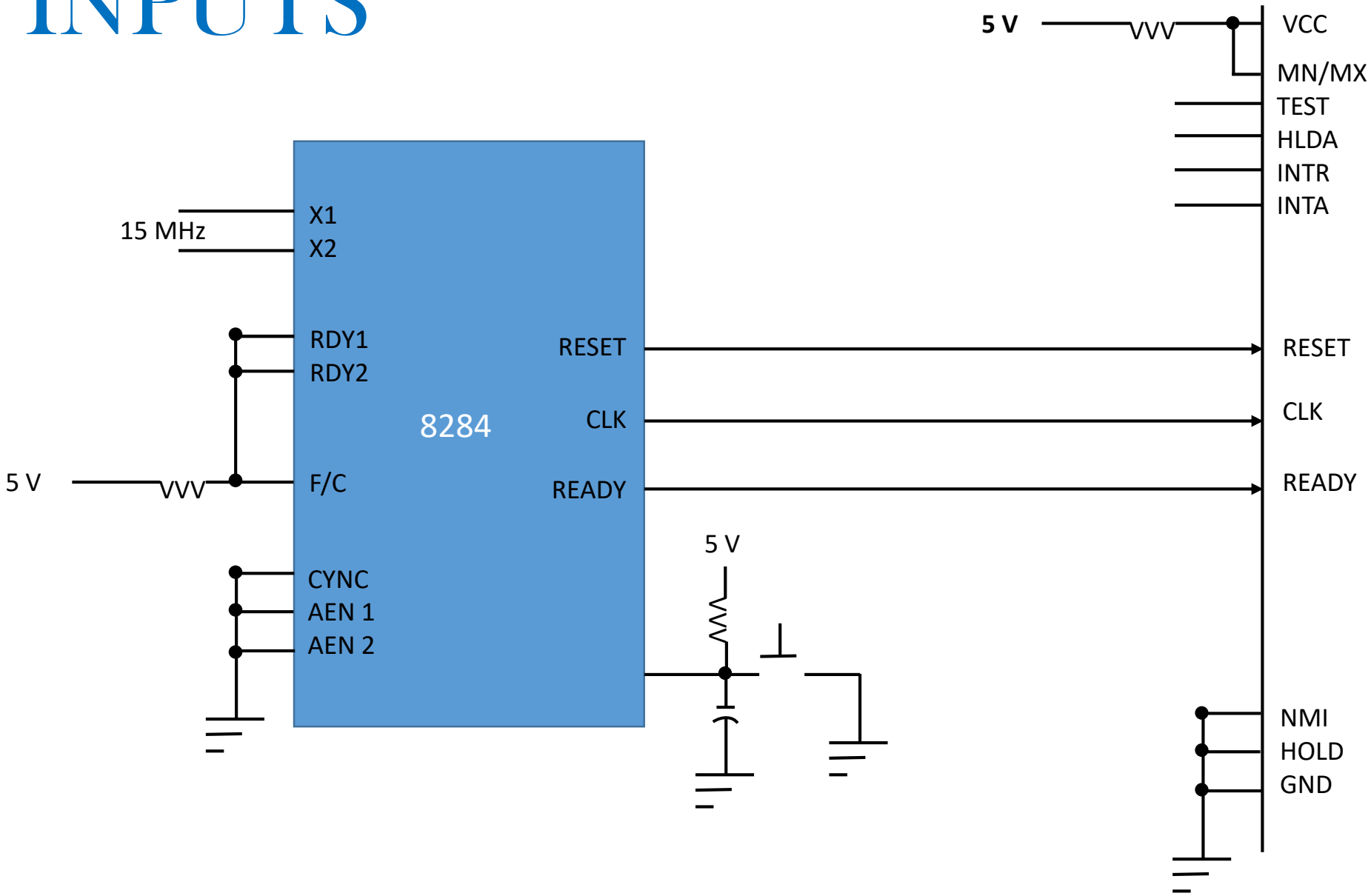
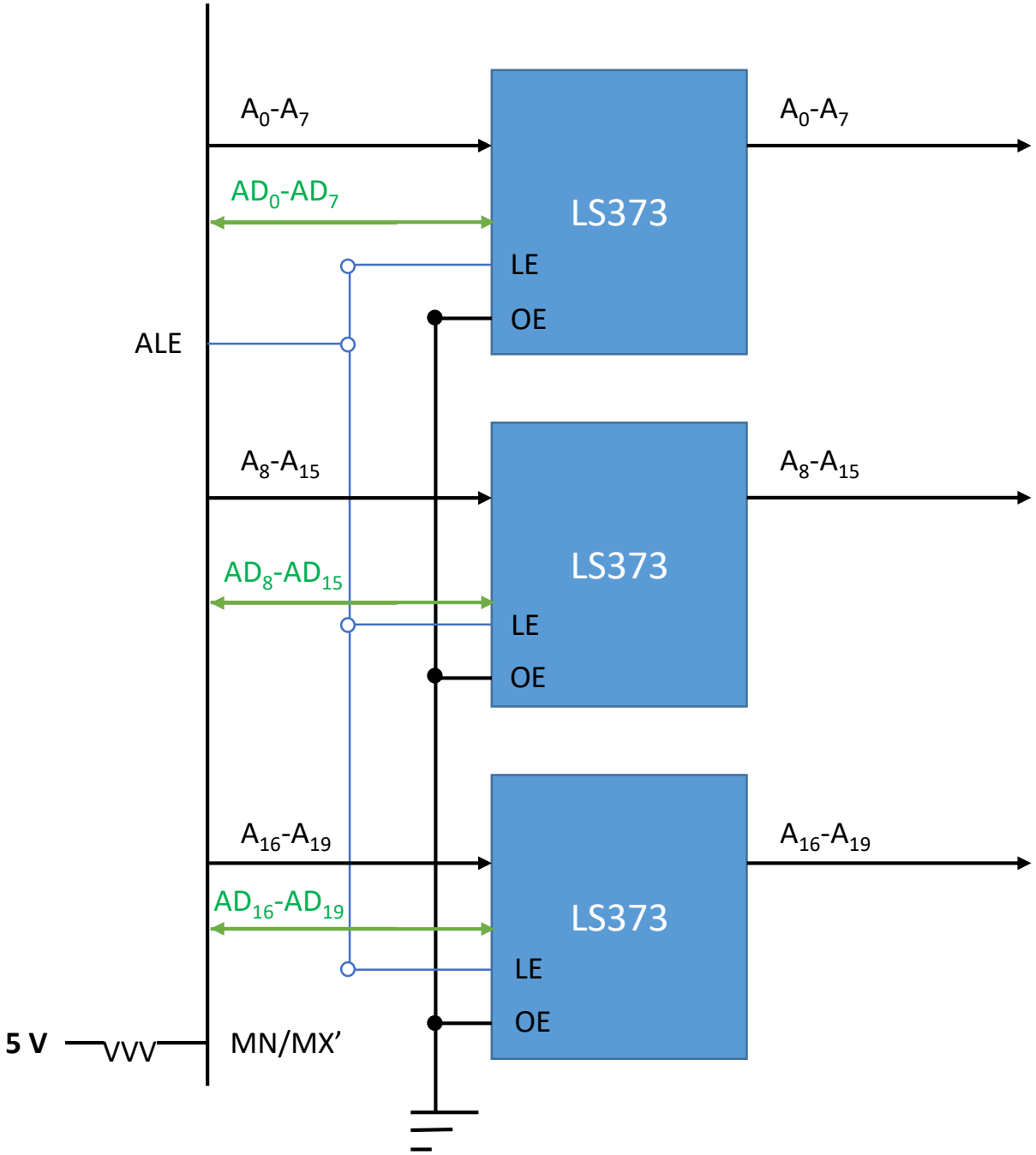
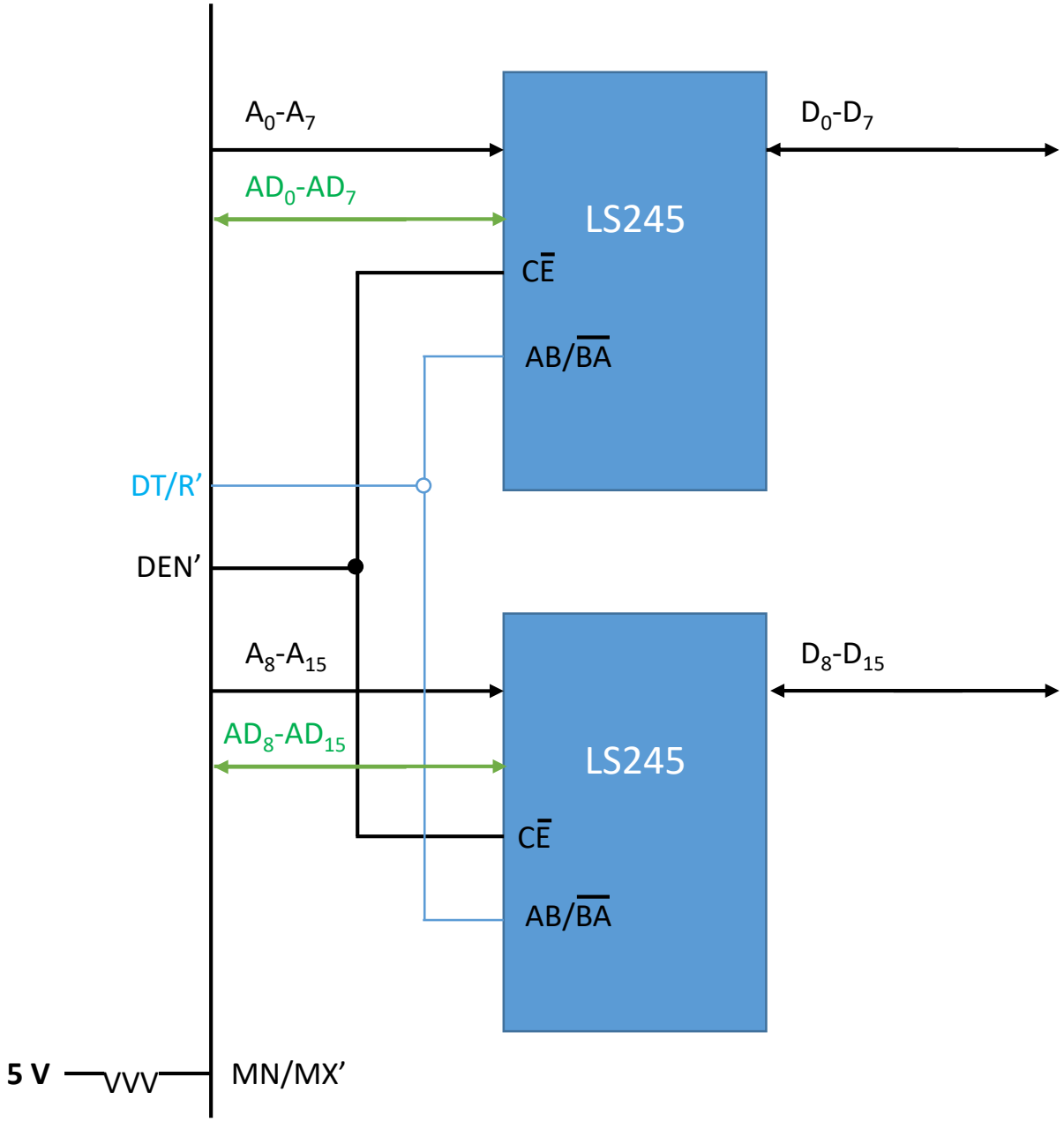
8086 INPUTS

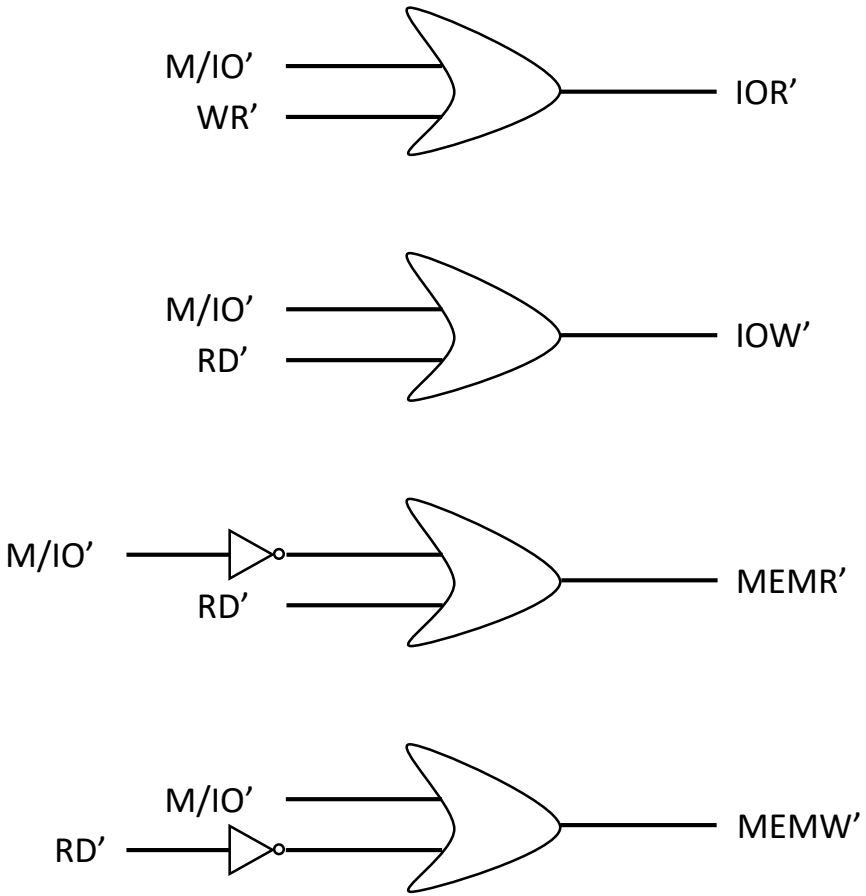

5 V
VCC
MN/MX
TEST
HLDA
INTR
INTA
15 MHz
X1
X2
RDY1
RDY2
8284
RESET
CLK
READY
5 V
F/C
CYNC
AEN 1
AEN 2
5 V
RESET
CLK
READY
NMI
HOLD
GND

SYSTEM BUS OF 8086 (ADDRESS)



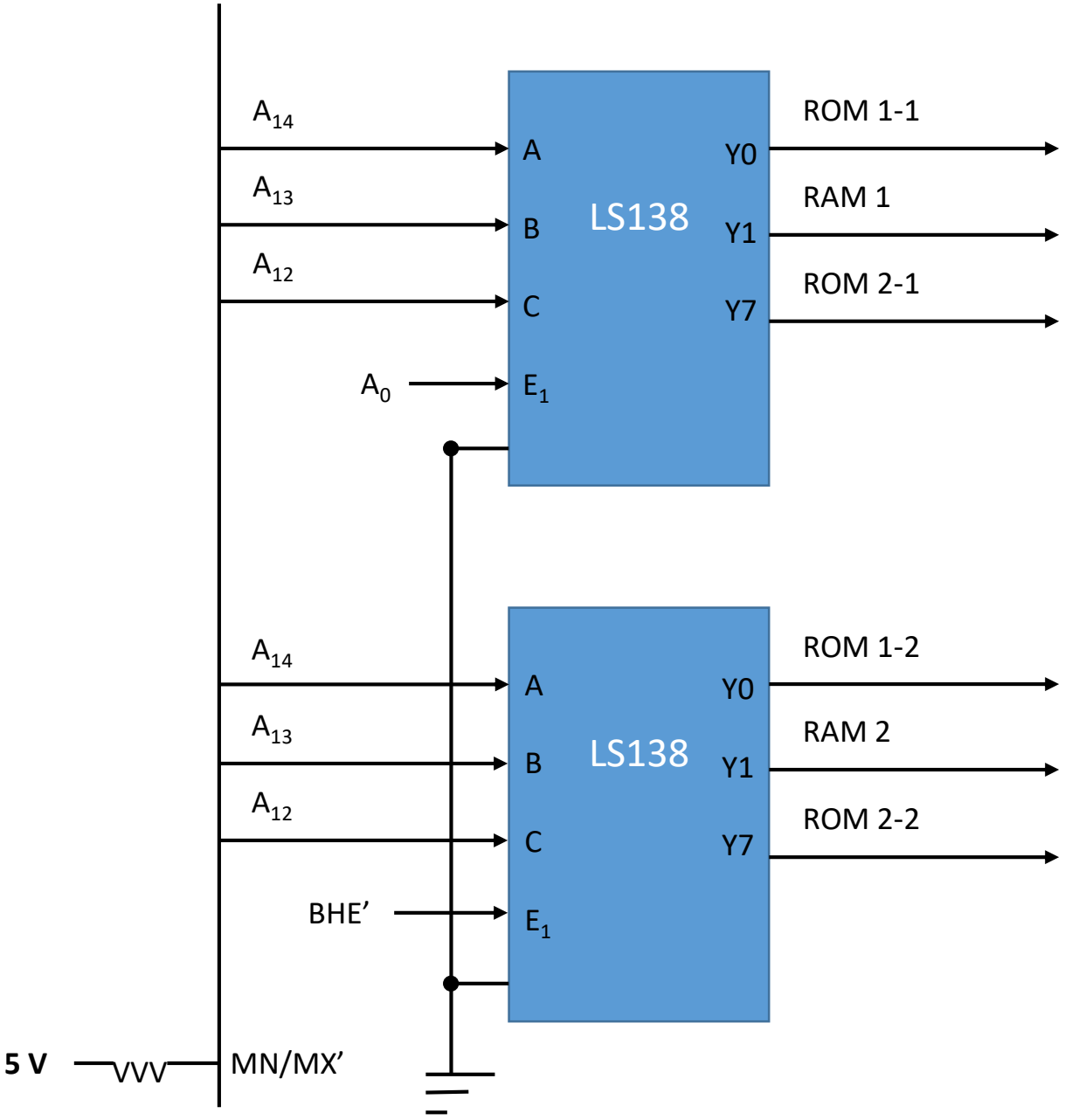
SYSTEM BUS OF 8086 (DATA+CONTROL)



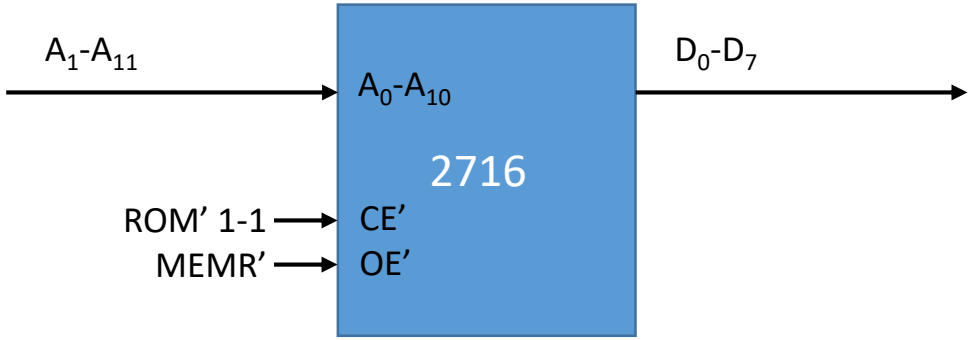


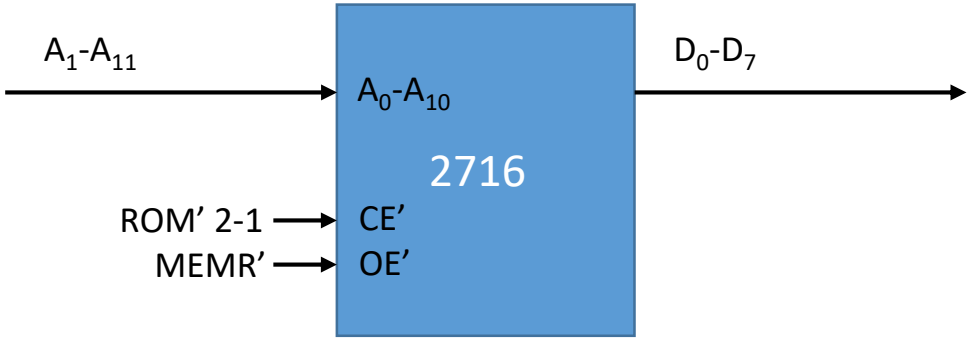
M/IO’	RD’	WR’	BUS CYCLE
1	0	1	MEMR’
1	1	0	MEMW’
0	0	1	IOR’
0	1	0	IOW’

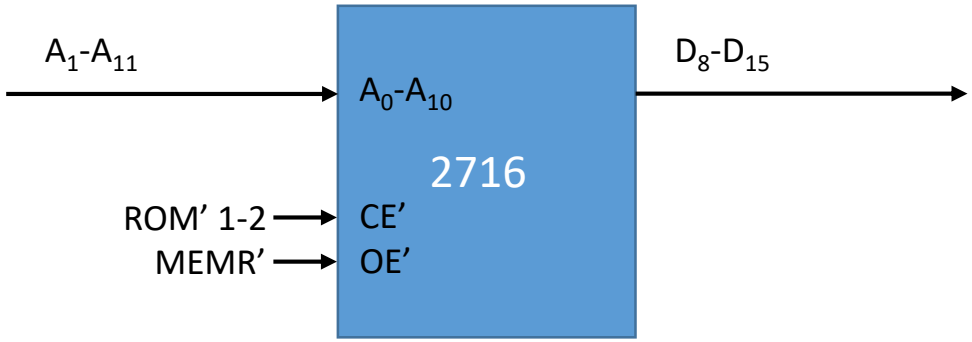
MEMORY DECODER

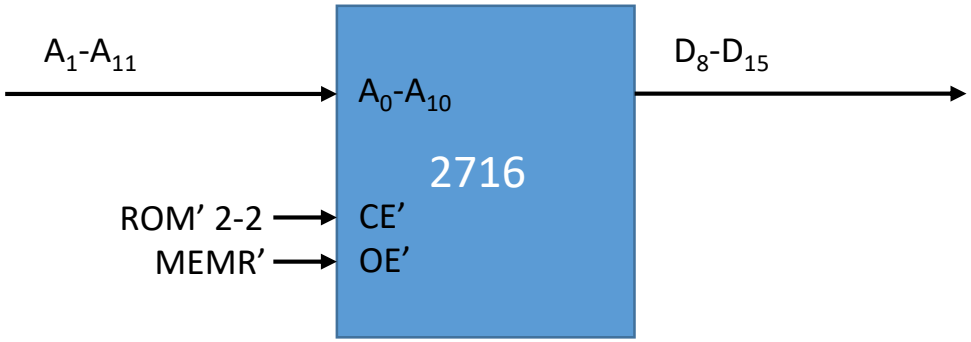


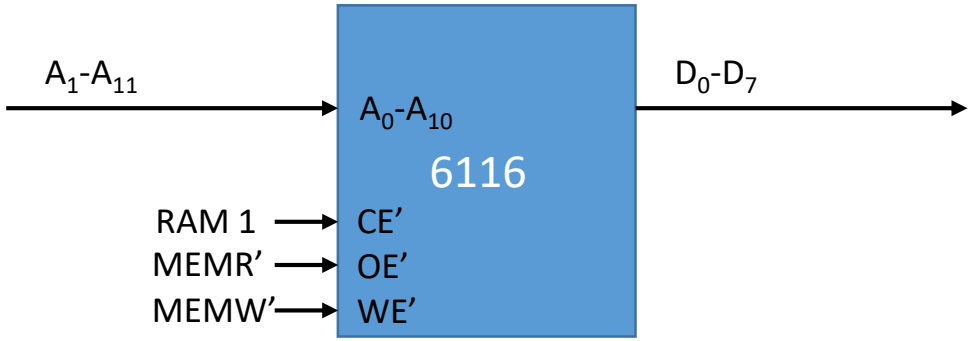
MEMORY INTERFACING

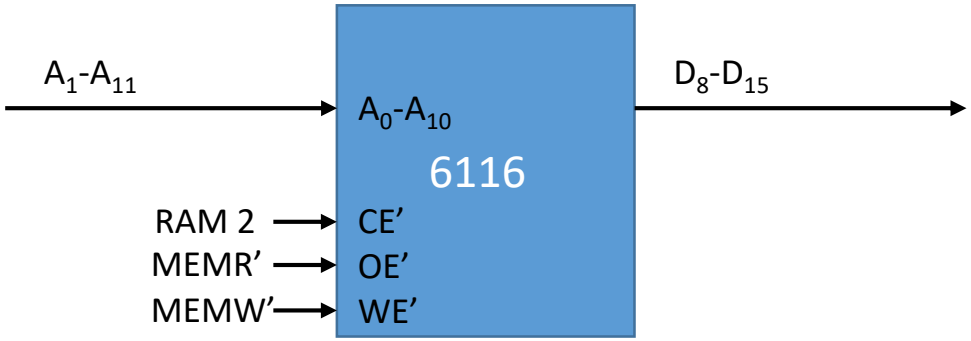




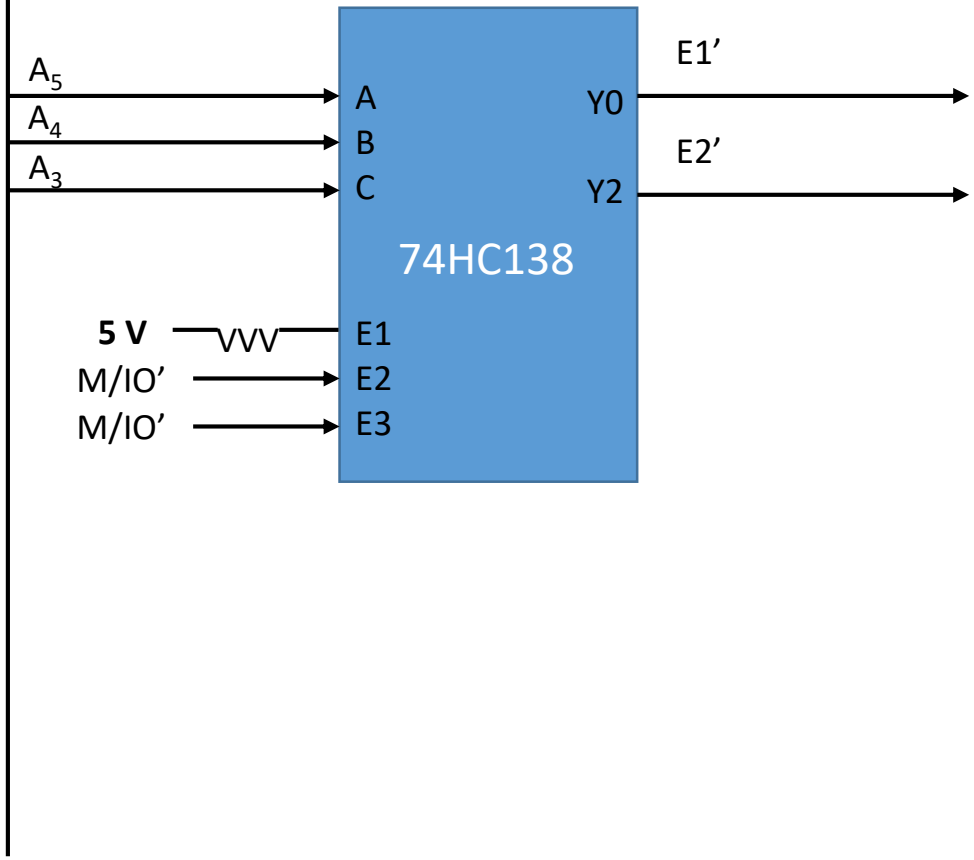




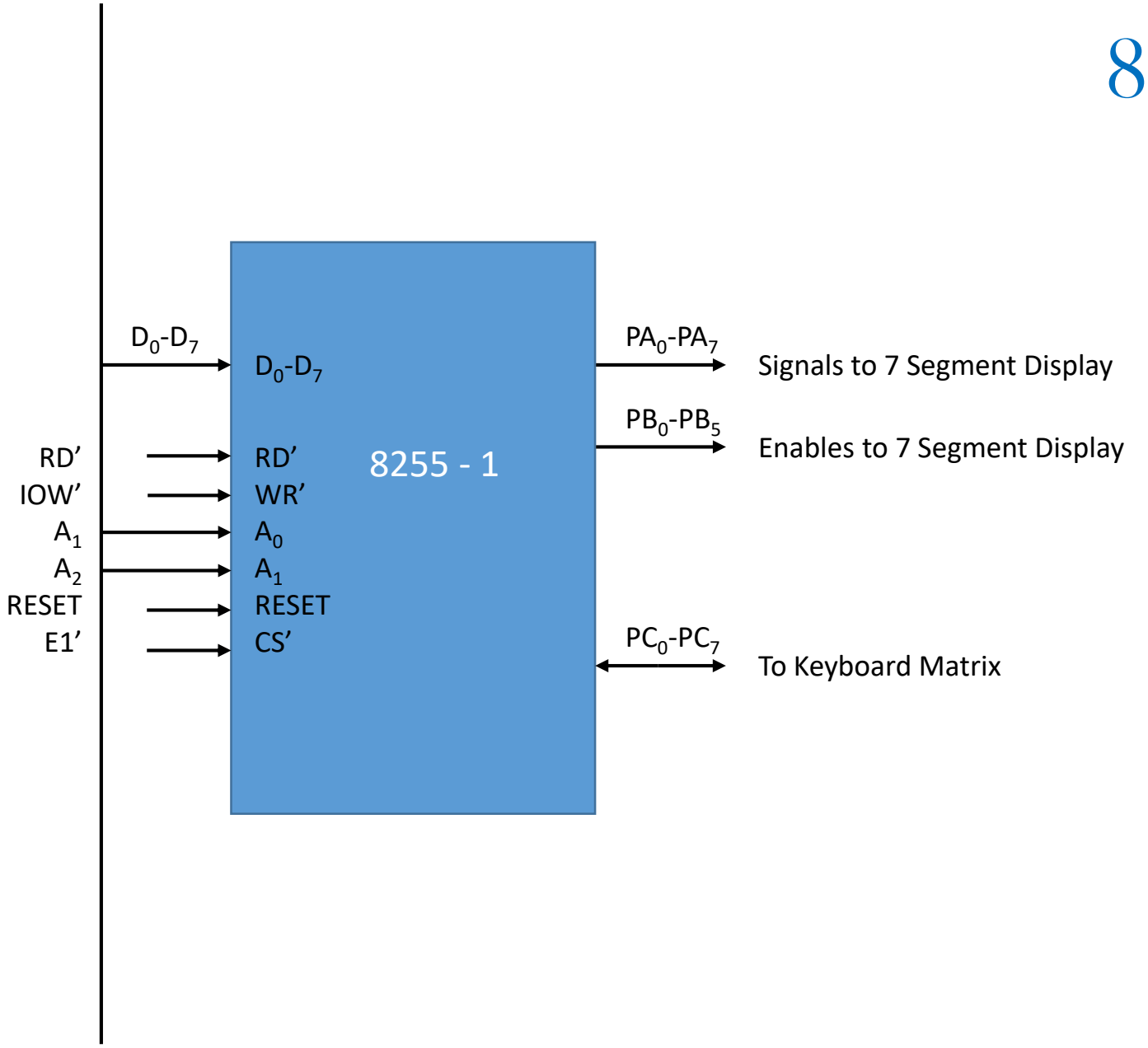




I/O DECODER

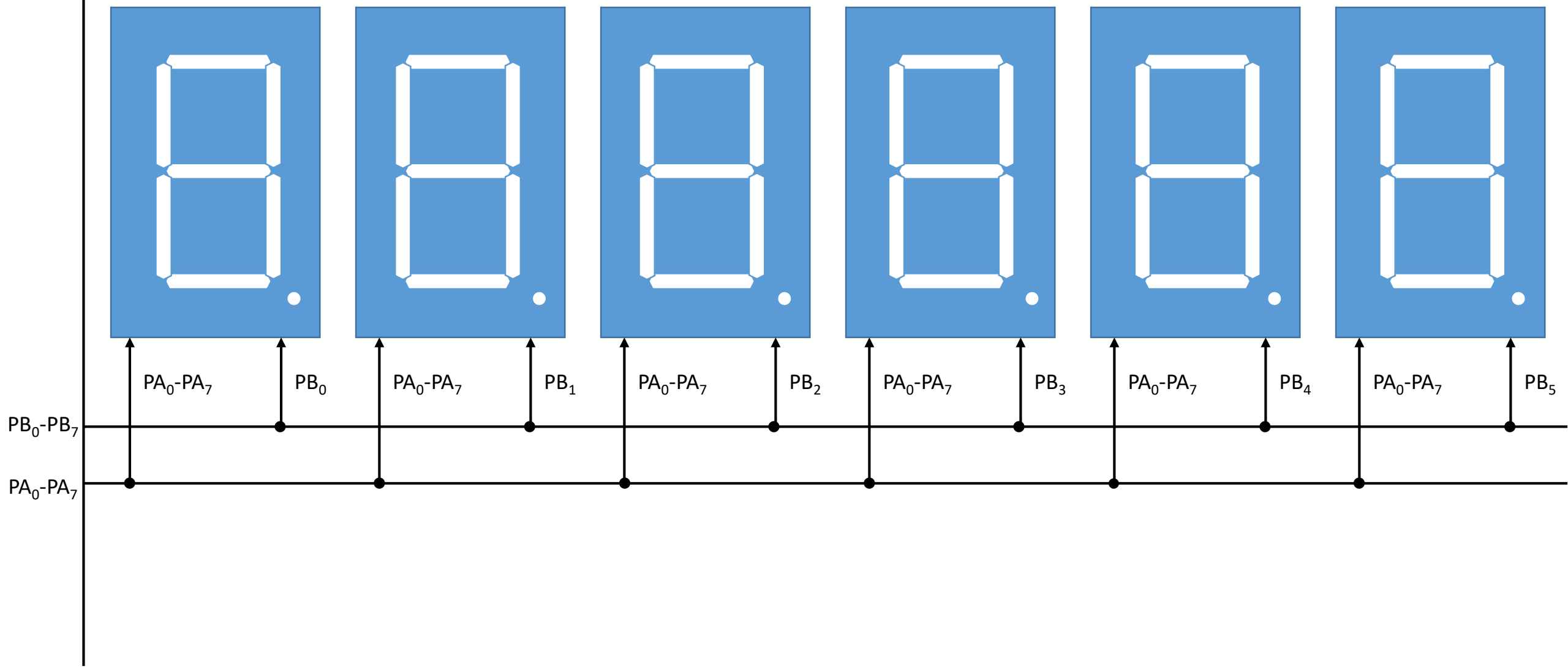


8255 INTERFACE TO THE PROCESSOR



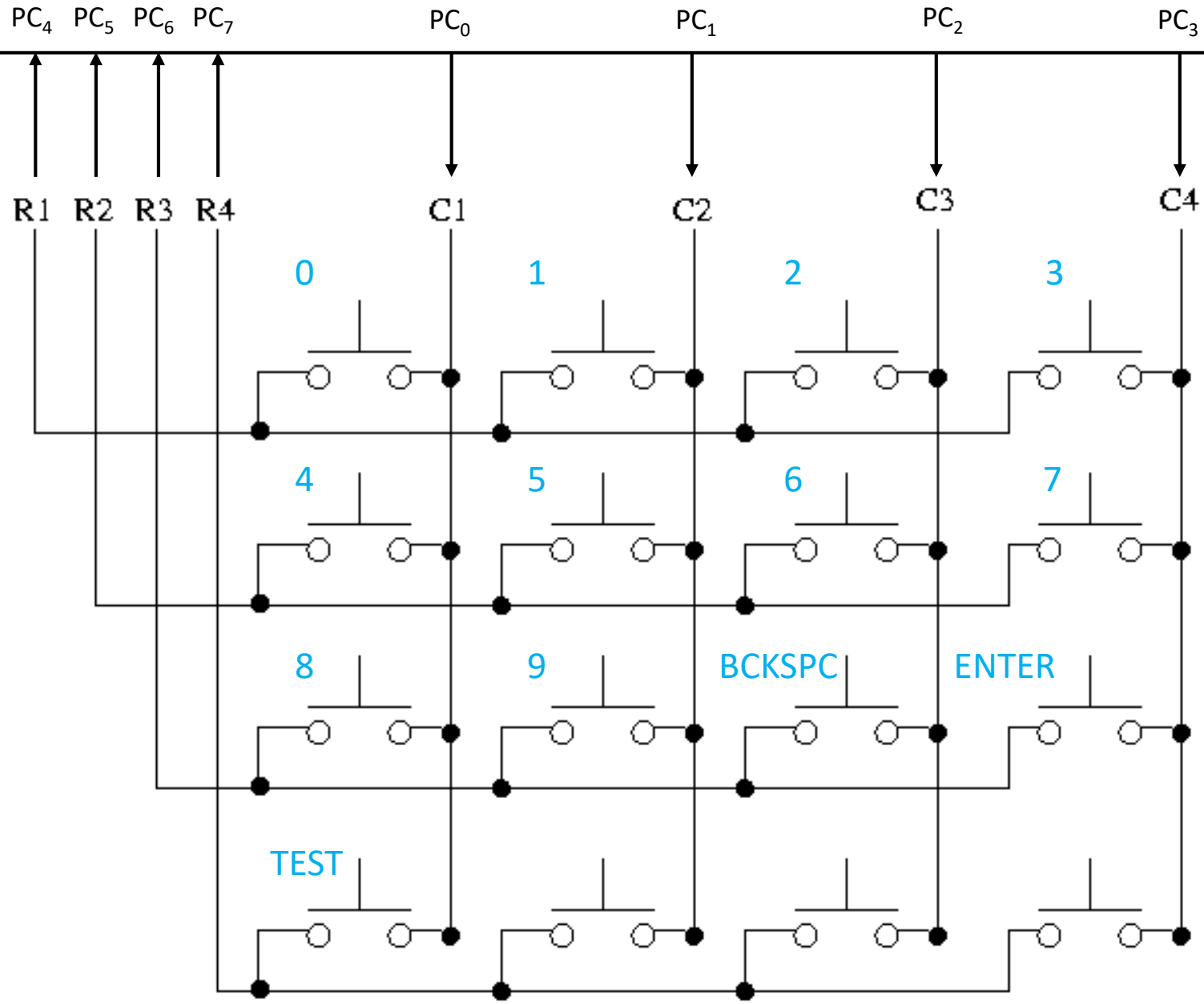
8255-1

INTERFACE TO I/O DEVICES

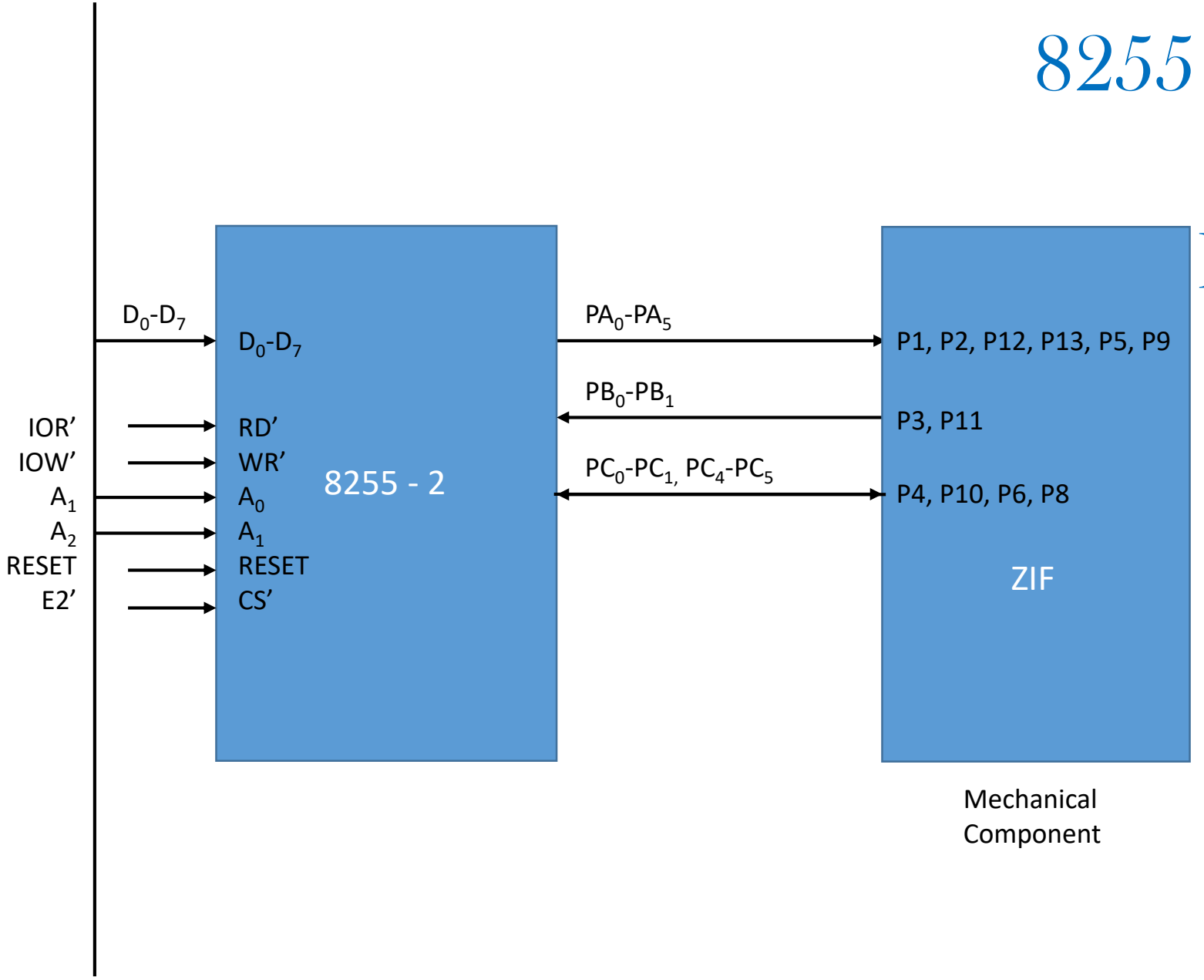


8255-1

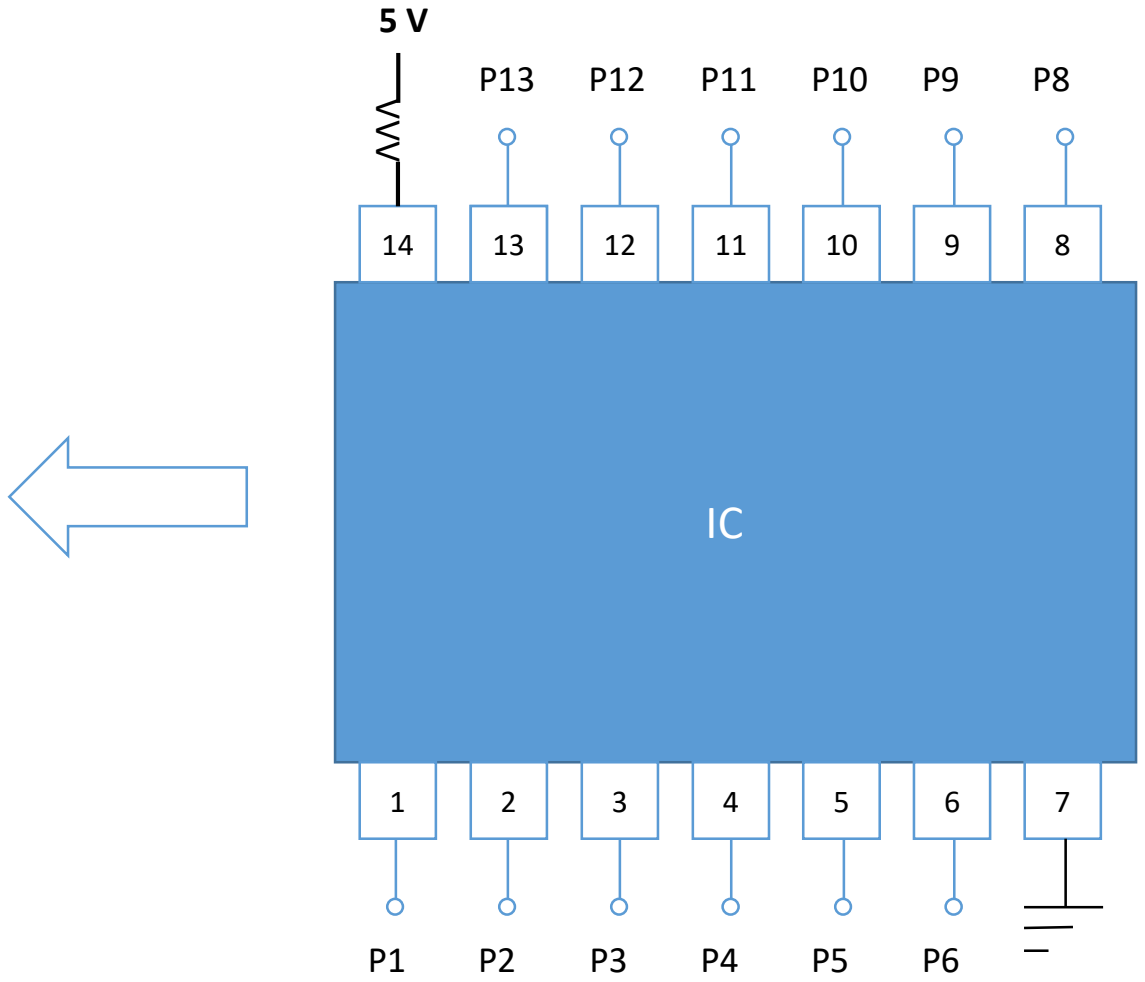
INTERFACE TO I/O DEVICES



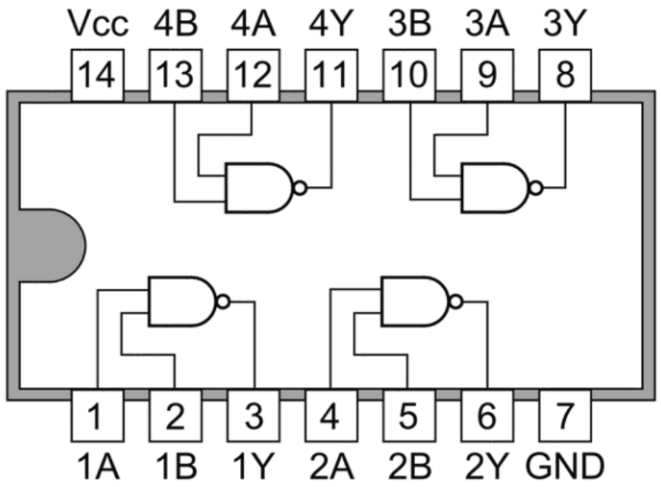
8255 INTERFACE TO THE PROCESSOR

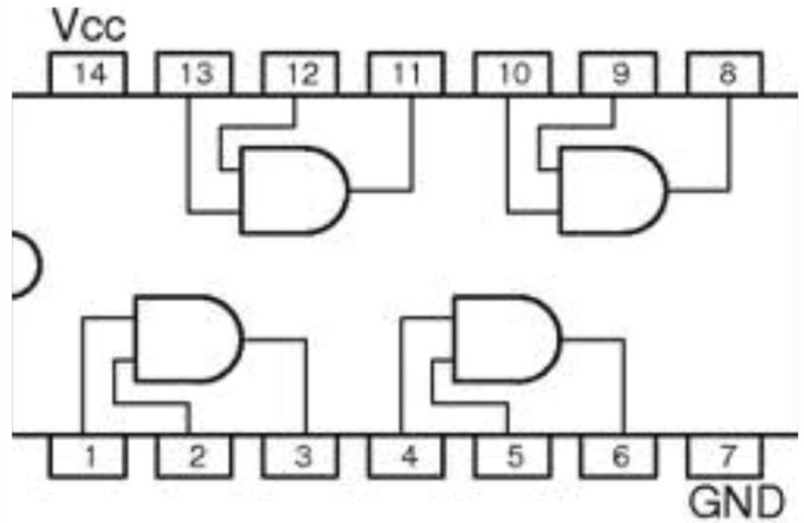


Connected
To ZIF

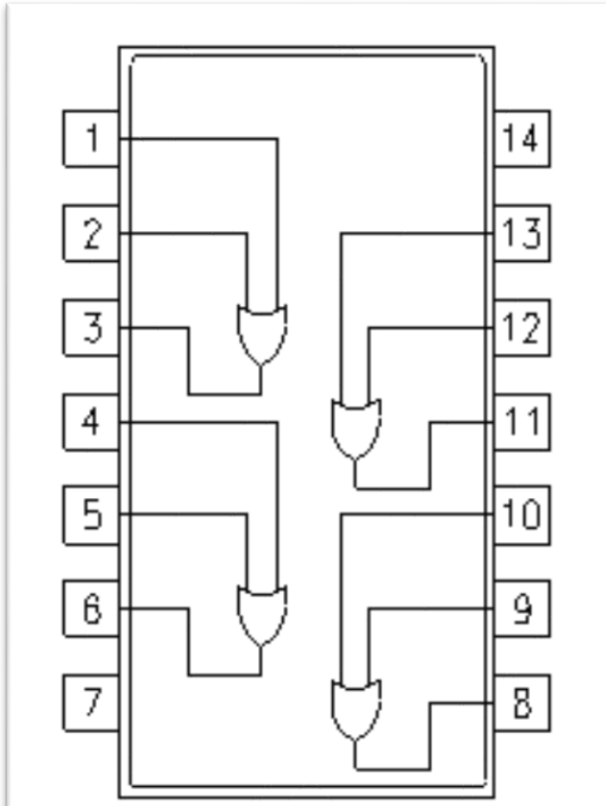


7400 Quad 2-input NAND Gates

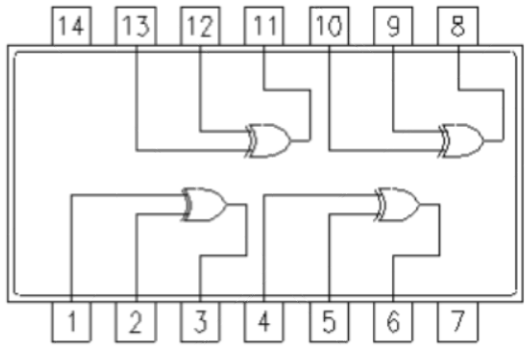




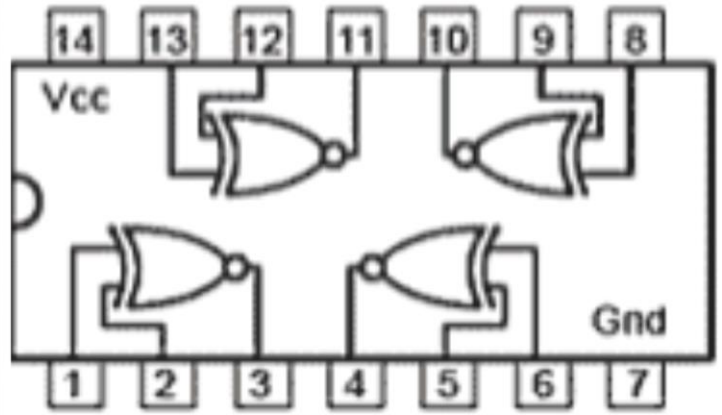
7408 Quad 2 Input AND



7432
Quad 2-Input
OR Gate



7486
Quad 2-Input
Exclusive - OR Gate



747266 Quad 2 input
XNOR Gates