ECE/EEE/ENI F241
MICROPROCESSORS AND INTERFACING

DESIGN ASSIGNMENT
IC TESTER

Prepared by members of Group :

1. Harsh Dabhade	2019B5A30196G
2. Jinan Ahmed Sarmadi	2019B2A31070G
3. Tushar Sharma	2019B2AA1065G
4. Sayan Samanta	2019B2A81088G
5. Shubham Chandra	2019B2AA1111G
6. Uday Sehgal	2019B2AA1089G

Submitted to :

Prof K. R. Anupama
Department of EEE

Project submitted in partial fulfillment of the requirements for the course
Microprocessors and Interfacing

(BITS Pilani K. K. Birla Goa Campus, Goa - 403726)

Contents

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User Requirements & Technical Specifications

Design a Microprocessor based Tester to test the logical functioning of the following chips:

1. 7400
2. 7408
3. 7432
4. 7486
5. 747266

The IC to be tested will be inserted in a 14 pin ZIF socket. The IC number is to be entered via a keyboard.

The keyboard has keys 0-9, backspace, enter and test.

The user places the IC in the ZIF socket, closes it – then enters the IC No, followed by the enter key.

The IC No. is displayed on the 7-segment display.

The testing will start once the user presses the test key.

After Test the result PASS/FAIL must be displayed on the 7-segment display.

After testing is complete, PASS/FAIL will be displayed for approximately 5s and then the display will be reset. During this time no input will be taken. After the reset, the user can give another input.

Assumptions

- Memory is able to provide data at the speed at which the processor is reading.
- Only IC numbers that are given in the problem statement are considered as valid IC numbers.
- Test key will only be pressed after the Enter key has been pressed.
- If Test Key is pressed before Enter Key, the 7 - segment LED will display ‘FAIL’.
- If the user presses Enter Key after giving invalid IC number as input, the 7 - segment LED will display ‘FAIL’.
- After attaching the IC into the ZIF socket, the user closes it and then types the IC number using the hex keypad.
- The ALP has been made assuming there is no debounce when a key is pressed in Proteus.
- Two or more keys cannot be pressed simultaneously and if pressed it will be ignored.
- The first input cannot be Backspace, Enter or Test key. It Must be a digit.
- The User cannot give inputs while PASS/FAIL is being displayed.

Components used with justification wherever required

- 8086 Microprocessor – 1 No
- 8255-A (Programmable Peripheral Interface with 24 1/0 lines) 2 Nos; to interface keyboard, display, and the IC.
- 74HC138 (3:8 Decoder) - 3 Nos
- 74HC245 (Octal BUS transceivers with tri-state output) - 2 Nos
- 74HC373 (Octal D-Type transparent latches with tri-state outputs) - 3 Nos
- 7SEG-MPX1-CA (7-Segment Anode Display) - 6 Nos
- 6116 (16K <2Kx8> Static RAM)- 2 Nos; smallest size available, required for temporary storage of data.
- 2716 (16K <2Kx8> EPROM)- 4 Nos; ROM is required at reset address i.e., FF000H and 00000H where there is the IVT.
- BUTTON (SPST Push Button)- 16 Nos

- SW-SPDT-MOM (interactive SPDT Switch with Momentary Action)
- 7400 (Quadruple 2-input positive NAND gates)
- 7408 (Quadruple 2-input positive AND gates)
- 7432 (Quadruple 2-input positive OR gates)
- 7486 (Quadruple 2-input exclusive OR gates)
- 747266 (Quadruple 2-input exclusive NOR gates)
- Simple 2-Input OR gate 4 Nos
- Simple digital Inverter - 2 Nos
- 8284 (Clock generator chip implemented in proteus using the internal clock of 8086)
- ZIF Socket (Designed using 'Default' Terminals in Proteus)

Address Map

Memory Map

00000 - 00FFF - ROM1
01000 - 01FFF - RAM 1
FF000 - FFFFF - ROM2

	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
ROM 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
RAM 1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
ROM 2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

A_{12}, A_{13} and A_{14} address lines are passed into 74HS138 (3:8 decoder) in order to select the required segment of memory, i.e., ROM_1 , RAM or ROM_2.

I/O Map

1st 8255 for 7 - segment display and hex keyboard :
00h - Port 1A
02h - Port 1B
04h - Port 1C
06h - Control register 1

A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0
0	0	0	0	0	1	0	0

2nd 8255 for interfacing with ZIF socket :
10h - Port 2A
12h - Port 2B
14h - Port 2C
16h - Control register 2

A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	1	0	0	0	0
0	0	0	1	0	0	1	0
0	0	0	1	0	1	0	0

The Port Allocation is done as follows:

1.8255A-1:

a. Port A-8 pins as outputs from the 8255, which are the inputs to the 7-segment display.

b. Port B-6 pins as outputs from the 8255, which are the enables to each 7-segment display.

c. Port C -

1. Lower: 4 pins as outputs from 8255; inputs to the keyboard.

2. Upper: 4 pins as inputs to 8255; outputs from the keyboard.

2.8255A-2:

a. Port A-6 pins as outputs from the 8255, which are inputs to the ZIF socket pins: P1, P2, P12, P13, P5 and P9.

b. Port B-2 pins as inputs to the 8255, which are outputs from the ZIF socket pins: P3 and P11.

c. Port C

Port C-lower-2 pins: P4 and P10. Port C-upper-2 pins: P6 and P8.

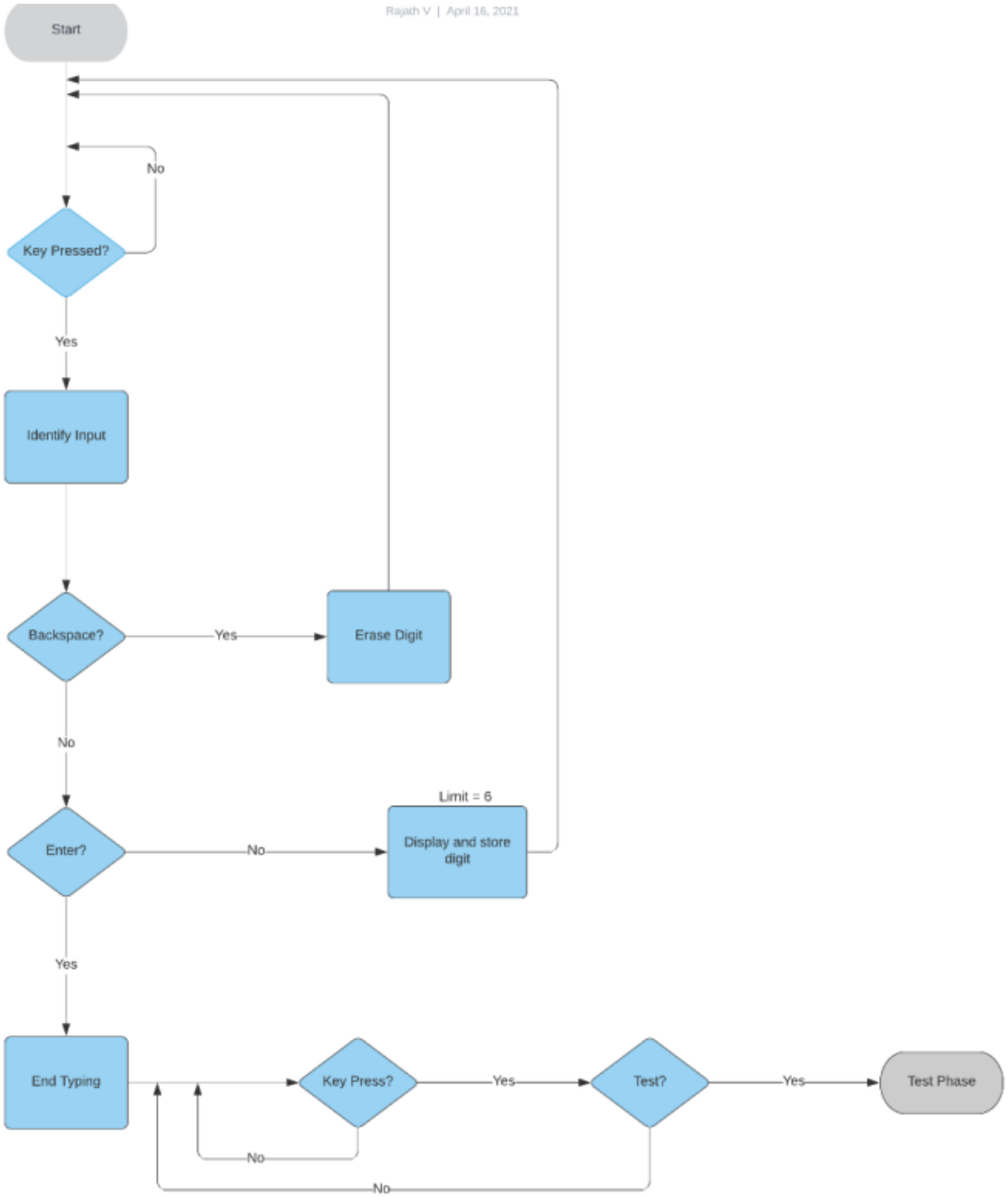
NOTE: The 5 ICs in the database are 7400, 7408, 7432, 7486, and 747266. We can group 7400, 7408, 7432, 7486 into group 1 and 747266 as group 2. As we can see, for group 1, P1, P2, P4, P5, P9, P10, P12, P13 act as input terminals (output from 8255-2), and P3, P6, P8 and P11 act as output terminals (input to 8255-2). But in group 2 the difference comes in P4, P10 & P6, P8. The former act as output terminals (input to 8255-2) whereas the latter act as input terminals (output from 8255-2). Due to this P1, P2, P12, P13, P5 and P9 have been always connected to Port-A (Output from 8255-2) and P3, and P11 have been always connected to Port-B (Input to 8255-2). Port-C has the property of having its upper and lower ports programmed separately, therefore P4, P10 have been connected to lower half of Port-C and P6, PB have been connected to upper half of Port-C. These 2 halves of Port-C switch between input/output ports depending on the IC that needs to be tested.

Design

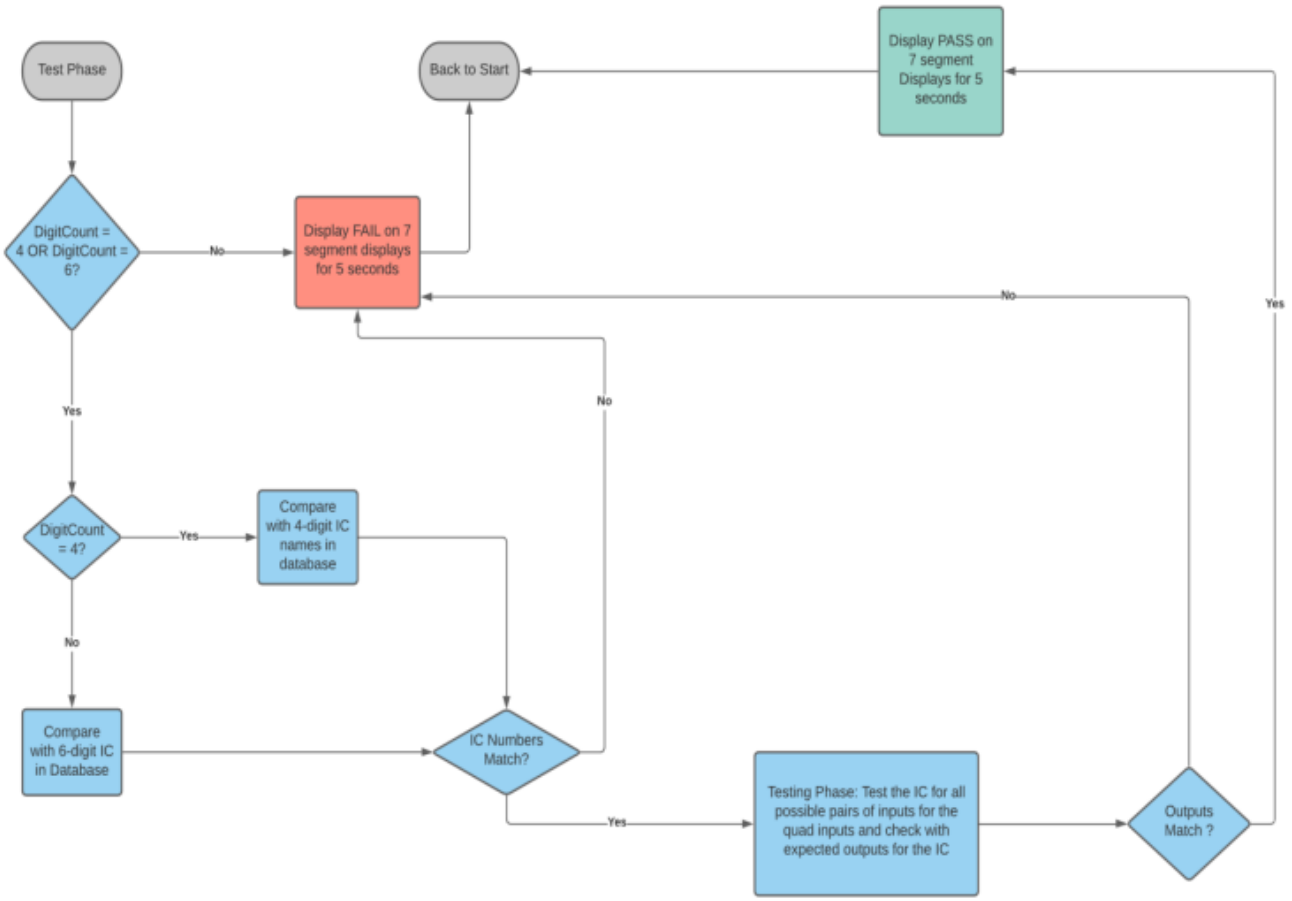
Complete design shown with proper labelling(G40_ICTESTER_DESIGN.pdf attached).

Flow Chart

Input and Display



IC Testing



Variations in Proteus Implementation with Justification

- 4077 (quad 2 input XNOR chip) has been used in place of 747266 due it being unavailable in Proteus.
- Since ZIF is a mechanical component, it's not available on Proteus. Thus, it has been designed using the 'Default' Terminals.
- 2732 is used instead of 2716 as the latter does not work on Proteus.

Firmware

- Implemented using emu8086 attached.

List of Attachments

1. Complete Hardware Real World Design – ICTESTER_DESIGN.pdf
2. Manuals
    a. ZIF 14 Pin Socket: ZIF_14_PIN.pdf
    b. 7400_NAND.pdf
    c. 7408_AND.pdf
    d. 7432_OR.pdf
    e. 7486_XOR.pdf
    f. 747266_XNOR.pdf
3. Proteus File – IC_TESTER.dsn
    a. 7400_NAND.dsn
    b. 7408_AND.dsn
    c. 7432_OR.dsn
    d. 7486_XOR.dsn
    e. 747266_XNOR.dsn
4. EMU8086 ASM File – IC_TESTER.asm
5. Binary File after assembly – IC_TESTER.bin

Note: Since the IC-Tester needs to test 5 ICS and each .dsn file tests one IC, we have included the .dsn files for all 5 designs as part of our submission for the proteus implementation.