Multiple Choice Questions and Answers on VLSI Design & Technology

1) The utilization of CAD tools for drawing timing waveform diagram and transforming it into a network of logic gates is known as _____.

a. Waveform Editor

b. Waveform Estimator

c. Waveform Simulator

d. Waveform Evaluator

ANSWER: Waveform Editor

2) Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?

a. Simulation

b. Optimization

c. Synthesis

d. Verification

ANSWER: Synthesis

3) _____ is the fundamental architecture block or element of a target PLD.

a. System Partitioning

b. Pre-layout Simulation

c. Logic cell

d. Post-layout Simulation

ANSWER: Logic cell

4) In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?

a. Floorplanning

b. Placement & Routing

c. Testing

d. Extraction

ANSWER: Extraction

5) Among the VHDL features, which language statements are executed at the same time in

parallel flow?

a. Concurrent

b. Sequential

c. Net-list

d. Test-bench

ANSWER: Concurrent

6) In Net-list language, the net-list is generated _____synthesizing VHDL code.

a. Before

b. At the time of (during)

c. After

d. None of the above

ANSWER: After

7) In VHDL, which object/s is/are used to connect entities together for the model formation?

a. Constant

b. Variable

c. Signal

d. All of the above

ANSWER: Signal

8) Which data type in VHDL is non synthesizable & allows the designer to model the objects of dynamic nature?

a. Scalar

b. Access

c. Composite

d. File

ANSWER: Access

9) Which type of simulation mode is used to check the timing performance of a design?

a. Behavioural

b. Switch-level

c. Transistor-level

d. Gate-level

ANSWER: Gate-level

10) In the simulation process, which step specifies the conversion of VHDL intermediate code so that it can be used by the simulator?

a. Compilation

b. Elaboration

c. Initialization

d. Execution

ANSWER: Elaboration

11) Which type of simulator/s neglect/s the intra-cycle state transitions by checking the status of target signals periodically irrespective of any events?

a. Event-driven Simulator

b. Cycle-based Simulator

c. Both a and b

d. None of the above

ANSWER: Cycle-based Simulator

12) Which among the following is not a characteristic of 'Event-driven Simulator'?

a. Identification of timing violations

b. Storage of state values & time information

c. Time delay calculation

d. No event scheduling

ANSWER: No event scheduling

13) Which among the following is an output generated by synthesis process?

a. Attributes & Library

b. RTL VHDL description

c. Circuit constraints

d. Gate-level net list

ANSWER: Gate-level net list

14) Register transfer level description specifies all of the registers in a design & _____ logic between them.

a. Sequential

b. Combinational

c. Both a and b

d. None of the above

ANSWER: Combinational

15) In synthesis process, the load attribute specify/ies the existing amount of _____load on a particular output signal.

a. Inductive

b. Resistive

c. Capacitive

d. All of the above

16) Which attribute in synthesis process specify/ies the resistance by controlling the quantity of current it can source?

a. Load attribute

b. Drive attribute

c. Arrival time attribute

d. All of the above

ANSWER: Drive attribute

17) Which type of digital systems exhibit the necessity for the existence of at least one feedback path from output to input?

a. Combinational System

b. Sequential system

c. Both a and b

d. None of the above

ANSWER: Sequential system

18) The output of sequential circuit is regarded as a function of time sequence of _____.

A. Inputs

B. Outputs

C. Internal States

D. External States

a. A & D

b. A & C

c. B & D

d. B & C

ANSWER: A & C

19) The time required for an input data to settle _____ the triggering edge of clock is known as ‘Setup Time’.

a. Before

b. During

c. After

d. All of the above

ANSWER: Before

20) Hold time is defined as the time required for the data to _____ after the triggering edge of clock.

a. Increase

b. Decrease

c. Remain stable

d. All of the above

ANSWER: Remain stable

21) An Antifuse programming technology is predominantly associated with _____.

a. SPLDs

b. FPGAs

c. CPLDs

d. All of the above

ANSWER: FPGAs

22) In fusible link technologies, the undesired fuses are removed by the pulse application of _____voltage & current to device input.

a. Low

b. Moderate

c. High

d. All of the above

ANSWER: High

23) Which programming technology/ies is/are predominantly associated with SPLDs and CPLDs?

a. EPROM

b. EEPROM

c. FLASH

d. All of the above

ANSWER: All of the above

24) Before the commencement of design, the clocking strategy determine/s _____

a. Number of clock signals necessary for routing throughout the chip

b. Number of transistors used per storage requirement

c. Power dissipated by chip & the size of chip

d. All of the above

ANSWER: All of the above

25) Which method/s of physical clocking is/are a /the recursive structure where the memory elements are grouped together to make the use of nearby or same distribution points?

a. H tree

b. Balanced tree clock network

c. Both a and b

d. None of the above

ANSWER: H tree

26) Increase in the physical distance of H-tree _____the skew rate.

a. Increases

b. Stabilizes

c. Decreases

d. All of the above

ANSWER: Increases

27) Which type of MOSFET exhibits no current at zero gate voltage?

a. Depletion MOSFET

b. Enhancement MOSFET

c. Both a and b

d. None of the above

ANSWER: Enhancement MOSFET

28) In enhancement MOSFET, the magnitude of output current _____ due to an increase in the magnitude of gate potentials.

a. Increases

b. Remains constant

c. Decreases

d. None of the above

ANSWER: Increases

29) In DIBL, which among the following is/are regarded as the source/s of leakage?

a. Subthreshold conduction

b. Gate leakage

c. Junction leakage

d. All of the above

ANSWER: All of the above

30) Which among the following can be regarded as an/the application/s of MOS switch in an IC design?

a. Multiplexing & Modulation

b. Transmission gate in digital circuits

c. Simulation of a resistor

d. All of the above

ANSWER: All of the above

31) In MOS switch, clock feedthrough effect is also known as _____.

A. charge injection

B. charge feedthrough

C. charge carrier

D. charge ejaculation

a. A & B

b. B & C

c. C & D

d. B & D

ANSWER: A & B

32) Which among the following is/are regarded as an/the active resistor/s?

a. MOS diode

b. MOS transistor

c. MOS switch

d. All of the above

ANSWER: MOS diode

33) In testability, which terminology is used to represent or indicate the formal evidences of correctness?

a. Validation

b. Verification

c. Simulation

d. Integration

ANSWER: Verification

34) Which among the following is regarded as an electrical fault?

a. Excessive steady-state currents

b. Delay faults

c. Bridging faults

d. Logical stuck-at-0 or stuck-at-1

ANSWER: Excessive steady-state currents

35) Which among the following faults occur/s due to physical defects?

a. Process variations & abnormalities

b. Defects in silicon substrate

c. Photolithographic defects

d. All of the above

ANSWER: All of the above

36) In logic synthesis, _____ is an EDIF that gives the description of logic cells & their interconnections.

a. Netlist

b. Checklist

c. Shitlist

d. Dualist

ANSWER: Netlist

37) Which level of system implementation includes the specific function oriented registers, counters & multiplexers?

a. Module level

b. Logical level

c. Physical level

d. All of the above

ANSWER: Module level

38) Which among the following is/are taken into account for post-layout simulation?

a. Interconnect delays

b. Propagation delays

c. Logic cells

d. All of the above

ANSWER: All of the above

39) Which among the following operation/s is/are executed in physical design or layout synthesis stage?

a. Placement of logic functions in optimized circuit in target chip

b. Interconnection of components in the chip

c. Both a and b

d. None of the above

ANSWER: Both a and b

40) In VHDL, which class of scalar data type represents the values necessary for a specific operation?

a. Integer types

b. Real types

c. Physical types

d. Enumerated types

ANSWER: Enumerated types

41) Which among the following is pre-defined in the standard package as one-dimensional array type comprising each element of BIT type?

a. Bit type

b. Bit_vector type

c. Boolean type

d. All of the above

ANSWER: Bit_vector type

42) In composite data type of VHDL, the record type comprises the elements of _____data types.

a. Same

b. Different

c. Both a and b

d. None of the above

ANSWER: Different

43) Which among the following wait statement execution causes the enclosing process to suspend and then wait for an event to occur on the signals?

a. Wait until Clk = ‘1’

b. Wait on x,y,z

c. Wait on clock until answer > 80

d. Wait for 12 ns

ANSWER: Wait on x,y,z

44) After an initialization phase, the simulator enters the _____phase.

a. Compilation

b. Elaboration

c. Execution

d. None of the above

ANSWER: Execution

45) Which concept proves to be beneficial in acquiring concurrency and order independence?

a. Alpha delay

b. Beta delay

c. Gamma delay

d. Delta delay

ANSWER: Delta delay

46) An event is nothing but _____ target signal, which is to be updated.

a. Fixed

b. Change on

c. Both a and b

d. None of the above

ANSWER: Change on

47) Which functions are performed by static timing analysis in simulation?

a. Computation of delay for each timing path

b. Logic analysis in a static manner

c. Both a and b

d. None of the above

ANSWER: Both a and b

48) Which among the following is/are regarded as the function/s of translation step in synthesis process?

a. Conversion of RTL description to boolean unoptimized description

b. Conversion of an unoptimized to optimized boolean description

c. Conversion of unoptimized boolean description to PLA format

d. All of the above

ANSWER: Conversion of RTL description to boolean unoptimized description

49) In synthesis flow, which stage/s is/are responsible for converting an unoptimized boolean description to PLA format?

a. Translation

b. Optimization

c. Flattening

d. All of the above

ANSWER: Flattening

50) In synthesis flow, the flattening process generates a flat signal representation of _____levels.

A. AND

B. OR

C. NOT

D. EX-OR

a. A & B

b. C & D

c. A & C

d. B & D

ANSWER: A & B

51) If the level of fan-out is beyond a limit in synthesis, it results in an insertion of buffer by ultimate effect of _____ the speed.

a. Enhancing

b. Reducing

c. Stabilizing

d. None of the above

ANSWER: Reducing

52) Which among the following constraint/s is/are involved in a state-machine description?

a. State variable & clock

b. State transitions & output specifications

c. Reset condition

d. All of the above

ANSWER: All of the above

53) Which among the following is/are identical in Mealy & Moore machines?

a. Combinational output signal

b. Clocked Process

c. Both a and b

d. None of the above

ANSWER: Clocked Process

54) Which method/s is/are adopted for acquiring spike-free outputs?

a. Moore machine with clocked outputs

b. Mealy machine with clocked outputs

c. Output-state machine

d. All of the above

ANSWER: All of the above

55) In SM chart for UART transmitter, which state/s indicate/s the waiting of sequential machine for the rising edge of bit clock and the consequent clearing of low order bit of TSR in order to transmit logic ‘0’ for one bit time?

a. IDLE State

b. Sync State

c. Transmit_Data_State

d. All of the above

ANSWER: Sync State

56) The devices which are based on fusible link or antifuse are _____time/s programmable.

a. one

b. two

c. four

d. infinite

ANSWER: one

57) Which among the following is/are not suitable for in-system programming?

a. EPROM

b. EEPROM

c. Flash

d. All of the above

ANSWER: EPROM

58) Simple Programmable Logic Devices (SPLDs) are also regarded as _____.

a. Programmable Array Logic (PAL)

b. Generic Array Logic (GAL)

c. Programmable Logic Array (PLA)

d. All of the above

ANSWER: All of the above

59) In signal integrity, which noise/s occur/s due to impedance mismatch, stubs, vias and other interconnection discontinuities?

a. Power/Ground Noise

b. Crosstalk Noise

c. Reflection Noise

d. All of the above

ANSWER: Reflection Noise

60) In floorplanning, placement and routing are _____ tools.

a. Front end

b. Back end

c. Both a and b

d. None of the above

ANSWER: Back end

61) In floorplanning, which phase/s play/s a crucial role in minimizing the ASIC area and the interconnection density?

a. Placement

b. Global Routing

c. Detailed Routing

d. All of the above

ANSWER: Placement

62) In CMOS inverter, the propagation delay of a gate is the/an _____ transition delay time for the signal during propagation from input to output especially when the signal changes its value.

a. Highest

b. Average

c. Lowest

d. None of the above

ANSWER: Average

63) In pull-up network, PMOS transistors of CMOS are connected in parallel with the provision of conducting path between output node & Vdd yielding _____ output.

a. 1

b. 0

c. Both a and b

d. None of the above

ANSWER: 1

64) For complex gate design in CMOS, OR function needs to be implemented by _____ connection/s of MOS.

a. Series

b. Parallel

c. Both series and parallel

d. None of the above

ANSWER: Parallel

65) In MOS devices, the current at any instant of time is _____of the voltage across their terminals.

a. constant & dependent

b. constant & independent

c. variable & dependent

d. variable & independent

ANSWER: constant & independent

66) On the basis of an active load, which type of inverting CMOS amplifier represents low gain with highly predictable small and large signal characteristics?

a. Active PMOS load inverter

b. Current source load inverter

c. Push-pull inverter

d. None of the above

ANSWER: Active PMOS load inverter

67) An ideal op-amp has _____

a. Infinite input resistance

b. Infinite differential voltage gain

c. Zero output resistance

d. All of the above

ANSWER: All of the above

68) Stuck open (off) fault occur/s due to _____

a. An incomplete contact (open) of source to drain node

b. Large separation of drain or source diffusion from the gate

c. Both a and b

d. None of the above

ANSWER: Both a and b

69) Which type/s of stuck at fault model exhibit/s the reduced complexity level of test generation?

a. Single

b. Multiple

c. Both a and b

d. None of the above

ANSWER: Multiple

70) Why is multiple stuck-at fault model preferred for DUT?

a. Because single stuck-at fault model is independent of design style & technology

b. Because single stuck-at tests cover major % of multiple stuck-at faults & unmodeled physical defects

c. Because complexity of test generation is reduced to greater extent in multiple stuck-at fault models

d. All of the above

ANSWER: All of the above

71) Which among the following EDA tool is available for design simulation?

a. OrCAD

b. ALDEC

c. Simucad

d. VIVElogic

ANSWER: VIVElogic

72) Which among the following functions are performed by MSI category of IC technology?

a. Gates, Op-amps

b. Microprocessor/A/D

c. Filters

d. Memory/DSP

ANSWER: Filters

73) The 'next' statements skip the remaining statement in the _____ iteration of loop and execution starts from first statement of next iteration of loop.

a. Previous

b. Next

c. Current (present)

d. None of the above

ANSWER: Current (present)

74) An Assert is _____ command.

a. Sequential

b. Concurrent

c. Both a and b

d. None of the above

ANSWER: Both a and b

75) Timing analysis is more efficient with synchronous systems whose maximum operating frequency is evaluated by the _____path delay between consecutive flip-flops.

a. shortest

b. average

c. longest

d. unpredictable

ANSWER: longest

76) What is/are the necessity/ies of Simulation Process in VHDL?

a. Requirement to test designs before implementation & usage

b. Reduction of development time

c. Decrease the time to market

d. All of the above

ANSWER: All of the above

77) Why is the use of mode buffer prohibited in the design process of synthesizer?

a. To avoid mixing of clock edges

b. To prevent the occurrence of glitches & metastability

c. Because critical path has preference in placement

d. Because Maximum ASIC vendors fail to support mode buffer in librari

ANSWER: Because Maximum ASIC vendors fail to support mode buffer in libraries

78) If a port is declared as buffer, then which problem is generated in hierarchical design due to mapping with port of buffer mode of other entities only?

a. Structural Modeling

b. Functional Modeling

c. Behavioral Modeling

d. Data Flow Modeling

ANSWER: Structural Modeling

79) Which UART component/s divide/s the system clock to provide the bit clock with the period equal to one bit time and Bclock x 8?

a. Baud Rate Generator

b. Transmitter Section

c. Receiver Section

d. All of the above

ANSWER: Baud Rate Generator

80) In Gray coding, when the state machine changes state, _____ bit/s in the state vector changes the value.

a. one

b. two

c. four

d. eight

ANSWER: one

81) Which type of CPLD packaging comprises pins on all four sides that wrap around the edges of chip?

a. Plastic-Leaded Chip Carrier (PLCC)

b. Quad Flat Pack (QFP)

c. Ceramic Pin Grid Array (PGA)

d. Ball Grid Array (BGA)

ANSWER: Plastic-Leaded Chip Carrier (PLCC)

82) An antifuse element initial provides _____ between two conductors in absence of the application of sufficient programming voltage.

a. Conduction

b. Insulation

c. Both a and b

d. None of the above

ANSWER: Insulation

83) In spartan-3 family architecture, which programmable functional element accepts two 18 bit binary numbers as inputs and computes the product?

a. Configurable Logic Blocks

b. Input Output Blocks

c. Block RAM

d. Multiplier Blocks

ANSWER: Multiplier Blocks

84) Which level of routing resources are supposed to be the dedicated lines allowing output of each tile to connect directly to every input of eight surrounding tiles?

a. Ultra-fast local resources

b. Efficient long-line resources

c. High speed, very long-line resources

d. High performance global networks

ANSWER: Ultra-fast local resources

85) Maze routing is also known as _____

a. Viterbi's algorithm

b. Lee/Moore algorithm

c. Prim’s algorithm

d. Quine-McCluskey algorithm

ANSWER: Lee/Moore algorithm

86) Maze routing is used to determine the _____path for a single wire between a set of points, if any path exists.

a. Shortest

b. Average

c. Longest

d. None of the above

ANSWER: Shortest

87) In a chip, which type/s of pad design/s is/are adopted to solve the problem of pin count?

a. Input pad design

b. Output pad design

c. Three state pad design

d. All of the above

ANSWER: Three state pad design

88) The power consumption of static CMOS gates varies with the _____ of power supply voltage.

a. square

b. cube

c. fourth power

d. 1/8 th power

ANSWER: square

89) Which factor/s play/s a crucial role in determining the speed of CMOS logic gate?

a. Load capacitance

b. Supply voltage

c. Gain factor of MOS

d. All of the above

ANSWER: All of the above

90) In high noise margin (NMH), the difference in magnitude between the maximum HIGH output voltage of driving gate and the maximum HIGH voltage is recognized by the _____gate.

a. Driven

b. Receiving

c. Both a and b

d. None of the above

ANSWER: Receiving

91) In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance?

a. Static dissipation

b. Dynamic dissipation

c. Both a and b

d. None of the above

ANSWER: Dynamic dissipation

92) In accordance to the scaling technology, the total delay of the logic circuit depends on _____

a. The capacitor to be charged

b. The voltage through which capacitance must be charged

c. Available current

d. All of the above

ANSWER: All of the above

93) In two-stage op-amp, what is the purpose of compensation circuitry?

a. To provide high gain

b. To lower output resistance & maintain large signal swing

c. To establish proper operating point for each transistor in its quiescent state

d. To achieve stable closed-loop performance

ANSWER: To achieve stable closed-loop performance

94) According to the principle of current mirror, if gate-source potentials of two identical MOS transistors are equal, then the channel currents should be _____

a. Equal

b. Different

c. Both a and b

d. None of the above

ANSWER: Equal

95) PSSR can be defined as the product of the ratio of change in supply voltage to change in output voltage of op-amp caused by the change in power supply & _____ of op-amp.

a. Open-loop gain

b. Closed-loop gain

c. Both a and b

d. None of the above

ANSWER: Open-loop gain

96) Which among the following serves as an input stage to most of the op-amps due to its compatibility with IC technology?

a. Differential amplifier

b. Cascode amplifier

c. Operational transconductance amplifiers (OTAs)

d. Voltage operational amplifier

ANSWER: Differential amplifier

97) Which among the following is/are responsible for the occurrence of 'Delay Faults'?

a. Variations in circuit delays & clock skews

b. Improper estimation of on-chip interconnect & routing delays

c. Aging effects & opens in metal lines connecting parallel transistors

d. All of the above

ANSWER: All of the above

98) Due to the limitations of the testers, the functional test is usually performed at speed _____the target speed.

a. Lower than

b. Equal to

c. Greater than

d. None of the above

ANSWER: Lower than

99) High observability indicates that _____number of cycles are required to measure the output node value.

a. More

b. Equal

c. Less

d. None of the above

ANSWER: Less

100) Basically, an observability of an internal circuit node is a degree to which one can observe that node at the _____ of an integrated circuit.

a. Inputs

b. Outputs

c. Both a and b

d. None of the above

ANSWER: Outputs