UNIT-2
Semiconductor Physics

N. Ramesh

UNIT-2 : SEMI CONDUCTORS

According to band theory solids can be classified into conductors, insulators, and semiconductors.

- In conductors the valance band and conduction band overlap. there is no forbidden energy gap.
- Insulators have large forbidden gap b/w conduction and valance band around 5 electron volt
- In semiconductors at zero temperature valance band is completely filled and conduction band is empty. They are separated by a small energy gap around one electron volt

Intrinstic & Extrinstic semiconductors.

Semiconductors are classified into 2 types.

1. Intrinstic semiconductor
2. Extrinstic semiconductor.

1. Intrinstic semiconductor:-

The intrinstic semiconductors are pure semiconductors. Crystals like intrinstic semiconductor have a tetrahedral structure and every atom forms 4 covalent bonds with neighbouring atoms

- In intrinstic semiconductors the no. of electrons in conduction band are equal to no. of holes in valance band at $t = 0°K$
- The fermi energy level in intrinstic semiconductors presented in middle of conduction & valance band. at $t = 0°K$

2. Extrinstic semiconductor:

A semiconductor in which charge carriers originate from impurity atoms added to it is called extrinstic semiconductor or impure semiconductor.

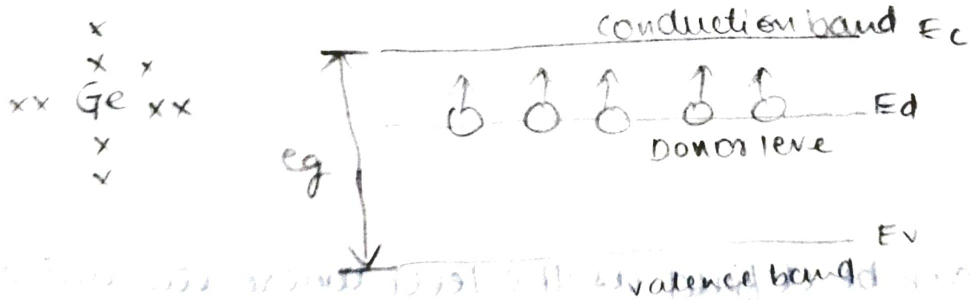
These are 2 type; 1. p-type 2. n-type.

1. ntype semiconductor:

when a pentavalent impurities like phosphorous, arsenic antimony etc added to the intrinstic semiconductor in small amount while the crystal growing we will get ntype semiconductor.

The impurity atom makes 4 covalent bonds with 4 neighbouring germenium atoms and 5th electron is loosely bonded to the nucleus. for a small amount of thermal energy 5th electron is ready to move

with increase of temperature the 5th electrons in donor level moves/ionises towards conduction band so electrons are becoming majority charge bariers in conduction band.



At low temperature fermi level lies in b/w conduction band to donar level.

$$E_F = \frac{E_c + E_d}{2}$$

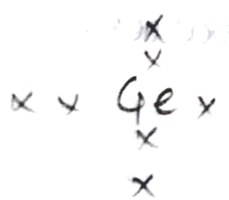
2. P-type semiconductor:

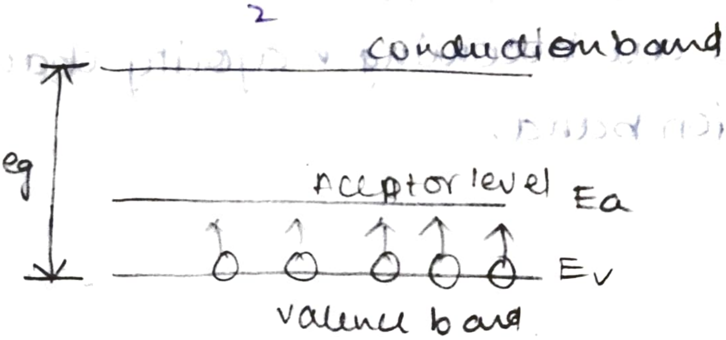
When trivalent impurities like aluminium, gallium, indium etc are added to the intrinsic semiconductor in small amount and while growing we will get p-type semiconductor

→ when trivalent impurity makes 3 covalent bonding with neighbouring germanium atoms. the 4th electron of germanium of electron is unpaired. which is loosely bound to the nucleus. these electrons of unpaired will get ionized from valence band to acceptor level with increase of temperature and holes become majority charge carriers in valance band

→ The fermi level lies b/w valance band to acceptor level at low temperature

$$E_F = \frac{E_V + E_a}{2}$$





Fermi level :-

Fermi level can be defined as the level where the electron occupation is maximum at 0°K. Hence

→ the fermi energy has the highest occupied energy state at 0°K

→ Fermi level also defined as where the probability of electron occupation is 50% at other than 0°K temp.

According Fermi-dirac statistics probability function for electron occupation in a energy level is $\boxed{F_E = \frac{1}{1+e^{(E-E_F)/KT}}}$

At T = 0°K where $E > E_F$

$$F(E) = \frac{1}{1+e^{\alpha}} = \frac{1}{1+\alpha} = 0$$

At T = 0°K when $E < E_F$

$$F(E) = \frac{1}{1+e^{-\alpha}} = \frac{1}{1+0} = 1$$

from above relation we can say that in a system all energy states above the fermi energy are empty.

→ The energy states below fermi energy state are completely filled with electrons

T > 0°K $E = E_F$

$$F(E) = \frac{1}{1+e^{0}} = \frac{1}{1+1} = \frac{1}{2} = 0.5$$

At other than ~~zero~~ 0°K temperature the fermi energy level represents the level with 50% probability for electron occupation

Dependence of fermi level on carrier concentration and temperature:

Fermi level in intrinsic semiconductors lies in b/w conduction band to valence band

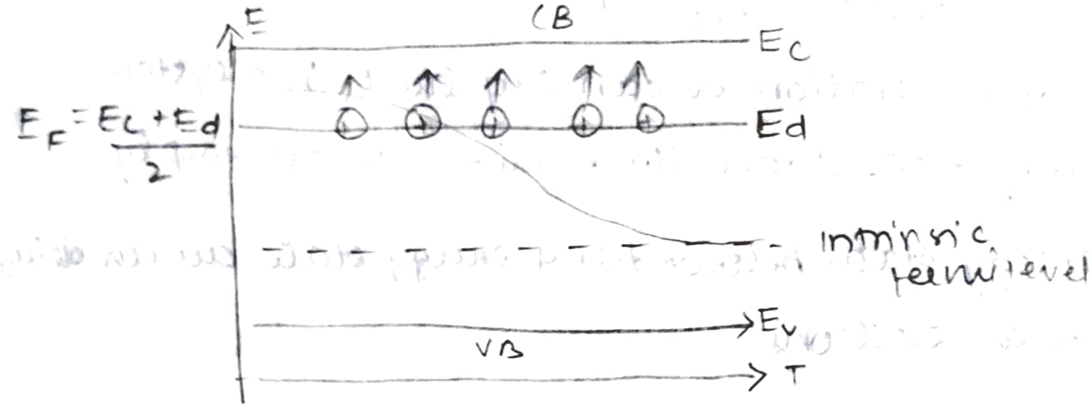
$$E_F = \frac{E_C + E_V}{2}.$$

Fermi level in intrinsic semiconductor is independent of temperature.

n-type semiconductor:-

In n type semiconductor fermi level lies in b/w conduction band and donar level. with increase of temperature fermi level increases slightly more donar atoms get ionized to conduction band.

For a particular temperature all donor atoms get ionised and further electron hole pairs will produce. And the fermi level moves towards intrinsic fermi level and finally matches with intrinsic fermi level.

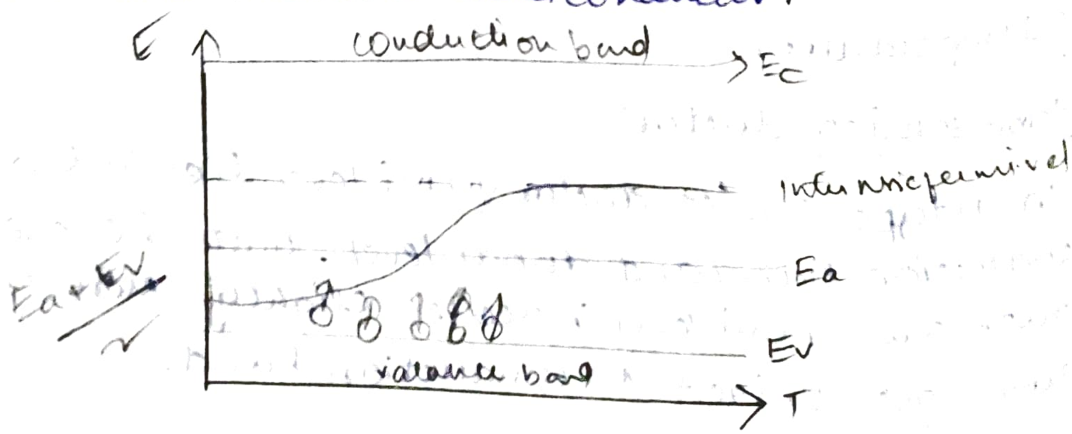


~~Carrier trans~~

P type semiconductor:-

~~Carrier generation is a process where electron hole pairs are created by exciting an e^- from the valance band of the semiconduc~~

P-type semiconductor also fermi level varies with temperature and concentration of acceptor impurities fermi level in P-type lies b/w valance band and acceptor level. As the temp. ↑es, fermi level decreases slightly and unpaired e^-s in valance band get ionized to acceptor level. At high temperature fermi level matches with intrinsic fermi level and p type material behaves like intrinsic semiconductor.



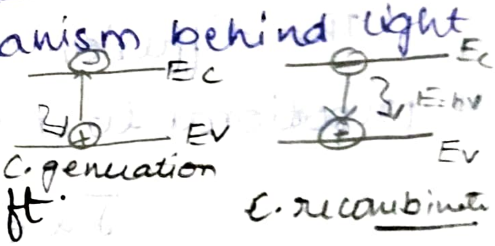
Carrier generation and recombination:-

Carrier generation is a process where electron - hole pairs are created by exiciting an $e^{\ominus}$ from the valance band of the semiconductor to conduction band by creating a hole in the valance band with application of thermal energy or electrical energy.

Carrier recombination is the reverse process where e^-s and holes from the dexicited from conduction and valance band gets recombined while electron dexicited from conduction band and valance band by releasing the energy in the form of photon. This recombination is proportional to amount of available electrons and holes

In thermal equilibrium the generation and recombination process are at equilibrium

→ Carrier recombination is the mechanism behind light emission in LED and LASER system



Carrier transport - Diffusion, Drift.

Carrier drift :- We know that motion of charge carier in semiconductor leads current. This motion can be ~~due~~ caused by electric field due to external voltage. Due to this transport mechanism generated current is called drift current.

As the applied field of voltage increases velocity of charge cariers also increases.

$$V_d \propto E$$

$$V_d = \mu E$$

V_d → drift velocity

μ → mobility of charge cariers

The current density can be calculated as $J = neV_d$

$$J = ne\mu E$$

drift current due to electrons $J_e = ne\mu_e E$

drift current due to holes is $J_p = ne\mu_n E$

$\therefore$ Total current density $J = J_e + J_p$

$$= ne\mu_e E + ne\mu_n E$$

$$\boxed{J = neE(\mu_e + \mu_n)}$$

carrier diffusion:

Carriers moves from regions where the current density is high to regions where the current density is low with effect of thermal energy. Due to the diffusion carriers experience random motion.

The diffusion current density due to electrons is proportional to change of charge carriers

$$J \propto e\left(-\frac{dn}{dx}\right)$$

$$J = De\left(-\frac{dn}{dx}\right)$$

The diffusion current density due to electrons is

$$J_n = D_n e \frac{dn}{dx}$$

The diffusion current density due to holes is

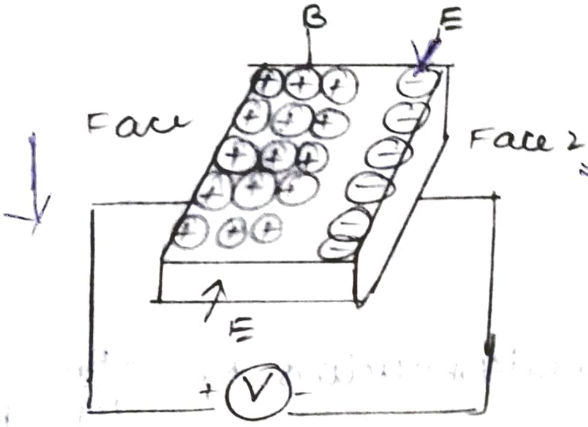
$$J_p = -D_p e \frac{dp}{dx}$$

The Total current density $J = J_n + J_p$

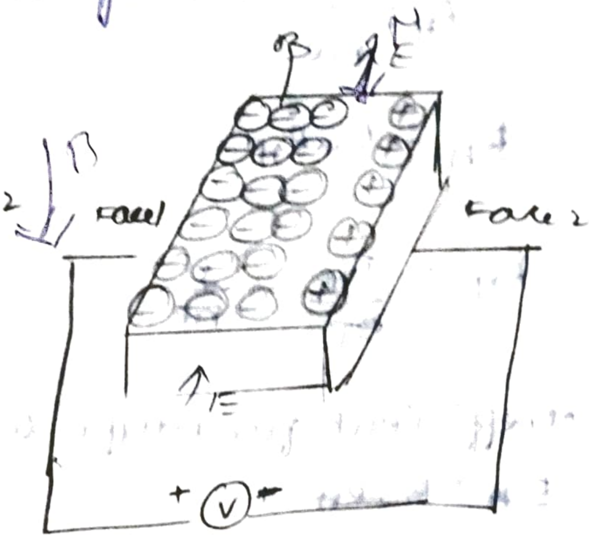
$$\boxed{J = D_n e \frac{dn}{dx} - D_p e \frac{dp}{dx}}$$

Hall effect :

" when a piece of conductor or semiconductor carrying current is placed in transversed magnetic field, an electric field is produced inside the conductor in a direction perpendicular to both current and magnetic field. This phenomenon is known as Hall effect" and generated voltage is known as hall voltage.



P type s.c



N type s.c

→ If ptype semiconductor introduced in magnetic field which already carries current so the positively charged holes accumulate at face-1 and produces hall voltage which is positive.

→ when a n type semiconductor carrying current introduced in magnetic field electrons accumulate at face-1 and hall voltage is negative.

→ If B is the magnetic field applied to the material electrons moves with velocity v and the experience force Bev

→ Bcoz of potential difference E_H at face 1 and 2 electric force is eE_H

at equilibrium $Bev = eE_H \Rightarrow E_H = Bv \rightarrow ①$

If J is the current density

$$J = nev$$

$$v = \frac{J}{ne}$$

$$① \Rightarrow E_H = \frac{BJ}{ne}$$

Hall effect described by hall coefficient

$$R_H = \frac{1}{ne}$$

$$E_H = BJR_H$$

$$R_H = \frac{E_H}{BJ} = \frac{1}{ne}$$

Hall coefficient for n type semiconductors $R_H = -\frac{E_H}{BJ} = -\frac{1}{ne}$

~~$E_H = BJR_H$~~

Hall coefficient for p type is $R_H = \frac{E_H}{BJ} = \frac{1}{Pe}$.

Determination of hall coefficient of a material.

If b is the width of the material across where hall voltage is V_H

$$\therefore E_h = \frac{V_H}{b}$$

Hence, $R_H = \frac{E_H}{BJ} = \frac{V_H}{BbJ}$

$$\Rightarrow V_H = R_H BbJ \rightarrow ②$$

If t is the thickness of the material, then cross section of the material is "bt"

$\therefore$ Current density $J = I/bt$

② $\Rightarrow V_H = R_H \, BbI / bt$

$$V_H = \frac{R_H \, BI}{t}$$

$$R_H = \frac{V_H t}{BI}$$

Applications of hall effect.

→ we can determine the type of semiconductor, because hall coefficient is negative for n type and positive for p type s.c.

→ we can calculate carrier concentration of a material by knowing hall coefficient R_H

$$n = \frac{1}{eR_H}$$

→ we can determine the mobility in a material by knowing Hall coefficient

$$\sigma_n = ne\mu_e$$

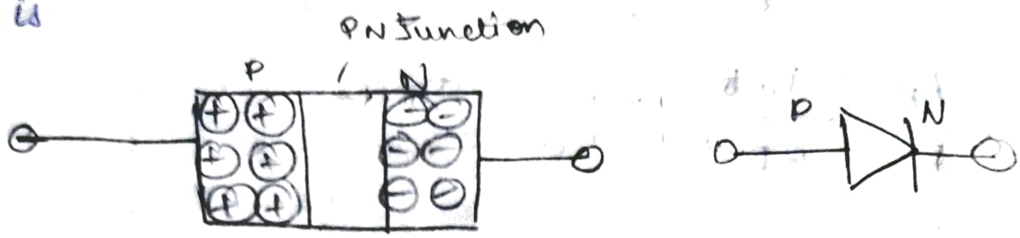
$\mu_e \rightarrow$ mobility

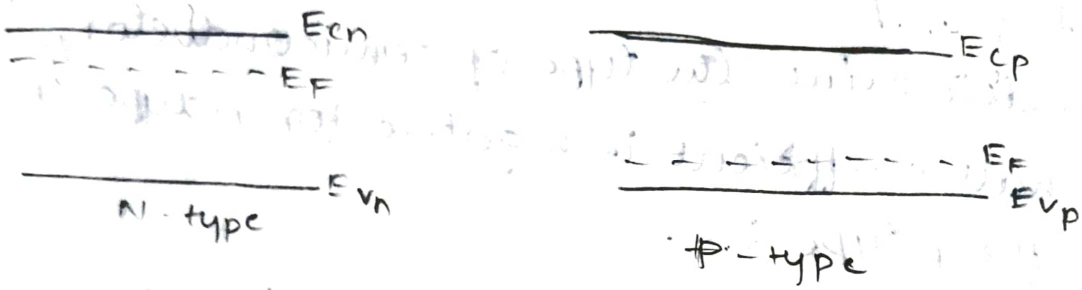
$\sigma_n \rightarrow$ conductivity

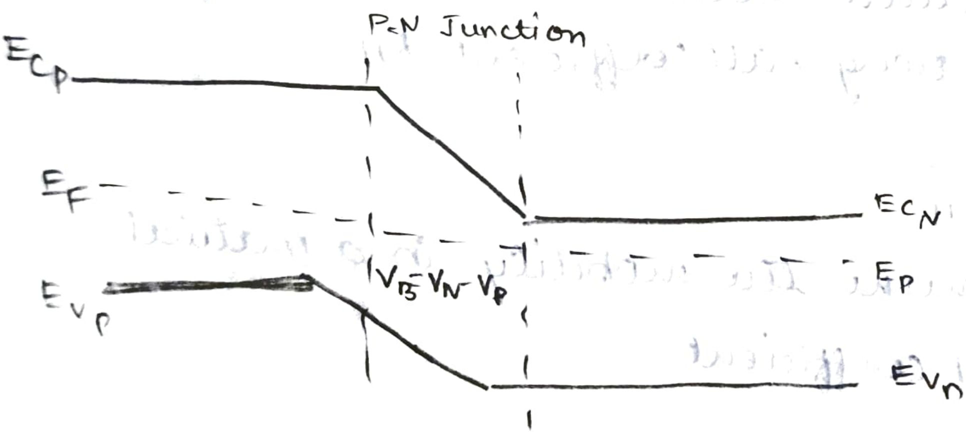
$$\boxed{\mu_e = \sigma_n R_H}$$

P-n junction diode VI characteristics:-

By combining ptype and ntype S.C we can construct P-n junction diode. The energy level diagram of p-n junction diode is







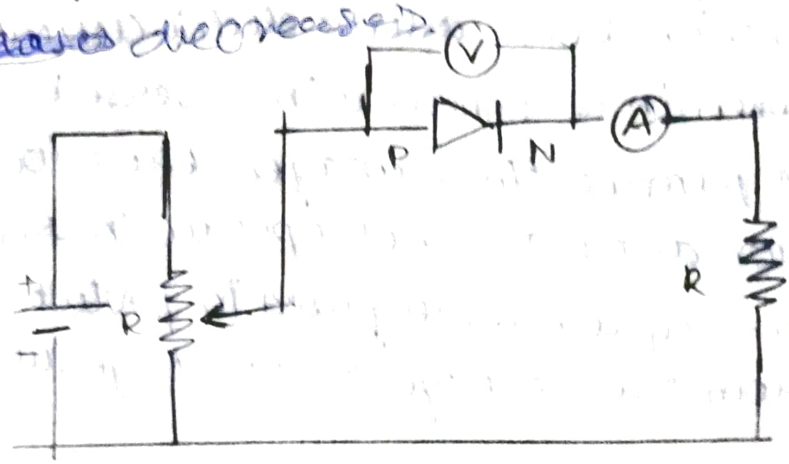
The P-n diode responds by applying voltage across the terminal and current flow through it is called VI characteristics.

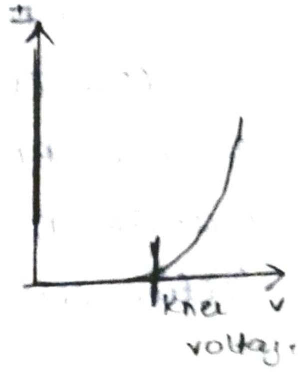
→ We can bias p-n diode in 2 ways.

1. forward bias
2. Reverse bias

1. forward bias: when we connect pn diode in forward bias mean p side two +ve terminal n side two -ve terminal of battery. If we increase the voltage current cannot passes through

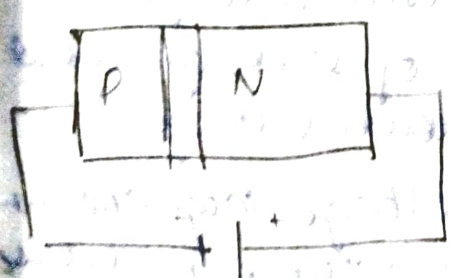
P-n junction until the voltage reaches to a certain value of voltage called knee voltage.
under forward bias the width of potential barrier ~~increases~~ decreases.

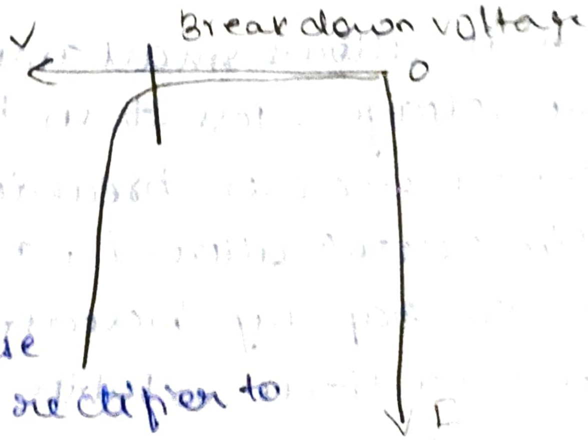




Reverse bias :-

In reverse biasing condition the negative terminal of battery connected to p type & positive terminal to n type of PN diode from the graph we can say that by increasing the voltage there is n rapid change in current with the voltage reaches to breakdown voltage. ~~&~~ breakdown voltage ~~a~~ small changing voltage results sharp change in current. The potential barrier width will increase in reverse bias.





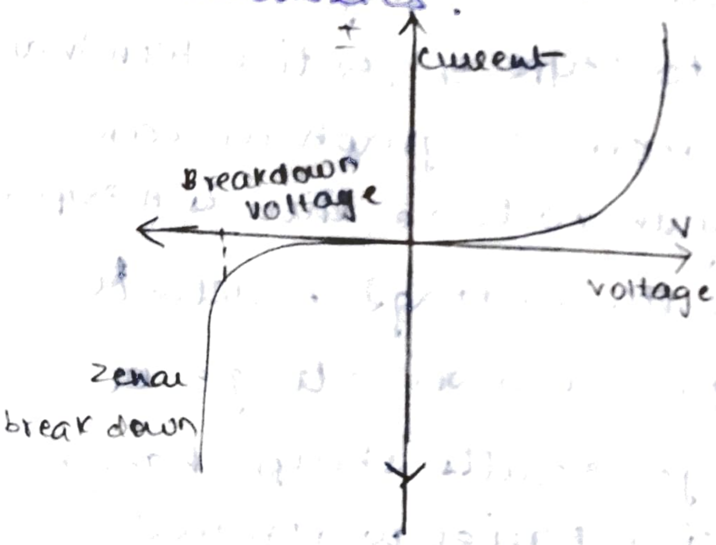
Applications:-
PN Junction diodes we can use in rectifier circuits as a rectifier to convert AC to DC

Zener diode

A heavily doped P-n junction diode works under reverse bias condition called zener diode.

⇒ A normal P-n junction diode allows electric current only in forward bias. when it is connected in reverse bias the excess current permanently damages the diode. There fore PN junction diode does not operate in reverse breakdown region. They are widely used to protect electric circuits from over voltage as a voltage stablizer.

V-I characteristics:



Zener diode under forward bias works as normal P-n junction diode. when reverse biased voltage is applied it allows small amount of leakage current until the voltage is less than breakdown voltage when voltage reaches breakdown voltage large amount of electric current allowed, a small increase in reverse voltage will rapidly increase electric current. However zener diode exhibits a control and sharp breakdown that does not damage the device

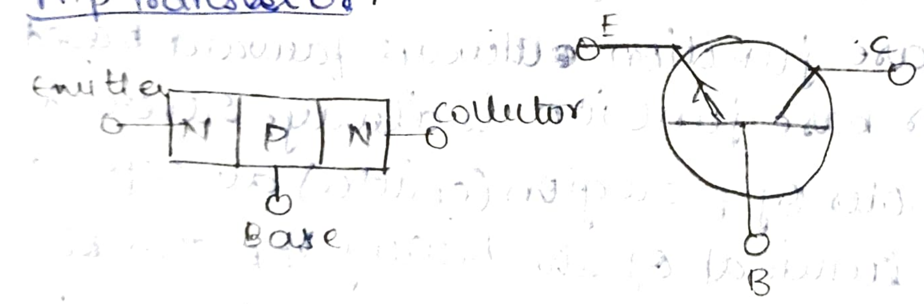
→ The zener diodes can be used as voltage stabilizers, switching operations etc.

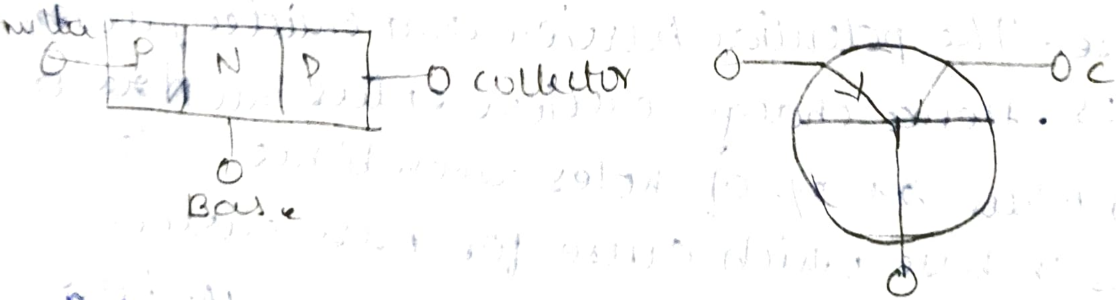
Bipolar Junction Transistor (BJT)

A junction transistor sandwitch of one type of semiconductor material b/w 2 types of the other type semiconductor material is a Bipolar Junction Transistor. These are 2 types.

1. npn transistor
2. pnp transistor

When a p type material sandwitched b/w two n type materials. the transistor known as <u>npn transistor</u>. A layer of n type semiconductor sandwitch b/w 2 p type materials. the transistor known as <u>pnp transistor</u>.





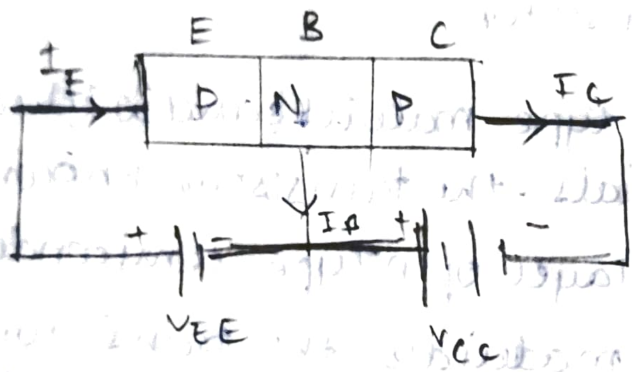
A transistor has the following sections.

1. Emitter :- This forms the left hand side of the transistor. the main function of this region is to supply majority charge carriers to base. It is more heavily doped comparing to other regions.

2. Base :- The middle section of the transistor known as base this is lightly doped and very thin (10^{-6}m) It may pass most of the injected carriers in a collector.

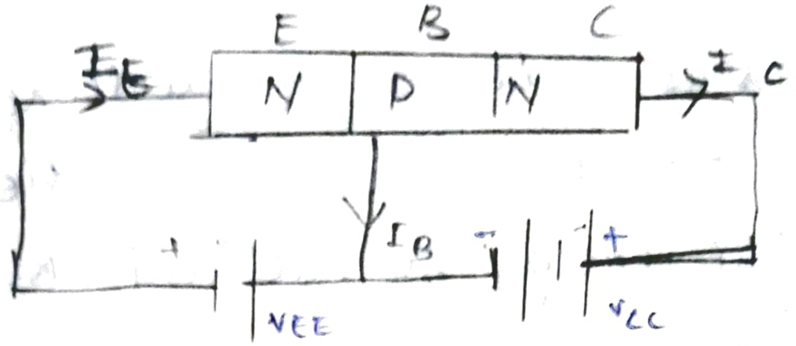
3. Collector :- The right hand side section of the transistor is called collector. It is moderately doped. its function is to collect the charge carriers from the base.

operation of pnp transistor:



The transistors are biased as shown above. the emitter base junction always forward biased while collector base junction is always reversed biased. The holes of p region (emitter) are repelled by the positive terminal of the battery V_{EE} towards the base. The potential barrier and emitter junction reduces. Hence charge carriers enters into N region (base) where 2to5% of holes recombine with electrons in base which cause for base current (I_B) The remaing holes drift across the base and enter to the collector region. They constitute the collector current (I_C).

operation of npn transistor:-



As we know the emitter junction is always forward bias, the electrons are repalled by the terminal V_{EE} towards emitter junction and enters into p region (base). The few of electrons combined with the holes in p region, causes the base current (I_B) and remaining electrons enters into collector which are rapidly swept up by the potential V_{CC} causes collector current (I_C)